Data Sheet

LTM8060F

Quad 40V_{IN}, 3A Silent Switcher µModule Regulator with Package-Level EMI Shield

FEATURES

- Package-Level EMI Shielding
  - Minimize Near-Field Electric Field Noise
  - Reduce Near-Field Magnetic Field Noise
- Pin-to-Pin Compatible with the *LTM8060*
- Four Complete 3A (4A peak) Step-Down Switching Power Supplies
- Low Noise Silent Switcher Architecture
- Compliant with CISPR22 Class B/CISPR25 Class 5
- Wide Input Voltage Range: 3V to 40V
- Wide Output Voltage Range: 0.8V to 8V
- 4A Continuous Output Current per Channel at 12V_{IN}, 3.3V_{OUT}, f_{SW} = 2MHz, T_A = 60°C
- Multiphase or Multi-module Parallelable for Increased Output Current
- Low Thermal Resistance, θ_{JA} = 8.4°C/W, θ_{JCtop} = 4.6°C/W, θ_{JCbot} = 1°C/W
- Selectable Switching Frequency: 200kHz to 3MHz
- Available in a Compact *165-Pin, 16mm × 11.9mm × 2.9mm, Pre-Soldered Grid Array (PSGA)* Package

APPLICATIONS

- Automated Test Equipment
- Industrial Supplies
- Medical Equipment

GENERAL DESCRIPTION

The *LTM8060F* is a quad 40V_{IN}, 3A (4A peak) step-down Silent Switcher® power µModule® (micromodule) regulator with package-level Electromagnetic interference (EMI) shield. The package-level EMI shield enables the Faraday cage to be applied directly to the LTM8060F package, and the EMI shield is electrically connected to the GND pins, providing a compact and effective near-field EMI reduction. The EMI shield eliminates all electric field noise, and a 10dB reduction is achieved on magnetic field noise. The *Silent Switcher* architecture minimizes EMI while delivering high efficiency.

Included in the package are the controllers, the power switches, the inductors, and the support components. Operating over a wide input voltage range, the LTM8060F supports output voltages from 0.8V to 8V and a switching frequency range of 200kHz to 3MHz, each set by a single resistor. Only the bulk input and the output filter capacitors are needed to finish the design. The LTM8060F outputs can be paralleled in an array for up to 12A (16A peak) capability (see *Figure 1*).

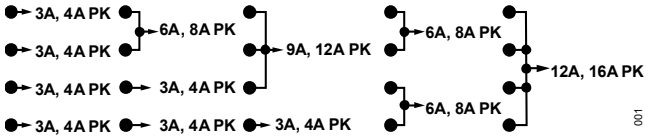


Figure 1. Configurable Output Array

The LTM8060F is packaged in a compact, 165-pin, 16mm × 11.9mm × 2.9mm, pre-soldered grid array (PSGA) package suitable for automated assembly by standard surface mount equipment. The LTM8060F is a pin-to-pin compatible with the LTM8060. The LTM8060F is RoHS-compliant.

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

TYPICAL APPLICATION

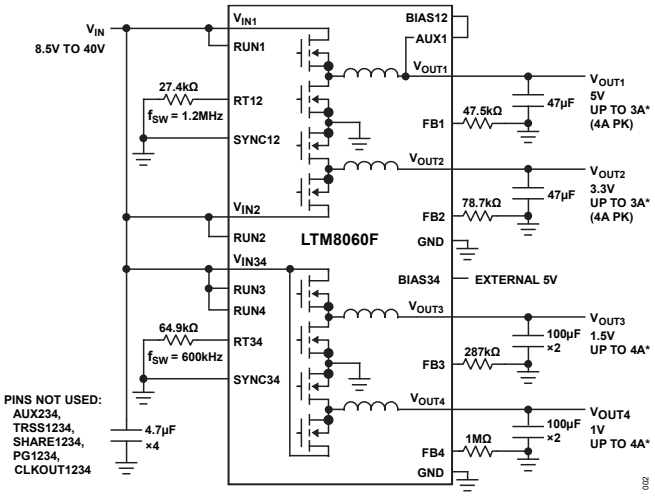


Figure 2. Quad 3A (4A Peak) Output from 8.5V to 40V Input

* The output current capability (transient peak or continuous) in *Figure 2* is subject to environmental factors such as ambient temperature, airflow, or other cooling techniques. For different V_{IN}, V_{OUT}, and T_A conditions, see the notes section (Note *3*) of the *Electrical Characteristics* table and the derating curves in the *Applications Information* section.

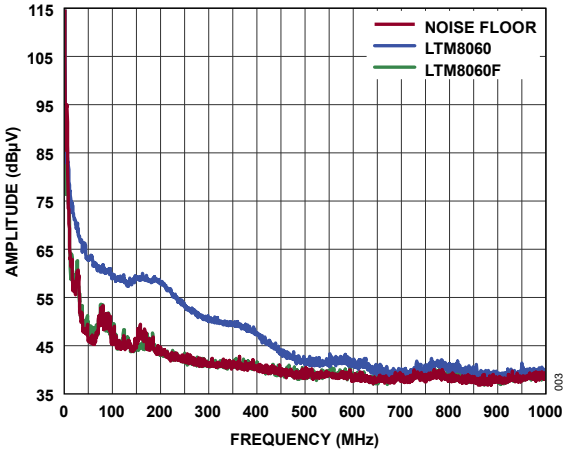


Figure 3. Near-Field E Field, 100% Reduction, All Near-Field Electric Field Noise removed, from 1MHz to 1GHz

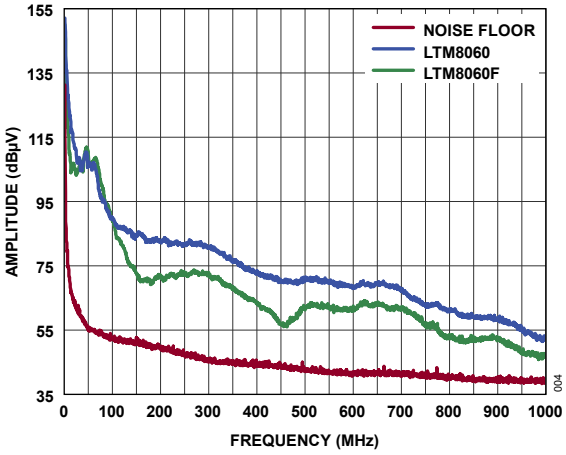


Figure 4. Near-Field H Field, 10db Reduction, Less Near-Field Electric Field Noise, from 1MHz to 1GHz

TABLE OF CONTENTS

REVISION HISTORY

10/2024 - Rev. 0: Initial Release.

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C, V_{INn} = 12V, RUNn = 2V unless otherwise noted.[1,2])

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Minimum V_{IN1} Input Voltage	V_{INn}		–40°C ≤ T_J ≤ 125°C			3.0	V
Minimum V_{IN34} Input Voltage	V_{INn}		–40°C ≤ T_J ≤ 125°C			3.0	V
Minimum V_{IN2} Input Voltage	V_{INn}	V_{IN1} = 3V	–40°C ≤ T_J ≤ 125°C			2.0	V
Output DC Voltage	V_{OUT}	FBn open			0.8		V
		FBn = 21.5kΩ			10		V
Maximum Output DC Current	$I_{OUT(MAX)}$	[3]				6	A
Quiescent Current into V_{INn}	$I_{Q(VIN)}$	RUNn = 0				8	µA
		BIASn = 5V, SYNCn = 3.3V, no load			7		mA
Current into BIASn	I_{BIASn}	RUNn = 0, BIASn = 5V				0.5	µA
		BIASn = 5V, SYNCn = 3.3V, no load			18		mA
Line Regulation	$V_{LINEREG}$	5V < V_{INn} < 40V, I_{OUTn} = 1A			0.05	0.3	%
Load Regulation	$V_{LOADREG}$	12V_{INn}, 0.1A < I_{OUTn} < 4A			0.1	0.5	%
Output RMS Ripple	V_{RIPPLE}	3.3V_{OUTn}, I_{OUTn} = 4A			10		mV
FBn Voltage	V_{FB}			792	800	808	mV
			–40°C ≤ T_J ≤ 125°C	784	800	816	mV
Current out of FBn	I_{FB}	V_{OUTn} = 1V, FBn = 0V			4		µA
Minimum BIASn for Proper Operation	I_{BIAS}					3.2	V
Switching Frequency	f_{SW}	R_{Tn} = 200kΩ			200		kHz
		R_{Tn} = 35.7kΩ			1		MHz
		R_{Tn} = 8.06kΩ			3		MHz
RUNn Threshold	$V_{RUN(ON)}$				0.74		V
RUNn Input Current	I_{RUN}	RUNn = 0V				100	nA
PGn Threshold at FBn	V_{FBL}	Lower threshold			740		mV
	V_{FBH}	Upper threshold			860		mV
PGn Output Sink Current	I_{PG}	PGn = 0.1V		100			µA
CLKOUTn V_{OL}	$V_{OL(CLK)}$				0.2		V
CLKOUTn V_{OH}	$V_{OH(CLK)}$				3.2		V
SYNCn Input High Threshold	$V_{INH(SYNC)}$			1.5			V
SYNCn Input Low Threshold	$V_{INL(SYNC)}$					0.8	V

(T_A = 25°C, V_{INn} = 12V, RUNn = 2V unless otherwise noted.[1,2])

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
SYNCn Threshold to Enable Spread Spectrum	$V_{EN(SYNC)}$			2.8		4.0	V
SYNCn Current	I_{SYNC}	SYNCn = 6V			60		µA
TRSSn Source Current	I_{TRSS}	TRSSn = 0V			2		µA
TRSSn Pull-Down Resistance	R_{TRSS}	Fault condition, TRSSn = 0.1V			200		Ω

1 The LTM8060FE is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM8060FI is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

2 The n represents each individual channel. Four outputs are tested separately, and the same testing condition is applied to each output.

3 The maximum current out of any channel may be limited by the internal temperature of the LTM8060F. For different V_{IN}, V_{OUT}, and T_A conditions, see the output current derating curves in the *Applications Information* section.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{INn}, RUNn, PGn	42V
V_{OUTn}, BIASn, AUXn	10V
FBn, TRSSn, SHAREn, RTn	4V
SYNCn	6V
Maximum Internal Temperature	125°C
Storage Temperature	–55°C to 125°C
Peak Solder Reflow Package Body Temperature	245°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to Printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only Human body model (HBM) per ANSI/ESDA/JEDEC JS-001 Field induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002. International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2. Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings

Table 3. LTM8060F ESD Ratings

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±4000	3A
CDM	±1250	C3

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

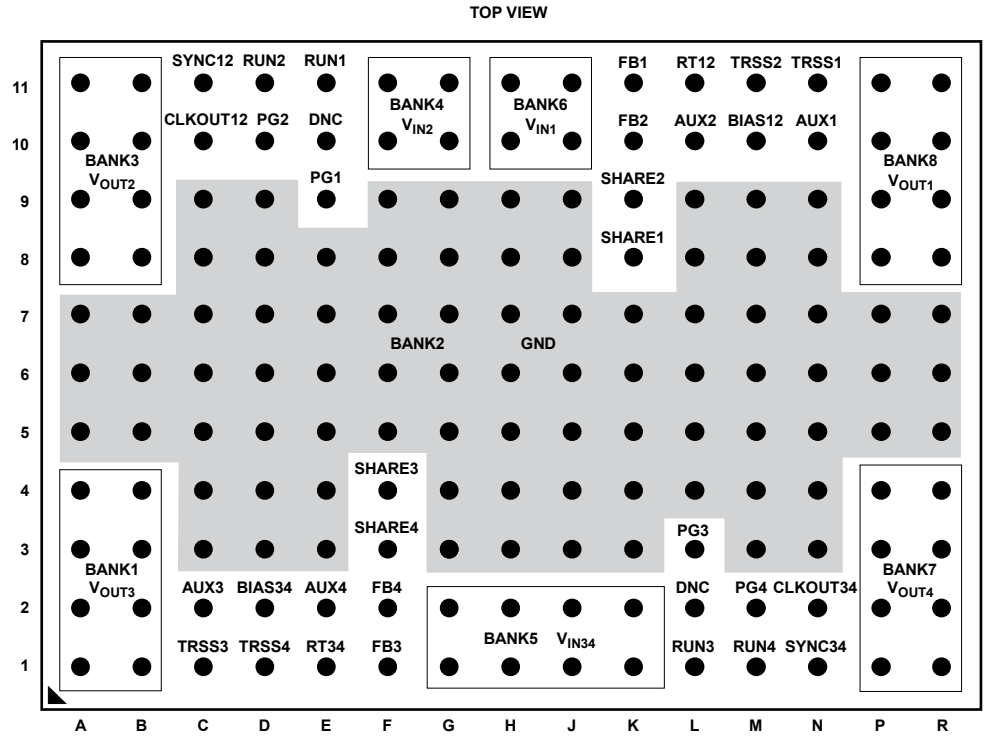


Figure 5. Pinout Configuration

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Pin Descriptions

Table 4. Pin Descriptions

PIN CFG 1	NAME	DESCRIPTION
Bank 2	GND	Connect these GND pins to a local ground plane below the LTM8060F and the circuit components. In most applications, the bulk of the heat flow out of the LTM8060F is through these pads, so the printed circuit board (PCB) design has a large impact on the thermal performance of the device. See the *PCB Layout* and *Thermal Considerations* sections for more details. Return the feedback divider (R_{FB}) to this net.

PIN CFG 1	NAME	DESCRIPTION
Bank 4	V_{IN2}	Input Power for the Channel 2 Regulator. Decouple V_{IN2} to ground with an external low Equivalent series resistance (ESR) capacitor. See *Table 6* for recommended values.
Bank 5	V_{IN34}	Input Power for the Channel 3 and Channel 4 Regulator. The V_{IN34} bank powers the internal control circuitry for both Channel 3 and Channel 4 and is monitored by undervoltage lockout circuitry. The V_{IN34} voltage must be greater than 3V for either Channel 3 or Channel 4 of the LTM8060F to operate. Decouple V_{IN34} to ground with an external low-ESR capacitor. See *Table 6* for recommended values.
Bank 6	V_{IN1}	Input Power for the Channel 1 Regulator. The V_{IN1} powers the internal control circuitry for Channel 1 and Channel 2 and is monitored by undervoltage lockout circuitry. The V_{IN1} voltage must be greater than 3V for either Channel 1 or Channel 2 of the LTM8060F to operate. Decouple V_{IN1} to ground with an external low-ESR capacitor. See *Table 6* for recommended values.
Banks 8, 3, 1, 7	$V_{OUT1–OUT4}$	Power Output for Channel 1, through Channel 4, respectively. Apply the output filter capacitor and the output load between these pins and the GND plane.
C10, N2	CLKOUT12, 34	Synchronization Output. When SYNC12, 34 > 2.8V, the CLKOUT12, 34 pins provide a waveform about 90° out-of-phase with Channel 1 and Channel 3, respectively. This allows synchronization with other regulators with up to four phases. When an external clock is applied to the SYNC12, 34 pins, the CLKOUT12, 34 pins will output a waveform with about the same phase, duty cycle, and frequency as the SYNC12, 34 waveform. In Burst Mode® operation, the CLKOUT12, 34 pins will be internally grounded. Float these pins if the CLKOUT12, 34 function is not used. Do not drive these pins.
C11, N1	SYNC12, 34	External Clock Synchronization Input. Ground these pins for low ripple Burst Mode operation at low output loads; this will also disable the CLKOUT function. Apply a DC voltage between 2.8V and 4V for forced continuous mode (FCM) operation with spread spectrum modulation. Float the SYNCn pin for FCM operation without spread spectrum modulation. Apply a clock source to the SYNCn pin for synchronization to an external frequency. The LTM8060F will be in FCM when an external frequency is applied.
E9, D10, L3, M2	PG1–PG4	The PGn pins are the open-drain output of an internal comparator. The PGn pin remains low until the FBn pin is within ±7.5% of the final regulation voltage, and until there are no fault conditions. The PGn pin is pulled low during V_{INn} UVLO, thermal shutdown, or when the RUNn pins are low.
E10, L2	DNC	Do not connect these pins.
E11, D11, L1, M1	RUN1–RUN4	The corresponding channel of the LTM8060F is shut down when these pins are low and active when these pins are high. Connect to V_{INn} if the shutdown feature is not used. An external resistor divider from V_{INn} can be used to program a V_{INn} threshold below which the corresponding channel of the LTM8060F will shut down. Do not float these pins.

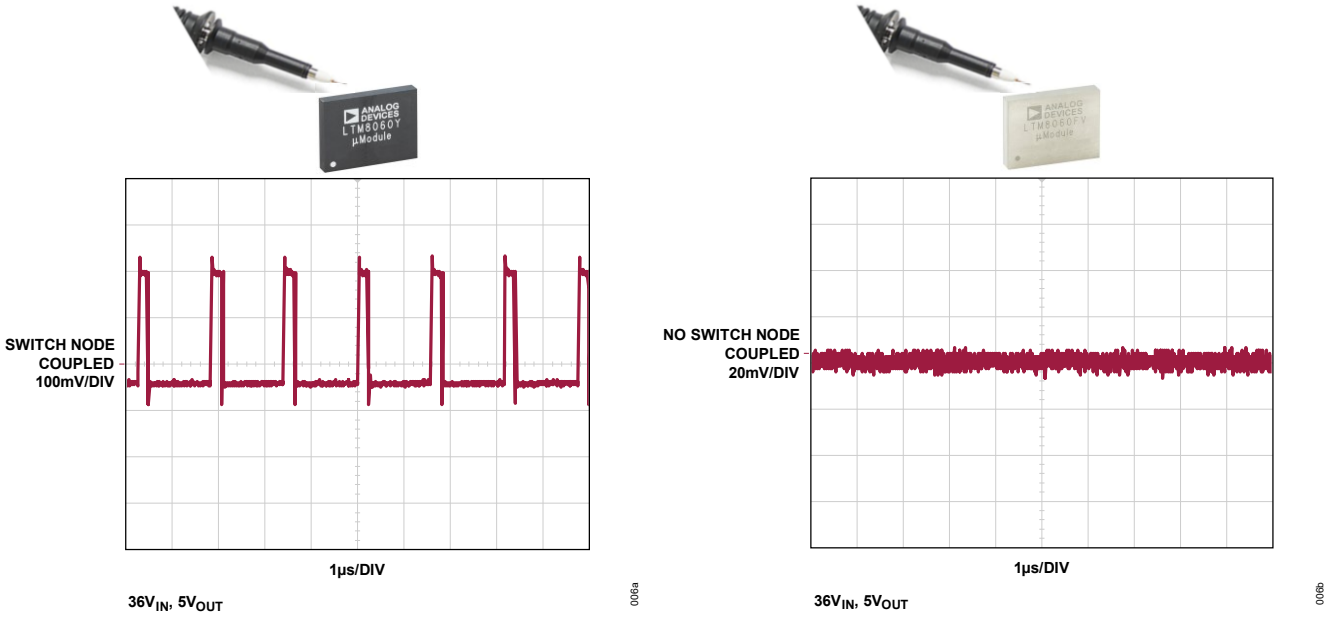
PIN CFG 1	NAME	DESCRIPTION
K8, K9, F4, F3	SHARE1−SHARE4	Channel 1 through Channel 4 Current Sharing Control. Connect SHAREn together when paralleling outputs. The LTM8060F can also share current between modules. See the *Typical Applications* section for current sharing between channels and current sharing between modules.
K11, K10, F1, F2	FB1−FB4	The LTM8060F regulates the FBn pin to 800mV. Connect the feedback resistor to these pins to set the output voltage.
L11, E1	RT12, 34	Connect a resistor between RTn and ground to set the switching frequency. Do not drive these pins.
M10, D2	BIAS12, 34	The internal regulator will draw current from BIASn instead of V_{IN1} or V_{IN34} when BIASn is connected to a voltage higher than 3.2V. For output voltages of 3.3V and above, these pins should be connected to V_{OUTn}. If these pins are connected to a supply other than V_{OUTn}, use a local bypass capacitor on these pins.
N10, L10, C2, E2	AUX1−AUX4	Low Current Voltage Source for BIAS. In many designs, the BIAS pin is simply connected to V_{OUT} via the AUX pin. The AUXn pins are internally connected to V_{OUTn} and placed adjacent to the BIASn pins to ease printed circuit board routing. Although these pins are internally connected to V_{OUT}, they are not intended to deliver a higher current, so do NOT connect these pins to the load. If these pins are not connected to BIAS, leave them floating.
N11, M11	TRSS1, 2	Output Tracking and Soft Start Pins. These pins allow the user to control the output voltage ramp rate during startup. A TRSSn voltage below 0.8V forces the LTM8060F to regulate the FBn pin to equal the TRSSn pin voltage. When TRSSn is above 0.8V, the tracking function is disabled, and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current on these pins allow a capacitor to program output voltage slew rate. These pins are pulled to ground during shutdown and fault conditions; use a series resistor if driving from a low impedance output. These pins may be left floating if the soft start feature is not being used.

Table 5. LTM8060F Pinout (Sorted by Pin Number)

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
A1–D11							
A1	V_{OUT3}	B1	V_{OUT3}	C1	TRSS3	D1	TRSS4
A2	V_{OUT3}	B2	V_{OUT3}	C2	AUX3	D2	BIAS34
A3	V_{OUT3}	B3	V_{OUT3}	C3	GND	D3	GND
A4	V_{OUT3}	B4	V_{OUT3}	C4	GND	D4	GND
A5	GND	B5	GND	C5	GND	D5	GND
A6	GND	B6	GND	C6	GND	D6	GND
A7	GND	B7	GND	C7	GND	D7	GND
A8	V_{OUT2}	B8	V_{OUT2}	C8	GND	D8	GND
A9	V_{OUT2}	B9	V_{OUT2}	C9	GND	D9	GND
A10	V_{OUT2}	B10	V_{OUT2}	C10	CLKOUT12	D10	PG2
A11	V_{OUT2}	B11	V_{OUT2}	C11	SYNC12	D11	RUN2
E1–H11							
E1	RT34	F1	FB3	G1	V_{IN34}	H1	V_{IN34}
E2	AUX4	F2	FB4	G2	V_{IN34}	H2	V_{IN34}
E3	GND	F3	SHARE4	G3	GND	H3	GND
E4	GND	F4	SHARE3	G4	GND	H4	GND
E5	GND	F5	GND	G5	GND	H5	GND
E6	GND	F6	GND	G6	GND	H6	GND
E7	GND	F7	GND	G7	GND	H7	GND
E8	GND	F8	GND	G8	GND	H8	GND
E9	PG1	F9	GND	G9	GND	H9	GND
E10	DNC	F10	V_{IN2}	G10	V_{IN2}	H10	V_{IN1}
E11	RUN1	F11	V_{IN2}	G11	V_{IN2}	H11	V_{IN1}
J1–M11							
J1	V_{IN34}	K1	V_{IN34}	L1	RUN3	M1	RUN4
J2	V_{IN34}	K2	V_{IN34}	L2	DNC	M2	PG4
J3	GND	K3	GND	L3	PG3	M3	GND
J4	GND	K4	GND	L4	GND	M4	GND
J5	GND	K5	GND	L5	GND	M5	GND
J6	GND	K6	GND	L6	GND	M6	GND
J7	GND	K7	GND	L7	GND	M7	GND
J8	GND	K8	SHARE1	L8	GND	M8	GND
J9	GND	K9	SHARE2	L9	GND	M9	GND
J10	V_{IN1}	K10	FB2	L10	AUX2	M10	BIAS12
J11	V_{IN1}	K11	FB1	L11	RT12	M11	TRSS2
N1–R11							
N1	SYNC34	P1	V_{OUT4}	R1	V_{OUT4}		
N2	CLKOUT34	P2	V_{OUT4}	R2	V_{OUT4}		
N3	GND	P3	V_{OUT4}	R3	V_{OUT4}		
N4	GND	P4	V_{OUT4}	R4	V_{OUT4}		
N5	GND	P5	GND	R5	GND		
N6	GND	P6	GND	R6	GND		
N7	GND	P7	GND	R7	GND		
N8	GND	P8	V_{OUT1}	R8	V_{OUT1}		
N9	GND	P9	V_{OUT1}	R9	V_{OUT1}		
N10	AUX1	P10	V_{OUT1}	R10	V_{OUT1}		
N11	TRSS1	P11	V_{OUT1}	R11	V_{OUT1}		

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, operating per *Table 6*, unless otherwise noted.



(a) LTM8060 without EMI Shielding

(b) LTM8060F with EMI Shielding

Figure 6. LTM8060F vs. LTM8060 SW Noise Comparison

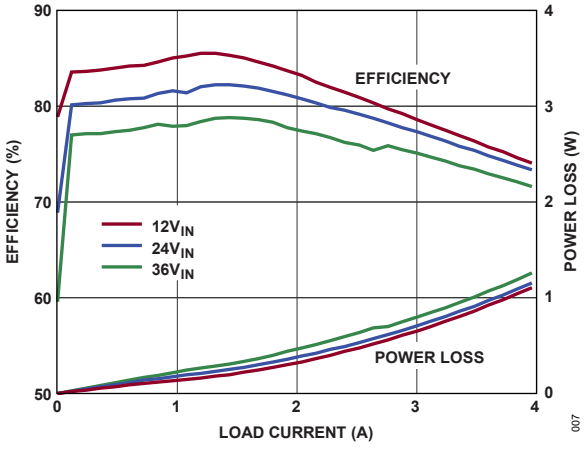


Figure 7. Efficiency vs. Power Loss, V_{OUT} = 0.8V, BIAS = 5V, Burst Mode Operation

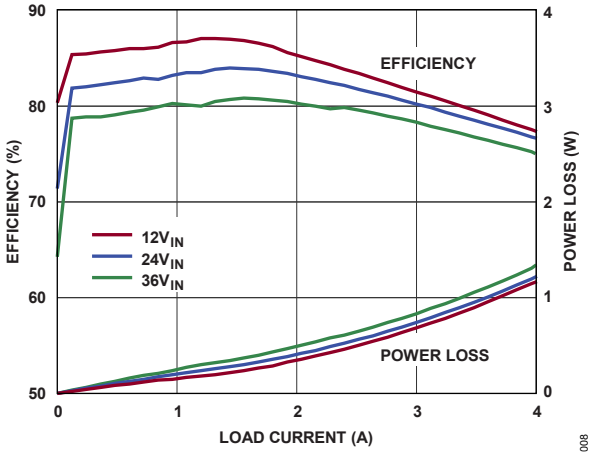


Figure 8. Efficiency vs. Power Loss, V_{OUT} = 1V, BIAS = 5V, Burst Mode Operation

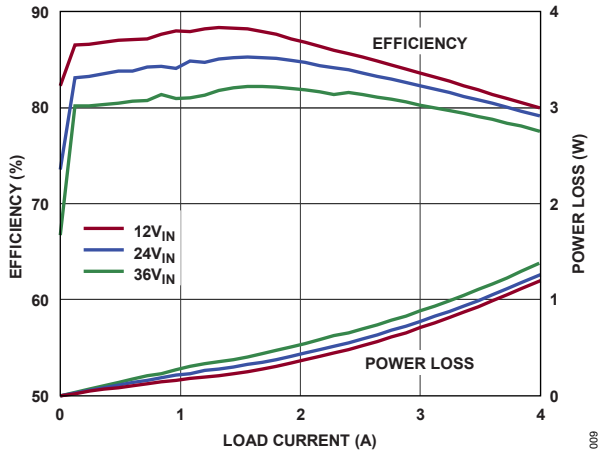


Figure 9. Efficiency vs. Power Loss, V_{OUT} = 1.2V, BIAS = 5V, Burst Mode Operation

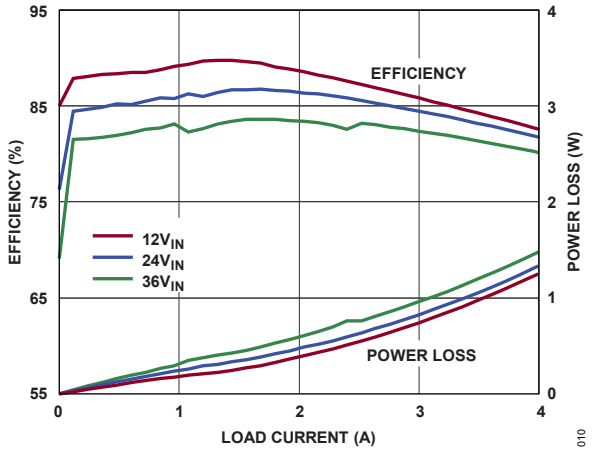


Figure 10. Efficiency vs. Power Loss, V_{OUT} = 1.5V, BIAS = 5V, Burst Mode Operation

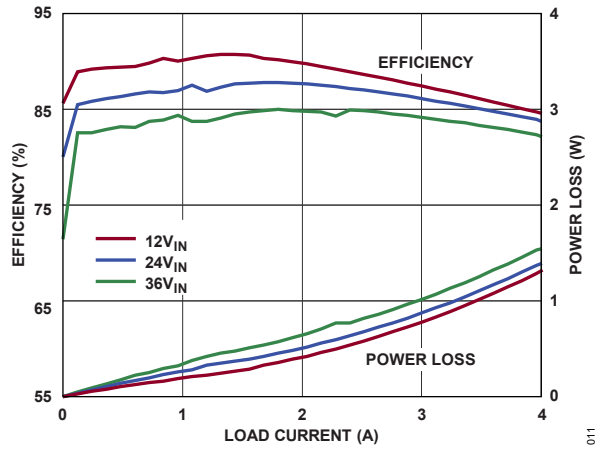


Figure 11. Efficiency vs. Power Loss, V_{OUT} = 1.8V, BIAS = 5V, Burst Mode Operation

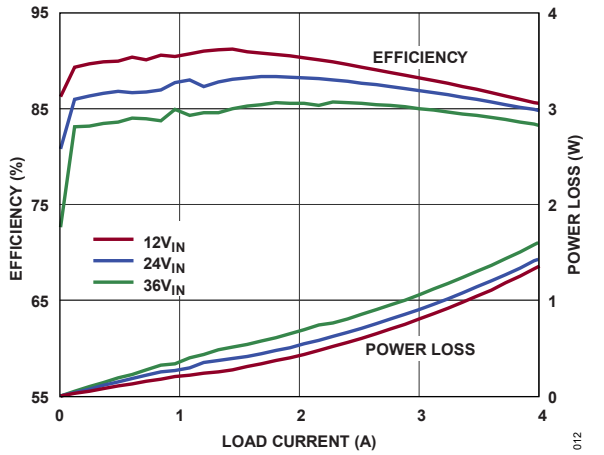


Figure 12. Efficiency vs. Power Loss, V_{OUT} = 2V, BIAS = 5V, Burst Mode Operation

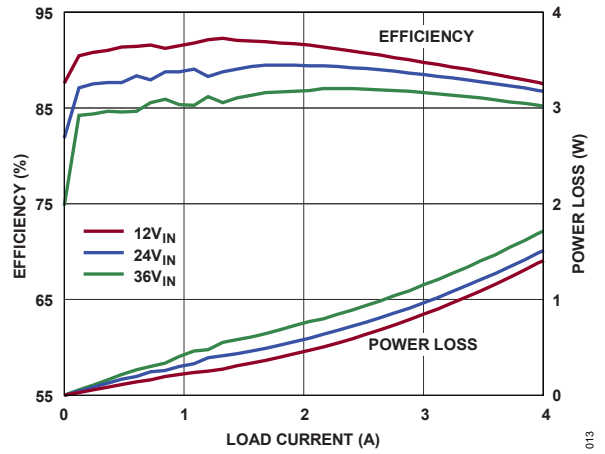


Figure 13. Efficiency vs. Power Loss, V_{OUT} = 2.5V, BIAS = 5V, Burst Mode Operation

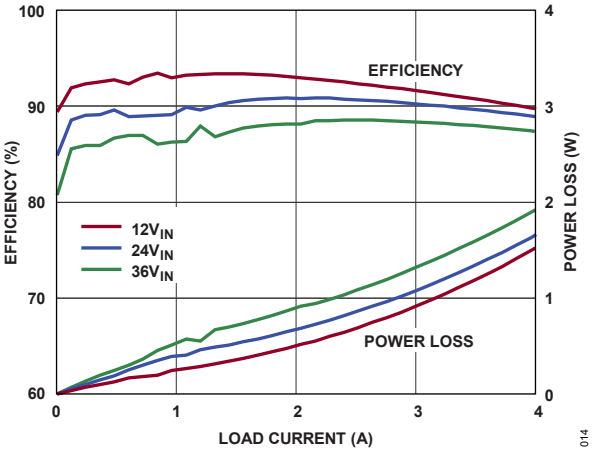


Figure 14. Efficiency vs. Power Loss, V_{OUT} = 3.3V, BIAS = 5V, Burst Mode Operation

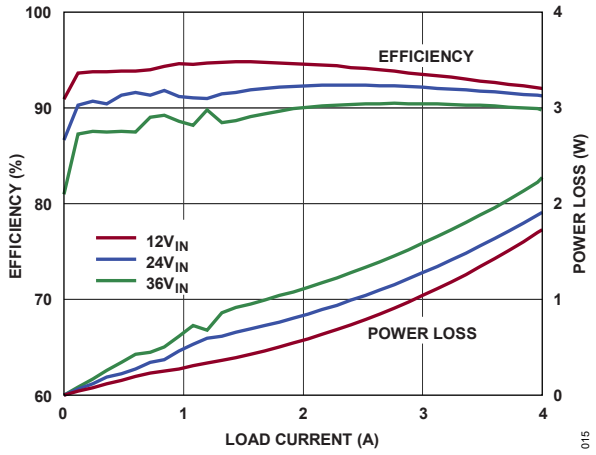


Figure 15. Efficiency vs. Power Loss, V_{OUT} = 5V, BIAS = 5V, Burst Mode Operation

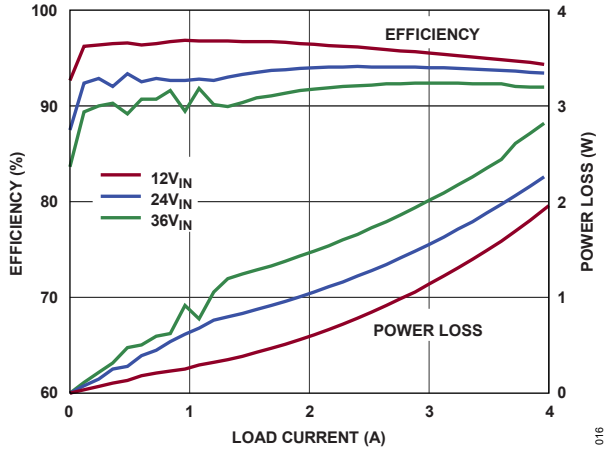


Figure 16. Efficiency vs. Power Loss, V_{OUT} = 8V, BIAS = 5V, Burst Mode Operation

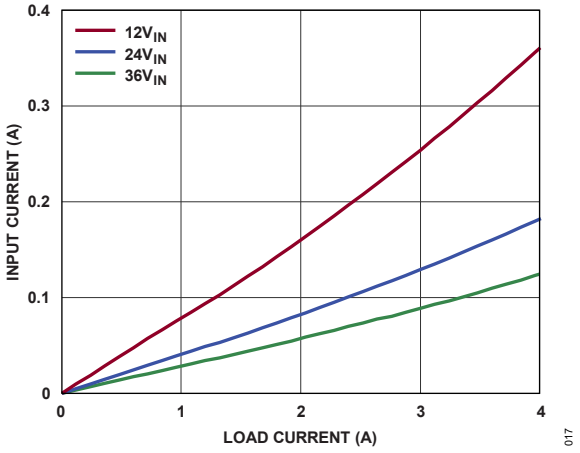


Figure 17. Input vs. Load Current, V_{OUT} = 0.8V, BIAS = 5V, Burst Mode Operation

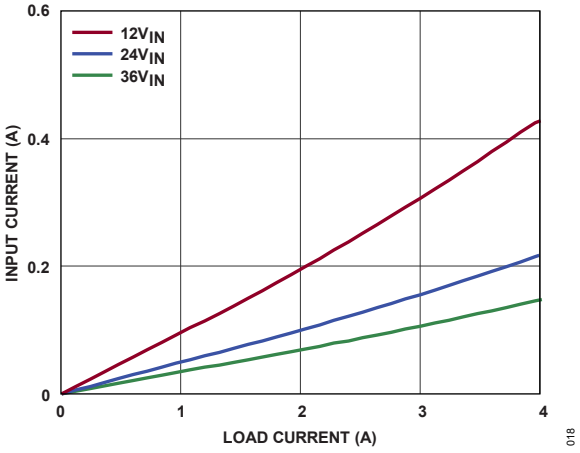


Figure 18. Input vs. Load Current, V_{OUT} = 1V, BIAS = 5V, Burst Mode Operation

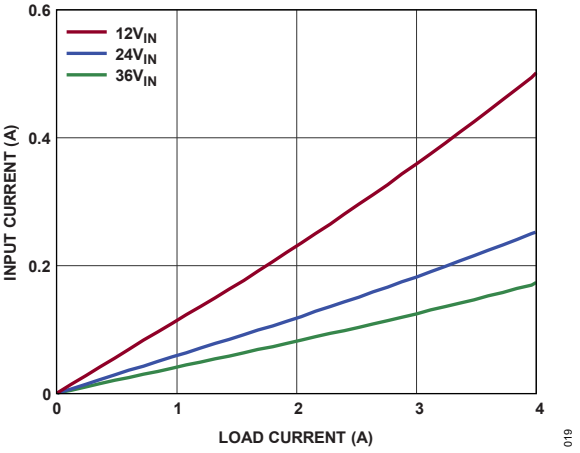


Figure 19. Input vs. Load Current, V_{OUT} = 1.2V, BIAS = 5V, Burst Mode Operation

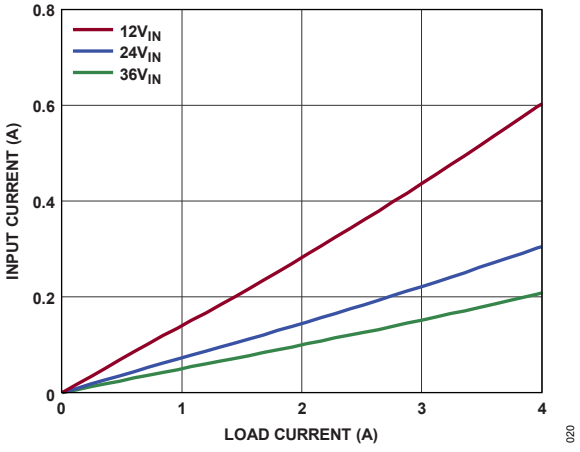


Figure 20. Input vs. Load Current, V_{OUT} = 1.5V, BIAS = 5V, Burst Mode Operation

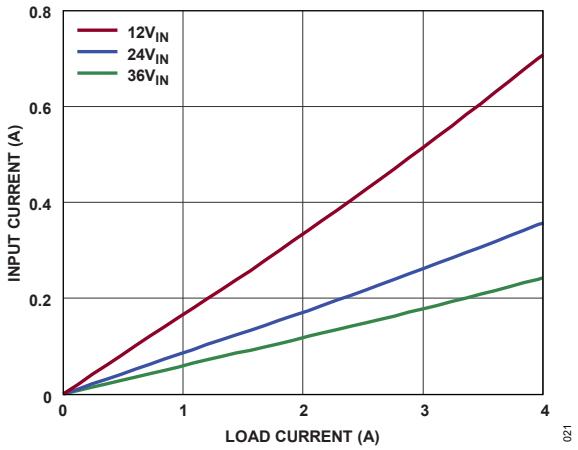


Figure 21. Input vs. Load Current, V_{OUT} = 1.8V, BIAS = 5V, Burst Mode Operation

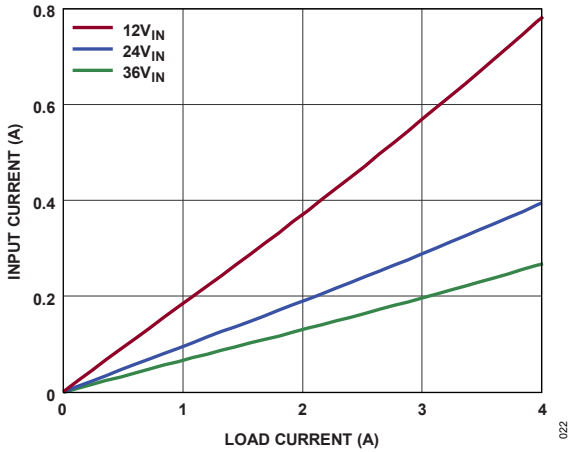


Figure 22. Input vs. Load Current, V_{OUT} = 2V, BIAS = 5V, Burst Mode Operation

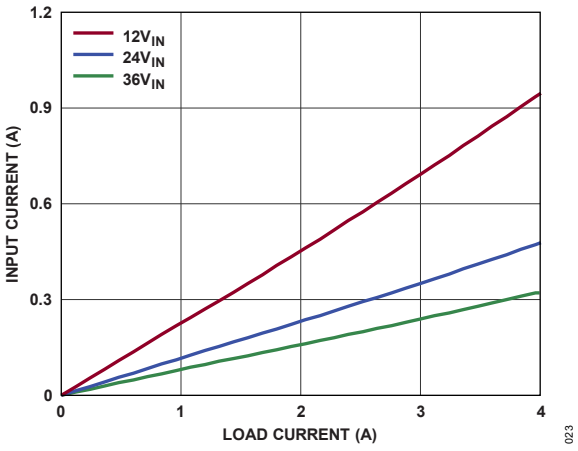


Figure 23. Input vs. Load Current, V_{OUT} = 2.5V, BIAS = 5V, Burst Mode Operation

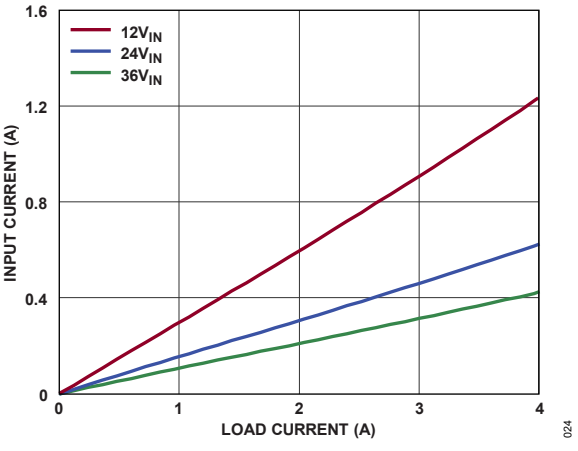


Figure 24. Input vs. Load Current, V_{OUT} = 3.3V, BIAS = 5V, Burst Mode Operation

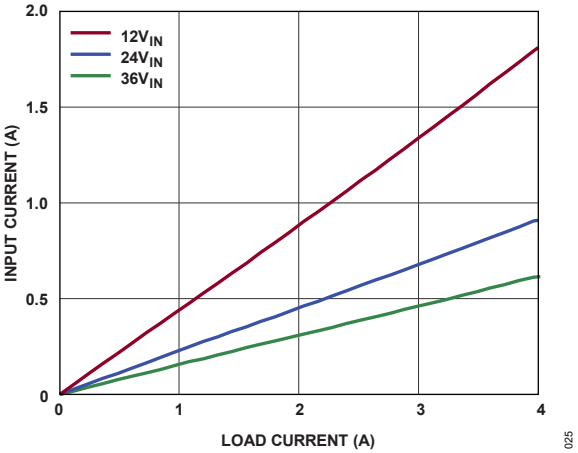


Figure 25. Input vs. Load Current, V_{OUT} = 5V, BIAS = 5V, Burst Mode Operation

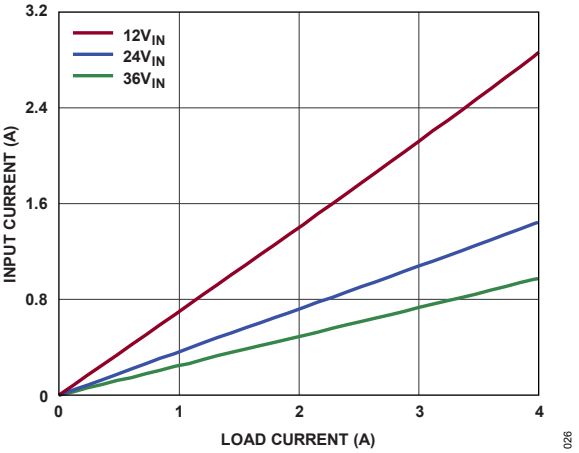


Figure 26. Input vs. Load Current, V_{OUT} = 8V, BIAS = 5V, Burst Mode Operation

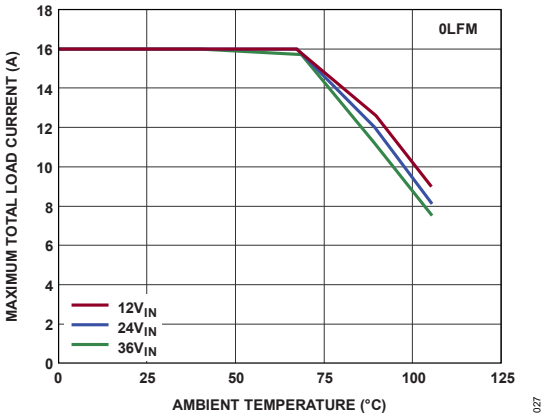


Figure 27. Derating, V_{OUT} = 0.8V, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation, All Channels at the same Load

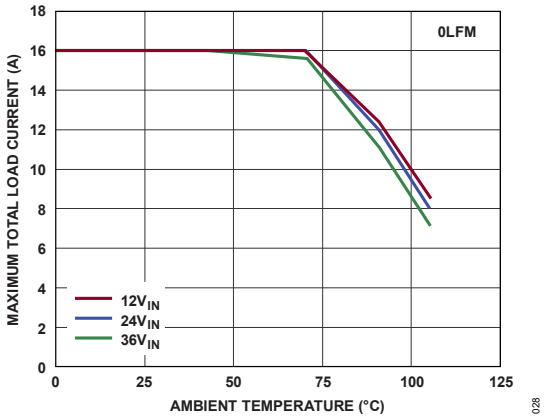


Figure 28. Derating, V_{OUT} = 1V, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation, All Channels at the same Load

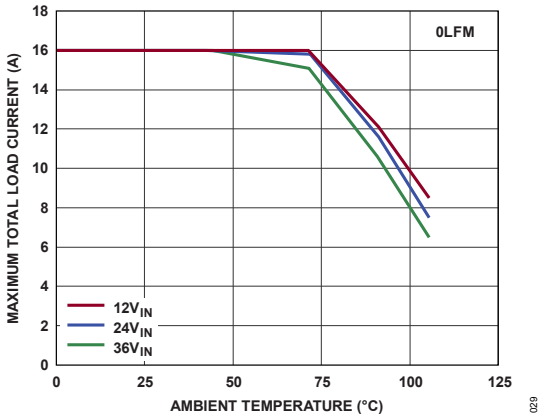


Figure 29. Derating, V_{OUT} = 1.2V, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation, All Channels at the same Load

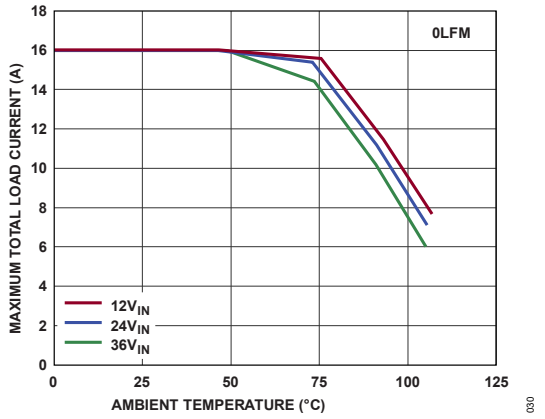


Figure 30. Derating, V_{OUT} = 1.5V, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode, All Channels at the same Load

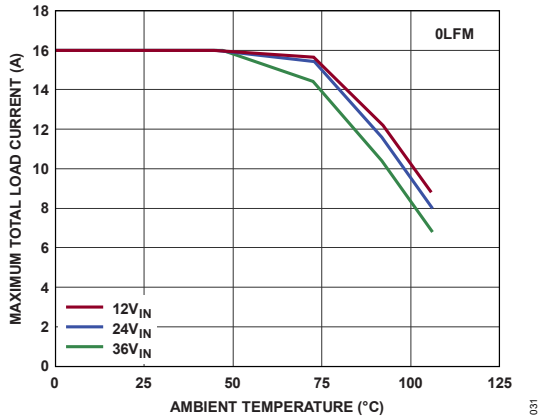


Figure 31. Derating, V_{OUT} = 1.8V, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation, All Channels at the same Load

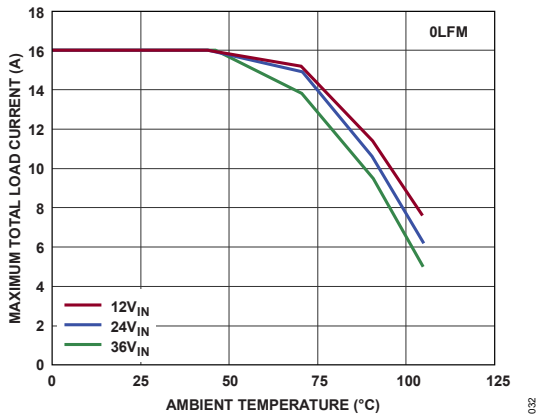


Figure 32. Derating, V_{OUT} = 2V, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation, All Channels at the same Load

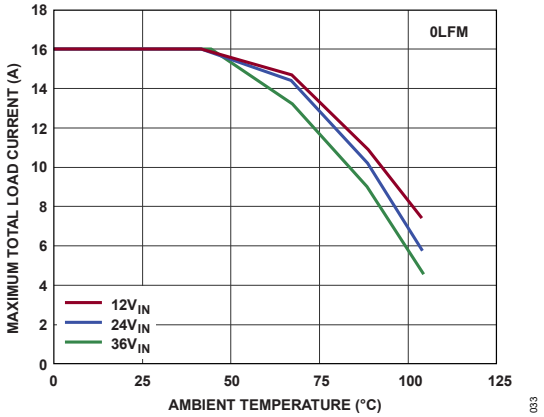


Figure 33. Derating, V_{OUT} = 2.5V, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation, All Channels at the same Load

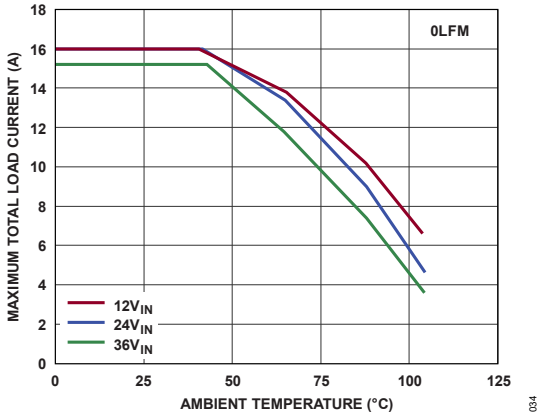


Figure 34. Derating, V_{OUT} = 3.3V, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation, All Channels at the same Load

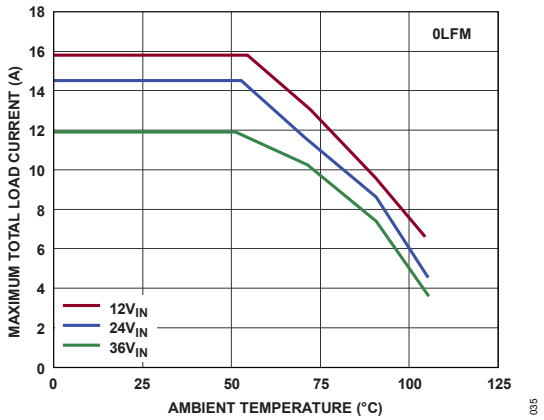


Figure 35. Derating, V_{OUT} = 3.3V, f_{SW} = 2MHz, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation, All Channels at the same Load

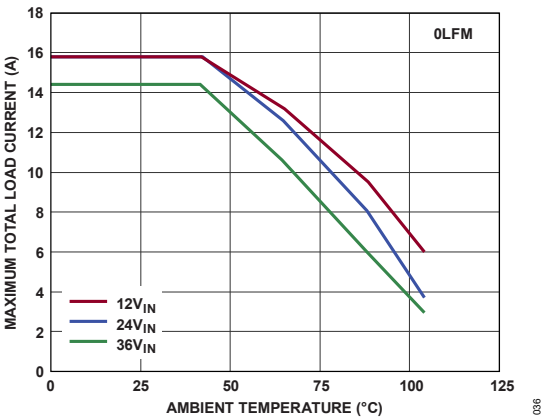


Figure 36. Derating, V_{OUT} = 5V, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation, All Channels at the same Load

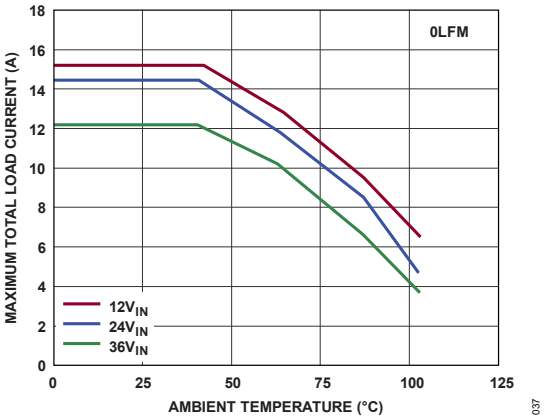


Figure 37. Derating, V_{OUT} = 5V, f_{SW} = 2MHz, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation, All Channels at the same Load

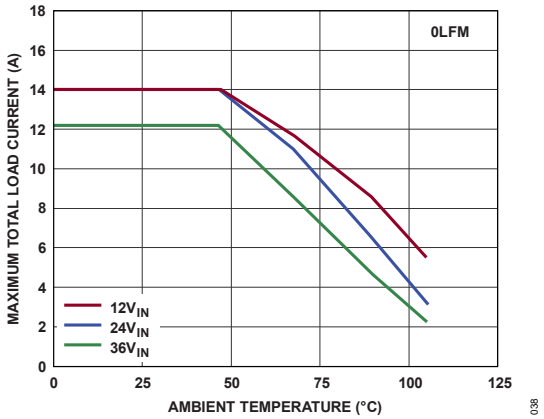


Figure 38. Derating, V_{OUT} = 8V, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation, All Channels at the same Load

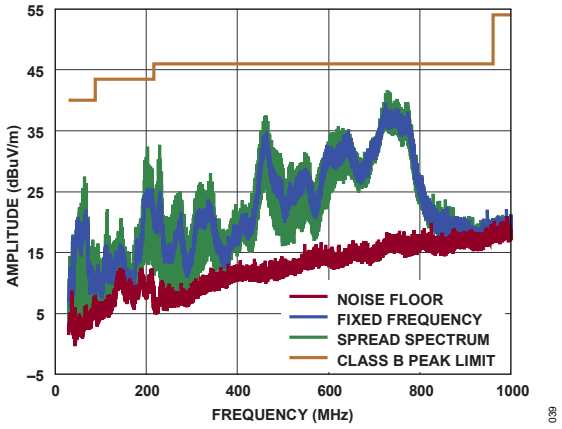


Figure 39. CISPR22 Class B Emissions, DC2820A-B Demo Board, V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 1.2MHz, All Channels Paralleled, I_{OUT} = 10A

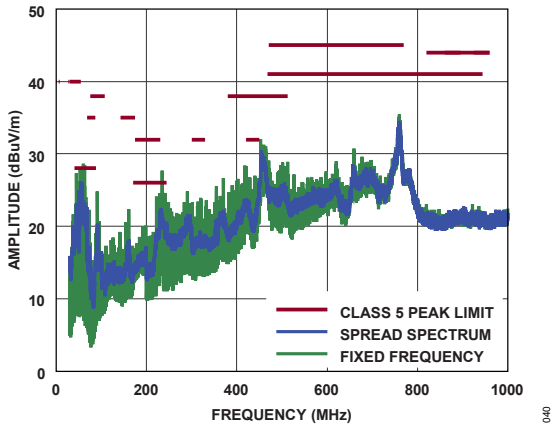


Figure 40. CISPR25 Radiated Emission with Class 5 Peak Limit, DC2820A-B Demo Board, V_{IN} = 14V, V_{OUT} = 5V, f_{SW} = 1.2MHz, All Channels Paralleled, I_{OUT} = 12A

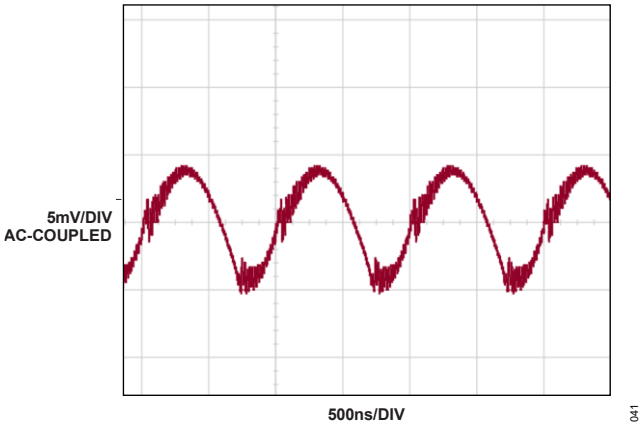


Figure 41. Output Voltage Ripple, DC2820A-B Demo Board, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, f_{SW} = 1MHz

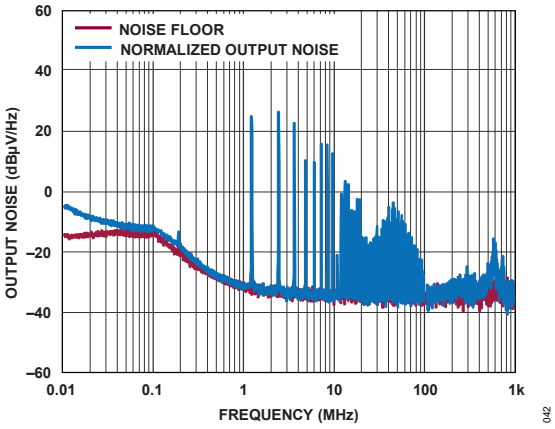


Figure 42. Output Noise Spectrum, DC2820A-B Demo Board, V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 3A, f_{SW} = 1.2MHz

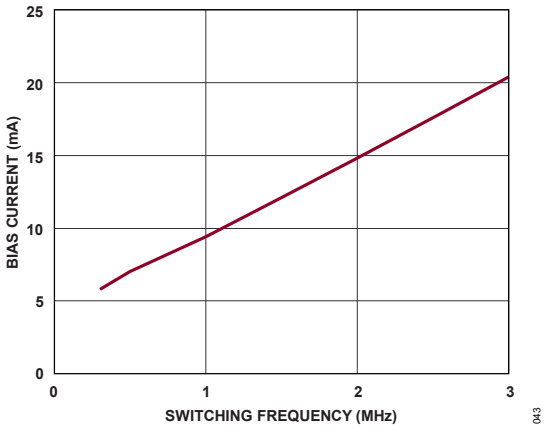


Figure 43. BIAS Current vs. Frequency, 12V_{IN} to 3.3V_{OUT}, FCM

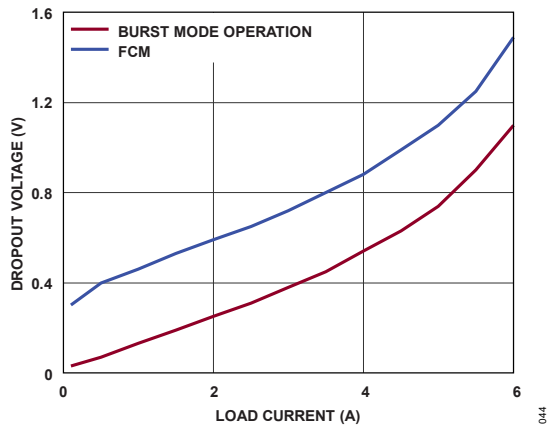


Figure 44. Dropout Voltage vs. Load Current

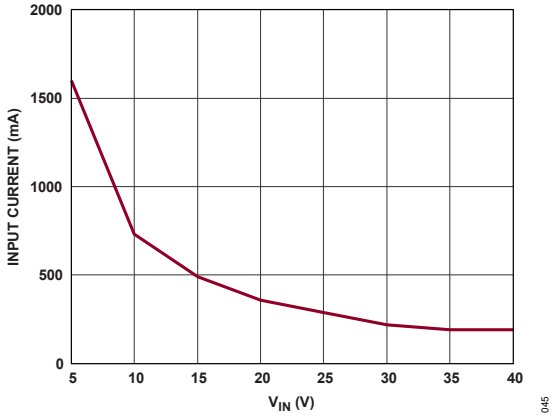


Figure 45. Input Current vs. V_{IN}, V_{OUT} Short-Circuited

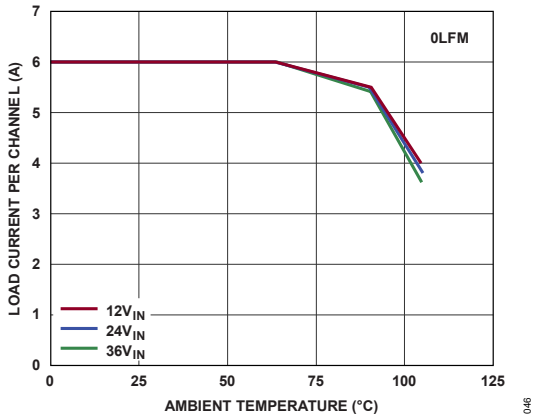


Figure 46. Single Channel Derating, V_{OUT} = 1.5V CH1 ON, CH2 to CH4 OFF, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation

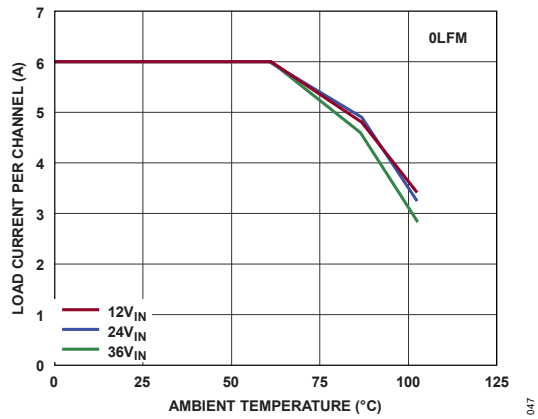


Figure 47. Single Channel Derating, V_{OUT} = 3.3V CH1 ON, CH2 to CH4 OFF, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation

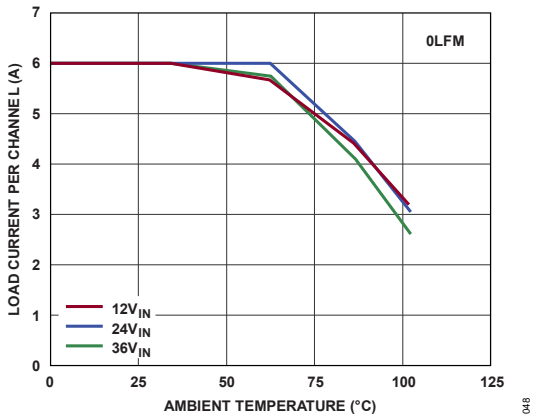


Figure 48. Single Channel Derating, V_{OUT} = 5V CH1 ON, CH2 to CH4 OFF, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation

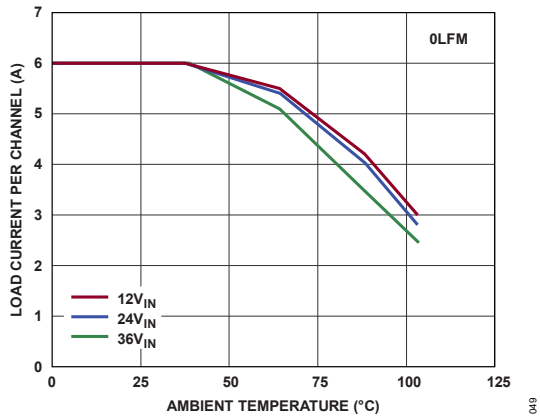


Figure 49. Dual Channel Derating, V_{OUT} = 1.5V CH1/CH3 ON, CH2/CH4 OFF, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation

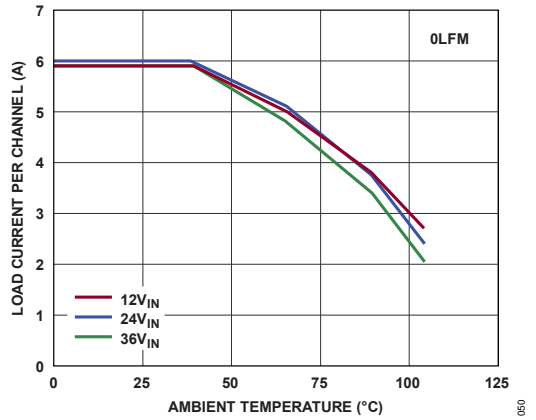


Figure 50. Dual Channel Derating, V_{OUT} = 3.3V CH1/CH3 ON, CH2/CH4 OFF, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation

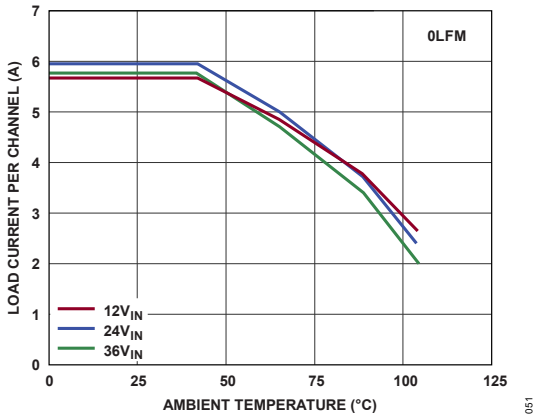


Figure 51. Dual Channel Derating, V_{OUT} = 5V CH1/CH3 ON, CH2/CH4 OFF, BIAS = 5V, DC2820A-B Demo Board, T_J = 120°C, Burst Mode Operation

THEORY OF OPERATION

LTM8060F Overview

The LTM8060F is a quad standalone non-isolated step-down switching dc-to-dc power supply that can deliver a peak current of up to 4A per channel. The continuous current is determined by the internal operating temperature. It provides a precisely regulated output voltage programmable through one external resistor from 0.8V to 8V. The input voltage range for V_{IN1} and V_{IN34} is 3V to 40V, while the input voltage range for V_{IN2} is 2V to 40V.

Given that the LTM8060F is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. The LTM8060F has a fixed f_{SW} peak current mode architecture which supports reliable clock interleaving. See *Figure 52* for the Simplified Block Diagram.

The LTM8060F contains current mode controllers, power switching elements, power inductors, and a modest amount of input and output capacitance. The LTM8060F is a fixed frequency pulse-width modulation (PWM) regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RTn pin to GND.

Internal regulators provide power to the control circuitries. Bias regulators normally draw power from the V_{INn} pin, but if the BIASn pin is connected to an external voltage higher than 3.2V, bias power is drawn from the external source (typically the regulated output voltage). This improves efficiency. Connect BIASn to GND if it is not used.

To enhance efficiency, the LTM8060F automatically switches to Burst Mode operation in light or no-load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to just a few µA.

The TRSSn node acts as an auxiliary input to the error amplifier. The voltage at FBn servos to the TRSSn voltage until TRSSn goes above 0.8V. Soft start is implemented by generating a voltage ramp at the TRSSn pin using an external capacitor, which is charged by an internal 2µA constant current. Alternatively, driving the TRSSn pin with a signal source or resistive network provides a tracking function. Do not drive the TRSSn pin with a low-impedance voltage source. See the *Applications Information* section for more details.

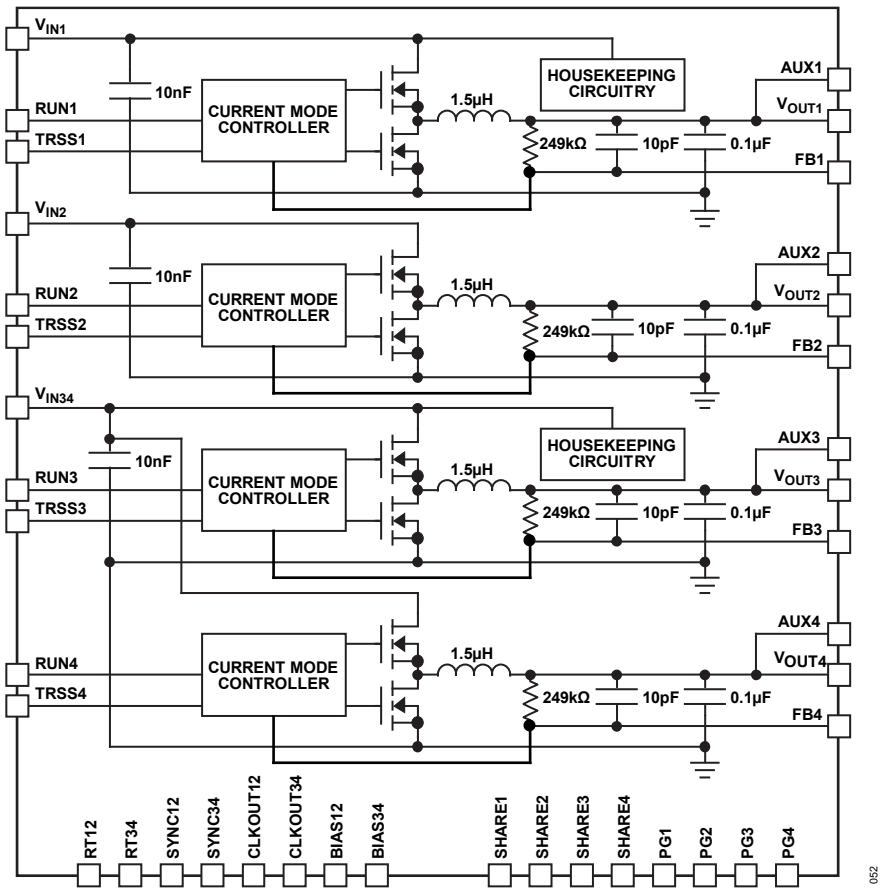


Figure 52. LTM8060F Simplified Block Diagram

The LTM8060F contains power good comparators that trip when the FBn pin is at about ±8% of its regulated value. The PGn output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PGn pin high.

The LTM8060F is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above the maximum temperature rating to avoid interfering with normal operation, so prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

APPLICATIONS INFORMATION

For most applications, the design process is straightforward, and summarized as follows.

1. See *Table 6* and find the row with the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{FB}, and R_T values.
3. Connect BIAS as indicated.

When using the LTM8060F with different output voltages, the higher frequency recommended by *Table 6* will usually result in the best operation. While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load, and environmental conditions. Bear in mind that the maximum output current is limited by the junction temperature, the relationship between the input and output voltage magnitude as well as other factors. See the graphs in the *Typical Performance Characteristics* section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8060F should be allowed to switch is given in *Table 6* in the Maximum f_{SW} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the f_{SW} column. There are additional conditions that must be satisfied if the synchronization function is used. See the *Synchronization* section for details.

Set Output Voltage

The output voltage is programmed with a FB resistor, as shown in *Figure 53*. Choose the resistor value according to Equation *1*.

$$R_{FB} = \frac{249k\Omega}{\frac{V_{OUT}}{0.8V}} - 1 \qquad (1)$$

A 1% resistor is recommended to maintain output voltage accuracy.

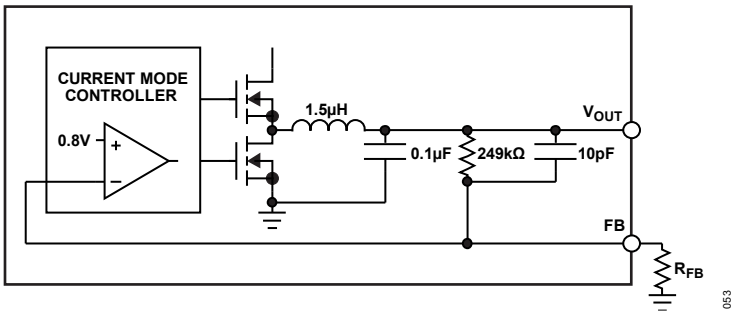


Figure 53. Set Output Voltage with a FB Resistor

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in *Table 6* are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in *Table 6* is not recommended and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load, and environmental conditions.

The ceramic capacitors are small, robust, and have very low ESR. However, not all ceramic capacitors are suitable. The X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types,

including Y5V, and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit, they may have only a small fraction of their nominal capacitance, resulting in a much higher output voltage ripple than expected. The ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8060F's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8060F operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this audible noise is unacceptable, use a high-performance electrolytic capacitor at the output. It may also be a paralleled combination of a ceramic capacitor and a low-cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8060F. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM8060F circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation can be avoided easily; see the *Hot-Plugging Safely* section.

Table 6. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN} [1] (V)	V_{OUT} (V)	R_{FB} (Ω)	C_{IN} [2] (µF)	C_{OUT} (µF)	BIAS	C_{FF} (pF)	f_{SW} (Hz)	R_T (kΩ)	MAX f_{SW} (Hz)	MIN R_T (kΩ)
3 to 40	0.8	Open	4.7 50V X5R 1206	2 × 100 4V X5R 0805	3.2 to 10	100	400k	100	600k	64.9
3 to 40	1	1M	4.7 50V X5R 1206	2 × 100 4V X5R 0805	3.2 to 10	100	400k	100	725k	52.3
3 to 40	1.2	499k	4.7 50V X5R 1206	2 × 100 4V X5R 0805	3.2 to 10	68	500k	76.8	875k	42.2
3.2 to 40	1.5	287k	4.7 50V X5R 1206	2 × 100 4V X5R 0805	3.2 to 10	–	600k	64.9	1M	35.7
3.5 to 40	1.8	200k	4.7 50V X5R 1206	1 × 100 4V X5R 0805	3.2 to 10	–	650k	59	1.3M	25.5
3.5 to 40	2	165k	4.7 50V X5R 1206	1 × 100 4V X5R 0805	3.2 to 10	–	700k	54.9	1.4M	23.2
4.2 to 40	2.5	118k	4.7 50V X5R 1206	1 × 47 4V X5R 0805	3.2 to 10	–	800k	46.4	1.7M	18.2
5.5 to 40	3.3	78.7k	4.7 50V X5R 1206	1 × 47 6.3V X5R 0805	3.2 to 10	–	1M	35.7	2.2M	12.7
8.5 to 40	5	47.5k	4.7 50V X5R 1206	1 × 47 6.3V X5R 1206	3.2 to 10	–	1.2M	27.4	3M	8.06
11 to 40	8	27.4k	4.7 50V X5R 1206	1 × 47 10V X5R 1206	3.2 to 10	–	1.6M	19.6	3M	8.06

[1] The LTM8060F may be capable of the operating at lower input voltages but may skip switching cycles.
[2] A bulk input capacitor is required.

Frequency Selection

The LTM8060F uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 3MHz by using a resistor connected from the RT pin to ground. *Table 7* provides a list of R_T resistor values and their resultant frequencies. The resistors in *Table 7* are standard 1% E96 values.

Operating Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in *Table 7* for the input and output operating conditions. When using the LTM8060F with different output voltages, the higher frequency recommended by *Table 7* will usually result in the best operation. System level or other considerations, however, may necessitate another operating frequency. While the LTM8060F is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat, or even damage the LTM8060F if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

Table 7. Switching Frequency vs. R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.2	200
0.3	137
0.4	100
0.5	76.8
0.6	64.9
0.7	54.9
0.8	46.4
0.9	41.2
1.0	35.7
1.2	27.4
1.4	23.2
1.6	19.6
1.8	16.9
2.0	14.7
2.2	12.7
2.4	11.3
2.6	10.2
2.8	9.09
3.0	8.06

BIASn Pin Considerations

The BIASn pin provides drive power for the internal power switching stage and operates other internal circuitry. For proper operation, it must be powered by at least 3.2V. If the output voltage is programmed to 3.2V or higher, BIASn may be simply connected to V_{OUTn}. If V_{OUTn} is less than 3.2V, BIASn can be connected to V_{INn} or some other voltage source. If the BIASn pin voltage is too high, the efficiency of the LTM8060F may suffer. The optimum BIASn voltage is dependent upon many factors, such as load current, input voltage, output voltage, and switching frequency. In all cases, ensure that the maximum voltage at the BIASn pin is less than 10V. If BIASn power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the pin. A 1µF ceramic capacitor works well. The BIASn pin may also be connected to GND at the cost of a small degradation in efficiency.

Maximum Load

The maximum practical continuous load that the LTM8060F can drive per channel, while rated at 3A (4A peak), depends upon both the internal current limit and the internal temperature. The internal current limit is designed to prevent damage to the LTM8060F in the case of overload or short-circuit. The internal temperature of the LTM8060F depends upon operating conditions such as the ambient temperature, the power delivered, and the heat-sinking capability of the system. For example, if V_{OUT1} of LTM8060F is configured to regulate at 1.5V, and the other three channels are turned off, V_{OUT1} may continuously deliver 4A from $24V_{IN}$ if the ambient temperature is controlled to less than 60°C. This is much higher than the 3A (4A peak) rating. See the *Typical Performance Characteristics* section. Similarly, if all four channels of the LTM8060F are delivering $3.3V_{OUT}$ and the ambient temperature is 100°C, each channel will deliver at most 1.5A from $24V_{IN}$, which is less than the 3A (4A peak) rating.

Power Derating

Figure 54 through *Figure 56*, power loss curves, can be used in coordination with the load current derating curves (*Figure 57* through *Figure 65*) for calculating an approximate θ_{JA} thermal resistance for the LTM8060F with airflow conditions. The power loss curves are taken at room temperature, and are increased with a 1.35 to 1.4 multiplicative factor at 125°C. These factors come from the fact that the power loss of the regulator increases by about 45% from 25°C to 150°C, thus a 45% spread over 125°C delta equates to ~0.35%/°C loss increase. A 125°C maximum junction minus 25°C room temperature equates to a 100°C increase. This 100°C increase multiplied by 0.35%/°C equals a 35% power loss increase at the 125°C junction, thus the 1.35 multiplier.

The derating curves are plotted with four V_{OUTn} at the same operating condition starting at 16A of total load current and low ambient temperature. The derating curves with the airflow are measured at output voltages of 1.5V, 3.3V and 5V. These are chosen to include the lower and higher output voltage ranges to correlate the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber, along with thermal finite element analysis (FEA) modeling.

The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increases with ambient temperature change and is factored into the derating curves. The junction temperatures are maintained at ~120°C maximum while lowering output current or power while increasing the ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased.

The derived thermal resistances in *Table 8* through *Table 10* for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the power loss curves and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick 6-layer board with two-ounce copper (50µm) for all the layers.

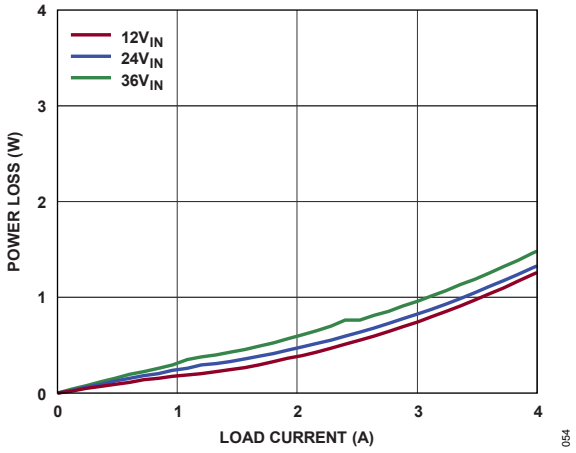


Figure 54. 1.5V$_{OUT}$ Power Loss Curves

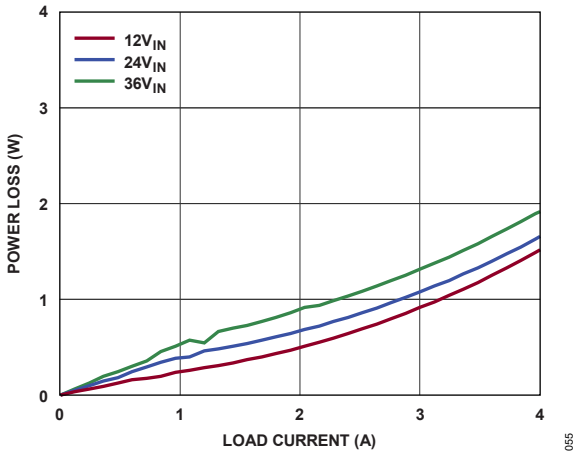


Figure 55. 3.3V$_{OUT}$ Power Loss Curves

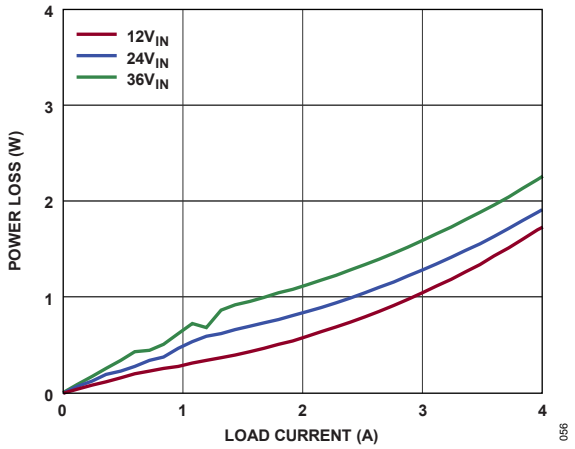


Figure 56. $5V_{OUT}$ Power Loss Curves

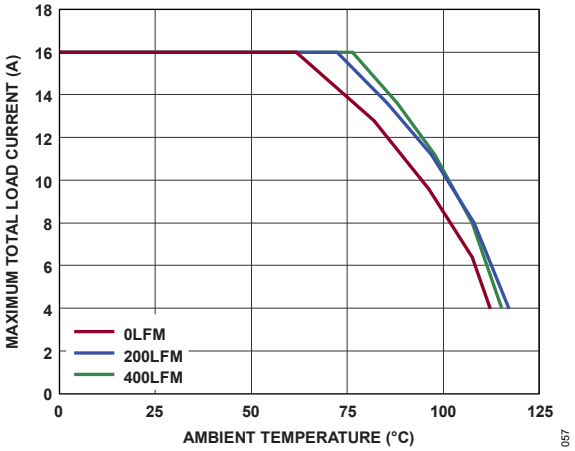


Figure 57. $12V_{IN}$ to $1.5V_{OUT}$ Derating with Airflow

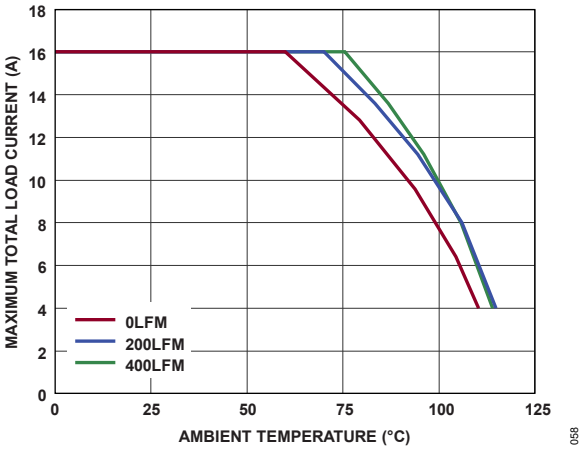


Figure 58. $24V_{IN}$ to $1.5V_{OUT}$ Derating with Airflow

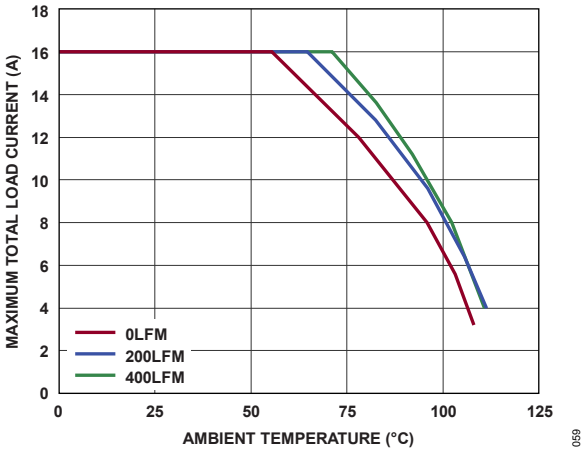


Figure 59. $36V_{IN}$ to $1.5V_{OUT}$ Derating with Airflow

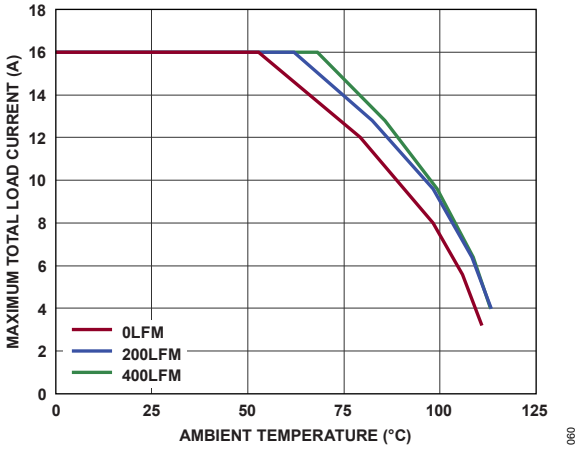


Figure 60. $12V_{IN}$ to $3.3V_{OUT}$ Derating with Airflow

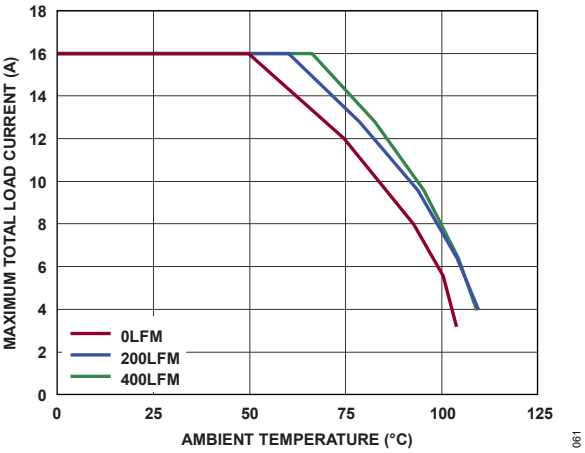


Figure 61. $24V_{IN}$ to $3.3V_{OUT}$ Derating with Airflow

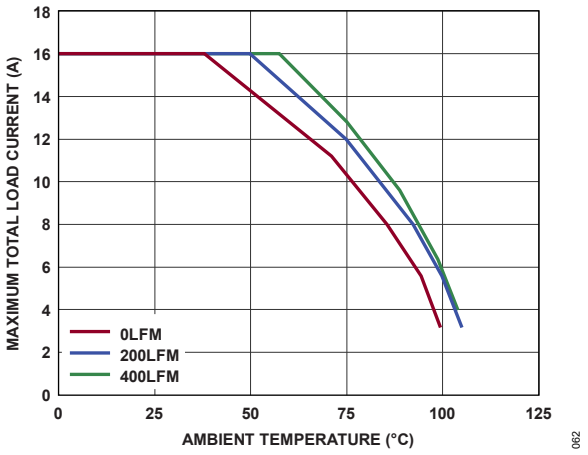


Figure 62. $36V_{IN}$ to $3.3V_{OUT}$ Derating with Airflow

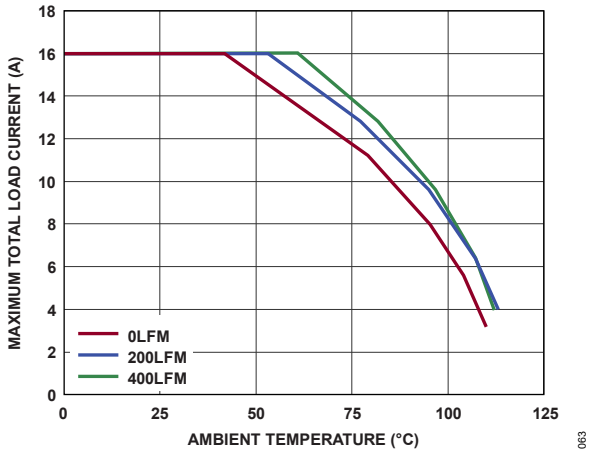


Figure 63. $12V_{IN}$ to $5V_{OUT}$ Derating with Airflow

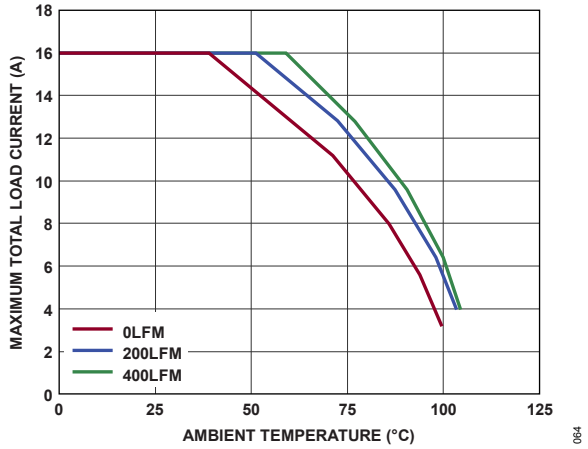


Figure 64. $24V_{IN}$ to $5V_{OUT}$ Derating with Airflow

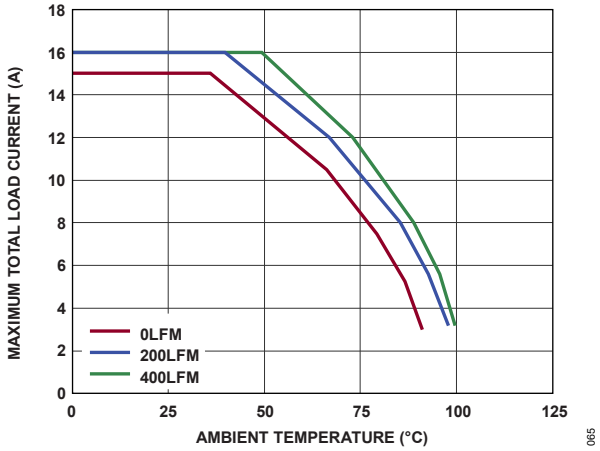


Figure 65. $36V_{IN}$ to $5V_{OUT}$ Derating with Airflow

Table 8. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVES	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 57, Figure 58, Figure 59	12, 24, 36	Figure 54	0	None	9
Figure 57, Figure 58, Figure 59	12, 24, 36	Figure 54	200	None	7.5
Figure 57, Figure 58, Figure 59	12, 24, 36	Figure 54	400	None	6.5

Table 9. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVES	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 60, Figure 61, Figure 62	12, 24, 36	Figure 55	0	None	9
Figure 60, Figure 61, Figure 62	12, 24, 36	Figure 55	200	None	7.5
Figure 60, Figure 61, Figure 62	12, 24, 36	Figure 55	400	None	6.5

Table 10. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVES	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 63, *Figure 64*, *Figure 65*	12, 24, 36	*Figure 56*	0	None	9
Figure 63, *Figure 64*, *Figure 65*	12, 24, 36	*Figure 56*	200	None	7.5
Figure 63, *Figure 64*, *Figure 65*	12, 24, 36	*Figure 56*	400	None	6.5

Load Sharing

The four LTM8060F channels may be paralleled to produce higher currents. To do this on two or more LTM8060F modules, connect the V_{INn}, V_{OUTn}, FBn, and SHAREn pins of all the paralleled channels/modules together. To ensure that paralleled channels startup together, the TRSSn pins may be all connected together, as well. If it is inconvenient to connect the TRSSn pins together, ensure that the same value soft start capacitors are used for each µModule regulator. When load sharing among n units and using a single R_{FB} resistor, the value of the resistor is given by Equation *2*.

$$R_{FB} = \frac{199.2}{n(V_{OUT} - 0.8)}, where\ R_{FB}\ is\ in\ k\Omega \quad (2)$$

Examples of load-sharing applications are given in *Figure 70* through *Figure 73* in the *Typical Applications* section.

Burst Mode Operation

To enhance efficiency at light loads, the LTM8060F automatically switches to Burst Mode operation, which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8060F delivers single-cycle bursts of current to the output capacitor followed by sleep periods where most of the internal circuitry is powered off, and energy is delivered to the load by the output capacitor. During the sleep time, V_{INn} and BIASn quiescent currents are greatly reduced, so, as the load current decreases towards a no-load condition, the percentage of time that the LTM8060F operates in sleep mode increases and the average input current is greatly reduced, resulting in higher light load efficiency.

The Burst Mode operation is enabled by tying SYNC to GND.

Minimum Input Voltage

The LTM8060F is a step-down converter, therefore, a minimum amount of headroom is required to keep the output in regulation. Keep the input above 3V to ensure proper operation. Voltage transients or ripple valleys that cause the input to fall below 3V may turn off the LTM8060F.

The VIN1 must be above 3V for Channel 1 and Channel 2 to operate. If VIN1 is above 3V, Channel 2 will operate if VIN2 is above 2V.

The VIN34 must be above 3V for Channel 3 and Channel 4 to operate.

Output Voltage Tracking and Soft Start

The LTM8060F allows the user to adjust its output voltage ramp rate using the TRSSn pin. An internal 2µA pulls up the TRSSn pin to about 2.4V. Putting an external capacitor on TRSSn enables the soft starting the output to reduce current surges on the input supply. During the soft start ramp the output voltage will proportionally track the TRSSn pin voltage. For output tracking applications, TRSSn can be externally driven by another voltage source. From 0V to 0.8V, the TRSSn voltage will override the internal 0.8V reference input to the error amplifier, thus regulating the FBn pin voltage to that of the TRSSn pin. When TRSSn is above 0.8V, tracking is disabled, and the

feedback voltage will be regulated to the internal reference voltage. The TRSSn pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the TRSSn pin, which will discharge the external soft start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft start capacitor are the RUNn pin transitioning low, V_{INn} voltage falling too low, or thermal shutdown.

Prebiased Output

As discussed in the *Output Voltage Tracking and Soft Start* section, the LTM8060F regulates the output to the FBn voltage determined by the TRSSn pin whenever TRSSn is less than 0.8V. If the LTM8060F output is higher than the target output voltage, and SYNCn is not held below 0.8V, the LTM8060F will attempt to regulate the output to the target voltage by returning a small amount of energy back to the input supply. If nothing is loading the input supply, its voltage may rise. Take care that it does not rise so high that the input voltage exceeds the absolute maximum rating of the LTM8060F. If SYNC is grounded, the LTM8060F will not return current to the input.

Frequency Foldback

The LTM8060F is equipped with frequency foldback, which acts to reduce the thermal and energy stress on the internal power elements during a short circuit or output overload condition. If the LTM8060F detects that the output has fallen out of regulation, the switching frequency is reduced as a function of how far the output is below the target voltage. This in turn limits the amount of energy that can be delivered to the load under fault. During the startup time, frequency foldback is also active to limit the energy delivered to the potentially large output capacitance of the load. When a clock is applied to the SYNCn pin, the SYNCn pin is floated or held high, the frequency foldback is disabled, and the switching frequency will slow down only during overcurrent conditions.

Synchronization

To select low ripple Burst Mode operation, connect the SYNCn pin below about 0.8V (this can be ground or a logic low output). To synchronize the LTM8060F oscillator to an external frequency, connect a square wave (with about 20% to 80% duty cycle) to the SYNCn pin. The square wave amplitude should have valleys that are below 0.8V and peaks above 1.5V.

The LTM8060F may be synchronized over a 200kHz to 3MHz range. The LTM8060F will not enter Burst Mode operation at light output loads while synchronized to an external clock. The R_T resistor should be chosen to set the switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 500kHz or lower.

The LTM8060F features spread-spectrum operation to further reduce electromagnetic interference/electromagnetic interference compatibility (EMI/EMC) emissions. To enable spread-spectrum operation, apply between 2.8V and 4V to the SYNCn pin. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by R_T to about 20% higher than that value. The modulation frequency is about 7kHz. For example, when the LTM8060F is programmed to 2MHz, the frequency will vary from 2MHz to 2.4MHz at a 7kHz rate. When spread-spectrum operation is selected, the Burst Mode operation is disabled, and the part may run in discontinuous-conduction mode.

Shorted Input Protection

Care needs to be taken in systems where the output is held high when the input to the LTM8060F is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR'ed with the LTM8060F's output. If the V_{INn} pin is allowed to float and the RUNn pin is held high (either by a logic signal or because it is connected to V_{INn}), then the LTM8060F's internal circuitry pulls its quiescent current

through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUNn pin, the internal current drops to zero. However, if the V_{INn} pin is grounded while the output is held high, parasitic diodes inside the LTM8060F can pull large currents from the output through the V_{INn} pin. *Figure 66* shows a circuit that runs only when the input voltage is present, and that protects against a shorted or reversed input.

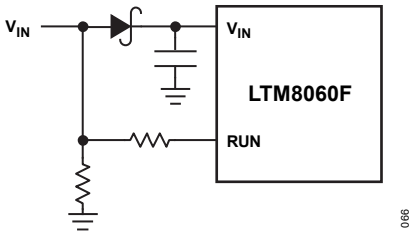


Figure 66. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Connected to the Output. It also Protects the Circuit from a Reversed Input, the LTM8060F Runs only when the Input is Present

PCB Layout

Most of the headaches associated with PCB layout design have been alleviated or even eliminated by the high level of integration of the LTM8060F. The LTM8060F is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See *Figure 67* for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place the R_{FB} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8060F.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8060F.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flows directly adjacent to or underneath the LTM8060F.
5. Connect all the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8060F.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the PCB. Pay attention to the location and density of the thermal vias in *Figure 67*. The LTM8060F can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the PCB design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

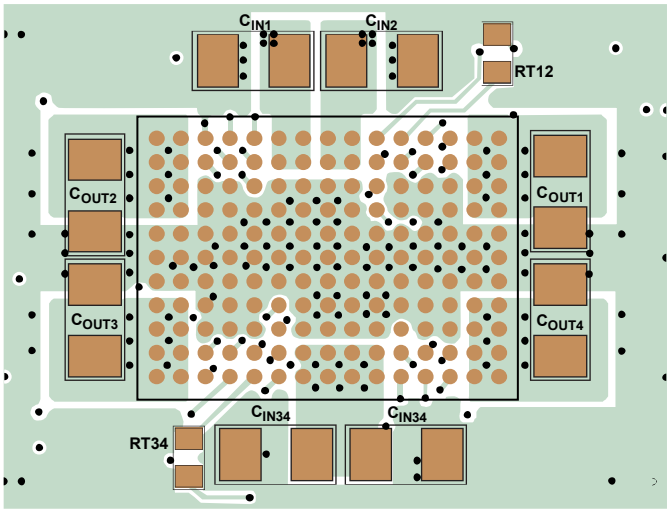


Figure 67. Layout Showing Suggested External Components, GND Plane, and Thermal Vias

Hot-Plugging Safely

The small size, robustness, and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8060F. However, these capacitors can cause problems if the LTM8060F is plugged into a live supply (Refer to the *Application Note 88* for a complete discussion). The low-loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{INn} pin of the LTM8060F can ring to more than twice the nominal input voltage, possibly exceeding the LTM8060F's rating and damaging the part. If the input supply is poorly controlled or the LTM8060F is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{INn}, but the most popular method of controlling input voltage overshoot is adding an electrolytic bulk cap to the V_{INn} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low-frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Thermal Considerations

The LTM8060F output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power, and ambient temperature. The derating curves shown in the *Typical Performance Characteristics* section can be used as a guide. These curves were generated by the LTM8060F mounted to a 104cm^2 6-layer FR4 PCB. Boards of other sizes and layer counts can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load, and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA or computational fluid dynamics (CFD) to predict thermal performance. To that end, the pin configuration typically gives three dominant thermal coefficients:

1. θ_{JA} – Thermal resistance from junction to ambient.
2. θ_{JCbot} – Thermal resistance from the junction to the bottom of the product case.
3. θ_{JCtop} – Thermal resistance from the junction to the top of the product case.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD5112 and are quoted or paraphrased as follows.

1. θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in one cubic foot sealed enclosure. This environment is sometimes referred to as “still air,” although natural convection causes the air to move. This value is determined with the part mounted to a JESD519-defined test board, which does not reflect an actual application or viable operating condition.
2. θ_{JCbot} is the junction-to-board thermal resistance with all the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions do not generally match the user’s application.
3. θ_{JCtop} is determined with nearly all the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot}, this value may be useful for comparing packages, but the test conditions do not generally match the user’s application.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use anyone coefficient to correlate to the junction temperature vs. load graphs given in the product’s datasheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all the thermal resistances simultaneously.

A graphical approximation of these dominant thermal resistances is shown in *Figure 68*. Some thermal resistance elements, such as heat flowing out the side of the package, are not defined by the JEDEC standard, and are not shown. The blue resistances are contained within the µModule regulator, and the green is outside.

The die temperature of the LTM8060F must be lower than the maximum rating, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8060F. The bulk of the heat flow out of the LTM8060F is through the bottom of the package and the pads into the PCB. Consequently, a poor PCB design can cause excessive heating, resulting in impaired performance or reliability. See the *PCB Layout* section for a design suggestion.

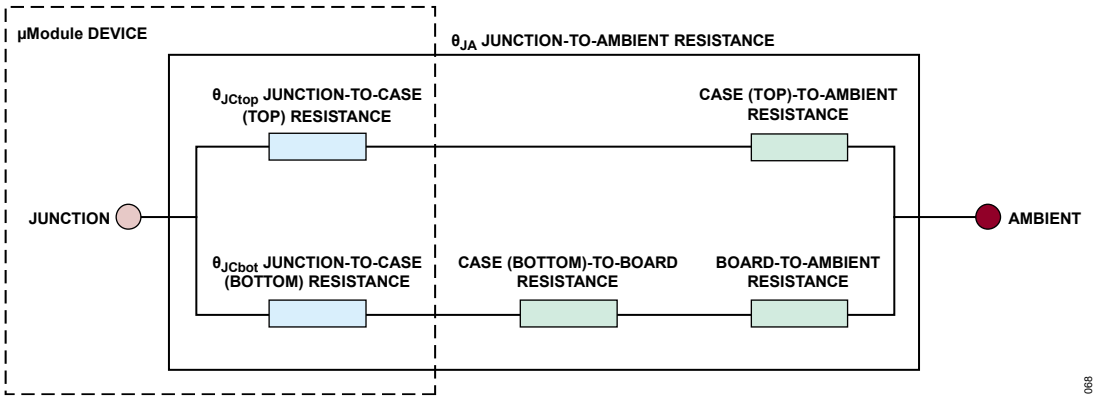


Figure 68. Graphical Representation of Thermal Coefficients, Including the JESD5112 Terms

Typical Applications

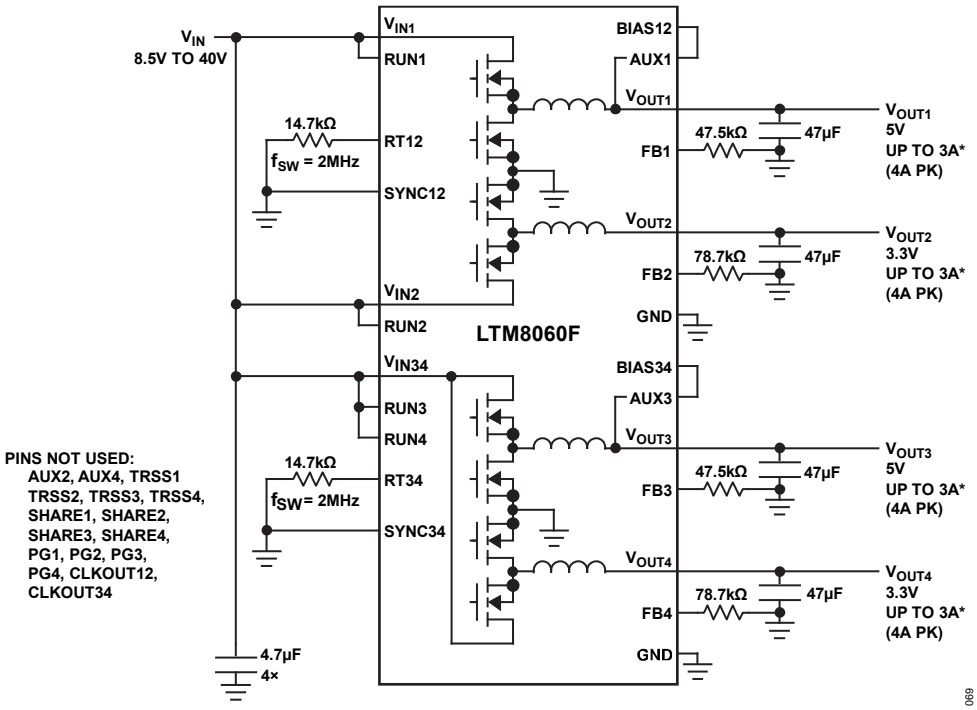


Figure 69. 8.5V to 40V Input to 5V at 3A (4A Peak), 3.3V at 3A (4A Peak), 5V at 3A (4A Peak), and 3.3V at 3A (4A Peak)

*Output current capability (transient peak or continuous) is subject to environmental factors such as ambient temperature, airflow, or other cooling techniques. For different VIN, VOUT, and TA conditions, see the notes section (Note *3*) of the *Electrical Characteristics* table and the derating curves in the *Applications Information* section.

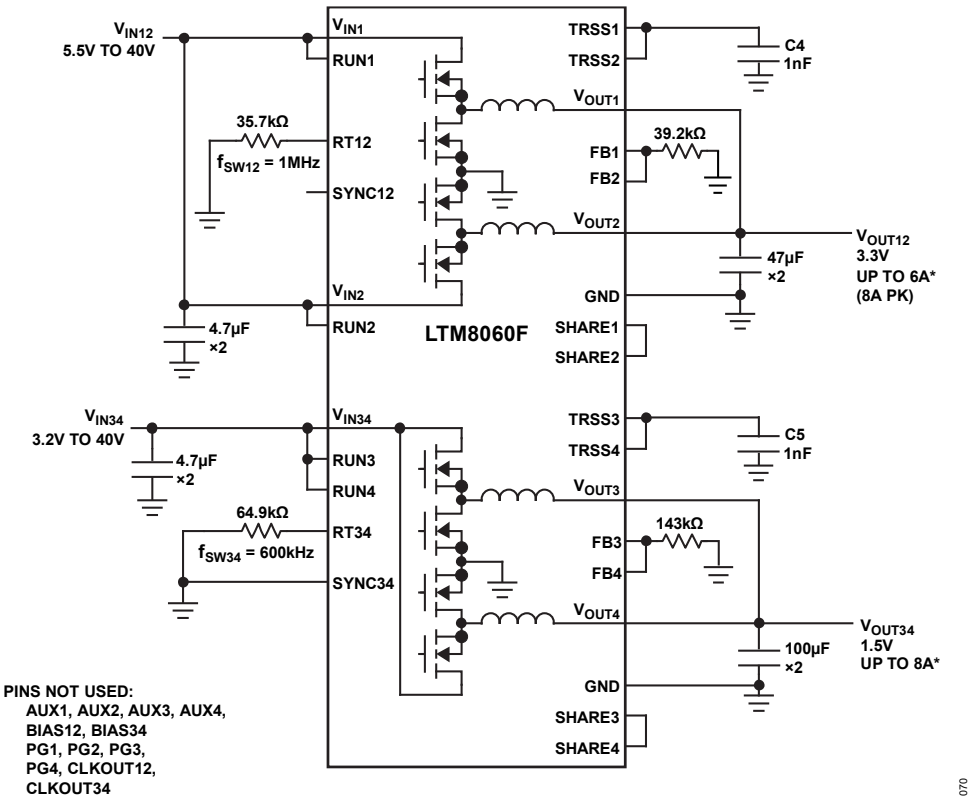


Figure 70. 5.5V to 40V Input to Paralleled 3.3V at 6A (8A Peak), 3.2V to 40V Input to Paralleled 1.5V at 8A

*Output current capability (transient peak or continuous) is subject to environmental factors such as ambient temperature, airflow, or other cooling techniques. For different VIN, VOUT, and TA conditions, see the notes section (Note *3*) of the *Electrical Characteristics* table and the derating curves in the *Applications Information* section.

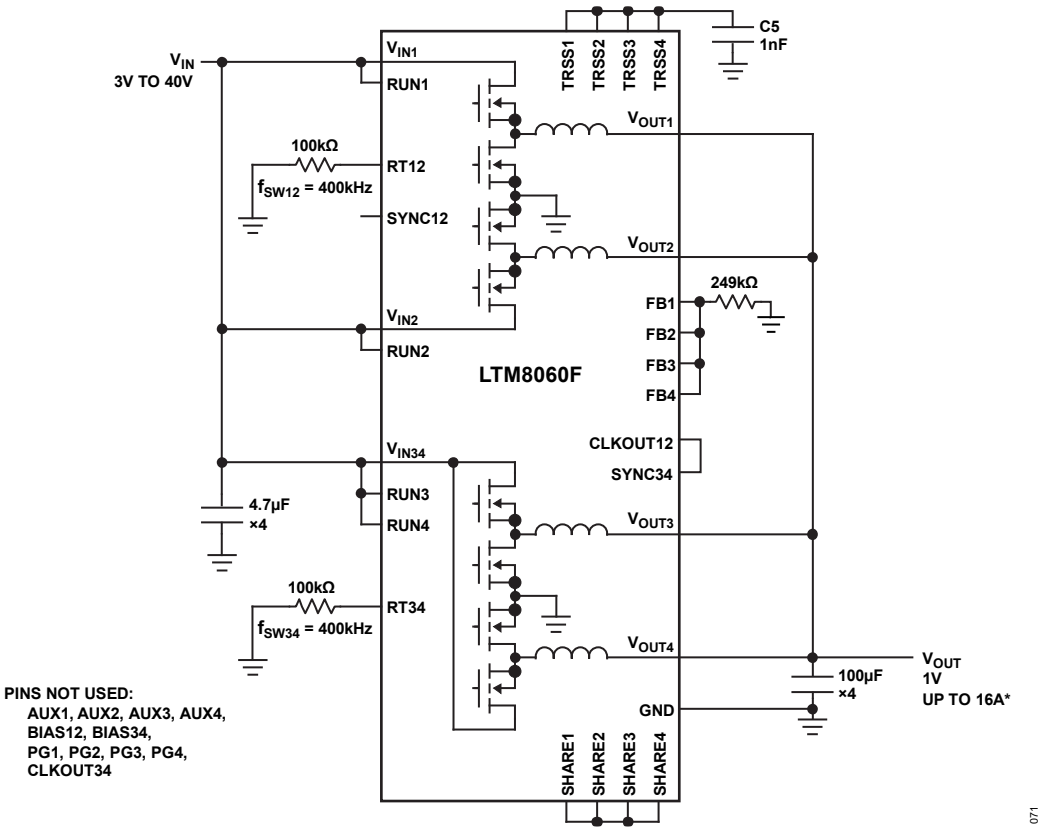


Figure 71. 3V to 40V Input to Paralleled 1V at 16A

*Output current capability (transient peak or continuous) is subject to environmental factors such as ambient temperature, airflow, or other cooling techniques. For different VIN, VOUT, and TA conditions, see the notes section (Note *3*) of the *Electrical Characteristics* table and the derating curves in the *Applications Information* section.

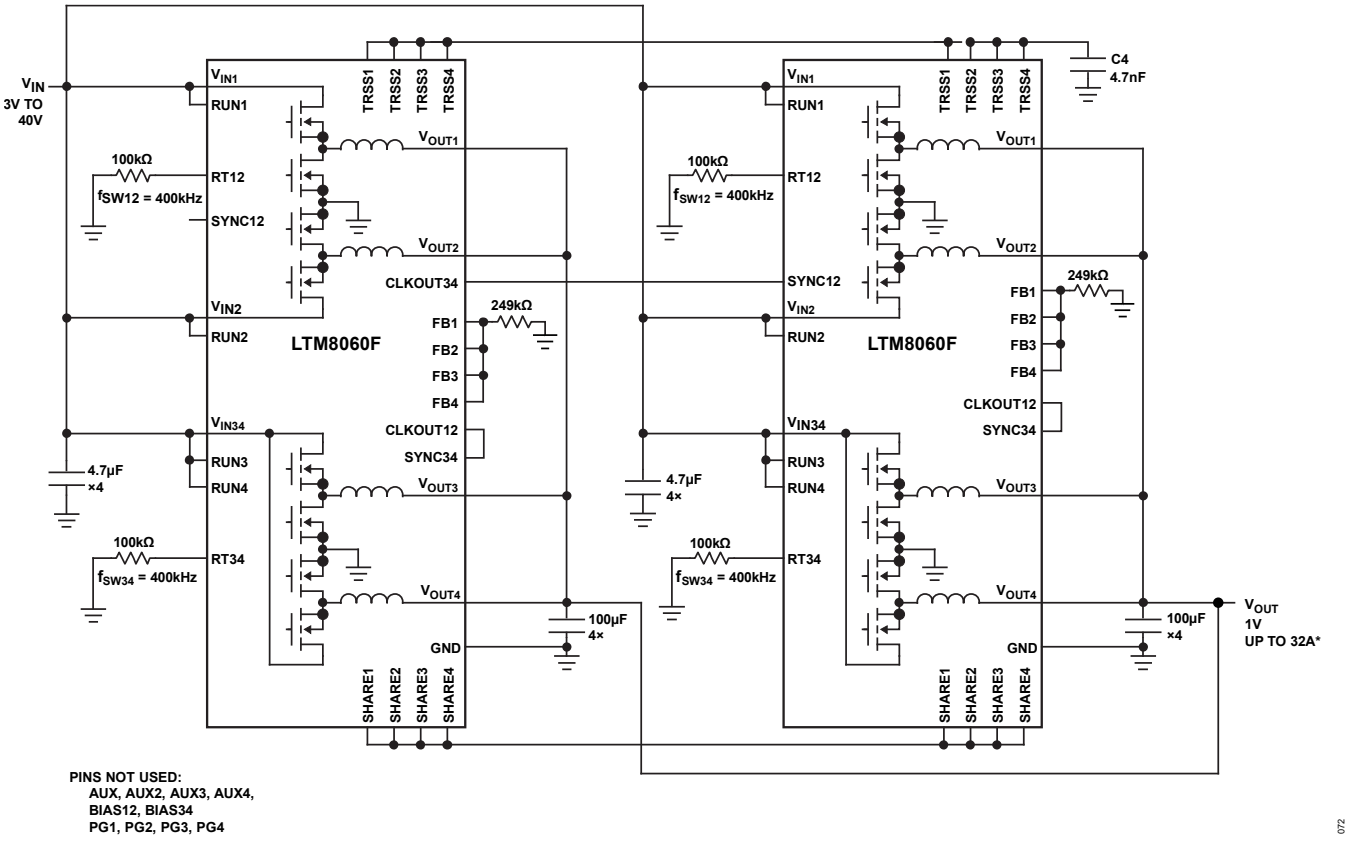


Figure 72. Two LTM8060F are Paralleled to Supply 1V at 32A Output in FCM

*Output current capability (transient peak or continuous) is subject to environmental factors such as ambient temperature, airflow, or other cooling techniques. For different VIN, VOUT, and TA conditions, see the notes section (Note *3*) of the *Electrical Characteristics* table and the derating curves in the *Applications Information* section.

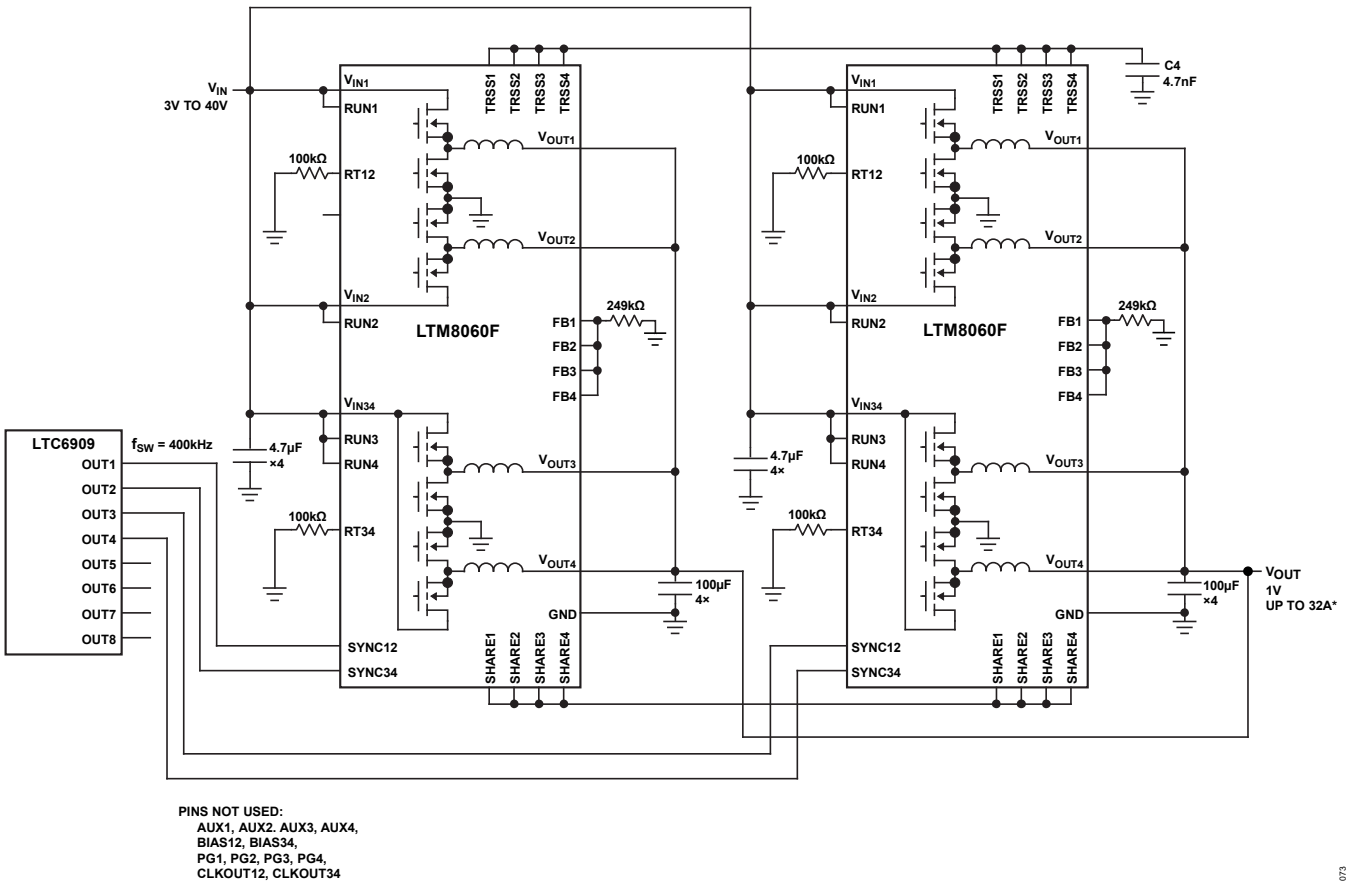


Figure 73. Two LTM8060F are Paralleled to Supply 1V at 32A Output with 45° Phase-Shift Interleaving Through All Eight Channels

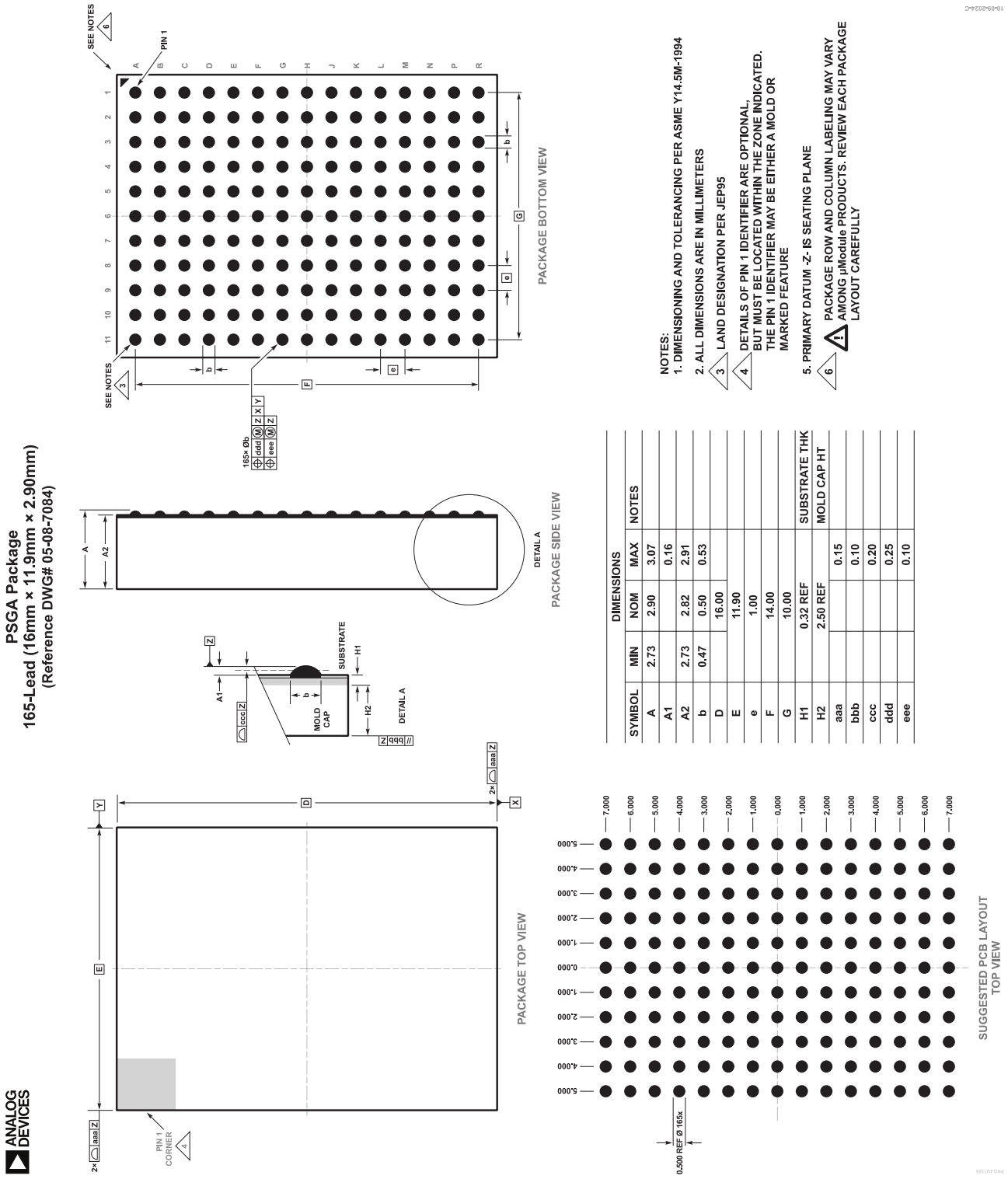
*Output current capability (transient peak or continuous) is subject to environmental factors such as ambient temperature, airflow, or other cooling techniques. For different VIN, VOUT, and TA conditions, see the notes section (Note *3*) of the *Electrical Characteristics* table and the derating curves in the *Applications Information* section.

Related Parts

Table 11. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LTM8063	40V, 2A step-down Silent Switcher µModule regulator	3.2V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 15V, 4mm × 6.25mm × 2.22mm BGA package
LTM8065	40V, 2.5A step-down Silent Switcher µModule regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 18V, 6.25mm × 6.25mm × 2.32mm BGA package
LTM8053	40V, 3.5A step-down Silent Switcher µModule regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 15V, 6.25mm × 9mm × 3.32mm BGA package
LTM8078	40V, dual 1.4A step-down Silent Switcher µModule regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 10V, 6.25mm × 6.25mm × 2.32mm BGA package
LTM8024	40V, dual 3.5A step-down Silent Switcher µModule regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 9mm × 11.25mm × 3.32mm BGA package
LTM8051	40V, quad 1.2A step-down Silent Switcher µModule regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 6.25mm × 11.25mm × 2.32mm BGA package
LTM8060	40V, quad 3A step-down Silent Switcher µModule regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 16mm × 11.9mm × 3.32mm BGA package
LTM8073	60V, 3A step-down µModule regulator	3.4V ≤ V_{IN} ≤ 60V, 0.85V ≤ V_{OUT} ≤ 15V, 6.25mm × 9mm × 3.32mm BGA package
LTM8071	60V, 5A step-down Silent Switcher µModule regulator	3.6V ≤ V_{IN} ≤ 60V, 0.97V ≤ V_{OUT} ≤ 15V, 9mm × 11.25mm × 3.32mm BGA package
LTM4644	Quad 4A, 14V step-down µModule regulator	4V ≤ V_{IN} ≤ 14V, 0.6V ≤ V_{OUT} ≤ 5.5V, 9mm × 15mm × 5.01mm BGA package
LTM4643	Quad 3A, 20V Step-Down µModule regulator	4V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 3.3V, 9mm × 15mm × 1.82mm LGA and 9mm × 15mm × 2.42mm BGA packages

OUTLINE DIMENSIONS



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.73	2.90	3.07	
A1			0.16	
A2	2.73	2.82	2.91	
b	0.47	0.50	0.53	
D		16.00		
E		11.90		
e		1.00		
F		14.00		
G		10.00		
H1		0.32 REF		SUBSTRATE THK
H2		2.50 REF		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.25	
eee			0.10	

Figure 74. 165-Pin, 16mm × 11.9mm × 2.9mm, Pre-Soldered Grid Array (PSGA)

ORDERING GUIDE

Table 12.Ordering Guide

MODEL	TEMPERATURE RANGE[1]	PACKAGE DESCRIPTION	PACKAGE OPTION
LTM8060FEV#PBF	–40°C to 125°C	LTM8060FV part marking SAC305 (RoHS) pad finish* E1 finish code Moisture sensitivity level 4 (MSL 4) rated device	*165-Pin, 16mm × 11.9mm × 2.9mm, Pre-Soldered Grid Array (PSGA)*
LTM8060FIV#PBF	–40°C to 125°C	LTM8060FV part marking SAC305 (RoHS) pad finish E1 finish code Moisture sensitivity level 4 (MSL 4) rated device	*165-Pin, 16mm × 11.9mm × 2.9mm, Pre-Soldered Grid Array (PSGA)*

1 The LTM8060FE is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM8060FI is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

Contact the factory for parts specified with wider operating temperature ranges. *Pad finish code is per IPC/JEDEC J-STD-609. The device temperature grade is indicated by a label on the shipping container.This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to *Recommended LGA and BGA PCB assembly and manufacturing procedures.* The PSGA package should follow BGA assembly and manufacturing procedures.

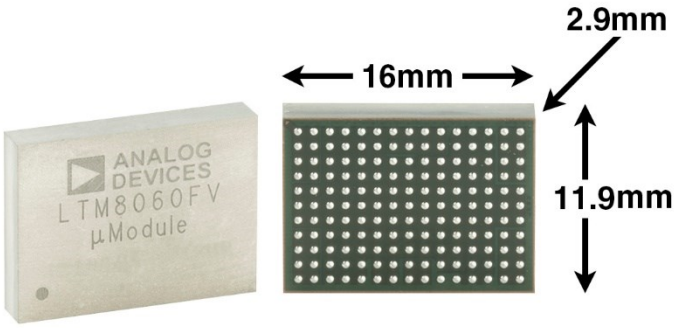
LGA and BGA package and tray drawings.

Table 13.Evaluation Board

PART NUMBER	DESCRIPTION
DC2820A-B	40V_{IN} quad 3A Silent Switcher µModule regulator with EMI shield.

SELECTOR GUIDE

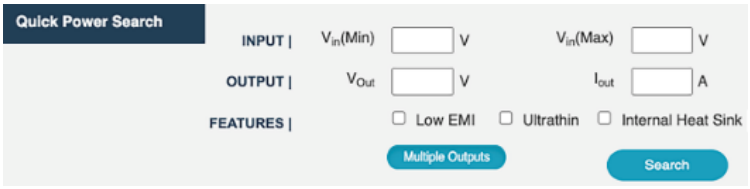
Package Photos



(Part Marking Is Laser Mark)

Design Resources

Table 14.Design Resources

	SUBJECT	DESCRIPTION
µModule Design and Manufacturing Resources	**Design:** ▶ Selector guides ▶ Demo boards and Gerber files. ▶ Free simulation tools	**Manufacturing:** ▶ Quick start guide ▶ PCB design, assembly, and manufacturing guidelines ▶ Package and board level reliability
µModule Regulator Products Search	▶ Sort table of products by parameters and download the result as a spread sheet. ▶ Search using the Quick Power Search parametric table. 	
Digital Power System Management	The Analog Devices family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	