Ultrathin Low V_{IN}, 2A Buck-Boost µModule Regulator

FEATURES

- Wide Input Voltage Range: 2.6V to 5.5V
- Adjustable Output Voltage Range: 1.8V to 5.5V
- 2A of Continuous Output Current with $V_{IN} \geq V_{OUT}$ (Buck Mode and Buck-Boost Mode); Minimum 1A Continuous Output Current with $V_{IN} < V_{OUT}$ (Boost Mode).
- Low Ripple Buck-Boost Architecture
- Programmable Soft-Start and V_{IN} UVLO
- Burst Mode I_Q 15µA for High Efficiency at Light Loads
- Ultrathin, Small Surface Mount Footprint 3.5mm × 4mm × 1.25mm LGA Package

APPLICATIONS

- Telecom, Datacom (Optical Modules) and Industrial Equipment
- Medical and Industrial Instruments
- Wireless RF Transmitter
- Battery Powered System

DESCRIPTION

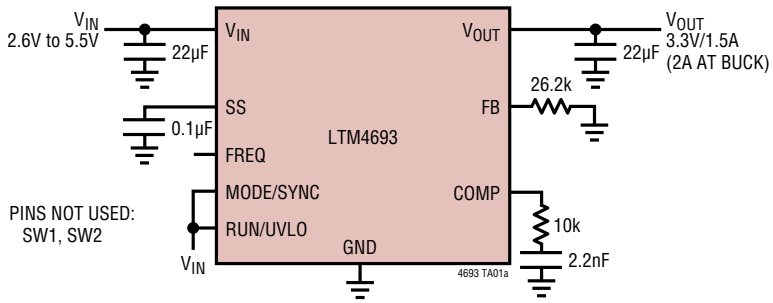
The LTM®4693 is an ultrathin, highly efficient, 2A buck-boost µModule® DC/DC converter that operates from input voltages above, below or equal to the output voltage. Included in the package are the switching controller, power MOSFETs, inductor and support components. The LTM4693's advanced topology provides a continuous transfer through all operating modes. V_{IN} operation from 2.6V to 5.5V covers a wide variety of power sources including typical 3.3V and 5V. Output voltage ranging from 1.8V to 5.5V is set by an external resistor. Only a few external components are needed for a typical application.

Selectable Burst Mode® operation reduces quiescent current to 15µA, ensuring high efficiency across the entire load range. To optimize applications for highest efficiency, the switching frequency can be programmed between 1MHz to 4MHz or synchronized to an external clock for noise sensitive circuits.

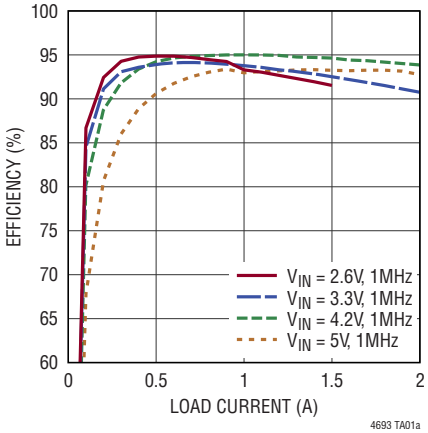
LTM4693 is available in ultrathin, 3.5mm × 4mm ×1.25mm LGA Package. The LTM4693 is Pb-free and RoHS compliant.

TYPICAL APPLICATION

3.3V_{OUT}, 2A DC/DC µModule Regulator



Efficiency at 3.3V_{OUT}



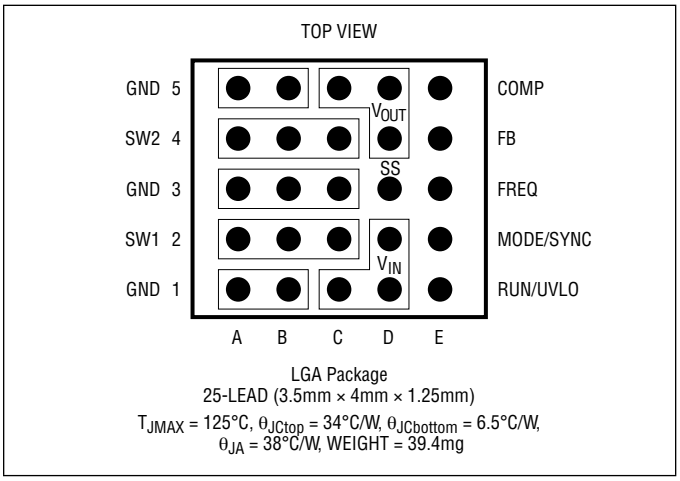
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
- V_{IN}, V_{OUT} ..... –0.3V to 6V
- SW1, SW2 Voltage..... –0.3V to 6V

All Other Pins..... –0.3V to 6V
Operating Junction Temperature
(Note 2)..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature..... 260°C

PIN CONFIGURATION



LGA Package
25-LEAD (3.5mm × 4mm × 1.25mm)
T_{JMAX} = 125°C, θ_{JCtop} = 34°C/W, $\theta_{JCbottom}$ = 6.5°C/W,
θ_{JA} = 38°C/W, WEIGHT = 39.4mg

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		JDEC FINISH CODE	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE				
LTM4693EV#PBF	Au (RoHS)	4693	V	e4	LGA	3	–40°C to 125°C
LTM4693IV#PBF							

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 3.8V, V_{OUT} = 3.3V unless otherwise noted

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage		●	2.6		5.5	V
Output Voltage Range	V_{IN} = 2.6V to 5.5V	●	1.8		5.5	V
Output DC Voltage	R_{FB} = 26.2kΩ			3.3		V
Feedback Pin Voltage		●	0.98	1.0	1.02	V
RUN/UVLO Pin Rising Threshold		●	1.16	1.2	1.24	V
RUN/UVLO Pin Falling Threshold		●	1.06	1.1	1.16	V
RUN/UVLO Pin Input Leakage Current	RUN/UVLO = 5V			1	50	nA
RUN/UVLO Pin Shutdown Threshold		●	0.27	0.45	0.60	V
Shutdown Current: V_{IN}	RUN/UVLO = 0V			1	2	µA
Input Supply Bias Current	MODE = V_{IN}			20		mA
	MODE = GND			15		µA
Output Current Limit				3.5		A
Line Regulation Accuracy	V_{IN} = 2.6V to 5.5V, I_{OUT} = 10mA	 ●		0.06 0.06	0.15 0.7	%/V %/V
Load Regulation Accuracy	I_{OUT} = 0A to 2A (Note 4)	●		0.1	1	%
Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, f_{SW} = 2.2MHz			5		mV
Switching Frequency	External R_T = 90.9kΩ	●	1.9	2.2	2.5	MHz
Oscillator Programmable Frequency Range	Programmed at FREQ, V_{IN} = 2.9V		1		4	MHz
MODE/SYNC Applied Clock Frequency	V_{IN} = 2.9V	●	1		4	MHz
Soft-Start Period	C_{SS} = 2.7nF			2.2		ms
External SS Regulation Voltage	Capacitor to GND Sets SS Time			1		V
Feedback Pin Input Current				0	50	nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

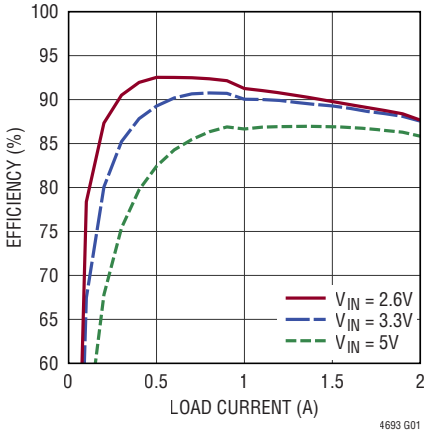
Note 2: The LTM4693 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4693E is guaranteed to meet performance specifications over the 0°C to 85°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4693I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the maximum operating junction temperature may impair device reliability or permanently damage the device.

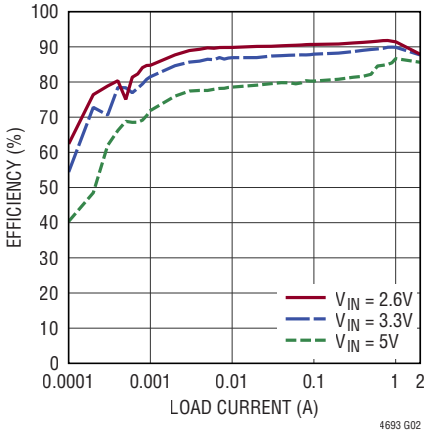
Note 4: See output current derating curves for different V_{IN}, V_{OUT} and ambient temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

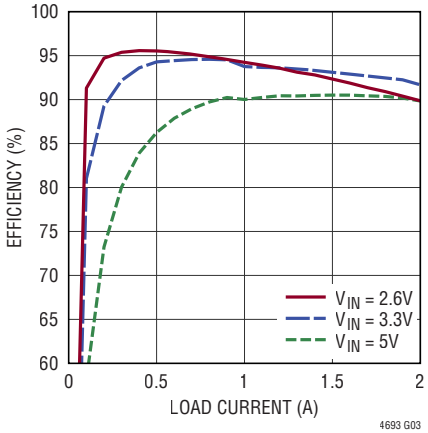
1.8V_{OUT} Efficiency, 1MHz, CCM



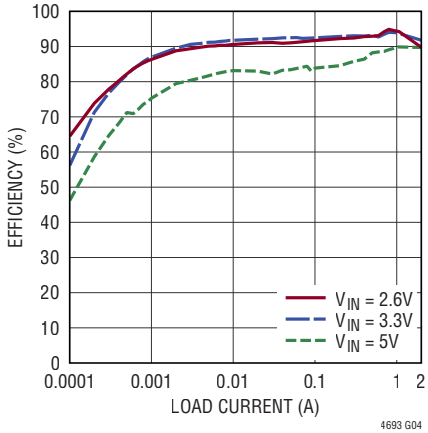
1.8V_{OUT} Efficiency, 1MHz, Burst Mode Operation



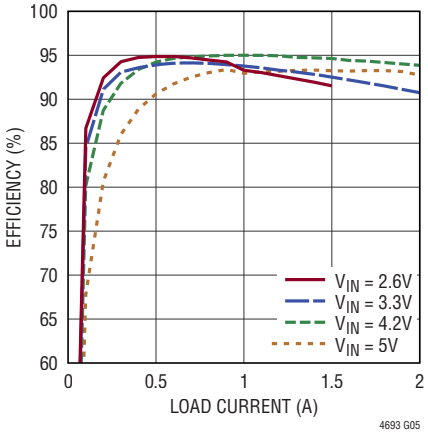
2.5V_{OUT} Efficiency, 1MHz,CCM



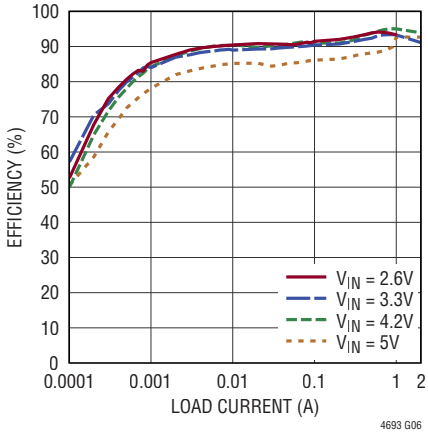
2.5V_{OUT} Efficiency, 1MHz, Burst Mode Operation



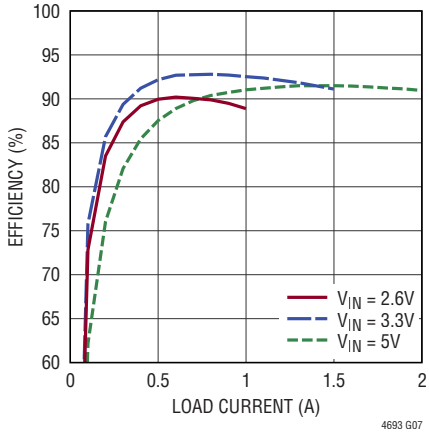
3.3V_{OUT} Efficiency, 1MHz, CCM



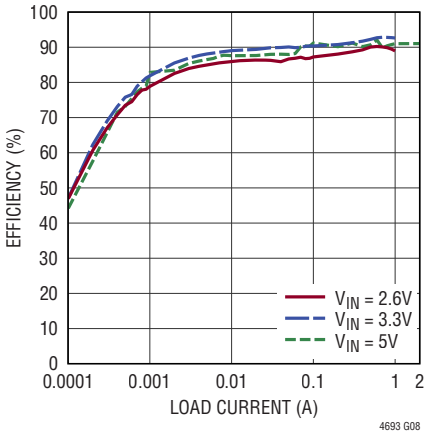
3.3V_{OUT} Efficiency, 1MHz, Burst Mode Operation



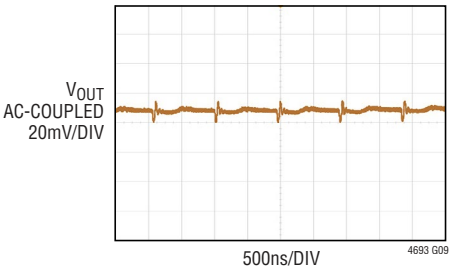
5V_{OUT} Efficiency, 1MHz, CCM



5V_{OUT} Efficiency, 1MHz, Burst Mode Operation



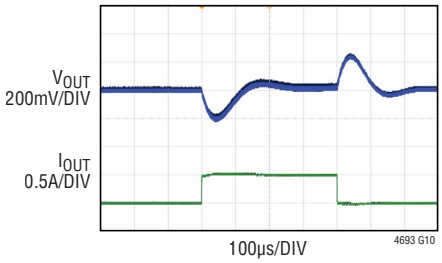
Output Ripple



V_{IN} = 3.3V, V_{OUT} = 3.3V, f_{SW} = 2.2MHz
I_{LOAD} = 0.8A, C_{OUT} = 22µF CERAMIC CAP

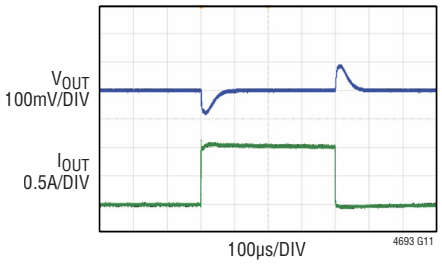
TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient Response $2.6V_{IN}$ to $5V_{OUT}$



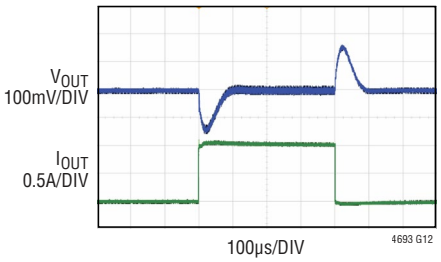
V_{IN} = 2.6V, V_{OUT} = 5V, f_{SW} = 1MHz
C_{OUT} = 2× 22µF CERAMIC CAP
C_{TH} = 2200pF, R_{TH} = 10k
LOAD STEP 1A–1.5A

Load Transient Response $3.3V_{IN}$ to $1.8V_{OUT}$



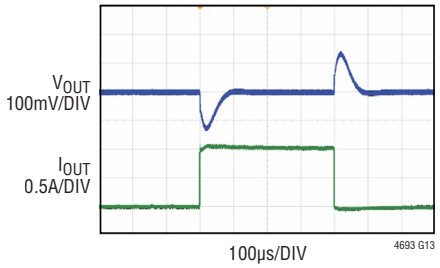
V_{IN} = 3.3V, V_{OUT} = 1.8V, f_{SW} = 1MHz
C_{OUT} = 2× 22µF CERAMIC CAP
C_{TH} = 2200pF, R_{TH} = 10k
LOAD STEP 1A–2A

Load Transient Response $3.3V_{IN}$ to $3.3V_{OUT}$



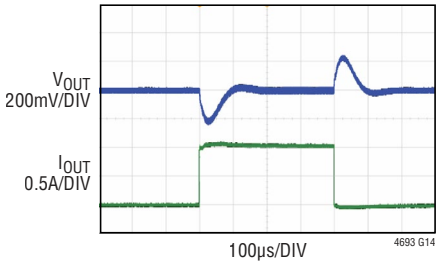
V_{IN} = 3.3V, V_{OUT} = 3.3V, f_{SW} = 1MHz
C_{OUT} = 2× 22µF CERAMIC CAP
C_{TH} = 2200pF, R_{TH} = 10k
LOAD STEP 1A–2A

Load Transient Response $5V_{IN}$ to $3.3V_{OUT}$



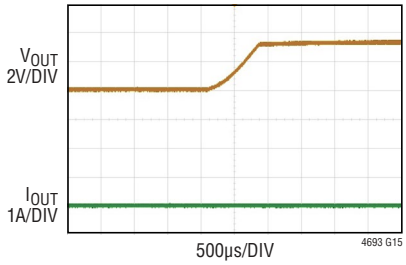
V_{IN} = 5V, V_{OUT} = 3.3V, f_{SW} = 1MHz
C_{OUT} = 2× 22µF CERAMIC CAP
C_{TH} = 2200pF, R_{TH} = 10k
LOAD STEP 1A–2A

Load Transient Response $5V_{IN}$ to $5V_{OUT}$



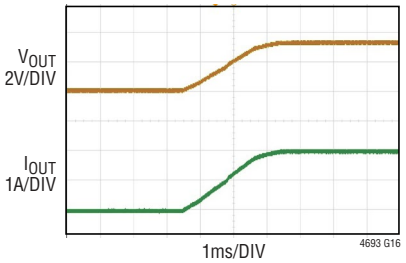
V_{IN} = 5V, V_{OUT} = 5V, f_{SW} = 1MHz
C_{OUT} = 2× 22µF CERAMIC CAP
C_{TH} = 2200pF, R_{TH} = 10k
LOAD STEP 1A–2A

Start-Up with No Load



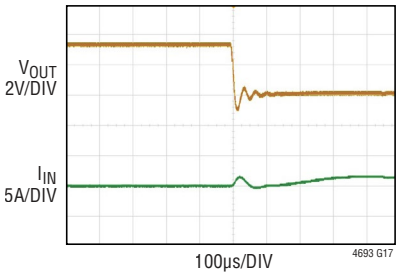
V_{IN} = 3.3V, V_{OUT} = 3.3V, f_{SW} = 1MHz, 0A LOAD
C_{OUT} = 3× 22µF + 3× 2.2µF CERAMIC
SOFT-START CAPACITOR = 0.01µF
USE RUN PIN TO CONTROL START-UP

Start-Up with 2A Load



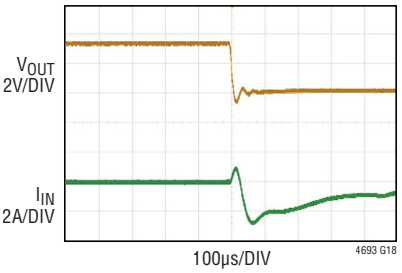
V_{IN} = 3.3V, V_{OUT} = 3.3V, f_{SW} = 1MHz, 2A LOAD
C_{OUT} = 3× 22µF + 3× 2.2µF CERAMIC
SOFT-START CAPACITOR = 0.01µF
USE RUN PIN TO CONTROL START-UP

Short-Circuit with No Load



V_{IN} = 3.3V, V_{OUT} = 3.3V, f_{SW} = 1MHz, 0A LOAD
C_{OUT} = 3× 22µF + 3× 2.2µF CERAMIC

Short-Circuit with 2A Load



V_{IN} = 3.3V, V_{OUT} = 3.3V, f_{SW} = 1MHz, 2A LOAD
C_{OUT} = 3× 22µF + 3× 2.2µF CERAMIC

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

GND (Pins A1, B1, A3, B3, C3, A5, B5): Power Ground Connection. These pins and exposed thermal pad must make full connection to PCB ground plane to meet specific thermal requirements.

SW1 (Pins A2, B2, C2): Buck-Boost Converter Switching Node Pin 1.

SW2 (Pins A4, B4, C4): Buck-Boost Converter Switching Node Pin 2.

V_{IN} (Pins C1, D1, D2): Power Input for Buck-Boost Converter. Connect a minimum 22µF low ESR capacitor to GND as close to the device as possible.

V_{OUT} (Pins C5, D4, D5): Power Output for Buck-Boost Converter. Connect a minimum 22µF low ESR capacitor to GND as close to the device as possible. Capacitor value may change depending on V_{OUT} voltage and load current requirements.

SS (Pin D3): External Soft-Start. Connect to V_{IN} for 2ms default soft-start period. Connect an external capacitor to set soft-start period according to Equation 1.

$$t_{SS}\ (ms) = 0.8 \bullet C_{SS}\ (nF) \qquad (1)$$

RUN/UVLO (Pin E1): Input to Enable the IC. Connect RUN to V_{IN} to enable the LTM4693 at the 2.6V minimum operating voltage. Connect to an external divider from V_{IN} to provide a programmable accurate V_{IN} undervoltage threshold, see application information for details.

MODE/SYNC (Pin E2): Mode Selection and Oscillator Synchronization. Do not leave this pin floating.

MODE/SYNC = High (V_{IN}). Disable Burst Mode operation and maintain low noise, constant frequency PWM operation.

MODE/SYNC = Low (GND). The converter operates in Burst Mode operation.

MODE/SYNC = External CLK. The internal oscillator is synchronized to the external CLK signal, Burst Mode operation is disabled. A clock pulse width between 75ns and t_{period} –75ns is required to synchronize the oscillator. An external resistor must be connected between FREQ and GND to program the oscillator 25% to 50% below the desired synchronization frequency.

FREQ (Pin E3): Oscillator Frequency Programming Input. Default switching frequency is 1MHz when this pin is left floating. Connect an external R_T resistor from FREQ to GND to program the switching frequency from 1MHz to 4MHz according to Equation 2.

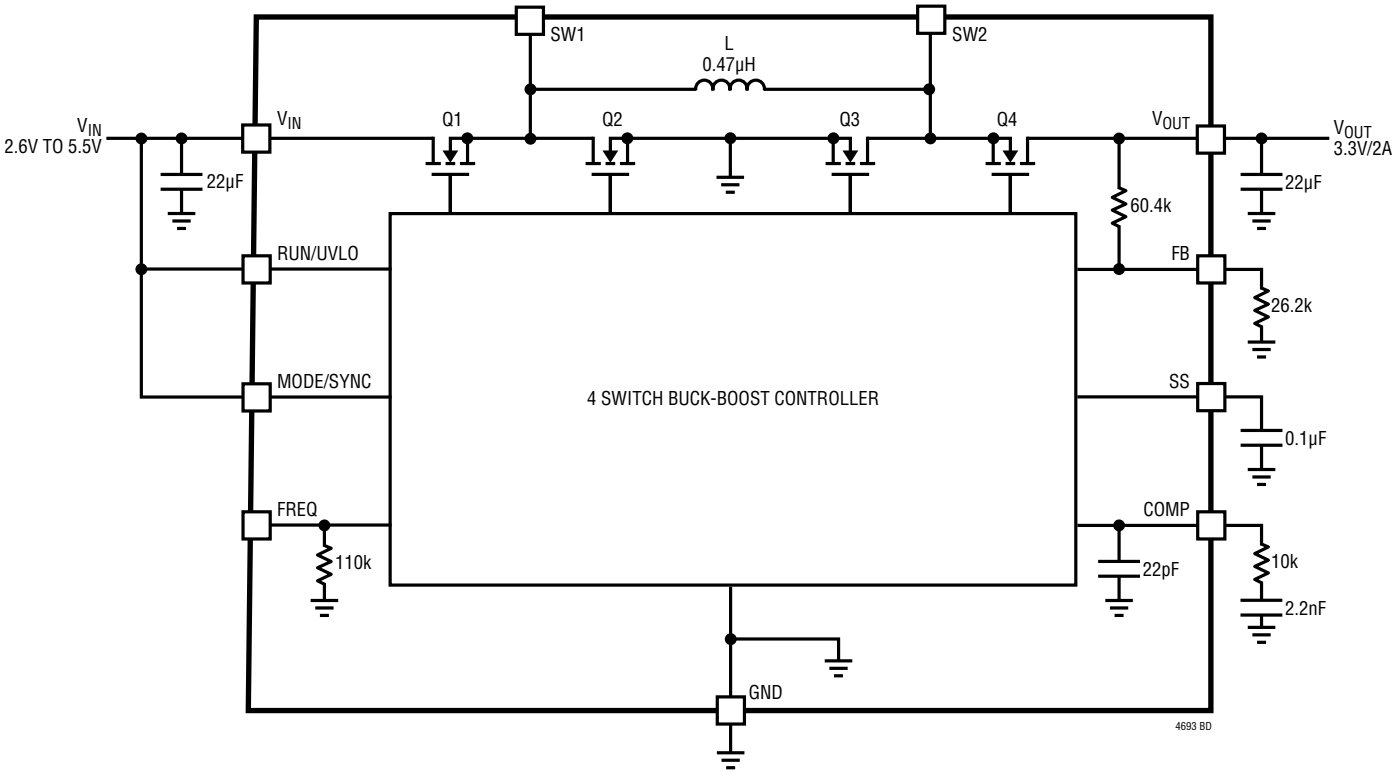
$$R_T\ (k\Omega) = \frac{110}{f_{SW}\ (MHz) - 1} \qquad (2)$$

FB (Pin E4): Feedback Input to Error Amplifier. The resistor connected to this pin sets the converter output voltage (Equation 3).

$$V_{OUT} = 1.0V \bullet \frac{R_{FB} + 60.4k}{R_{FB}} \qquad (3)$$

COMP (Pin E5): The output of the voltage error amplifier used to program average inductor current inside the module. An R-C from this pin to ground sets the voltage loop compensation.

BLOCK DIAGRAM



OPERATION

The LTM4693 is a standalone nonisolated buck-boost switching DC/DC power supply. The buck-boost topology allows the LTM4693 to regulate its output voltage above or below the input voltage, and the maximum output current depends upon the input voltage. In buck and buck-boost region, the converter can source 2A output current, while in boost region, the converter can source at least 1A output current. The low $R_{DS(ON)}$, low gate charge synchronous switches and low DCR inductor inside provide highly efficient power module with a tiny 3.5mm × 4mm × 1.25mm size. The LTM4693 utilizes a proprietary low noise switching algorithm to provide a seamless transition between operating modes. These advantages result in increased efficiency and stability in comparison to the traditional buck-boost converter. A simplified block diagram is given on the previous page.

The LTM4693 provides a precisely regulated output voltage programmable from 1.8V to 5.5V via an external resistor connecting from the FB pin to GND. The input voltage range is from 2.6V to 5.5V.

The LTM4693 utilizes average current mode control for its pulse width modulator. Current mode control, both average and the better known peak method, provide some benefits compared to other control methods including: simplified loop compensation, rapid response to load transients and inherent line voltage rejection. The switching frequency is set by connecting the appropriate resistor value from the FREQ pin to GND. The LTM4693 default frequency is 1MHz, and it can be configured to operate over a wide range of switching frequencies, from 1MHz to 4MHz, allowing applications to be optimized for broad area and efficiency. Driving the MODE/SYNC pin will synchronize the LTM4693 to an external clock.

Burst Mode operation is available in the LTM4693 and is user-selected via the MODE/SYNC input pin. In Burst Mode operation, the LTM4693 provides exceptional efficiency at light output loads by operating the converter only when necessary to maintain voltage regulation. The typical quiescent current in Burst Mode operation is only 15µA at no load. At higher loads, the LTM4693 automatically transitions to fixed frequency PWM operation. Continuous PWM mode can also be selected via the MODE/SYNC pin for low switching ripple and low noise operation.

The LTM4693 features an accurate, resistor programmable RUN/UVLO comparator which allows the buck-boost DC/DC converter to turn on and off at user-selected voltage thresholds depending on the power source. Besides, the soft-start period is also programmable by an appropriate capacitor connecting from SS to GND.

APPLICATIONS INFORMATION

The front page shows a typical LTM4693 application circuit. This Applications Information section serves as a guideline of selecting external components for typical applications. The examples and equations in this section assume continuous conduction mode unless otherwise specified.

V_{IN} UVLO THRESHOLD

The V_{IN} threshold is internally set to a typical value of 1.7V for turn-on and 1.6V for turn-off when RUN/UVLO is connected to V_{IN}. The V_{IN} UVLO can be adjusted to a higher threshold voltage with a resistor network on RUN/UVLO according to Equation 4 and Equation 5.

$$V_{TURN(ON)} = 1.2V \bullet (1+R1/R2) \quad (4)$$

The accurate RUN/UVLO pin threshold has 100mV of hysteresis provided internally.

$$V_{TURN(OFF)} = 1.1V \bullet (1+R1/R2) \quad (5)$$

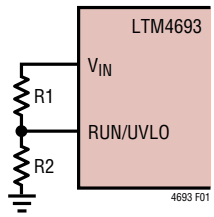


Figure 1. Circuit to Set V_{IN} UVLO

OUTPUT VOLTAGE PROGRAMMING

The PWM controller has an internal 1V reference voltage. As shown in the Block Diagram, a 60.4k internal feedback resistor connects from V_{FB} to V_{OUT}. Adding a resistor R_{FB} from FB pin to GND pin programs the output voltage (Equation 6).

$$V_{OUT} = 1.0V \bullet \frac{60.4k + R_{FB}}{R_{FB}} \quad (6)$$

SETTING THE SWITCHING FREQUENCY

The operating frequency of the LTM4693 is optimized to achieve the compact package size and the minimum output ripple voltage while keeping high efficiency. The default operating frequency is internally set to 1MHz by an internal resistor. In most applications, no additional frequency adjusting is required.

If any operating frequency higher than 1MHz is required by application, the operating frequency can be adjusted by adding a resistor R_T between FREQ pin and GND. The R_T resistor required to set a specific switching frequency can be calculated with Equation 7.

$$R_T(k\Omega) = \frac{110}{f_{SW}(MHz) - 1} \quad (7)$$

The programmable operating frequency range is from 1MHz to 4MHz. The typical value of R_T and the switching frequency is shown as Table 1.

Table 1. R_T Value for Common Switching Frequencies

f_{SW}	R_T
1.0MHz	OPEN
2.0MHz	110kΩ
3.0MHz	55kΩ
4.0MHz	36.5kΩ

The LTM4693 can be synchronized to an external clock applied to the MODE/SYNC pin. The frequency of the external clock must be higher than the internal oscillator frequency as set by the FREQ pin. In order to accommodate the ±20% possible variation in the oscillator frequency, the R_T resistor should be chosen to set the internal oscillator frequency between 25% to 50% below the synchronization frequency. For example, to synchronize to an external 2.5MHz clock, R_T should be selected to set the internal oscillator at 1.9MHz or lower.

APPLICATIONS INFORMATION

SOFT-START

The soft-start circuit linearly ramps the average inductor current during the soft-start period (t_{SS}). An internal soft-start interval of approximately 2ms can be selected by connecting SS to V_{IN}. For applications requiring a longer soft-start period, an external capacitor C_{SS} on SS sets soft-start period according to Equation 8. The total soft-start time can be calculated as:

$$t_{SS}\ (ms) = 0.8 \bullet C_{SS}\ (nF) \qquad (8)$$

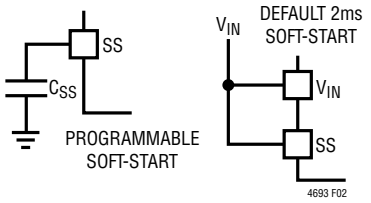


Figure 2. Circuit to Set Soft-Start Time

where C_{SS} is the capacitance on the SS pin.

The soft-start circuit slowly ramps the error amplifier output at V_C. In doing so, the current command of the IC is slowly increased, starting from zero. The soft-start period is defined as the time it takes the SS capacitor to ramp to 0.9V, allowing V_C to command full rated current. In most situations, V_{OUT} comes into regulation without needing full inductor current, resulting in power up times at a fraction of the soft-start period. After initial power up, soft-start can be reset by V_{IN} UVLO asserting, thermal shutdown, or a V_{OUT} short-circuit.

OUTPUT CAPACITORS

A low effective series resistance (ESR) output capacitor should be connected at the output of the buck-boost converter in order to minimize output voltage ripple. Multilayer ceramic capacitor is an excellent option as it has low ESR and is available in small footprint. The capacitor value should be chosen large enough to reduce the output voltage ripple to acceptable levels. The output voltage ripple increases with load current and is generally higher in boost mode than in buck mode. Both output voltage ripple generated across the output capacitance, and output voltage ripple produced across the internal resistance of the output capacitor need to be considered. In most LTM4693 applications, an output capacitor between 68µF and 220µF from V_{OUT} to GND will work well. An additional low value ceramic capacitor such as 4.7µF can be placed between V_{OUT} to GND to reduce switching noise to the control circuitry. The LTpowerCAD® design tool is available to download online to perform ripple analysis based on certain number and type of the capacitors.

INPUT DECOUPLING CAPACITORS

The V_{IN} pin carries the full inductor current, provides power to internal switches and drivers, and powers control circuits in the IC. To minimize input voltage ripple and ensure proper operation of the IC, a low ESR bypass capacitor with a value of at least 22µF should be located as close to V_{IN} as possible. The traces connecting this capacitor to V_{IN} and the ground plane (GND) should be made as short as possible. An additional low value ceramic capacitor such as 4.7µF can be placed between V_{IN} and GND to reduce switching noise to the control circuitry.

RECOMMENDED INPUT AND OUTPUT CAPACITORS

The capacitors used to filter the input and output of the LTM4693 must have low ESR and must be rated to handle the large AC currents generated by the switching converters. While there are many capacitor types for these applications (including low ESR tantalum, OSCON and POSCAP), ceramic capacitors are often utilized in switching converter applications due to their small size, low ESR and low leakage currents. The major providers of ceramic capacitors are AVX, Kemet, Murata, Taiyo Yuden and TDK. Many ceramic capacitors intended for power applications experience a significant loss in capacitance from their rated value as the DC bias voltage on the capacitor increases. It is not uncommon for a small surface mount capacitor to lose more than 50% of its rated capacitance when operated near its maximum rated voltage. This effect is generally reduced as the case size is increased for the same nominal value capacitor. As a result, it is often necessary to use a larger value capacitance or a higher voltage rated capacitor than would ordinarily be required to actually realize the intended capacitance at

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the operating voltage of the application. X5R, X6S or X7R dielectric types are recommended as they exhibit the best performance over the wide operating and temperature ranges. To verify that the intended capacitance is achieved in the application circuit, be sure to consult the capacitor vendor's curve of capacitance vs DC bias voltage.

FORCED CONTINUOUS MODE (FCM)

If the MODE/SYNC pin is high or if the load current on the converter is high enough to enter forced continuous mode operation, the LTM4693 operates at a fixed frequency programmed by the FREQ pin. FCM minimizes output voltage ripple and yields a low noise switching frequency spectrum. A proprietary switching algorithm provides seamless transitions between operating modes and eliminates discontinuities in the average inductor current, inductor ripple current and loop transfer function throughout all modes of operation. These advantages result in increased efficiency, improved loop stability, and lower output voltage ripple. In response to the internal control loop command, an internal pulse width modulator generates the appropriate switch duty cycle to maintain regulation of the output voltage.

Burst Mode OPERATION

When the MODE/SYNC pin is held low, the LTM4693 is configured for Burst Mode operation. As a result, the buck-boost DC/DC converter will operate with normal continuous PWM switching above a predetermined average inductor current and will automatically transition to power saving Burst Mode operation below this level. With MODE/SYNC low, at light output loads, the LTM4693 will go into a standby or sleep state when the output voltage achieves its nominal regulation level. The sleep state halts PWM switching and powers down all non-essential functions of the IC, significantly reducing the quiescent current of the LTM4693. This greatly improves overall power conversion efficiency when the output load is light. Since the converter is not operating in sleep, the output voltage will slowly decay at a rate determined by the output load resistance and the output capacitor value. When the output voltage has decayed by a small amount, typically less than 1%, the LTM4693 will wake up and resume normal switching operation until the voltage on V_{OUT} is restored to the previous level. If the load is very light, the LTM4693 may only need to switch for a few cycles to restore V_{OUT} and may sleep for extended periods of time, significantly improving efficiency.

AVERAGE CURRENT MODE CONTROL AND STABILITY COMPENSATION

The LTM4693 utilizes average current mode control for the pulse width modulator as shown in Figure 3. Current mode control, both average and the better known peak methods, enjoy some benefits compared to other control methods including: simplified loop compensation, rapid response to load transients and inherent line voltage rejection.

Referring to Figure 3, an internal high gain transconductance error amplifier labeled V_{AMP} monitors V_{OUT} through a voltage divider connected to the FB node and generates an output, V_C, used by the current mode control loop to command the appropriate inductor current level. To ensure stability, external frequency compensation components (R_C and C_C) must be installed between V_C and GND and C_{HF} is optional.

V_C is internally connected to the non-inverting input of a second amplifier, referred to in Figure 3 as I_{AMP}. The inverting input of the average current amplifier is connected to the inductor current sense resistor R_{CS} with a 200mV offset. I_{AMP} contains an internal averaging filter and frequency compensation network to stabilize operation of the internal current loop. The average current amplifier's output (I_{COMP}) provides the cycle-by-cycle

APPLICATIONS INFORMATION

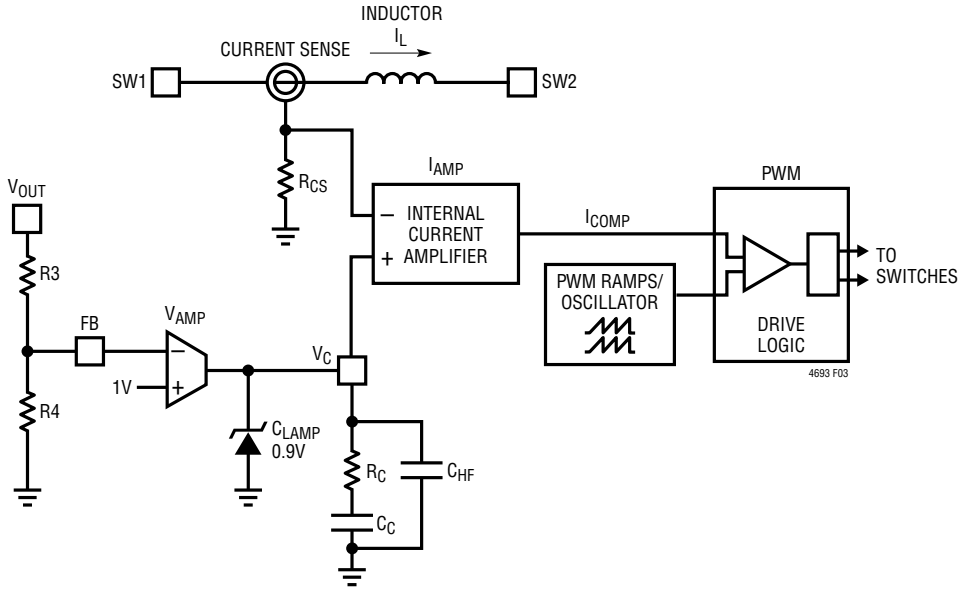

Figure 3. Average Current Mode Control Loop

duty cycle command into the buck-boost PWM circuitry. The inductor current sensing circuitry alternately measures the current through the power switches. The output of the sensing circuitry produces a voltage across resistor R_{CS} that resembles the inductor current waveform transformed to a voltage. If there is an increase in the power converter load on V_{OUT}, the instantaneous level of V_{OUT} will drop slightly, which will increase the voltage level on V_C by the inverting action of the voltage error amplifier. When the increase on V_C first occurs, the output of the current averaging amplifier, I_{COMP}, will increase momentarily to command a larger duty cycle. This duty cycle increase will result in a higher inductor current level, ultimately raising the average voltage across R_{CS}. Once the average value of the voltage on R_{CS} is equivalent to the V_C level, the voltage on I_{COMP} will revert very closely to its previous level into the PWM and force the correct duty cycle to maintain voltage regulation at this new higher inductor current level. The average current amplifier is configured, so in steady state, the average value of the voltage applied to its inverting input (voltage across R_{CS}) will be equivalent to the voltage on its non-inverting input V_C. As a result, the average value of the inductor current is controlled in order to maintain voltage regulation. The entire current amplifier and PWM can be simplified as a voltage controlled current source, with the driving voltage coming from V_C. The voltage error amplifier monitors V_{OUT} through a voltage divider and makes adjustments to the current command as necessary to maintain regulation. The voltage error amplifier therefore controls the outer voltage regulation loop. The average current amplifier makes adjustments to the inductor current as directed by the voltage error amplifier output via V_C and is commonly referred to as the inner current loop amplifier. The average current mode control technique is similar to peak current mode control except that the average current amplifier controls average current instead of the peak current. This difference eliminates the peak to average current error inherent to peak current mode control, while maintaining most of the advantages inherent to peak current mode control. The inner loop compensation components are fixed internally on the LTM4693 to simplify the loop design and provide the highest possible bandwidth over a wide operating range. However, the compensation of the voltage loop is external for the LTM4693 which allows the overall loop characteristics to be customized depending on the programmed output voltage, oscillator frequency, output capacitance and equivalent ESR of the output capacitors.

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The average current mode control used in the LTM4693 can be conceptualized as a voltage controlled current source (V_{CCS}), driving the output load formed primarily by R_{LOAD} and C_{OUT}, as shown in Figure 4.

The voltage error amplifier output (V_C), provides a command input to the V_{CCS}. As with peak current mode control, the inner average current control loop effectively turns the inductor into a current source over the frequency range of interest, resulting in a frequency response from the power stage that exhibits a single pole (–20dB/decade) roll-off. The output capacitor (C_{OUT}) and load resistance (R_{LOAD}) form a dominant low frequency pole, where the effective series resistance of the output capacitor and its capacitance form a zero, usually at a high enough frequency to be ignored, if ceramic capacitors are employed.

A potentially troublesome Right Half Plane Zero (RHPZ) is also encountered if the converter is operated in boost mode. The RHPZ causes an increase in gain, like a zero, but a decrease in phase, like a pole. This can ultimately limit the maximum converter bandwidth that can be achieved with the LTM4693. The RHPZ is not present when operating in buck mode.

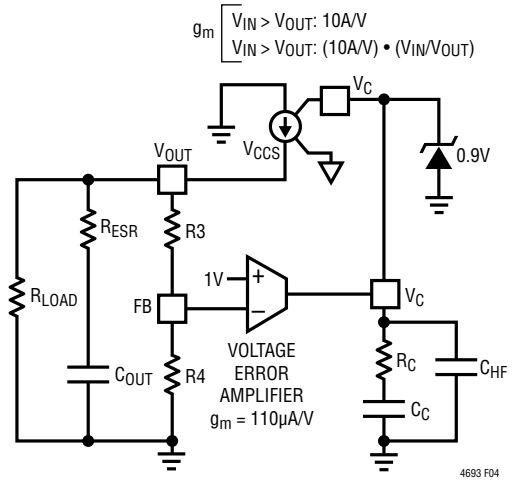

Figure 4. Simplified Representation of Average Current Mode Control Loop Small Signal Model

The voltage amplifier's frequency response is designed to optimize the response for the overall loop. Measurement of the power stage gain over line, load, component variation, and frequency is strongly recommended prior to loop design. The design parameters for compensation design will focus on the series resistor and capacitors connected from V_C to GND (R_C, C_C and C_{HF} (Optional)). Being a buck-boost converter, the target loop crossover frequency for the compensation design will be dictated by the highest boost ratio and load current as this will result in the lowest RHPZ frequency. The general goal is to set the crossover frequency and provide sufficient phase boost using the external compensation network.

The LTpowerCAD design tool is available to download online to perform loop compensation and transient optimization.

Table 5 is provided for most application requirements.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients can be found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in-and-of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance

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pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives three thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a four-layer demo circuit DC3016A.
2. $\theta_{JCbottom}$, the thermal resistance from junction to bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical module regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

A graphical representation of the aforementioned thermal resistances is given in Figure 5; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or subgroup of the three thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4693 module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software defined JEDEC environment consistent with JSED51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4693 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as simulated. An outcome of this process and due-diligence yields a set of derating curves shown in this data sheet.

After these laboratory test have been performed and correlated to LTM4693 model, then the θ_{JA} is provided assuming approximately 100% of the power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

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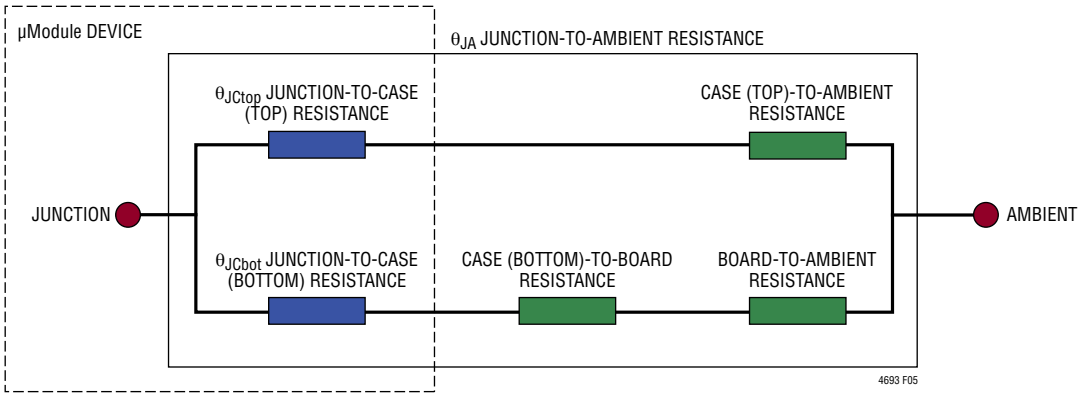

Figure 5. Graphical Representation of JESD51-12 Thermal Coefficients, Including JESD 51-12 Terms

The 1.8V, 3.3V and 5V power loss curves in Figure 6 to Figure 8 can be used in coordination with the load current derating curves in Figure 9 to Figure 14 for calculating an approximate θ_{JA} thermal resistance for the LTM4693 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors according to the junction temperature. This approximate factor is: 1.2 for 120°C at junction temperature. Maximum load current is achievable while increasing ambient temperature as long as the junction temperature is less than 120°C, which is 5°C guard band from maximum junction temperature of 125°C. When the ambient temperature reaches a point where the junction temperature is 120°C, then the load current is lowered to maintain the junction at 120°C while increasing ambient temperature up to 120°C. The derating curves are plotted with the output current starting at 2A and the ambient temperature at 30°C. The output voltages are 1.8V, 3.3V and 5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 9, the load current is derated to 1.5A at ~ 105°C with no air or heat sink and the power loss for the 3.3V to 1.8V at 1.5A output is about 0.323W. The 0.388W loss is calculated with the ~ 0.323W room temperature loss from the 3.3V to 1.8V power loss curve at 1.5A, and the 1.2 multiplying factor. If the 105°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 15°C divided by 0.388W equals a 38.7°C/W θ_{JA} thermal resistance. Table 2 specifies a 38°C/W which is very close. Table 2 to Table 4 provide equivalent thermal resistances for 1.8V, 3.3V and 5V outputs with and without airflow. The derived thermal resistances in Table 2 to Table 4 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 76mm × 76mm.

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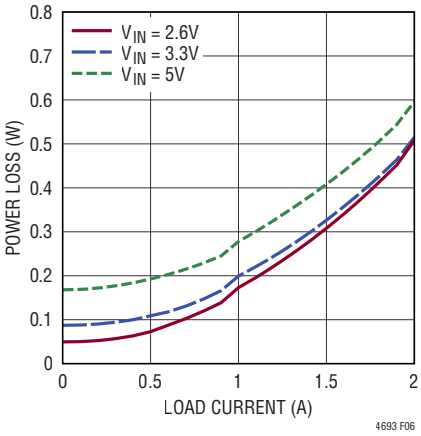

Figure 6. Power Loss at 1.8V Output and 1MHz Switching Frequency

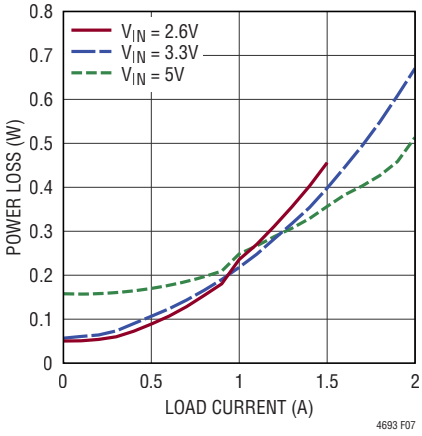

Figure 7. Power Loss at 3.3V Output and 1MHz Switching Frequency

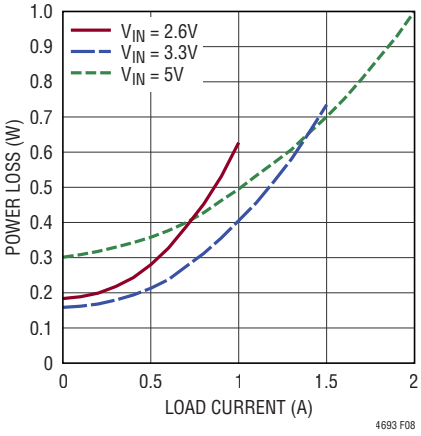

Figure 8. Power Loss at 5V Output and 1MHz Switching Frequency

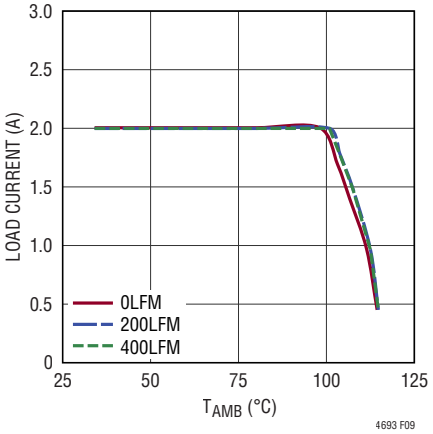

Figure 9. 3.3V to 1.8V Derating Curve, No Heat Sink

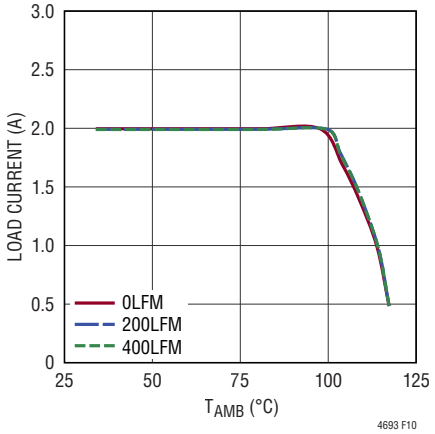

Figure 10. 3.3V to 3.3V Derating Curve, No Heat Sink

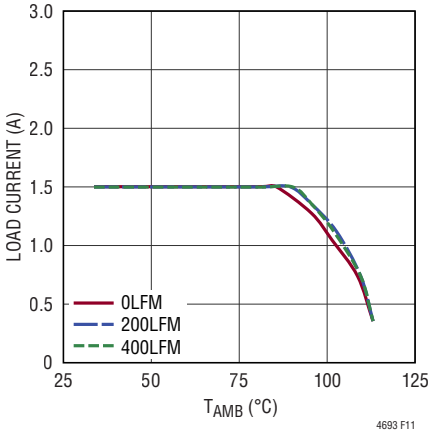

Figure 11. 3.3V to 5V Derating Curve, No Heat Sink

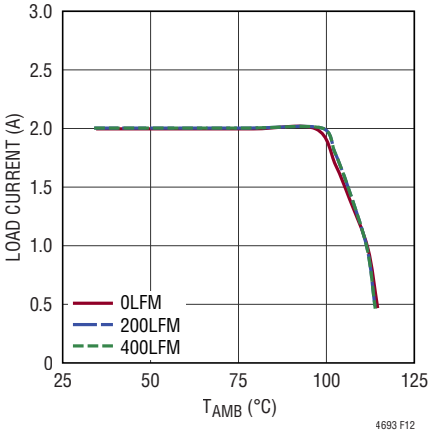

Figure 12. 5V to 1.8V Derating Curve, No Heat Sink

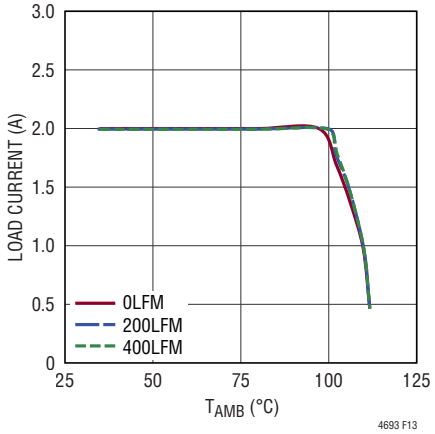

Figure 13. 5V to 3.3V Derating Curve, No Heat Sink

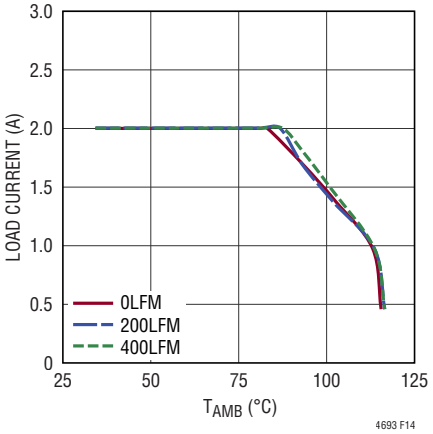

Figure 14. 5V to 5V Derating Curve, No Heat Sink

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SAFETY CONSIDERATIONS

The LTM4693 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and short-circuit protection.

LAYOUT CHECKLIST/EXAMPLE

The high integration of LTM4693 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

Table 2. 1.8V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 9, Figure 12	3.3, 5	Figure 6	0	None	38
Figure 9, Figure 12	3.3, 5	Figure 6	200	None	34
Figure 9, Figure 12	3.3, 5	Figure 6	400	None	34

Table 3. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 10, Figure 13	3.3, 5	Figure 7	0	None	38
Figure 10, Figure 13	3.3, 5	Figure 7	200	None	34
Figure 10, Figure 13	3.3, 5	Figure 7	400	None	34

Table 4. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 11 ,Figure 14	3.3, 5	Figure 8	0	None	38
Figure 11 ,Figure 14	3.3, 5	Figure 8	200	None	34
Figure 11 ,Figure 14	3.3, 5	Figure 8	400	None	34

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Table 5. Output Voltage Response vs Component Matrix

C_{OUT}	VALUE	PART NUMBER
MURATA	22µF ×2, 25V, 1210, X5R	GRM32ER61E226ME15L

V_{IN} (V)	V_{OUT} (V)	f_{SW} (MHz)	C_{OUT} (CERAMIC)	COMPENSATION	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)	P-P DERIVATION (mV)	RECOVERY TIME (µs)
2.6	5	1	22µF ×2	C_{TH} = 2.2nF, R_{TH} = 10k	1A – 1.5A	0.5	500	200
3.3	1.8	1	22µF ×2	C_{TH} = 2.2nF, R_{TH} = 10k	1A – 2A	1	180	70
3.3	3.3	1	22µF ×2	C_{TH} = 2.2nF, R_{TH} = 10k	1A – 2A	1	310	95
5	3.3	1	22µF ×2	C_{TH} = 2.2nF, R_{TH} = 10k	1A – 2A	1	270	95
5	5	1	22µF ×2	C_{TH} = 2.2nF, R_{TH} = 10k	1A – 2A	1	500	170

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- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Bring out test points on the signal pins for monitoring.

Figure 15 gives a good example of the recommended layout.

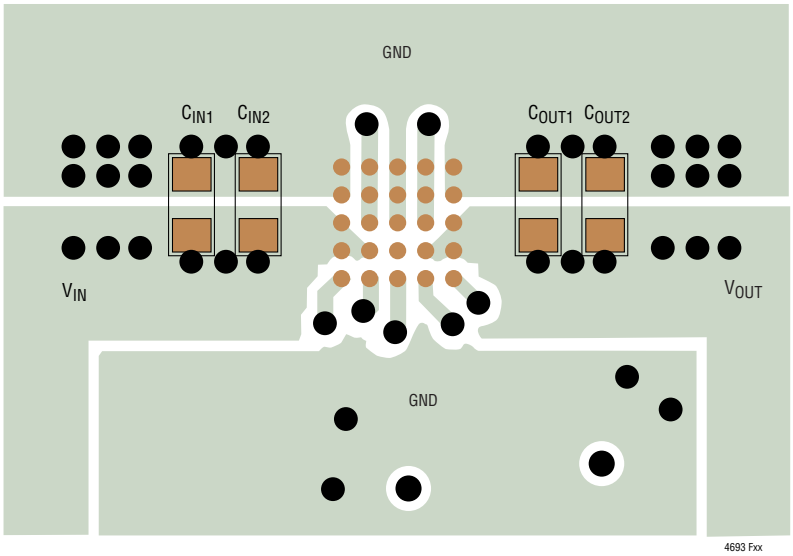


Figure 15. Recommended PCB Layout

TYPICAL APPLICATIONS

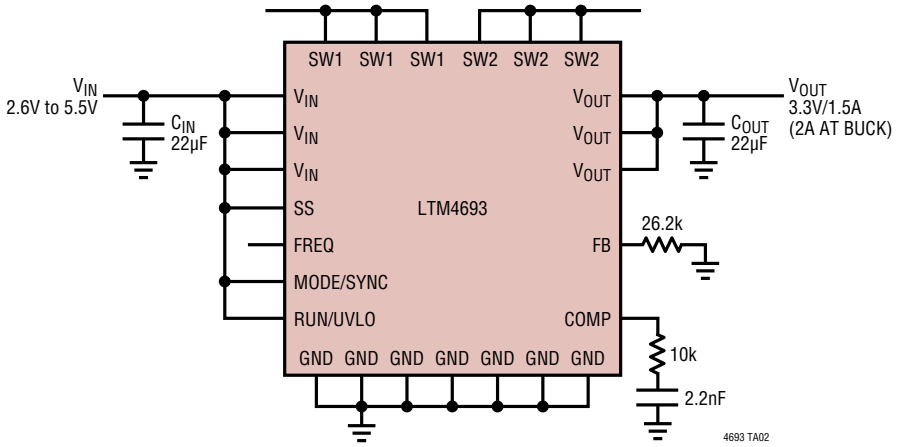


Figure 16. 2.6V to 5.5V Input, 3.3V Output with Minimum Components (Default 2ms Soft-Start Time and 1MHz Switching Frequency)

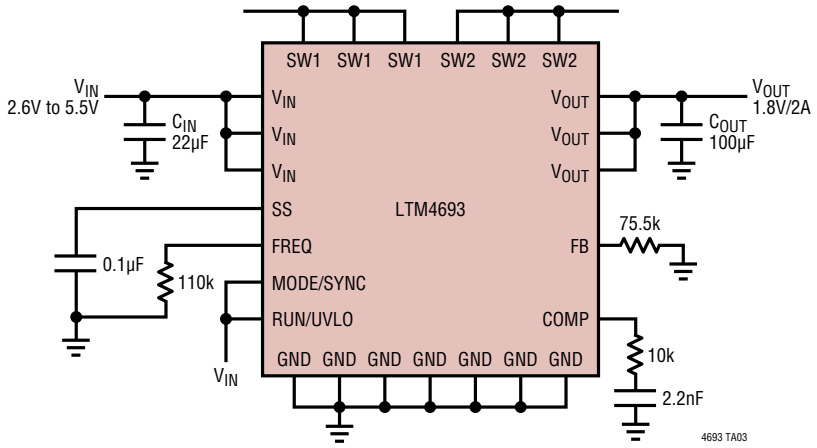


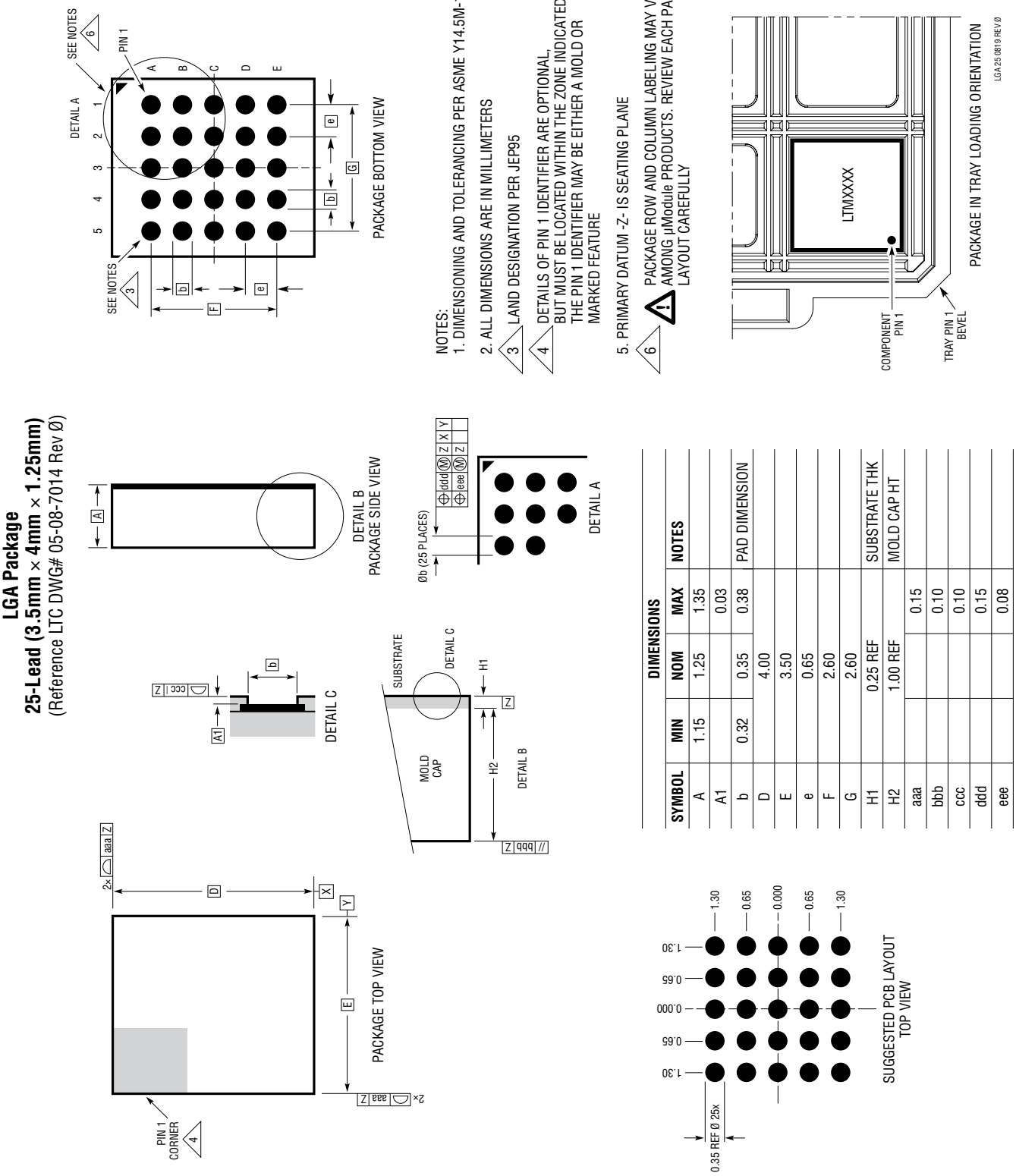
Figure 17. 2.6V to 5.5V Input, 1.8V Output with Adjustable SS Time and 2MHz Switching Frequency

PACKAGE DESCRIPTION

LTM4693 LGA Pinout

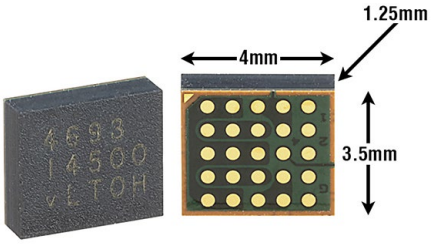
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND	A2	SW1	A3	GND	A4	SW2	A5	GND
B1	GND	B2	SW1	B3	GND	B4	SW2	B5	GND
C1	V_{IN}	C2	SW1	C3	GND	C4	SW2	C5	V_{OUT}
D1	V_{IN}	D2	V_{IN}	D3	SS	D4	V_{OUT}	D5	V_{OUT}
E1	RUN/UVLO	E2	MODE/SYNC	E3	FREQ	E4	FB	E5	COMP

PACKAGE DESCRIPTION



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.15	1.25	1.35	
A1			0.03	
b	0.32	0.35	0.38	PAD DIMENSION
D		4.00		
E		3.50		
e		0.65		
F		2.60		
G		2.60		
H1		0.25 REF		SUBSTRATE THK
H2		1.00 REF		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.10	
ddd			0.15	
eee			0.08	

PACKAGE PHOTO



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search INPUT | V_{in}(Min) V V_{in}(Max) V OUTPUT | V_{Out} V I_{out} A FEATURES | Low EMI Ultrathin Internal Heat Sink Multiple Outputs Search	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8083	$36V_{IN}$, $36V_{OUT}$, 1.5A Buck-Boost µModule Regulator	$3V \le V_{IN} \le 36V$, $1V \le V_{OUT} \le 36V$, 6.25mm × 6.25mm × 2.22mm BGA
LTM8054	$36V_{IN}$, $36V_{OUT}$, 5.4A Buck-Boost µModule Regulator	$5V \le V_{IN} \le 36V$, $1.2V \le V_{OUT} \le 36V$, 11.25mm × 15mm × 3.42mm BGA
LTM8055	$36V_{IN}$, $36V_{OUT}$, 8.5A Buck-Boost µModule Regulator	$5V \le V_{IN} \le 36V$, $1.2V \le V_{OUT} \le 36V$, 15mm × 15mm × 4.92mm BGA
LTM8056	$58V_{IN}$, $48V_{OUT}$, 5.5A Buck-Boost µModule Regulator	$5V \le V_{IN} \le 58V$, $1.2V \le V_{OUT} \le 48V$, 15mm × 15mm × 4.92mm BGA
LTM8045	Single, Inverting or SEPIC µModule DC/DC Convertor	$2.8V \le V_{IN} \le 18V$. $\pm 2.5V \le V_{OUT} \le \pm 15V$, 6.25mm × 11.25mm × 4.92mm BGA
LTM8049	Dual Outputs, SEPIC and/or Inverting µModule Regulator	$2.6V \le V_{IN} \le 20V$. $\pm 2.5V \le V_{OUT} \le \pm 25V$, 9mm × 15mm × 2.42mm BGA