Ultrathin Dual 14A or Single 28A µModule Regulator with Digital Power System Management

FEATURES

- **Dual, Fast, Analog Loops with Digital Interface for Control and Monitoring**
- **Input Voltage Range: 4.5V to 5.75V Standalone, 2.375V to 5.75V with Aux 5V Bias**
- **Output Voltage Range: 0.5V to 3.6V**
- **±0.5% Maximum DC Output Error Over Temperature**
- **14A DC Typical, 17A Peak Output Current, per Channel**
- **±10% Current Readback Accuracy at 10A Load**
- **400kHz PMBus-Compliant I²C Serial Interface**
- **Integrated 16-Bit ΔΣ ADC**
- **Supports Telemetry Polling Rates Up to 125Hz**
- **Constant Frequency Current Mode Control**
- **Parallel and Current Share Multiple Modules**
- All 7-Bit Slave Addresses Supported
- Drop-In Pin-Compatible to Dual 10A LTM4686 and Dual 9A LTM4675 and Dual 13A LTM4676A and Dual 18A LTM4677
- 16mm × 11.9mm × 1.82mm LGA Package

Readable Data

- Input and Output Voltages, Currents, and Temperatures
- Running Peak Values, Uptime, Faults and Warnings
- Onboard EEPROM with ECC and Fault Log Record

Writable Data and Configurable Parameters

- Output Voltage, Voltage Sequencing and Margining
- Digital Soft-Start/Stop Ramp
- OV/UV/OT, UVLO, Frequency and Phasing

APPLICATIONS

- System Optimization in Prototype and Production

DESCRIPTION

The LTM®4686B is a dual 14A (17A peak) or single 28A (34A peak) step-down µModule® (micromodule) DC/DC regulator with 39ms turn-on time. It features remote configurability and telemetry-monitoring of power management parameters over PMBus—an open standard I²C-based digital interface protocol. The LTM4686B is comprised of fast analog control loops, precision mixed-signal circuitry, EEPROM, power MOSFETs, inductors and supporting components. A video on ultrathin module products is available on the website. Click here.

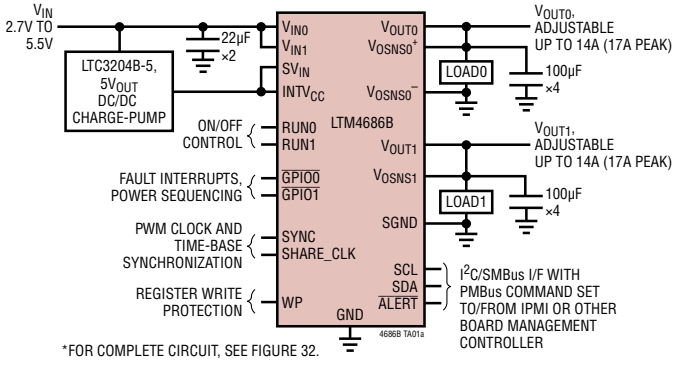
The LTM4686B's 2-wire serial interface allows outputs to be margined, tuned and ramped up and down at programmable slew rates with sequencing delay times. Input and output currents and voltages, output power, temperature, uptime and peak values are readable. Custom configuration of the EEPROM contents is not required. Pin-strap resistors configure start-up settings. The LTpowerPlay® GUI, DC1613 USB-to-PMBus converter, DC2086 programming adapter and demo kits are available.

Pb-free and RoHS compliant, the LTM4686B is available in a 16mm × 11.9mm × 1.82mm LGA package.

Click to view associated Video Design Idea.

TYPICAL APPLICATION

Dual 14A µModule Regulator with Digital Interface for Control and Monitoring*



*FOR COMPLETE CIRCUIT, SEE FIGURE 32.

Using PMBus and LTpowerPlay to Monitor Telemetry and Margin V_{OUT0}/V_{OUT1} During Load Pattern Tests; 10Hz Polling Rate; 3.3V_{IN}

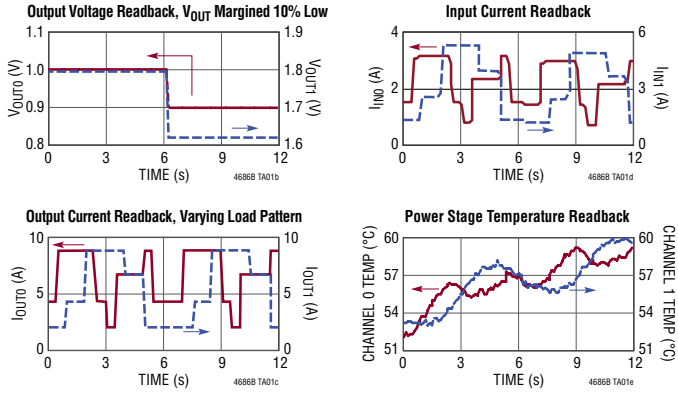


TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS

(Note 1)

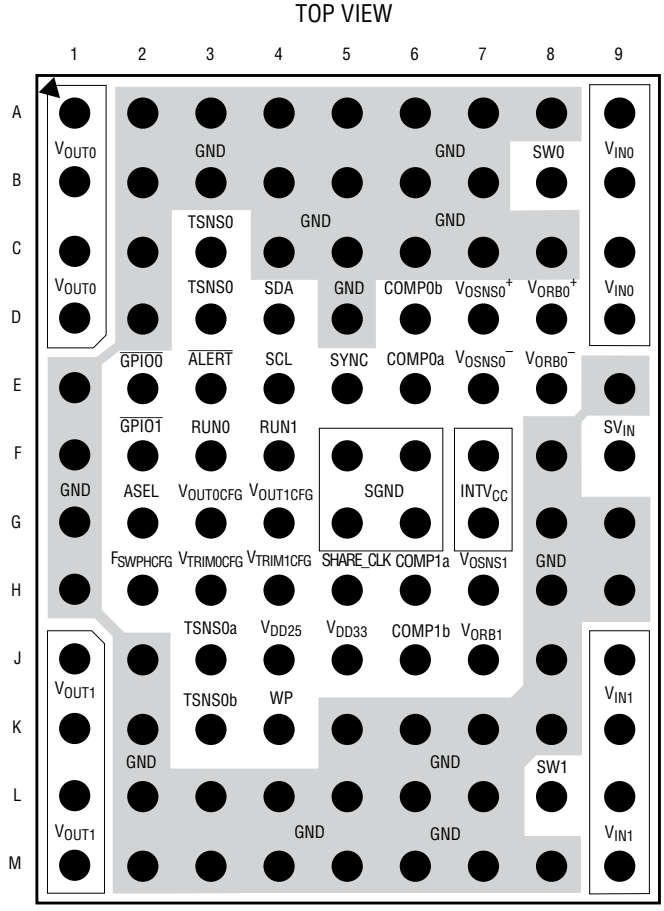
Terminal Voltages

V_{IN}*n* (Note 4), SV_{IN} ..... –0.3V to 6V
V_{OUT}*n* ..... –0.3V to 6V
V_{OSNS0}^+, V_{ORB0}^+, V_{OSNS1}, V_{ORB1}, $INTV_{CC}$ .... –0.3V to 6V
RUN*n*, SDA, SCL, $\overline{ALERT}$ ..... –0.3V to 5.5V
$F_{SWPHCFG}$, V_{OUT}*n*CFG, V_{TRIM}*n*CFG, ASEL .. –0.3V to 2.75V
V_{DD33}, $\overline{GPIO}$*n*, SYNC, SHARE_CLK, WP,
COMP*n*a, V_{OSNS0}^-, V_{ORB0}^- ..... –0.3V to 3.6V
SGND ..... –0.3V to 0.3V

Temperatures

Internal Operating Temperature Range
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Package Body Temperature ... 260°C

PIN CONFIGURATION



LGA PACKAGE
108-LEAD (16mm × 11.9mm × 1.82mm)

T_{JMAX} = 125°C, θ_{JA} = 9.7°C/W, θ_{JCtop} = 5.5°C/W, θ_{JCbot} = 3.1°C/W
WEIGHT = 1.1 GRAMS

NOTES:
1) θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
2) θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
3) REFER TO APPLICATION INFORMATION SECTION FOR LAB MEASUREMENT AND DERATING INFORMATION.

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4686BEV#PBF	Au (RoHS)	LTM4686BV	e4	LGA	4	–40°C to 125°C
LTM4686BIV#PBF	Au (RoHS)	LTM4686BV	e4	LGA	4	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Device temperature grade is indicated by a label on the shipping container.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 5V, RUN*n* = 5V, FREQUENCY_SWITCH = 1MHz, VOUT_COMMAND*n* = 1V and VOUT_UV_FAULT_RESPONSE*n* = TON_MAX_FAULT_RESPONSE*n* = 0x00 unless otherwise noted. All other command codes configured per factory-default EEPROM settings unless otherwise noted. Tested per Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage	Test Circuit 1; 4.5V ≤ SV_{IN} ≤ 5.75V; $INTV_{CC}$ = SV_{IN}; VIN_OFF < VIN_ON = 4.25V Test Circuit 2; 4.5V ≤ SV_{IN} ≤ 5.75V; $INTV_{CC}$ = SV_{IN}; VIN_OFF < VIN_ON = 4.25V	● ●	4.5 2.375		5.75 5.75	V V
V_{OUTn}	Range of Output Voltage Regulation	V_{OUT0} Differentially Sensed on V_{OSNS0}^+/V_{OSNS0}^- Pin-Pair; V_{OUT1} Differentially Sensed on V_{OSNS1}/SGND Pin-Pair; Commanded by Serial Bus or with Resistors Present at Start-Up on $V_{OUTn}CFG$ and/or $V_{TRIMn}CFG$	● ●	0.5 0.5		3.6 3.6	V V
$V_{OUTn(DC)}$	Output Voltage, Total Variation with Line and Load	(Note 5) V_{OUTn} Low Range (MFR_PWM_MODE*n*[1] = 1_b), Digital Servo Engaged (MFR_PWM_MODE*n*[6] = 1_b) Digital Servo Disengaged (MFR_PWM_MODE*n*[6] = 0_b)	 ● 	 0.995 0.985	 1.000 1.000	 1.005 1.015	 V V
Input Specifications							
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	Test Circuit 1, V_{OUTn} =1V, V_{IN} = 5V; No Load Besides Capacitors; TON_RISE*n* = 3ms			400		mA
$I_{Q(SVIN)}$	Input Supply Bias Current	Forced Continuous Mode, MFR_PWM_MODE*n*[0] = 1_b RUN*n* = 5V, RUN[1–*n*] = 0V, $INTV_{CC}$ = 5V Shutdown, RUN0 = RUN1 = 0V, $INTV_{CC}$ Open Circuit	 	 	 1.2 20	 	 mA mA
$I_{S(VINn,PSM)}$	Input Supply Current in Pulse-Skipping Mode Operation	Pulse-Skipping Mode, MFR_PWM_MODE*n*[0] = 0_b, I_{OUTn} = 100mA			45		mA
$I_{S(VINn,FCM)}$	Input Supply Current in Forced-Continuous Mode Operation	Forced Continuous Mode, MFR_PWM_MODE*n*[0] = 1_b I_{OUTn} = 100mA I_{OUTn} = 14A	 	 	 120 4	 	 mA A
$I_{S(VINn,SHUTDOWN)}$	Input Supply Current in Shutdown	Shutdown, RUN*n* = 0V			80		µA
Output Specifications							
I_{OUTn}	Output Continuous Current Range	(Note 6)		0		14	A
$\frac{\Delta V_{OUTn(LINE)}}{V_{OUTn}}$	Line Regulation Accuracy	Digital Servo Engaged (MFR_PWM_MODE*n*[6] = 1_b, Note 12) Digital Servo Disengaged (MFR_PWM_MODE*n*[6] = 0_b) SV_{IN} and V_{INn} and $INTV_{CC}$ Electrically Shorted Together; I_{OUTn} = 0A, 4.5V ≤ V_{IN} ≤ 5.75V, V_{OUT} Low Range (MFR_PWM_MODE*n*[1] = 1_b) FREQUENCY_SWITCH = 1MHz (Referenced to $5V_{IN}$) (Note 5)	 ●	 	0.03 0.03	 ±0.2	% %/V
$\frac{\Delta V_{OUTn(LOAD)}}{V_{OUTn}}$	Load Regulation Accuracy	Digital Servo Engaged (MFR_PWM_MODE*n*[6] = 1_b, Note 12) Digital Servo Disengaged (MFR_PWM_MODE*n*[6] = 0_b) 0A ≤ I_{OUTn} ≤ 14A, V_{OUT} Low Range, (MFR_PWM_MODE*n*[1] = 1_b) FREQUENCY_SWITCH = 1MHz (Note 5)	 ●	 	0.03 0.2	 0.5	% %
$V_{OUTn(AC)}$	Output Voltage Ripple	(Note 12)			10		mV_{P-P}
f_S (Each Channel)	V_{OUTn} Ripple Frequency	FREQUENCY_SWITCH Set to 1MHz (0x03E8)	●	950	1000	1050	kHz
$\Delta V_{OUTn(START)}$	Turn-On Overshoot	TON_RISE*n* = 2ms (Note 12)			8		mV
t_{START}	Turn-On Start-Up Time	Time from V_{IN} Toggling from 0V to $5V_{IN}$ to Rising Edge of $\overline{GPIO}n$. TON_DELAY*n* = 0ms, TON_RISE*n* = 2ms, MFR_GPIO_PROPAGATE*n* = 0x0100, MFR_GPIO_RESPONSE*n* = 0x0000	●		34	39	ms
$t_{DELAY(0ms)}$	Turn-On Delay Time	Time from First Rising Edge of RUN*n* to Rising Edge of $\overline{GPIO}n$. TON_DELAY*n* = 0ms, TON_RISE*n* = 3ms, MFR_GPIO_PROPAGATE*n* = 0x0100, MFR_GPIO_RESPONSE*n* = 0x0000. V_{IN} Having Been Established for at Least 39ms	●	2.7	3.1	3.5	ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 5V, RUN*n* = 5V, FREQUENCY_SWITCH = 1MHz, VOUT_COMMAND*n* = 1V and VOUT_UV_FAULT_RESPONSE*n* = TON_MAX_FAULT_RESPONSE*n* = 0x00 unless otherwise noted. All other command codes configured per factory-default EEPROM settings unless otherwise noted. Tested per Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\Delta V_{OUTn(LS)}$	Peak Output Voltage Deviation for Dynamic Load Step	Load: 0A to 7A and 7A to 0A at 5A/µs, Figure 62 Circuit, V_{OUTn} = 1V, V_{IN} = 5V_{IN} (Note 12)			42		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0A to 7A and 7A to 0A at 5A/µs, Figure 62 Circuit, V_{OUTn} = 1V, V_{IN} = 5V_{IN} (Note 12)			60		µs
$I_{OUTn(OCL\_PK)}$	Output Current Limit, Peak	Cycle-by-Cycle Inductor Peak Current Limit Inception Commanded by IOUT_OC_FAULT_LIMIT*n* (Note 12)			36		A
$I_{OUTn(OCL\_AVG)}$	Output Current Limit, Time Averaged	Time-Averaged Output Inductor Current Limit Inception Threshold			26A; See $I_{O-RB-ACC}$ Specification (Output Current Readback Accuracy)		
Control Section							
V_{FBCM0}	Channel 0 Feedback Input Common Mode Range	V_{OSNS0}^- Valid Input Range (Referred to SGND) V_{OSNS0}^+ Valid Input Range (Referred to SGND)	● ●	–0.1		0.1 3.6	V V
V_{FBCM1}	Channel 1 Feedback Input Common Mode Range	SGND Valid Input Range (Referred to GND) V_{OSNS1} Valid Input Range (Referred to SGND)	● ●	–0.3		0.1 3.6	V V
$V_{OUT-RNG0}$	Full-Scale Command Voltage, Range 0	(Notes 7, 15) V_{OUTn} Commanded to 3.600V, MFR_PWM_MODE*n*[1] = 0_b Resolution LSB Step Size		3.548	 12 1.375	3.651	V Bits mV
$V_{OUT-RNG1}$	Full-Scale Command Voltage, Range 1	(Notes 7, 15) V_{OUTn} Commanded to 2.750V, MFR_PWM_MODE*n*[1] = 1_b Resolution LSB Step Size		2.711	 12 0.6875	2.788	V Bits mV
R_{VOSNS0}^+	V_{OSNS0}^+ Impedance to SGND	0.05V ≤ $V_{VOSNS0}^+ - V_{SGND}$ ≤ 3.6V			41		kΩ
R_{VOSNS1}	V_{OSNS1} Impedance to SGND	0.05V ≤ $V_{VOSNS1} - V_{SGND}$ ≤ 3.6V			37		kΩ
$t_{ON(MIN)}$	Minimum On-Time	(Note 8)			45		ns
V_{OUT} OV/UV (Overvoltage/Undervoltage) Supervisor Comparators (VOUT_OV/UV_FAULT_LIMIT and VOUT_OV/UV_WARN_LIMIT Monitors)							
N_{OV/UV_COMP}	Resolution, Output Voltage Supervisors	(Note 15)			8		Bits
V_{OV-RNG}	Output OV Comparator Threshold Detection Range	(Note 15) High Range Scale, MFR_PWM_MODE*n*[1] = 0_b Low Range Scale, MFR_PWM_MODE*n*[1] = 1_b		 1 0.5		 4.0 2.7	 V V
V_{OU-STP}	Output OV and UV Comparator Threshold Programming LSB Step Size	(Note 15) High Range Scale, MFR_PWM_MODE*n*[1] = 0_b Low Range Scale, MFR_PWM_MODE*n*[1] = 1_b			 22 11		 mV mV
V_{OV-ACC}	Output OV Comparator Threshold Accuracy	(See Note 14) 2V ≤ $V_{VOSNS0}^+ - V_{VOSNS0}^-$ ≤ 4V, MFR_PWM_MODE0[1] = 0_b 1V ≤ $V_{VOSNS0}^+ - V_{VOSNS0}^-$ ≤ 2.7V, MFR_PWM_MODE0[1] = 1_b 0.5V ≤ $V_{VOSNS0}^+ - V_{VOSNS0}^-$ < 1V, MFR_PWM_MODE0[1] = 1_b 2V ≤ $V_{VOSNS1} - V_{SGND}$ ≤ 4V, MFR_PWM_MODE1[1] = 0_b 1.5V ≤ $V_{VOSNS1} - V_{SGND}$ ≤ 2.7V, MFR_PWM_MODE1[1] = 1_b 0.5V ≤ $V_{VOSNS1} - V_{SGND}$ < 1.5V, MFR_PWM_MODE1[1] = 1_b	 ● ● ● ● ● ●			 ±2 ±2 ±20 ±2 ±2 ±30	 % % mV % % mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 5V, RUN*n* = 5V, FREQUENCY_SWITCH = 1MHz, VOUT_COMMAND*n* = 1V and VOUT_UV_FAULT_RESPONSE*n* = TON_MAX_FAULT_RESPONSE*n* = 0x00 unless otherwise noted. All other command codes configured per factory-default EEPROM settings unless otherwise noted. Tested per Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{UV-RNG}	Output UV Comparator Threshold Detection Range	(Note 15) High Range Scale, MFR_PWM_MODE*n*[1] = 0_b Low Range Scale, MFR_PWM_MODE*n*[1] = 1_b		 1 0.5		 3.6 2.7	 V V
V_{UV-ACC}	Output UV Comparator Threshold Accuracy	(See Note 14) 2V ≤ $V_{VOSNS0}^+ - V_{VOSNS0}^-$ ≤ 3.6V, MFR_PWM_MODE0[1] = 0_b 1V ≤ $V_{VOSNS0}^+ - V_{VOSNS0}^-$ ≤ 2.7V, MFR_PWM_MODE0[1] = 1_b 0.5V ≤ $V_{VOSNS0}^+ - V_{VOSNS0}^-$ < 1V, MFR_PWM_MODE0[1] = 1_b 2V ≤ $V_{VOSNS1} - V_{SGND}$ ≤ 3.6V, MFR_PWM_MODE1[1] = 0_b 1.5V ≤ $V_{VOSNS1} - V_{SGND}$ ≤ 2.7V, MFR_PWM_MODE1[1] = 1_b 0.5V ≤ $V_{VOSNS1} - V_{SGND}$ < 1.5V, MFR_PWM_MODE1[1] = 1_b	 ● ● ● ● ● ●			 ±2 ±2 ±20 ±2 ±2 ±30	 % % mV % % mV
$t_{PROP-OV}$	Output OV Comparator Response Times	Overdrive to 10% Above Programmed Threshold				35	µs
$t_{PROP-UV}$	Output UV Comparator Response Times	Underdrive to 10% Below Programmed Threshold				50	µs
SV_{IN} OV/UV Analog Input Voltage Supervisor Comparators (Threshold Detectors for VIN_ON and VIN_OFF)							
$N_{SVIN-OV/UV-COMP}$	SV_{IN} OV/UV Comparator Threshold-Programming Resolution	(Note 15)			8		Bits
$SV_{IN-OU-RANGE}$	SV_{IN} OV/UV Comparator Threshold-Programming Range		●	4.5		5.75	V
$SV_{IN-OU-STP}$	SV_{IN} OV/UV Comparator Threshold-Programming LSB Step Size	(Note 15)			82		mV
$SV_{IN-OU-ACC}$	SV_{IN} OV/UV Comparator Threshold Accuracy	4.5V ≤ SV_{IN} ≤ 5.75V	●			±225	mV
$t_{PROP-SVIN-LOW-VIN}$	SV_{IN} OV/UV Comparator Response Time, Low V_{IN} Operating Configuration	Test Circuit 1, and: VIN_ON = 4.5V; SV_{IN} Driven from 4.225V to 4.725V VIN_OFF = 4.5V; SV_{IN} Driven from 4.725V to 4.225V	 ● ●			 35 35	 µs µs
Channels 0 and 1 Output Voltage Readback (READ_VOUT*n*)							
N_{VO-RB}	Output Voltage Readback Resolution and LSB Step Size	(Note 15)			16 244		Bits µV
$V_{O-F/S}$	Output Voltage Full-Scale Digitizable Range	V_{RUNn} = 0V (Notes 7, 15)			8		V
$V_{O-RB-ACC}$	Output Voltage Readback Accuracy	Channel 0: 1V ≤ $V_{VOSNS0}^+ - V_{VOSNS0}^-$ ≤ 3.6V Channel 0: 0.5V ≤ $V_{VOSNS0}^+ - V_{VOSNS0}^-$ < 1V Channel 1: 1V ≤ $V_{VOSNS1} - V_{SGND}$ ≤ 3.6V Channel 1: 0.5V ≤ $V_{VOSNS1} - V_{SGND}$ < 1V	● ● ● ●	Within ±0.5% of Reading Within ±5mV of Reading Within ±0.5% of Reading Within ±5mV of Reading			
$t_{CONVERT-VO-RB}$	Output Voltage Readback Update Rate	MFR_ADC_CONTROL = 0x00 (Notes 9, 15) MFR_ADC_CONTROL = 0x0D (Notes 9, 15) MFR_ADC_CONTROL = 0x05 or 0x09 (Notes 9, 15)			90 27 8		ms ms ms

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage (SV_{IN}) Readback (READ_VIN)							
$N_{SVIN–RB}$	Input Voltage Readback Resolution and LSB Step Size	(Notes 10, 15)			10 15.625		Bits mV
$SV_{IN–F/S}$	Input Voltage Full-Scale Digitizable Range	(Notes 11, 15)			38.91		V
$SV_{IN–RB–ACC}$	Input Voltage Readback Accuracy	READ_VIN, 4.5V ≤ SV_{IN} ≤ 5.75V	●		Within ±2% of Reading		
$t_{CONVERT–SVIN–RB}$	Input Voltage Readback Update Rate	MFR_ADC_CONTROL = 0x00 (Notes 9, 15) MFR_ADC_CONTROL = 0x01 (Notes 9, 15)			90 8		ms ms
Channels 0 and 1 Output Current (READ_IOUT*n*), Duty Cycle (READ_DUTY_CYCLE*n*), and Computed Input Current (MFR_READ_IIN*n*) Readback							
$N_{IO–RB}$	Output Current Readback Resolution and LSB Step Size	(Notes 10, 12)			10 15.6		Bits mA
$I_{O–F/S}$, $I_{I–F/S}$	Output Current Full-Scale Digitizable Range and Input Current Range of Calculation	(Note 12)			±40		A
$I_{O–RB–ACC}$	Output Current, Readback Accuracy	READ_IOUT*n*, Channels 0 and 1, 0 ≤ I_{OUTn} ≤ 10A, Forced-Continuous Mode, MFR_PWM_MODE*n*[1:0] = 11_b	●		Within 1A of Reading		
$I_{O–RB(10A)}$	Full Load Output Current Readback	I_{OUTn} = 10A (Note 12). See Histograms in Typical Performance Characteristics			10		A
$N_{II–RB}$	Computed Input Current, Readback Resolution and LSB Step Size	(Notes 10, 12)			10 1.95		Bits mA
$I_{I–RB–ACC}$	Computed Input Current, Readback Accuracy, Neglecting I_{SVIN}	MFR_READ_IIN*n*, Channels 0 and 1, 0 ≤ I_{OUTn} ≤ 10A, Forced Continuous Mode, MFR_PWM_MODE*n*[1:0] = 11_b, MFR_IIN_OFFSET*n* = 0mA	●		Within 150mA of Reading		
$t_{CONVERT–IO–RB}$	Output Current Readback Update Rate	MFR_ADC_CONTROL = 0x00 (Notes 9, 15) MFR_ADC_CONTROL = 0x0D (Notes 9, 15) MFR_ADC_CONTROL = 0x06 or 0x0A (Notes 9, 15)			90 27 8		ms ms ms
$t_{CONVERT–II–RB}$	Computed Input Current, Readback Update Rate	MFR_ADC_CONTROL = 0x00 (Notes 9, 15)			90		ms
$N_{DUTY–RB}$	Resolution, Duty Cycle Readback	(Notes 10, 15)			10		Bits
$D_{RB–ACC}$	Duty Cycle TUE	READ_DUTY_CYCLE*n*, 16.3% Duty Cycle (Note 15)				±3	%
$t_{CONVERT–DUTY–RB}$	Duty Cycle Readback Update Rate	MFR_ADC_CONTROL = 0x00 (Notes 9, 15)			90		ms

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Temperature Readback for Channel 0, Channel 1, and Controller (Respectively: READ_TEMPERATURE_1$_0$, READ_TEMPERATURE_1$_1$, and READ_TEMPERATURE_2)							
$T_{RES–RB}$	Temperature Readback Resolution	Channel 0, Channel 1, and Controller (Note 15)			0.0625		°C
$T_{RB–CH–ACC(72mV)}$	Channel Temperature TUE, Switching Action Off	Channels 0 and 1, PWM Inactive, RUN*n* = 0V, ΔV_{TSNSna} = 72mV	●		Within ±3°C of Reading		
$T_{RB–CH–ACC(ON)}$	Channel Temperature TUE, Switching Action On	READ_TEMPERATURE_1$_n$, Channels 0 and 1, PWM Active, RUN*n* = 5V (Note 12)			Within ±3°C of Reading		
$T_{RB–CTRL–ACC(ON)}$	Control IC Die Temperature TUE, Switching Action On	READ_TEMPERATURE_2, PWM Active, RUN0 = RUN1 = 5V (Note 12)			Within ±1°C of Reading, Typ		
$t_{CONVERT–TEMP–RB}$	Temperature Readback Update Rate	MFR_ADC_CONTROL = 0x00 (Notes 9, 15) MFR_ADC_CONTROL = 0x06 or 0x0A (Notes 9, 15)			90 8		ms ms
V_{DD33} Regulator							
V_{VDD33}	Internal V_{DD33} Voltage			3.2	3.3	3.4	V
$I_{LIM(VDD33)}$	V_{DD33} Current Limit	V_{DD33} Electrically Short-Circuited to GND			70		mA
V_{VDD33_OV}	V_{DD33} Overvoltage Threshold	(Note 15)			3.5		V
V_{VDD33_UV}	V_{DD33} Undervoltage Threshold	(Note 15)			3.1		V
V_{DD25} Regulator							
V_{VDD25}	Internal V_{DD25} Voltage				2.5		V
$I_{LIM(VDD25)}$	V_{DD25} Current Limit	V_{DD25} Electrically Short-Circuited to GND			50		mA
Oscillator and Phase-Locked Loop (PLL)							
f_{OSC}	Oscillator Frequency Accuracy	FREQUENCY_SWITCH = 1MHz (0x03E8) 500kHz ≤ FREQUENCY_SWITCH ≤ 1MHz (Note 15)	●			±5 ±5	% %
f_{SYNC}	PLL SYNC Capture Range	(Note 16)	●	450		1050	kHz
$V_{TH,SYNC}$	SYNC Input Threshold	V_{SYNC} Rising (Note 15) V_{SYNC} Falling (Note 15)			1.5 1		V V
$V_{OL,SYNC}$	SYNC Low Output Voltage	I_{SYNC} = 3mA	●		0.3	0.4	V
I_{SYNC}	SYNC Leakage Current in Frequency Slave Mode	0V ≤ V_{SYNC} ≤ 3.6V MFR_CONFIG_ALL[4] = 1_b	●			±5	µA
$\theta_{SYNC}–\theta0$	SYNC-to-Channel 0 Phase Relationship, Lag from Falling Edge of Sync to Rising Edge of Top MOSFET (MT0) Gate	(Note 15) MFR_PWM_CONFIG[2:0] = 000_b, $01X_b$ MFR_PWM_CONFIG[2:0] = 101_b MFR_PWM_CONFIG[2:0] = 001_b MFR_PWM_CONFIG[2:0] = $1X0_b$			 0 60 90 120		 Deg Deg Deg Deg
$\theta_{SYNC}–\theta1$	SYNC-to-Channel 1 Phase Relationship, Lag from Falling Edge of Sync to Rising Edge of Top MOSFET (MT1) Gate	(Note 15) MFR_PWM_CONFIG[2:0] = 011_b MFR_PWM_CONFIG[2:0] = 000_b MFR_PWM_CONFIG[2:0] = 010_b, $10X_b$ MFR_PWM_CONFIG[2:0] = 001_b MFR_PWM_CONFIG[2:0] = 110_b			 120 180 240 270 300		 Deg Deg Deg Deg Deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 5V, RUN*n* = 5V, FREQUENCY_SWITCH = 1MHz, VOUT_COMMAND*n* = 1V and VOUT_UV_FAULT_RESPONSE*n* = TON_MAX_FAULT_RESPONSE*n* = 0x00 unless otherwise noted. All other command codes configured per factory-default EEPROM settings unless otherwise noted. Tested per Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
EEPROM Characteristics							
Endurance	(Note 13)	0°C ≤ T_J ≤ 85°C During EEPROM Write Operations (Note 3)	●	10,000			Cycles
Retention	(Note 13)	T_J < $T_{J(MAX)}$, with Most Recent EEPROM Write Operation Having Occurred at 0°C ≤ T_J ≤ 85°C (Note 3)	●	10			Years
Mass_Write	Mass Write Operation Time	Execution of STORE_USER_ALL Command, 0°C ≤ T_J ≤ 85°C (ATE-Tested at T_J = 25°C) (Notes 3, 13)			440	4100	ms
Digital I/Os							
V_{IH}	Input High Threshold Voltage	SCL, SDA, RUN*n*, $\overline{GPIO}$*n* (Note 15) SHARE_CLK, WP (Note 15)		1.35 1.8			V V
V_{IL}	Input Low Threshold Voltage	SCL, SDA, RUN*n*, $\overline{GPIO}$*n* (Note 15) SHARE_CLK, WP (Note 15)				0.8 0.6	V V
V_{HYST}	Input Hysteresis	SCL, SDA (Note 15)			80		mV
V_{OL}	Output Low Voltage	SCL, SDA, $\overline{ALERT}$, RUN*n*, $\overline{GPIO}$*n*, SHARE_CLK: I_{SINK} = 3mA	 ●		 0.3	 0.4	 V
I_{OL}	Input Leakage Current	SDA, SCL, $\overline{ALERT}$, RUN*n*: 0V ≤ V_{PIN} ≤ 5.5V $\overline{GPIO}$*n* and SHARE_CLK: 0V ≤ V_{PIN} ≤ 3.6V	● ●			±5 ±2	µA µA
t_{FILTER}	Input Digital Filtering	RUN*n* (Note 15) $\overline{GPIO}$*n* (Note 15)			10 3		µs µs
C_{PIN}	Input Capacitance	SCL, SDA, RUN*n*, $\overline{GPIO}$*n*, SHARE_CLK, WP (Note 15)				10	pF
PMBus Interface Timing Characteristics							
f_{SMB}	Serial Bus Operating Frequency	(Note 15)		10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start	(Note 15)		1.3			µs
$t_{HD,STA}$	Hold Time After Repeated Start Condition	Time Period After Which First Clock Is Generated (Note 15)		0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time	(Note 15)		0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time	(Note 15)		0.6			µs
$t_{HD,DAT}$	Data Hold Time	Receiving Data (Note 15) Transmitting Data (Note 15)		0 0.3		 0.9	µs µs
$t_{SU,DAT}$	Data Setup Time	Receiving Data (Note 15)		0.1			µs
$t_{TIMEOUT\_SMB}$	Stuck PMBus Timer Timeout	Measured from the Last PMBus Start Event: Block Reads, MFR_CONFIG_ALL[3] = 0_b (Note 15) Non-Block Reads, MFR_CONFIG_ALL[3] = 0_b (Note 15) MFR_CONFIG_ALL[3] = 1_b (Note 15)			 150 32 250		 ms ms ms
t_{LOW}	Serial Clock Low Period	(Note 15)		1.3		10000	µs
t_{HIGH}	Serial Clock High Period	(Note 15)		0.6			µs

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listing under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating conditions for extended periods may affect device reliability and lifetime.

Note 2: The LTM4686B is tested under pulsed-load conditions such that $T_J \approx T_A$. The LTM4686BE is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4686BI is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The LTM4686B's EEPROM temperature range for valid write commands is 0°C to 85°C. To achieve guaranteed EEPROM data retention, execution of the "STORE_USER_ALL" command—i.e., uploading RAM contents to NVM—outside this temperature range is not recommended. However, as long as the LTM4686B's EEPROM temperature is less than 130°C, the LTM4686B *will* obey the STORE_USER_ALL command. Only when EEPROM temperature exceeds 130°C, the LTM4686B will not act on any STORE_USER_ALL transactions: instead, the LTM4686B NACKs the serial command and asserts its relevant CML (communications, memory, logic) fault bits. EEPROM temperature can be queried prior to commanding STORE_USER_ALL; see the Applications Information section.

Note 4: The two power inputs—V_{IN0} and V_{IN1}—and their respective power outputs—V_{OUT0} and V_{OUT1}—are tested independently in production. A shorthand notation is used in this document that allows these parameters to be referred to by "V_{INn}" and "V_{OUTn}", where *n* is permitted to take on a value of 0 or 1. This italicized "*n*" notation and convention is extended to encompass all such pin names, as well as register names with channel-specific, i.e., paged data. For example, VOUT_COMMAND*n* refers to the VOUT_COMMAND command code data located in Pages 0 and 1, which in turn relate to Channels 0 (V_{OUT0}) and Channel 1 (V_{OUT1}). Registers containing non-page-specific data, i.e., whose data is "global" to the module or applies to both of the module's Channels lack the italicized "*n*", e.g., FREQUENCY_SWITCH.

Note 5: $V_{OUTn(DC)}$ and line and load regulation tests are performed in production with digital servo disengaged (MFR_PWM_MODE*n*[6] = 0_b) and low V_{OUTn} range selected (MFR_PWM_MODE*n*[1]) = 1_b. The digital servo control loop is exercised in production (setting MFR_ PWM_MODE*n*[6] = 1_b), but convergence of the output voltage to its final settling value is not necessarily observed in final test—due to potentially long time constants involved—and is instead guaranteed by the output voltage readback accuracy specification. Evaluation in application demonstrates capability; see the Typical Performance Characteristics section.

Note 6: See output current derating curves for different V_{IN}, V_{OUT}, and T_A, located in the Applications Information section.

Note 7: Even though V_{OUT0} and V_{OUT1} are specified for 6V absolute maximum, the maximum recommended regulation-command voltage is: 3.6V for a high-V_{OUT} range setting of MFR_PWM_MODE*n*[1] = 0_b; 2.5V for a low-V_{OUT} range setting of MFR_PWM_MODE*n*[1] = 1_b.

Note 8: Minimum on-time is tested at wafer sort.

Note 9: Data conversion is performed in round-robin (cyclic) fashion. All telemetry signals are continuously digitized, and reported data is based on measurements not older than 90ms, typical. Some telemetry parameters can be digitized at a faster update rate by configuring MFR_ADC_CONTROL.

Note 10: The following telemetry parameters are formatted in PMBus-defined "Linear Data Format", in which each register contains a word comprised of 5 most significant bits—representing a signed exponent, to be raised to the power of 2—and 11 least significant bits—representing a signed mantissa: input voltage (on SV_{IN}), accessed via the READ_VIN command code; output currents (I_{OUTn}), accessed via the READ_IOUT*n* command codes; module input current ($I_{VIN0} + I_{VIN1} + I_{SVIN}$), accessed via the READ_IIN command code; channel input currents ($I_{VINn} + 1/2 \bullet I_{SVIN}$), accessed via the MFR_READ_IIN*n* command codes;and duty cycles of channel 0 and channel 1 switching power stages, accessed via the READ_DUTY_CYCLE*n* command codes. This data format limits the resolution of telemetry readback data to 10 bits even though the internal ADC is 16 bits and the LTM4686B's internal calculations use 32-bit words.

Note 11: The absolute maximum rating for the SV_{IN} pin is 6V. Input voltage telemetry (READ_VIN) is obtained by digitizing a voltage scaled down from the SV_{IN} pin.

Note 12: These typical parameters are based on bench measurements and are not production tested.

Note 13: EEPROM endurance and retention are guaranteed by wafer-level testing for data retention. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification, and whose EEPROM data was written to at $0°C \le T_J \le 85°C$. Downloading NVM contents to RAM by executing the RESTORE_USER_ALL or MFR_RESET commands is valid over the entire operating temperature range and does not influence EEPROM characteristics.

Note 14: Channel 0 OV/UV comparator threshold accuracy for MFR_PWM_MODE0[1] = 1_b tested in ATE at $V_{VOSNS0}^{+} - V_{VOSNS0}^{-}$ = 0.5V and 2.7V. Channel 0's 1V test corner condition is tested at IC-level, only. Channel 1 OV/UV comparator threshold accuracy for MFR_PWM_MODE1[1] = 1_b tested in ATE with V_{VOSNS1} to V_{SGND} = 0.5V and 2.7V. Channel 1's 1.5V test corner condition is tested at IC-level, only.

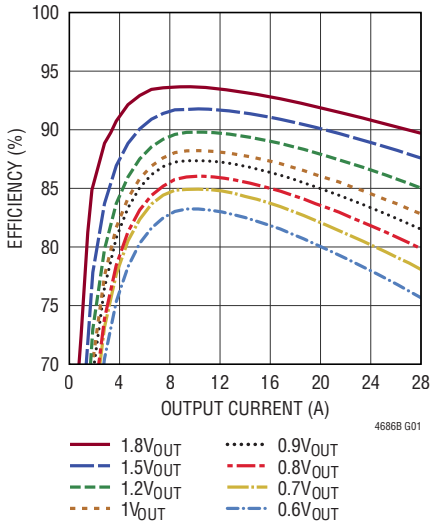
Note 15: Tested at IC-level ATE.

Note 16: PLL SYNC capture range tested with FREQUENCY_SWITCH set to frequency slave mode (0x0000), with MFR_CONFIG_ALL[4] = 1_b, and with SYNC driven by external clock. Low end of SYNC capture range (450kHz) verified at V_{INn} = 2.375V and V_{OUTn} = 0.5V. High end of SYNC capture range (1.05MHz) verified at V_{IN} = 5V and V_{OUTn} = 3.3V.

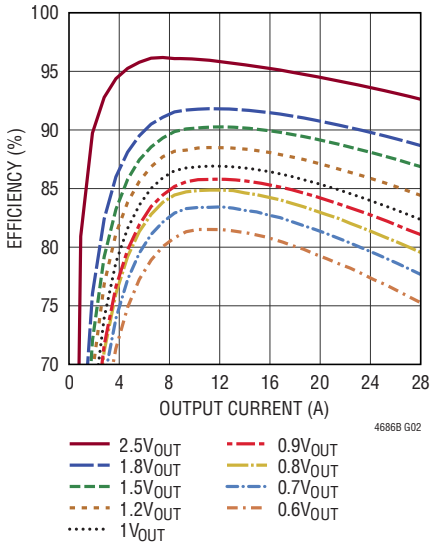
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $5V_{IN}$ to $1V_{OUT}$, switching frequency set per Table 7, unless otherwise noted.

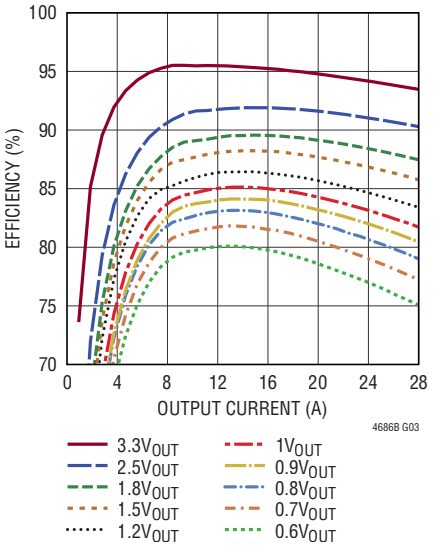
Efficiency vs Load Current at $2.5V_{IN}$



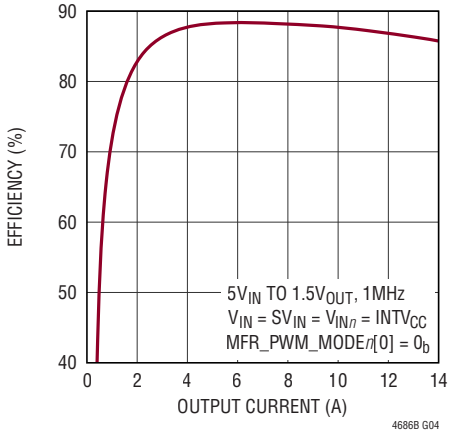
Efficiency vs Load Current at $3.3V_{IN}$



Efficiency vs Load Current at $5V_{IN}$



Single Phase Single Output Pulse-Skipping (Discontinuous) Mode Efficiency



Dual Phase Single Output Load Transient Response, $5V_{IN}$ to $1V_{OUT}$

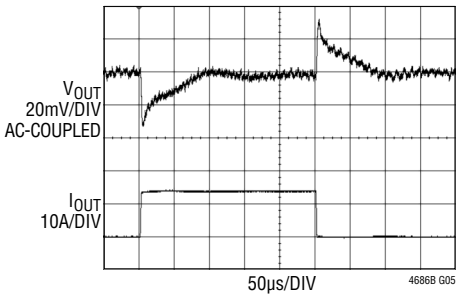


FIGURE 30 CIRCUIT AT $5V_{IN}$, VOUT_COMMAND*n* SET TO 1.000V. 14A TO 28A LOAD STEP AT 14A/µs

Single Phase Single Output Load Transient Response, $5V_{IN}$ to $1V_{OUT}$

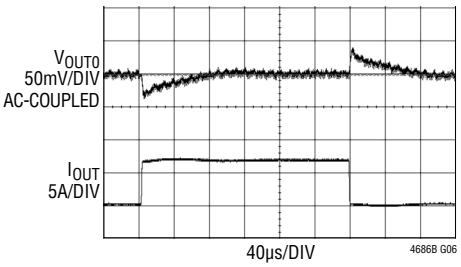


FIGURE 63 CIRCUIT AT $5V_{IN}$, 0A TO 7A LOAD STEP AT 7A/µs

Single Phase Single Output Load Transient Response, $3.3V_{IN}$ to $1V_{OUT}$

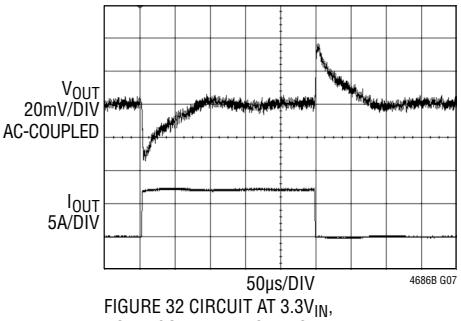


FIGURE 32 CIRCUIT AT $3.3V_{IN}$, VOUT_COMMAND*n* SET TO 1.000V. 7A TO 14A LOAD STEP AT 7A/µs

Dual Output Concurrent Rail Start-Up/Shutdown

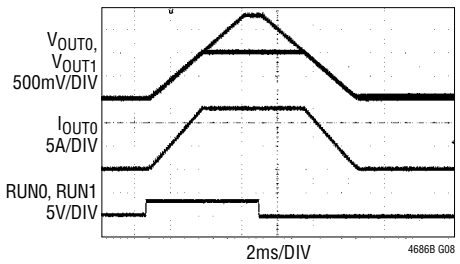


FIGURE 63 CIRCUIT AT $5V_{IN}$, 80mΩ LOAD ON V_{OUT0}, NO LOAD ON V_{OUT1}. TON_RISE0 = 3ms, TON_RISE1 = 5.297ms, TOFF_DELAY1 = 0ms, TOFF_DELAY0 = 2.43ms, TOFF_FALL1 = 5.328ms, TOFF_FALL0 = 3ms, ON_OFF_CONFIG*n* = 0x1E

Dual Output Start-Up/Shutdown with a Prebiased Load

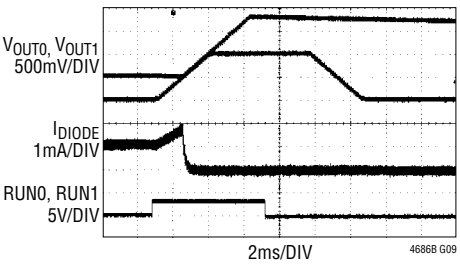


FIGURE 63 CIRCUIT AT $5V_{IN}$, 80mΩ LOAD ON V_{OUT0}, 500Ω ON V_{OUT1}. V_{OUT1} PRE-BIASED THROUGH A DIODE. TON_RISE0 = 3ms, TON_RISE_1 = 5.297ms, TOFF_DELAY1 = 0ms, TOFF_DELAY0 = 2.43ms, TOFF_FALL1 = 5.328ms, TOFF_FALL0 = 3ms, ON_OFF_CONFIG1 = 0x1F, ON_OFF_CONFIG0 = 0x1E

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $5V_{IN}$ to $1V_{OUT}$, switching frequency set per Table 7, unless otherwise noted.

Single Phase Single Output Short-Circuit Protection at No Load

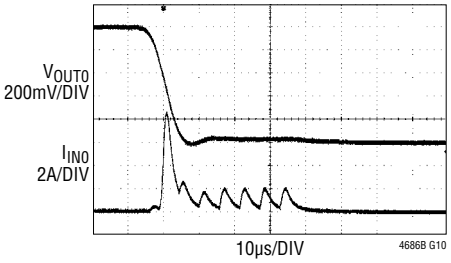


FIGURE 63 CIRCUIT AT $5V_{IN}$, NO LOAD ON V_{OUT0} PRIOR TO APPLICATION OF SHORT CIRCUIT

Single Phase Single Output Short-Circuit Protection at Full Load

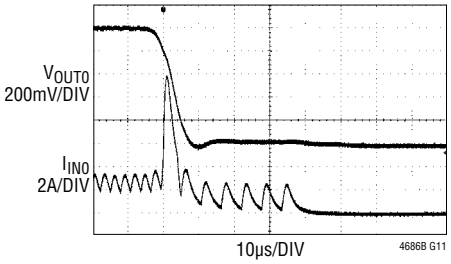
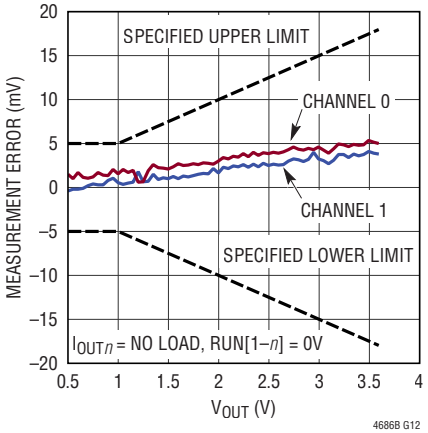
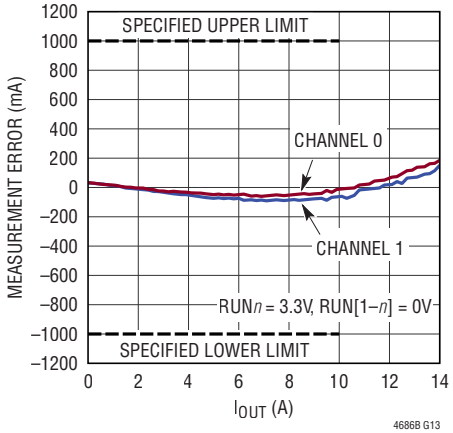


FIGURE 63 CIRCUIT AT $5V_{IN}$, 100mΩ LOAD ON V_{OUT0} PRIOR TO APPLICATION OF SHORT-CIRCUIT

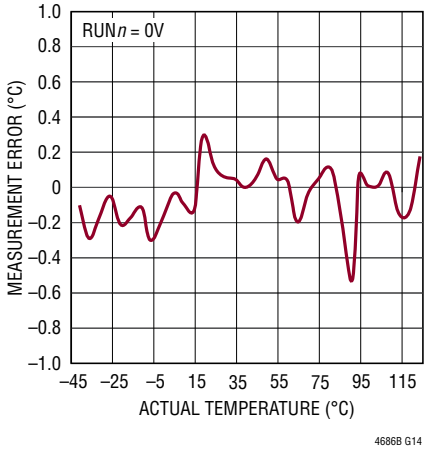
READ_VOUT*n* (Output Voltage Readback) Error vs V_{OUTn}



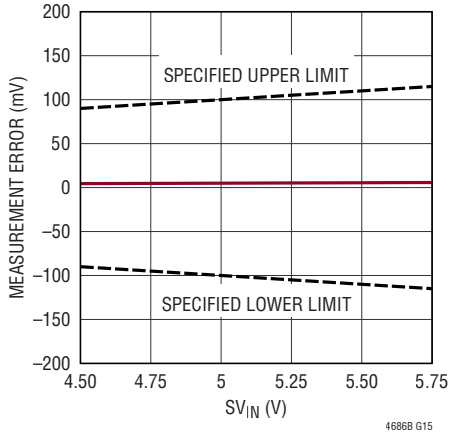
READ_IOUT*n* (Output Current Readback) Error vs I_{OUTn}



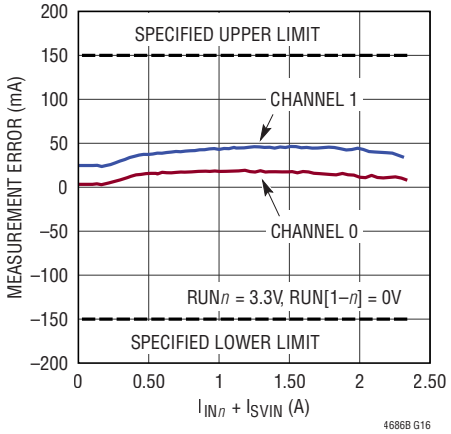
READ_TEMPERATURE_2 (Control IC Temperature Error) vs Junction Temperature



READ_VIN (Input Voltage Readback Telemetry) Error vs SV_{IN}



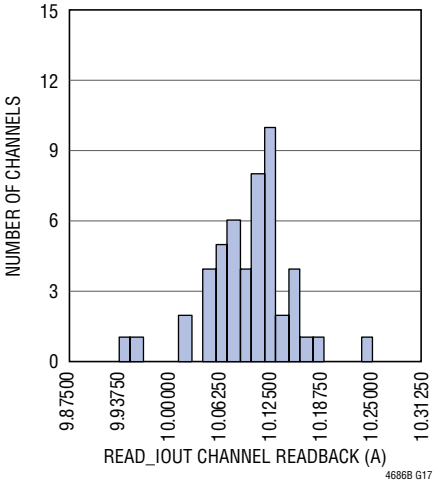
MFR_READ_IIN*n* (Input Current Readback) Error vs (I_{VINn} + I_{SVIN})



TYPICAL PERFORMANCE CHARACTERISTICS

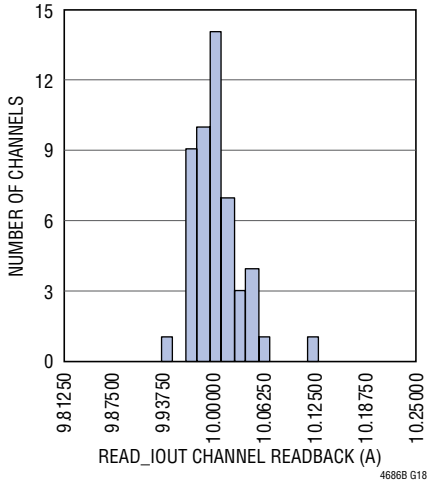
T_A = 25°C, $5V_{IN}$ to $1V_{OUT}$, switching frequency set per Table 7, unless otherwise noted.

READ_IOUT of 25 LTM4686Bs (DC3089) $5V_{IN}$, $1V_{OUT}$



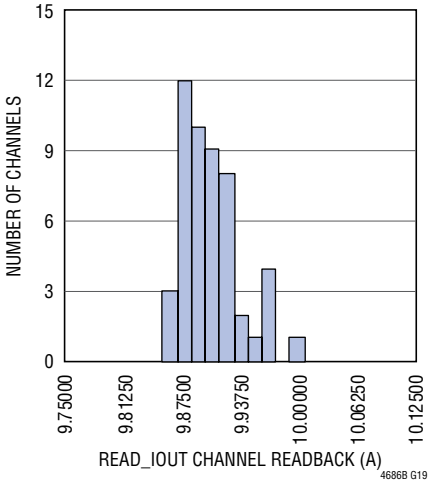
T_J = –40°C, I_{OUTn} = 10A, SYSTEM HAVING REACHED THERMALLY STEADY-STATE CONDITION, NO AIRFLOW

READ_IOUT of 25 LTM4686Bs (DC3089) $5V_{IN}$, $1V_{OUT}$



T_J = 25°C, I_{OUTn} = 10A, SYSTEM HAVING REACHED THERMALLY STEADY-STATE CONDITION, NO AIRFLOW

READ_IOUT of 25 LTM4686Bs (DC3089) $5V_{IN}$, $1V_{OUT}$



T_J = 125°C, I_{OUTn} = 10A, SYSTEM HAVING REACHED THERMALLY STEADY-STATE CONDITION, NO AIRFLOW

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{OUT0} (A1, B1, C1, D1): Channel 0 Output Voltage.

GND (A2–A8, B2–B7, C2, C4–C8, D2, D5, E1, E9, F1, F8, G1, G8–G9, H1, H8–H9, J2, J8, K2, K5–K8, L2–L7, M2–M8): Power Ground of the LTM4686B. Power return for V_{OUT0} and V_{OUT1}.

V_{IN0} (A9, B9, C9, D9): Positive Power Input to Channel 0 Switching Stage. Provide sufficient decoupling capacitance in the form of multilayer ceramic capacitors (MLCCs) and low ESR electrolytic (or equivalent) to handle reflected input current ripple from the step-down switching stage. MLCCs should be placed as close to the LTM4686B as physically possible. See Layout Recommendations in the Applications Information section.

SW0 (B8): Switching Node of Channel 0 Step-Down Converter Stage. Used for test purposes or EMI-snubbing. May be routed a short distance to a local test point to monitor switching action of Channel 0, if desired, but do not route near any sensitive signals; otherwise, leave electrically isolated (open).

TSNS0 (C3 and D3): Temperature Sensor Node for Channel 0. Pads C3 and D3 are connected to each other internal to the module. It is permissible to leave these pads electrically open circuit and to only solder these pins to mounting pads on the PC board for mechanical integrity purposes. However, it is acceptable to electrically connect C3 to D3 on the PC board.

SDA (D4): Serial Bus Data Open-Drain Input and Output. A pull-up resistor to 3.3V is required in the application.

COMP0b, COMP1b (D6 and J6, Respectively): Internal Loop Compensation Networks for Channels 0 and 1, Respectively. For the vast majority of applications, the internal, default loop compensation of the LTM4686B is suitable to apply “as is”, and yields very satisfactory results: apply the default loop compensation to the control loops of Channels 0 and 1 by simply connecting COMP0a to COMP0b and COMP1a to COMP1b, respectively. In contrast, when more specialized applications require a personal touch the optimization of control loop response,

PIN FUNCTIONS

this can be easily accomplished by connecting (an) R-C network(s) from COMP0a and/or COMP1a—terminated to SGND—and leaving COMP0b and/or COMP1b open, as desired.

V_{OSNS0}^+ (D7): Channel 0 Positive Differential Voltage Sense Input. Together, V_{OSNS0}^+ and V_{OSNS0}^- serve to kelvin-sense the V_{OUT0} output voltage at V_{OUT0}'s point of load (POL) and provide the differential feedback signal directly to Channel 0's control loop and voltage supervisor circuits. V_{OUT0} can regulate up to 3.6V output. Command V_{OUT0}'s target regulation voltage by serial bus. Its initial command value at SV_{IN} power-up is dictated by NVM (nonvolatile memory) contents (factory default: 1.200V)—or, optionally, may be set by configuration resistors; see $V_{OUT0CFG}$, $V_{TRIM0CFG}$ and the Applications Information section.

V_{ORB0}^+ (D8): Channel 0 Positive Readback Pin. Shorted to V_{OSNS0}^+ internal to the LTM4686B. If desired, place a test point on this node and measure its impedance to V_{OUT0} on one's hardware (e.g., motherboard, during in circuit test (ICT) post-assembly process) to provide a means of verifying the integrity of the feedback signal connection between V_{OSNS0}^+ and V_{OUT0}.

$\overline{GPIO0}$, $\overline{GPIO1}$ (E2 and F2, Respectively): Digital, Programmable General Purpose Inputs and Outputs. Open-drain outputs and/or high impedance inputs. The LTM4686B's factory-default NVM settings for MFR_GPIO_PROPAGATE*n*—0x7993—and MFR_GPIO_RESPONSE*n*—0x00—configure the GPIO*n* pins to behave as conventional "power good" (PGOOD) outputs for their respective channels. If PGOOD needs to be valid in the interval between the application of SV_{IN} and NVM-to-RAM download completion (~32ms after SV_{IN} is applied): connect Schottky diodes between $\overline{GPIO}n$ and RUN*n*, per Figure 1. In parallel applications, do not connect $\overline{GPIO0}$ to $\overline{GPIO1}$ unless MFR_GPIO_RESPONSE*n* and MFR_GPIO_PROPAGATE*n* are set accordingly. Pull-up resistors from $\overline{GPIO}n$ to 3.3V are required for proper operation. See the Applications Information section for details.

$\overline{ALERT}$ (E3): Open-Drain Digital Output. A pull-up resistor to 3.3V is required in the application only if SMBALERT interrupt detection is implemented in one's SMBus system.

SCL (E4): Serial Bus Clock Open-Drain Input (Can Be an Input and Output, if Clock Stretching is Enabled). A pull-up resistor to 3.3V is required in the application for digital communication to the SMBus master(s) that nominally drive this clock. The LTM4686B will never encounter scenarios where it would need to engage clock stretching unless SCL communication speeds exceed 100kHz—and even then, LTM4686B will not clock stretch unless clock stretching is enabled by means of setting MFR_CONFIG_ALL[1] = 1_b. The factory-default NVM configuration setting has MFR_CONFIG_ALL[1] = 0_b: clock stretching disabled. If communication on the bus at clock speeds above 100kHz is required, the user's SMBus master(s) need to implement clock stretching support to assure solid serial bus communications, and only then should MFR_CONFIG_ALL[1] be set to 1_b. When clock stretching is enabled, SCL becomes a bidirectional, open-drain output pin on LTM4686B.

SYNC (E5): PWM Clock Synchronization Input and Open-Drain Output Pin. The setting of the FREQUENCY_SWITCH command dictates whether the LTM4686B is a "sync master" or "sync slave" module. When the LTM4686B is a sync master, FREQUENCY_SWITCH contains the commanded switching frequency of Channels 0 and 1—in PMBus linear data format—and it drives its SYNC pin low for 500ns at a time, at this commanded rate. In contrast, a sync slave uses MFR_CONFIG_ALL[4] = 1_b and does not pull its SYNC pin low. The LTM4686B's PLL synchronizes the LTM4686B's PWM clock to the waveform present on the SYNC pin—and therefore, a resistor pull-up to 3.3V is required in the application, regardless of whether the LTM4686B is a sync master or slave. EXCEPTION: driving the SYNC pin with an external clock is permissible; see the Applications Information section for details.

COMP0a, COMP1a (E6 and H6, Respectively): Current Control Threshold and Error Amplifier Compensation Nodes for Channels 0 and 1, Respectively. The trip threshold of each channel's current comparator increases with a respective rise in COMP*n*a voltage. Small filter capacitors (22pF) internal to the LTM4686B on these COMP pins

PIN FUNCTIONS

(terminated to SGND) introduce high frequency roll off of the error-amplifier response, yielding good noise rejection in the control loop. See COMP0b/COMP1b.

V_{OSNS0}^- (E7): Channel 0 Negative Differential Voltage Sense Input. See V_{OSNS0}^+.

V_{ORB0}^- (E8): Channel 0 Negative Readback Pin. Shorted to V_{OSNS0}^- internal to the LTM4686B. If desired, place a test point on this node and measure its impedance to GND on one's hardware (e.g., motherboard, during ICT post-assembly process) to provide a means of verifying the integrity of the feedback signal connection between V_{OSNS0}^- and GND (V_{OUT0} power return).

RUN0, RUN1 (F3 and F4, Respectively): Enable Run Input for Channels 0 and 1, Respectively. Open-drain input and output. Logic high on these pins enables the respective outputs of the LTM4686B. These open-drain output pins hold the pin low until the LTM4686B is out of reset and SV_{IN} is detected to exceed VIN_ON. A pull-up resistor to 3.3V is required in the application. Do not pull RUN logic high with a low impedance source.

SGND (F5–F6, G5–G6): Channel 1 Negative Voltage Sense Input. See V_{OSNS1}. Additionally, SGND is the signal ground return path of the LTM4686B. If desired, one may place a test point on one of the four SGND pins and measure its impedance to GND on one's hardware (e.g., motherboard, during ICT post-assembly process) to provide a means of verifying the integrity of the feedback signal connection between the other three SGND pins and GND (V_{OUT1} power return). SGND is not electrically connected to GND internal to the LTM4686B. Connect SGND to GND local to the LTM4686B.

$INTV_{CC}$ (F7, G7): Control Circuit and MOSFET Driver Bias Pin. Always connect to SV_{IN}. No external decoupling is required.

SV_{IN} (F9): Input Supply for LTM4686B's Internal Control IC. In most applications, SV_{IN} connects to V_{IN0} and/or V_{IN1}, in which case no external decoupling beyond that already allocated for V_{IN0}/V_{IN1} is required. If SV_{IN} is operated from an auxiliary supply separate from V_{IN0}/V_{IN1}, decouple this pin to GND with a capacitor (0.1µF to 1µF).

ASEL (G2): Serial Bus Address Configuration Pin. On any given I^2C/SMBus serial bus segment, every device must have its own unique slave address. If this pin is left open, the LTM4686B powers up to a slave address set by MFR_ADDRESS[6:0] (see Table 5). The factory-default setting is 0x4F (hexadecimal), i.e., 1001111_b (industry standard convention is used throughout this document: 7-bit slave addressing). The lower four bits of the LTM4686B's slave address can be altered from the NVM-set value by connecting a resistor from this pin to SGND. Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state.

$V_{OUT0CFG}$ (G3): Output Voltage Select Pin for V_{OUT0}, Coarse Setting. If the $V_{OUT0CFG}$ and $V_{TRIM0CFG}$ pins are both left open—or, if the LTM4686B is configured to ignore pin-strap (R_{CONFIG}) resistors, i.e., MFR_CONFIG_ALL[6] = 1_b—then the LTM4686B's target V_{OUT0} output voltage setting (VOUT_COMMAND0) and associated power-good and OV/UV warning and fault thresholds are dictated at SV_{IN} power-up according to the LTM4686B's NVM contents. A resistor* connected from this pin to SGND—in combination with resistor pin settings on $V_{TRIM0CFG}$, and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0_b—can be used to configure the LTM4686B's Channel 0 output to power-up to a VOUT_COMMAND value (and associated output voltage monitoring and protection/fault-detection thresholds) different from those of NVM contents. (See the Applications Information section.) Connecting resistor(s) from $V_{OUT0CFG}$ to SGND and/or $V_{TRIM0CFG}$ to SGND in this manner allows a convenient way to configure multiple LTM4686Bs with identical NVM contents for different output voltage settings—all without GUI intervention or the need to "custom-pre-program" module NVM contents. Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of $R_{CONFIGs}$* on $V_{OUT0CFG}/V_{TRIM0CFG}$ can affect the V_{OUT0} range setting (MFR_PWM_MODE0[1]) and loop gain.

$V_{OUT1CFG}$ (G4): Output Voltage Select Pin for V_{OUT1}, Coarse Setting. If the $V_{OUT1CFG}$ and $V_{TRIM1CFG}$ pins are both left open—or, if the LTM4686B is configured to ignore pin-strap (R_{CONFIG}) resistors, i.e., MFR_CONFIG_ALL[6] = 1_b—then the LTM4686B's target V_{OUT1} output voltage setting (VOUT_COMMAND1) and associated OV/

*In applications where V_{OUT0} and V_{OUT1} are paralleled, the respective $V_{OUTnCFG}$ and $V_{TRIMnCFG}$ pin-pairs can be electrically connected together; common RCONFIG resistors can be applied, whose values are half of what is prescribed in Table 2 and Table 3. See Figure 35, for example.

PIN FUNCTIONS

UV warning and fault thresholds are dictated at SV_{IN} power-up according to the LTM4686B's NVM contents, in precisely the same fashion that the $V_{OUT0CFG}$ and $V_{TRIM0CFG}$ pins affect the respective settings of V_{OUT0}/Channel 0. (See $V_{OUT0CFG}$, $V_{TRIM0CFG}$ and the Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of $R_{CONFIGs}$* on $V_{OUT1CFG}$/$V_{TRIM1CFG}$ can affect the V_{OUT1} range setting (MFR_PWM_MODE1[1]) and loop gain.

$F_{SWPHCFG}$ (H2): Switching Frequency, Channel Phase-Interleaving Angle and Phase Relationship to SYNC Configuration Pin. If this pin is left open—or, if the LTM4686B is configured to ignore pin-strap (R_{CONFIG}) resistors, i.e., MFR_CONFIG_ALL[6] = 1_b—then the LTM4686B's switching frequency (FREQUENCY_SWITCH) and channel phase relationships (with respect to the SYNC clock; MFR_PWM_CONFIG[2:0]) are dictated at SV_{IN} power-up according to the LTM4686B's NVM contents. Default factory values are: 1MHz operation; Channel 0 at 0°; and Channel 1 at 180° (convention throughout this document: a phase angle of 0° means the channel's switch node rises coincident with the falling edge of the SYNC pulse). Connecting a resistor from this pin to SGND (and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0_b) allows a convenient way to configure multiple LTM4686Bs with identical NVM contents for different switching frequencies of operation and phase interleaving angle settings of intra- and extra-module-paralleled channels—all, without GUI intervention or the need to "custom pre-program" module NVM contents. (See the Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state.

$V_{TRIM0CFG}$ (H3): Output Voltage Select Pin for V_{OUT0}, Fine Setting. Works in combination with $V_{OUT0CFG}$ to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 0, at SV_{IN} power-up. (See $V_{OUT0CFG}$ and the Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of $R_{CONFIGs}$* on $V_{OUT0CFG}$/$V_{TRIM0CFG}$ can affect the V_{OUT0} range setting (MFR_PWM_MODE0[1]) and loop gain.

$V_{TRIM1CFG}$ (H4): Output Voltage Select Pin for V_{OUT1}, Fine Setting. Works in combination with $V_{OUT1CFG}$ to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 1, at SV_{IN} power-up. (See $V_{OUT1CFG}$ and the Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of $R_{CONFIGs}$* on $V_{OUT1CFG}$/$V_{TRIM1CFG}$ can affect the V_{OUT1} range setting (MFR_PWM_MODE1[1]) and loop gain.

SHARE_CLK (H5): Share Clock, Bidirectional Open-Drain Clock Sharing Pin. Nominally 100kHz. Used for synchronizing the time base between multiple LTM4686Bs (and any other Analog Devices, Inc. devices with a SHARE_CLK pin)—to realize well-defined rail sequencing and rail tracking. Tie the SHARE_CLK pins of all such devices together; all devices with a SHARE_CLK pin will synchronize to the fastest clock. A pull-up resistor to 3.3V is required when synchronizing the time base between multiple devices. If synchronizing the time base between multiple devices is not needed and MFR_CHAN_CONFIG*n*[2] = 0_b, only then is a pull-up resistor not required.

V_{OSNS1} (H7): Channel 1 Positive Voltage Sense Input. Connect V_{OSNS1} to V_{OUT1} at the POL. This provides the feedback signal for Channel 1's control loop and voltage supervisor circuits. V_{OUT1} can regulate up to 3.6V output. Command V_{OUT1}'s target regulation voltage by serial bus. Its initial command value at SV_{IN} power-up is dictated by NVM (nonvolatile memory) contents (factory default: 1.200V)—or, optionally, may be set by configuration resistors; see $V_{OUT1CFG}$, $V_{TRIM1CFG}$ and the Applications Information section.

V_{OUT1} (J1, K1, L1, M1): Channel 1 Output Voltage.

PIN FUNCTIONS

TSNS1a, TSNS1b (J3 and K3, Respectively): Channel 1 Temperature Excitation/Measurement and Thermal Sensor Pins, Respectively. In most applications, connect TSNS1a to TSNS1b. This allows the LTM4686B to monitor the Power Stage Temperature of Channel 1. See the Applications Information section for information on how to use TSNS1a to monitor a temperature sensor external to the module, e.g., a PN junction on the die of a microprocessor.

V_{DD25} (J4): Internally Generated 2.5V Power Supply Output Pin. Do not load this pin with external current; it is used strictly to bias internal logic and provides current for the internal pull-up resistors connected to the configuration-programming pins. No external decoupling is required.

V_{DD33} (J5): Internally Generated 3.3V Power Supply Output Pin. This pin should only be used to provide external current for the pull-up resistors required for $\overline{GPIO}n$, SHARE_CLK, and SYNC, and may be used to provide external current for pull-up resistors on RUN*n*, SDA, SCL and $\overline{ALERT}$. No external decoupling is required.

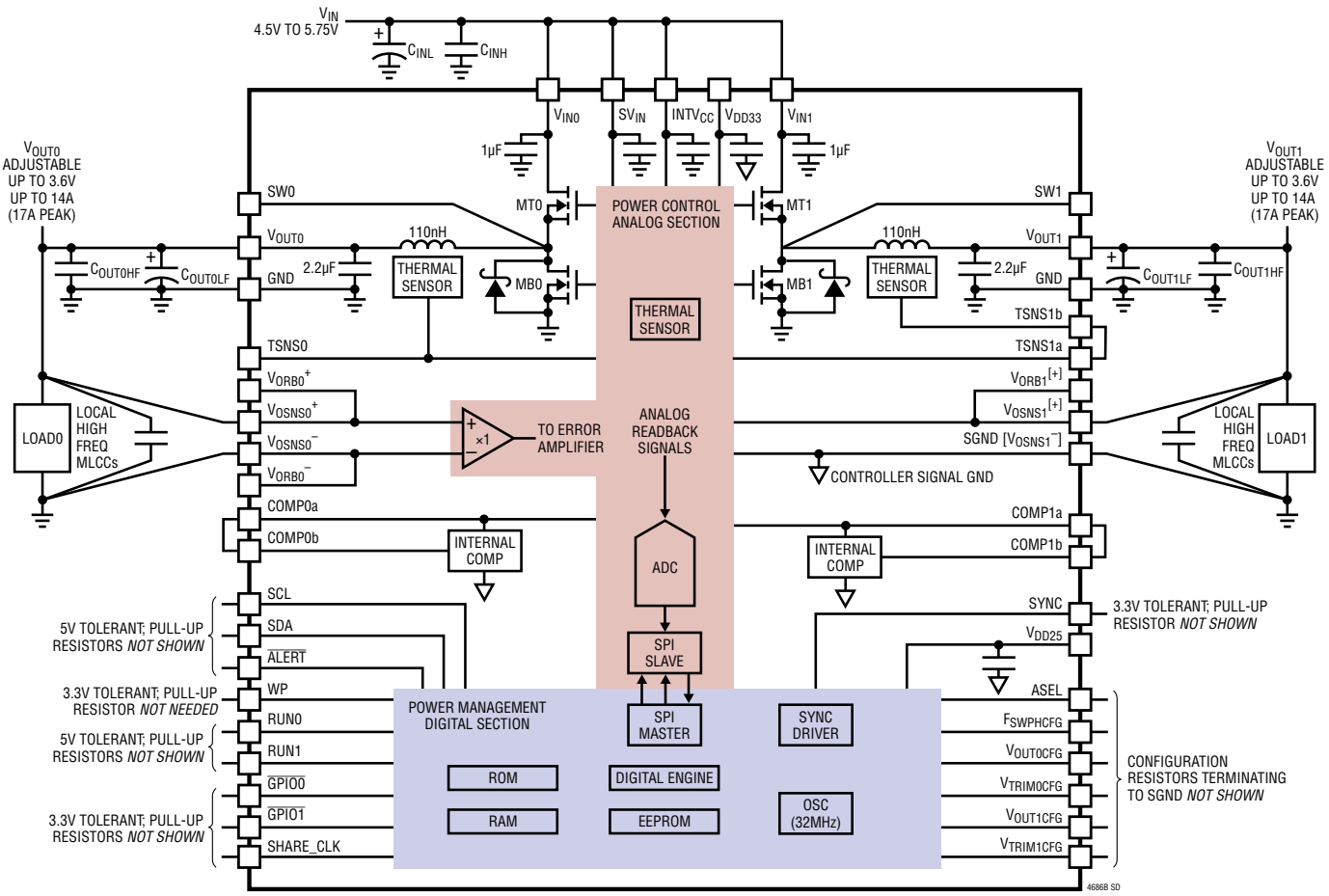
V_{ORB1} (J7): Channel 1 Positive Readback Pin. Shorted to V_{OSNS1} internal to the LTM4686B. At one's option, place a test point on this node and measure its impedance to V_{OUT1} on one's hardware (e.g., motherboard, during ICT post-assembly process) to provide a means of verifying the integrity of the feedback signal connection between V_{OUT1} and V_{OSNS1}.

V_{IN1} (J9, K9, L9, M9): Positive Power Input to Channel 1 Switching Stage. Provide sufficient decoupling capacitance in the form of MLCCs and low ESR electrolytic (or equivalent) to handle reflected input current ripple from the step-down switching stage. MLCCs should be placed as close to the LTM4686B as physically possible. See Layout Recommendations in the Applications Information section.

WP (K4): Write Protect Pin, Active High. An internal 10µA current source pulls this pin to V_{DD33}. If WP is open circuit or logic high, only I^2C writes to PAGE, OPERATION, CLEAR_FAULTS, MFR_CLEAR_PEAKS and MFR_EE_UNLOCK are supported. Additionally, individual faults can be cleared by writing 1_b's to bits of interest in registers prefixed with "STATUS". If WP is low, I^2C writes are unrestricted.

SW1 (L8): Switching Node of Channel 1 Step-Down Converter Stage. Used for test purposes or EMI-snubbing. May be routed a short distance to a local test point to monitor switching action of Channel 1, if desired, but do not route near any sensitive signals; otherwise, leave open.

SIMPLIFIED BLOCK DIAGRAM

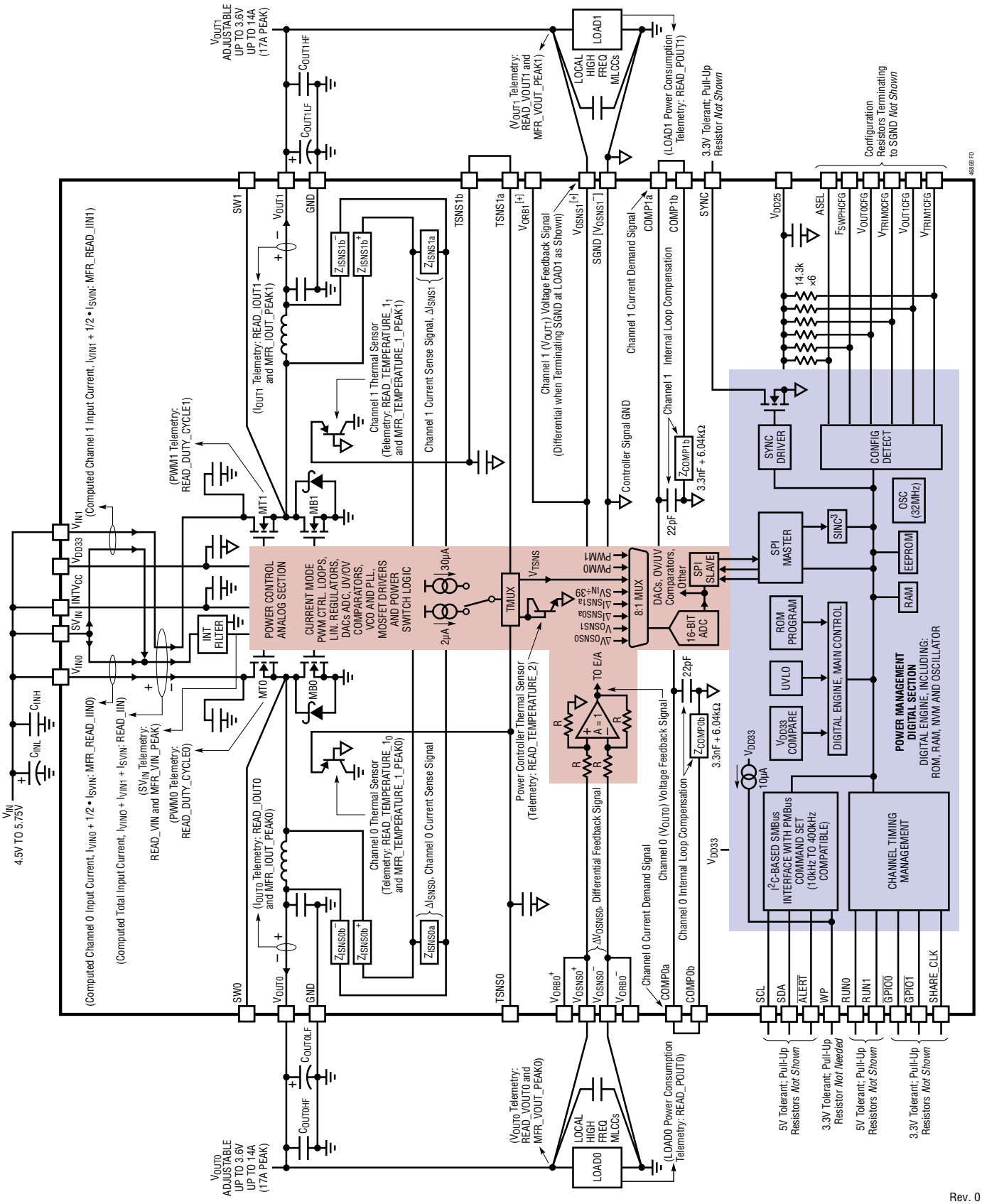


DECOUPLING REQUIREMENTS

T_A = 25°C. Using the Simplified Block Diagram configuration.

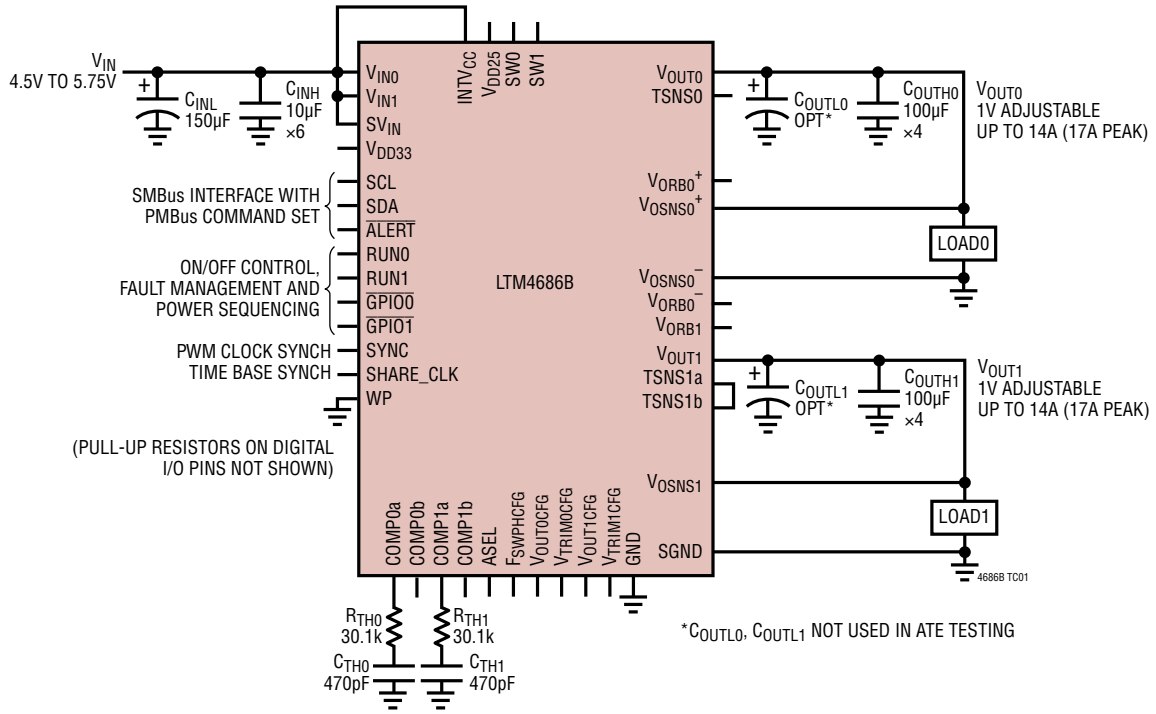
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{INH}	External High Frequency Input Capacitor Requirement ($4.5V \le V_{IN} \le 5.75V$, V_{OUTn} Commanded to 1.000V)	I_{OUT0} = 14A, 22µF ×2, or 10µF ×3 I_{OUT1} = 14A, 22µF ×2, or 10µF ×3	30	44		µF
$C_{OUTn HF}$	External High Frequency Output Capacitor Requirement ($4.5V \le V_{IN} \le 5.75V$, V_{OUTn} Commanded to 1.000V)	I_{OUT0} = 14A I_{OUT1} = 14A		400 400		µF µF

FUNCTIONAL DIAGRAM

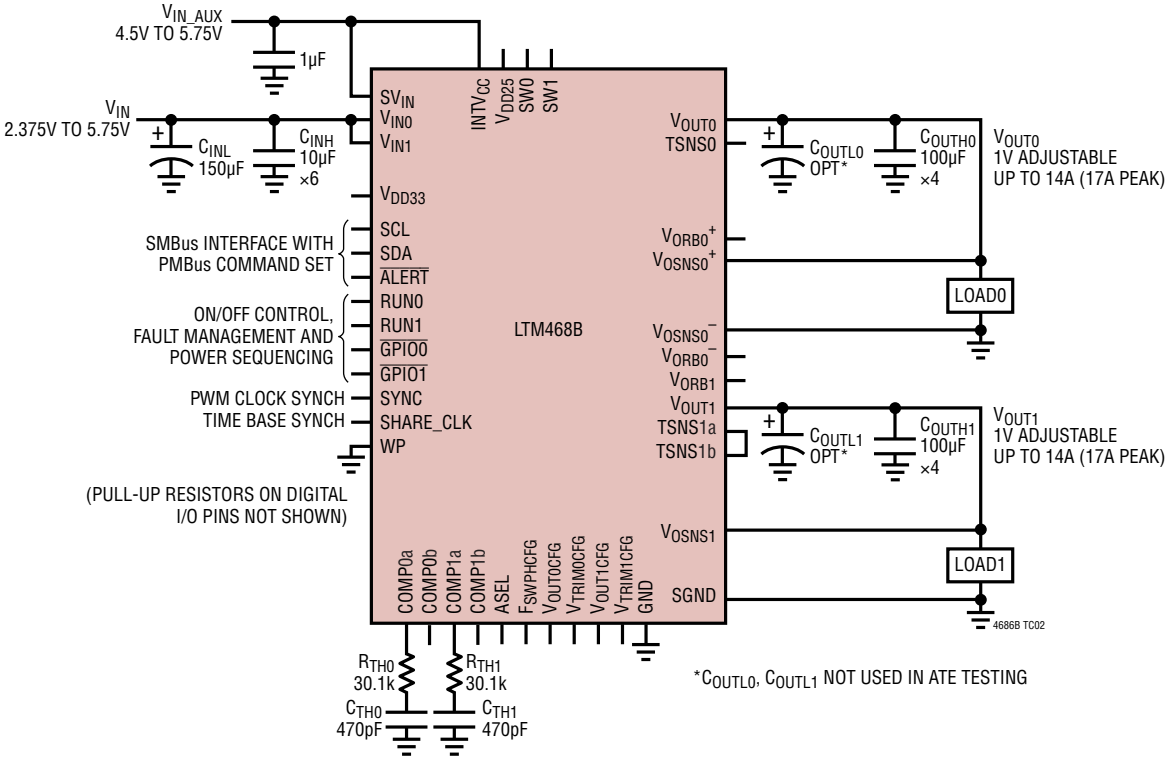


TEST CIRCUITS

Test Circuit 1. LTM4686B ATE Single-Input-Supply Configuration, 4.5V ≤ V_{IN} ≤ 5.75V



Test Circuit 2. LTM4686B ATE Multi-Input-Supply Configuration, 2.375V ≤ V_{IN} ≤ 5.75V



OPERATION

POWER MODULE INTRODUCTION

The LTM4686B is a highly configurable dual 14A (17A peak) output standalone nonisolated switching mode step-down DC/DC power supply with built-in EEPROM NVM (nonvolatile memory) with ECC and I²C-based PMBus/SMBus 2-wire serial communication interface capable of 400kHz SCL bus speed. Two output voltages can be regulated (V_{OUT0}, V_{OUT1}—collectively, V_{OUTn}) with a few external input and output capacitors and pull-up resistors. Readback telemetry data of average input and output voltages and currents, Channel PWM duty cycles, and module temperatures are continually digitized cyclically by an integrated 16-bit ADC (analog-to-digital converter). Many fault thresholds and responses are customizable. Data can be autonomously saved to EEPROM when a fault occurs, and the resulting fault log can be retrieved over I²C at a later time, for analysis.

The LTM4686B provides precisely regulated output voltages between 0.5VDC to 3.6VDC (±0.5% above 1VDC, ±5mV below 1VDC). The target output voltage can be set according to pin-strapping resistors ($V_{OUTnCFG}$ and $V_{TRIMnCFG}$ pins), NVM/register settings, and altered on the fly via the I²C interface. The output voltage can be modified by the user at any time with a write to PMBus VOUT_COMMAND. Executing this command has a typical latency less than 10ms. Writes to PMBus OPERATION have a typical latency less than 1ms. The NVM factory-default switching frequency is 1MHz and the phase-interleaving angle between its two channels is 180°. Channel switching frequency, phase angle, and phase relationship with respect to the falling edge of the SYNC pin waveform can be configured according to a pin-strap resistor ($F_{SWPHCFG}$ pin) and NVM/register settings—though, not on the fly during regulation. The 7-bit I²C slave address of the module defaults to the value retrieved from MFR_ADDRESS[6:0] at power-up (factory default: 0x4F), but the least significant four bits of the address are set by resistor pin-strapping the ASEL pin. Bits[6:4] of MFR_ADDRESS can be written and stored to EEPROM. Between the ASEL resistor pin-strap and user-configurable MFR_ADDRESS[6:4], the LTM4686B can take on any 7-bit slave address desired. With the exception of the ASEL pin, the module can be configured to ignore all pin-strap resistors, if desired (see MFR_CONFIG_ALL[6]).

Table 1 provides a summary of LTM4686B's supported PMBus commands. For details on the supported commands, payloads and data formats see Appendix C: PMBus Command Details.

For introductory information about the PMBus Specification, see Appendix A: Similarity Between PMBus, SMBus and I²C 2-Wire Interface. For information about the data communication link layer and timing diagrams, see Appendix B: PMBus Serial Digital Interface.

Major features of the LTM4686B strictly from a DC/DC converter power delivery point of view are as follows:

- Up to 14A (17A peak) Output Current Delivery from Each of Two Integrated Power Stages (See Front Page Figure)—or Up to 28A (34A peak) Output, Combined (See Figure 29 and Figure 35).
- DC/DC Step-Down Conversion from 4.5V to 5.75V Input. (see Figure 29).
- DC/DC Step-Down Conversion Possible from Less Than 4.5V Input When an Auxiliary 5V Bias Supply Powers SV_{IN} and $INTV_{CC}$ (see Figure 31).
- Wide Input Voltage Range: DC/DC Step-Down Conversion from 2.375V to 5.75V Input, Driving SV_{IN} and $INTV_{CC}$ with ~5V Auxiliary Bias (see Test Circuit 2).
- Output Voltage Range: 0.5V to 3.6V on both V_{OUT0} and V_{OUT1}.
- Differential Remote Sensing of V_{OUT0} (V_{OSNS0}^+/V_{OSNS0}^-). For paralleled outputs, the V_{OSNS0}^+/V_{OSNS0}^- pin-pair can be configured as the feedback path for both V_{OUT0} and V_{OUT1} (see Figure 35 and, optionally, MFR_PWM_CONFIG[7]).
- Start-Up Into a Prebiased Load Without Sinking Current.
- Four LTM4686Bs Can Be Paralleled to Deliver Up to ~108A (See Figure 32).
- One LTM4686B Can Be Paralleled with Three LTM4650 Modules to Deliver Up to 174A; Infer Rail Status and Telemetry of Paralleled LTM4650 via the Sole LTM4686B (See Figure 33).
- Discontinuous Mode Operation Available for Higher Light-Load Efficiency (MFR_PWM_MODE*n*[0]).
- Output Current Limit and Overvoltage Protection.

OPERATION

- Three Integrated Temperature Sensors, Over/Undertemperature Protection.
- Constant Frequency Peak Current Mode Control.
- Configurable Switching Frequency, 500kHz to 1MHz; Synchronizable to External Clock; Seven Configurable Channel Phase Interleaving Settings.
- Internal Loop Compensation Provided; External Loop Compensation Can Be Applied, if Preferred.
- Low Profile (16mm × 11.9mm × 1.82mm) LGA Package Power Solution Requires Only Input and Output Capacitors; at Most, Nine Pull-Up Resistors for Open-Drain Digital Signals; at Most, Six Pull-Down Resistors to Configure All Possible Pin-Strapping Options.

Features of the LTM4686B that enable power system management, rail sequencing, and fault monitoring and reporting are as follows:

- I^2C-based PMBus/SMBus 2-Wire Serial Communication Interface (SDA, SCL) with $\overline{\text{ALERT}}$ Interrupt Pin, SCL Clock Capable of 400kHz Bus Communication Speeds with Clock Low Extending—or 100kHz, Otherwise.
- Configurable Output Voltage.
- Configurable Input Undervoltage Comparators (UVLO Rising, UVLO Falling).
- Configurable Switching Frequency.
- Configurable Current Limit.
- Configurable Output Over/Undervoltage Comparators.
- Configurable Turn-On and Turn-Off Delay Times.
- Configurable Output Ramp Rise and Fall Times.
- Nonvolatile Configuration Memory (NVM EEPROM) with ECC to Configure Aforementioned Settings, and More—Yielding Standalone Operation, if Desired, and Also Enabling In-Situ Changes to the LTM4686B's Configuration in Embedded Designs.
- Monitoring and Reporting of Telemetry Data: Average Output and Input Currents and Voltages, Internal Temperatures, and Power Stage Duty Cycles—Continuously Digitized Cyclically by a 16-Bit ADC.
  - Peak Observed Output Current and Voltage, Input Voltage, and Module Temperatures Can Be Polled and Cleared/Reset.
  - ADC Latency Not Greater Than 90ms, Nominal.
  - Option to Monitor One External Temperature in Lieu of Channel 1 (V_{OUT1}) Module Power Stage Temperature.
- Monitoring, Reporting, and Configurable Response to Latching and Non-Latching Individual Fault and/or Warning Status, Including but Not Limited to:
  - Output Over/Undervoltages.
  - Input (SV_{IN}) Over/Undervoltages.
  - Module Input and Power Stage Output Overcurrents.
  - Module Power Stage Over/Under Temperatures.
  - Internal Control IC Overtemperature.
  - Communication, Memory and Logic (CML) Faults.
- Fault Logging Upon Detection of a Fault Condition. The LTM4686B Can Be Configured to Automatically Upload a Fault Log to Its NVM, Consisting of: an Uptime Counter, Peak Observed Telemetry, Telemetry Gathered from the Six Most Recent Rounds of Cyclical ADC Data Leading Up to the Detection of the Fault That Triggered Fault Log Writing, and Fault Status Associated with That ADC History.
- Two Configurable Open-Drain General Purpose Input/Output Pins ($\overline{\text{GPIO0}}$, $\overline{\text{GPIO1}}$), Which Can Be Used for:
  - Fault Reporting, e.g., as a System Interrupt Signal.
  - Coordinating Turn-On/Off of the LTM4686B in Multiphase/Multirail Systems.
  - Propagating an Unfiltered Power Good Signal (Output of a V_{OUTn} Undervoltage Comparator) to Command Turn-On/Off of a Downstream Rail.
- A Write Protect (WP) Pin and Configurable WRITE_PROTECT Register to Protect the Internal Configuration of RAM and NVM Against Unintended Changes via I^2C.
- Time-Base Interconnect (SHARE_CLK, 100kHz Heartbeat) for Synchronization in the Time Domain Between Multiple LTM4686Bs.
- Optional External Configuration Resistors ($R_{CONFIGs}$) for Setting Start-Up Output Voltages, Switching Frequency and Channel-to-Channel Phase Interleaving Angle.
- Any 7-Bit Slave Address Can Be Assigned to the LTM4686B (0x4F Default), Configured by Resistor Pin Strapping the ASEL Pin and User-Editable Bits [6:4] of MFR_ADDRESS.

OPERATION

POWER MODULE CONFIGURABILITY AND READBACK DATA

This section of the data sheet describes all the configurable features and readable data of the LTM4686B accessible via I²C. The relevant command code name(s) are indicated by use of all capital letters, e.g., "VIN_ON". Refer to Table 1 and Appendix C: PMBus Command Details of this data sheet for details of the command code, payload size, data format and factory-default value. Specific register bits of some registers are indicated with the use of brackets, i.e., "[" and "]". The least significant bit (LSB) of a register is bit number zero, indicated by "[0]". The most significant bit of a byte-long (8-bit-long) register is bit number seven, indicated by "[7]". The most significant bit (MSB) of a word-long (16-bit-long) register is bit number fifteen, indicated by "[15]". Multiple bits of a register can be alluded to with the use of a colon, e.g., bits 2, 1 and 0 of the MFR_PWM_CONFIG register are indicated by "MFR_PWM_CONFIG[2:0]". Bits can take on values of 0_b or 1_b. The subscripted "$_b$" suffix indicates the number's value is in binary. Values in hexadecimal are indicated with a "0x" prefix. For example, decimal value "89" is indicated by 0x59 and 01011001_b (8-bit-long values), as well as 0x0059 and 0000000001011001_b (16-bit-long values).

One further shorthand notion the reader will notice is the italicized "*n*" or "*n*". "*n*" can take on a value of 0 or 1—and provides an easy way to refer to registers which are paged commands, i.e., register names which have the same command code value but can be configured independently (or yield channel-specific telemetry) for Channel 0 (Page 0, or 0x00) vs Channel 1 (Page 1, or 0x01). Registers lacking an "*n*" are therefore easily identified as being global in nature, i.e., common to both Channels/Outputs. For example, the switching frequency setting commanded by register FREQUENCY_SWITCH is common to both channels, and lacks "*n*". Another example: the READ_VIN register contains the digitized input voltage as seen at the SV_{IN} pin, and SV_{IN} is unique, i.e., common to both Channels. In contrast, the nominal commanded output voltage is indicated by the register VOUT_COMMAND*n*. The "*n*" indicates that VOUT_COMMAND can be set differently for Channel 0 vs Channel 1. Executing the PAGE Command (Command Code 0x00) with payload 0x00 sets the LTM4686B to write/read data pertaining to Channel 0 in all subsequent I²C transactions until the Page is changed. Executing the PAGE Command with payload 0x01 sets the LTM4686B to write/read data pertaining to Channel 1 in all subsequent I²C transactions until the Page is changed. Executing the PAGE Command with payload 0xFF sets the LTM4686B to write data pertaining to Channels 0 and 1 in all subsequent I²C write transactions until the Page is changed. Reads from and writes to global registers do not require setting the Page to 0xFF. Reads from channel-specific (i.e., non-global) registers when the Page is set to 0xFF result in the LTM4686B reporting the value on Page 0x00 (i.e., Channel 0-specific data).

The list below itemizes aspects of the LTM4686B relating to power supply functions that are configurable by I²C communications—provided the state of the WP (write protect) pin and the WRITE_PROTECT register value permit the I²C writes—and by EEPROM settings:

- Output start-up voltages (VOUT_COMMAND*n*), the maximum commandable output voltages (VOUT_MAX*n*), output margin high (VOUT_MARGIN_HIGH*n*) and margin low (VOUT_MARGIN_LOW*n*) command voltages, and output over/undervoltage warning and fault thresholds (VOUT_OV_WARN_LIMIT*n*, VOUT_OV_FAULT_LIMIT*n*, VOUT_UV_WARN_LIMIT*n*, and VOUT_UV_FAULT_LIMIT*n*). Additionally, these values can be configured at SV_{IN} power-up according to resistor-pin strapping of the $V_{OUT0CFG}$, $V_{TRIM0CFG}$, $V_{OUT1CFG}$ and/or $V_{TRIM1CFG}$ pins, provided MFR_CONFIG_ALL[6] = 0_b.
- Output voltages, on the fly, including transition rate ($\Delta V/\Delta t$), VOUT_TRANSITION_RATE*n*—either by I²C writes to the VOUT_COMMAND*n*, VOUT_MARGIN_HIGH*n*, or VOUT_MARGIN_LOW*n* registers, and/or to the OPERATION*n* register.
- Input undervoltage-lockout, rising (VIN_ON) and input undervoltage lockout, falling (VIN_OFF), based on the SV_{IN} pin voltage.
- Switching frequency (FREQUENCY_SWITCH) and channel phase-interleaving angle (MFR_PWM_CONFIG[2:0]). However, these parameters can be changed via I²C communications only when the LTM4686B's channels are off, i.e., not switching. The LTM4686B synchronizes

OPERATION

its switching frequency to a clock signal supplied to its SYNC pin when MFR_CONFIG_ALL[4] = 1_b. These parameters can be configured at SV_{IN} power-up according to resistor-pin strapping of the $F_{SWPHCFG}$ pin, provided MFR_CONFIG_ALL[6] = 0_b.

- Output voltage turn-on and turn-off sequencing and associated watchdog timers, namely:
  - Output voltage turn-on delay time (the time delay from the LTM4686B being commanded to turn on, e.g., by the RUN*n* pin toggling from logic low to high, before switching action commences. TON_DELAY*n*).
  - Output voltage soft-start ramp-up time (TON_RISE*n*).
  - The amount of time (TON_MAX_FAULT_LIMIT*n*) permitted to elapse after the LTM4686B is commanded to turn on, e.g., by the RUN*n* pin toggling from logic low to high, after which, if the output voltage fails to exceed the output undervoltage fault threshold (VOUT_UV_FAULT_LIMIT*n*), the LTM4686B's output (V_{OUTn}) is declared to have not come up in a timely manner.
  - The LTM4686B's response to any such aforementioned TON_MAX_FAULT_LIMIT*n* event (TON_MAX_FAULT_RESPONSE*n*).
  - Output voltage soft-stop ramp-down time (TOFF_FALL*n*).
  - Output voltage turn-off delay time (the time delay from the LTM4686B being commanded to turn off, e.g., by the RUN*n* pin toggling from logic high to low, before switching action ceases. TOFF_DELAY*n*).
  - When commanded to turn off its output—or, when turning off its output in response to a fault—configuring whether the LTM4686B's output (V_{OUTn}) becomes high impedance ("High-Z" or "three state"—turning off both MT*n* and MB*n* in the power stage). ("Immediate Off", ON_OFF_CONFIG*n*[0] = 1_b vs configuring the output voltage to be ramped down according to TOFF_FALL*n* and/or TOFF_DELAY*n* settings, ON_OFF_CONFIG*n*[0] = 0_b).
  - The amount of time (TOFF_MAX_WARN_LIMIT*n*) permitted to elapse after the LTM4686B is supposed to have turned off its output, i.e., at the end of the period dictated by TOFF_FALL*n*, after which, If the output voltage has not fallen below 12.5% of the former target voltage of regulation, the LTM4686B's output (V_{OUTn}) is declared to have not powered down in a timely manner.
- Configurable output voltage restart time. Subsequent to the RUN*n* pin being pulled low, the LTM4686B pulls RUN*n* logic low, itself, and the output cannot be restarted until a minimum time has elapsed—the restart delay time. This delay assures proper sequencing of all system rails. The minimum restart delay processed by the LTM4686B is the longer of (TOFF_DELAY*n* + TOFF_FALL*n* + 136ms) vs the commanded MFR_RESTART_DELAY*n* register value. At the end of this delay, the LTM4686B releases its RUN*n* pin.
- Configurable fault-hiccup retry delay time. When a fault occurs in which the LTM4686B's fault response behavior to that fault is to reattempt power-up of its output voltage after said fault ceases to be present (e.g., "Infinite Retry"), the delay time for the LTM4686B to re-engage switching action is the longer of the MFR_RETRY_DELAY*n* time vs the time required for the output to decay below 12.5% of the formerly commanded output voltage value (unless this latter most criteria, i.e., requiring the output to decay below 12.5% is negated by the setting of MFR_CHAN_CONFIG*n*[0] to "1_b"—which is the LTM4686B's factory-NVM default setting).
- Output over/undervoltage fault responses (VOUT_OV_FAULT_RESPONSE*n*, VOUT_UV_FAULT_RESPONSE*n*).
- Time-averaged current limit warning and instantaneous peak (cycle-by-cycle) fault thresholds, and fault response (IOUT_OC_WARN_LIMIT*n*, IOUT_OC_FAULT_LIMIT*n*, IOUT_OC_FAULT_RESPONSE*n*).
- Channel (V_{OUT0}, V_{OUT1}) overtemperature warning and fault thresholds, and fault response (OT_WARN_LIMIT*n*, OT_FAULT_LIMIT*n*, OT_FAULT_RESPONSE*n*).
- Channel (V_{OUT0}, V_{OUT1}) undertemperature fault thresholds and fault response (UT_FAULT_LIMIT*n*, UT_FAULT_RESPONSE*n*).

OPERATION

- Input overvoltage fault threshold and response (VIN_OV_FAULT_LIMIT, VIN_OV_FAULT_RESPONSE), based on the SV_{IN} pin voltage.
- Input undervoltage warning threshold (VIN_UV_WARN_LIMIT) based on the SV_{IN} pin voltage.
- Module input overcurrent warning threshold (IIN_OC_WARN_LIMIT).

The control IC within the LTM4686B module ceases switching action if control IC temperature exceeds 160°C (Note 12). The control IC resumes operation after a 10°C cool-down hysteresis. Note that these typical parameters are based on measurements in a lab oven and are not production tested. This overtemperature protection is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

TIME-AVERAGED AND PEAK READBACK DATA

Time-averaged telemetry readback data accessible via I^2C communications follow:

- Channel output current (READ_IOUT*n*) and peak observed value of READ_IOUT*n* (MFR_IOUT_PEAK*n*).
- Channel output voltage (READ_VOUT*n*) and peak observed value of READ_VOUT*n* (MFR_VOUT_PEAK*n*).
- Channel output power (READ_POUT*n*).
- Channel input current (MFR_READ_IIN*n*) and module input current (READ_IIN).
- Channel temperatures (READ_TEMPERATURE_1_*n*) and peak observed values of READ_TEMPERATURE_1_*n* (MFR_TEMPERATURE_1_PEAK*n*).
- Control IC temperature (READ_TEMPERATURE_2) and peak observed value (MFR_TEMPERATURE_2_PEAK).
- Input voltage (READ_VIN), based on the voltage of the SV_{IN} pin, and peak observed value of READ_VIN (MFR_VIN_PEAK).
- Channel topside power MOSFET (MT*n*) duty cycle (READ_DUTY_CYCLE*n*).

Digitized cyclical telemetry is available at a 10Hz update rate, typical. Through the use of the MFR_ADC_CONTROL command, some signals of interest can be digitized more frequently—up to a 125Hz update rate, typical. Availability of newly digitized telemetry data can be made known via the MFR_ADC_TELEMETRY_STATUS command.

Peak observed values of telemetry readback data can be cleared with the MFR_CLEAR_PEAKS I^2C command, provided the WRITE_PROTECT register value permits it. (Executing MFR_CLEAR_PEAKS can be performed regardless of the state of the WP pin.)

Details on the LTM4686B's Fault Log Feature follow:

- Fault logging is enabled when MFR_CONFIG_ALL[7] = 1_b.
- A fault log is present in NVM when STATUS_MFR_SPECIFIC*n*[3]Reports "1_b", which is propagated to the MFR Bit (Bit 12) of the STATUS_WORD register.
- Retrieving fault log data, if present, is performed with the MFR_FAULT_LOG command. 147 bytes of data are retrieved using the PMBus-defined variant to the SMBus block read protocol.
- The fault log contents in NVM, if present, are cleared by executing the MFR_FAULT_LOG_CLEAR command.
- The fault log will not be written if a fault log is already present in NVM.
- The LTM4686B can be forced to write a fault log to its NVM by executing the MFR_FAULT_LOG_STORE command; the LTM4686B will behave as if a channel faulted off. Note the command is NACKed and a CML fault is reported if a fault log is already present at the time of executing MFR_FAULT_LOG_STORE.

OPERATION

When an external stimulus pulls the LTM4686B's $\overline{GPIO}n$ pin(s) logic low, the respective channel ($V_{OUT}n$) either: takes no action on it, i.e., ignores it completely—if MFR_GPIO_RESPONSE*n* = 0x00; or, turns off immediately, i.e., the power stage(s) become high impedance ("inhibited")—if MFR_GPIO_RESPONSE*n* = 0xC0.

The MFR_GPIO_PROPAGATE*n* register contents configure which fault(s) cause the LTM4686B to pull its $\overline{GPIO}n$ pin(s) logic low.

I^2C communications are originated by the user's (system's)I^2C master device. Writes/reads to/from Channel 0 of the LTM4686B (V_{OUT0}: PAGE 0x00), to/from Channel 1 of the LTM4686B (V_{OUT1}: PAGE 0x01), or writes to both Channels 0 and 1 of the LTM4686B (V_{OUT0} and V_{OUT1}: PAGE 0xFF) are possible. The target channel(s) of interest are selected by the I^2C master by executing the PAGE command and sending the appropriate argument (0x00, 0x01, 0xFF) in the payload. The PAGE command is unrestricted, i.e., not affected by the WP pin or WRITE_PROTECT register settings.

The LTM4686B always responds to its global slave addresses, 0x5A and 0x5B. Commands sent to the global address 0x5A act the same as if the PAGE command were set to 0xFF, i.e., received commands are written to both channels simultaneously. Commands sent to the global address 0x5B are applied to the PAGE active at the time of the global address transaction, i.e., allows channel-specific command of all LTM4686B devices on the bus.

I^2C commands not listed above that relate to Fault Status and EEPROM NVM Operations follow. Writing of the following is possible provided the state of the WP (write protect) pin and the WRITE_PROTECT register value permits the I^2C writes:

- Soliciting (reading) module fault status and clearing (writing) module fault status (CLEAR_FAULTS, STATUS_BYTE*n*, STATUS_WORD*n*, STATUS_VOUT*n*, STATUS_IOUT*n*, STATUS_INPUT, STATUS_TEMPERATURE*n*, STATUS_CML [communications, memory, and/or logic], and STATUS_MFR_SPECIFIC*n* [miscellaneous]).
- Storing the LTM4686B's user-writable RAM register data to the EEPROM NVM (STORE_USER_ALL).
- An alternate means to the STORE_USER_ALL command to directly erase and write the LTM4686B's EEPROM contents, protected by unlock keys, to facilitate programming of the LTM4686B EEPROM in environments such as ICT (in-circuit test) and bulk programming by, e.g., embedded hardware or by the LTpowerPlay GUI. Also, a means to directly read the LTM4686B EEPROM contents (MFR_EE_UNLOCK, MFR_EE_ERASE, MFR_EE_DATA).
- Instigating a soft reset of the LTM4686B without power-cycling SV_{IN} power (MFR_RESET). The MFR_RESET command triggers the download of EEPROM NVM data to RAM registers, as if SV_{IN} power had been cycled.
- Forcing a download of EEPROM NVM data to RAM registers (RESTORE_USER_ALL). This is indistinguishable from executing MFR_RESET.

Other data that can be obtained from the LTM4686B via I^2C communications are as follows:

- Soliciting the LTM4686B for its PMBus capabilities, as defined by PMBus (CAPABILITY):
  - PEC (packet error checking). Note, the LTM4686B requires valid PEC in I^2C communications when MFR_CONFIG_ALL[2] = 1_b. The NVM factory-default configuration is MFR_CONFIG_ALL[2] = 0_b, i.e., PEC not required.
  - I^2C communications can be supported at up to 400kHz SCL bus speed. Note, clock low extending (clock stretching) must be enabled on the LTM4686B to ensure robust communications above 100kHz SCL bus speeds, i.e., MFR_CONFIG_ALL[1] = 1_b. The NVM factory-default configuration is MFR_CONFIG_ALL[1] = 0_b, i.e. Clock stretching is disabled.
  - The LTM4686B has an $\overline{SMBALERT}$ ($\overline{ALERT}$) pin and does support the SMBus ARA (alert response address) protocol.
- Soliciting the module for the maximum output voltage it can be commanded to produce (MFR_VOUT_MAX*n*).
- Soliciting the device for the data format of its output voltage-related registers (VOUT_MODE*n*).

OPERATION

- Soliciting the device for the revisions of PMBus specifications that it supports (Part I: Rev. 1.2; Part II: Rev 1.2).
- Soliciting the device for the identification of the manufacturer of the LTM4686B, “LTC” (MFR_ID) and the manufacturer code representing the LTM4686B and revision, 0x477X (MFR_SPECIAL_ID).
- Soliciting the device for its part number, "LTM4686" (MFR_MODEL).*
- Soliciting the module for its serial number (MFR_SERIAL).
- The digital status of the LTM4686B’s I/O pads and validity of the ADC (MFR_PADS) and WP pin status (MFR_COMMON[0]).

The following list indicates other aspects of the LTM4686B relating to power system management and power sequencing that are configurable by I^2C communications—provided the state of the WP (write protect) pin and the WRITE_PROTECT register value permit the I^2C writes—and by EEPROM settings:

- Providing multiple means to read/write data directly to a particular channel of the LTM4686B by assigning additional slave address for channels 0 and 1 (MFR_RAIL_ADDRESS*n*), the benefit of which is that it reduces page command usage and associated I^2C traffic. It also facilitates altering the same register of multiple LTM4686B in unison without invoking the PMBus group command protocol. See also PAGE_PLUS_READ and PAGE_PLUS_WRITE.
- Configuring the output voltage to be on or off by means other than the RUN*n* pin (ON_OFF_CONFIG*n*[3], OPERATION commands).
- Configuring whether the LTM4686B performs a CLEAR_FAULTS command upon itself when either RUN*n* pin toggles from logic low to logic high. (MFR_CONFIG_ALL[0]).
- Configuring whether the LTM4686B pulls RUN*n* logic low when the LTM4686B is commanded off by other means (MFR_CHAN_CONFIG*n*[4]).
- Configuring the response of the LTM4686B when it is commanded to turn on its output prior to the completion of processing TOFF_DELAY*n* and TOFF_FALL*n* power-down sequencing (MFR_CHAN_CONFIG*n*[3]).
- Configuring whether the LTM4686B’s output is disabled when SHARE_CLK is held low (MFR_CHAN_CONFIG*n*[2]).
- Configuring whether the $\overline{\text{ALERT}}$ pin is pulled low when $\overline{\text{GPIO}}$*n* is pulled low by external stimulus (MFR_CHAN_CONFIG*n*[1]).
- Setting the value of the MFR_IIN_OFFSET*n* registers, representing an estimate of the current drawn by the SV_{IN} pin. The SV_{IN} pin current is not measured by the LTM4686B but the MFR_IIN_OFFSET*n* is used in computing and reporting channel and total module input currents (MFR_READ_IIN*n*, READ_IIN).
- Three words (six bytes) of the LTM4686B’s EEPROM that are available for storing user data. (USER_DATA_03*n*, USER_DATA_04).
- Invoking or releasing several levels of I^2C write protection (WRITE_PROTECT).
- Configuring the bus timeout for 255ms (MFR_CONFIG_ALL[3] = 1_b) if the host needs more time to complete I^2C transactions.
- Determining whether the user-editable RAM register values are identical to the contents of the user NVM (MFR_COMPARE_USER_ALL).
- Setting the programmable output voltage range of V_{OUT} to a narrower range (0.5V to 2.75V) in order to achieve a higher resolution of V_{OUT} adjustment than is available by default (MFR_PWM_MODE*n*[1]). MFR_PWM_MODE cannot be changed on the fly; switching action must be off. Note that altering the V_{OUT} range alters the gain of the control loop and may therefore require loop compensation to be adjusted.
- Altering the temperature coefficient of the LTM4686B’s current sensing elements, if needed

* The MFR_MODEL value is “LTM4686 ”. The value consists of 8 ASCII characters and the last character is a blank space punctuation character (“ ”), i.e., ASCII code 0x20 or 32d.

OPERATION

(MFR_IOUT_CAL_GAIN_TC*n*) (uncommon to alter this parameter from its NVM-Factory default setting).

- Altering the gain or offset of the power stage sensors (MFR_TEMP_1_GAIN*n* and MFR_TEMP_1_OFFSET*n*)—or that of the external temperature sensor, when an external temperature sensor is used on the TSNS1a pin. (Uncommon to alter this parameter from its NVM-factory default setting).
- Configuring whether the LTM4686B Pulls SHARE_CLK logic low when SV_{IN} has fallen outside Its UVLO thresholds (MFR_PWM_CONFIG[4]). MFR_PWM_CONFIG cannot be changed on the fly; switching action must be off (uncommon to alter this parameter from its NVM-factory default setting).
- Configuring whether the LTM4686B's output voltage digital servos are active vs disengaged (MFR_PWM_MODE*n*[6]. Uncommon to alter this parameter from its NVM-factory default settings).
- Configuring whether the LTM4686B's current limit range is set to high range vs low range. (MFR_PWM_MODE*n*[7]. Not recommended to alter this parameter from its NVM-factory default settings).

Remaining LTM4686B status that can be queried over I^2C communications follow:

- Access to three "hand-shaking" status bits (MFR_COMMON[6:4]) to ease implementation of PMBus busy protocols, i.e., enabling fast and robust system level communication through polling of these bits to infer LTM4686B's readiness to act on subsequent I^2C writes. (See PMBus communication and command processing, in the Applications Information section.)
- Providing a means to determine whether the LTM4686B NVM download to RAM has occurred ("NVM Initialized," MFR_COMMON[3]).
- Providing a means other than ARA protocol to determine whether the LTM4686B is pulling ALERT low (MFR_COMMON[7]).
- Detecting a SHARE_CLK timeout event (MFR_COMMON[1]).
- Verifying or Altering the Slave Address of the LTM4686B (MFR_ADDRESS).

POWER MODULE OVERVIEW

A dedicated remote-sense amplifier precisely kelvin-senses V_{OUT0}'s load via the differential pin-pair formed by V_{OSNS0}^+ and V_{OSNS0}^-. V_{OUT0} can be commanded to between 0.5VDC and 3.6VDC. V_{OUT1} is sensed via the pin-pair formed by V_{OSNS1} and signal ground of the module's SGND. V_{OUT1} can be commanded to between 0.5VDC and 3.6VDC. Output voltage readback telemetry is available over I^2C (READ_VOUT*n* registers). Peak output voltage readback telemetry is accessible in the MFR_READ_VOUT_PEAK*n* registers. If V_{OSNS0}^- exceeds V_{OSNS0}^+, no phase reversal of the differentially-sensed output voltage feedback signal occurs (Note 12). Similarly, no phase reversal occurs when SGND exceeds V_{OSNS1}(Note 12). For added flexibility, the V_{OSNS0}^+/V_{OSNS0}^- feedback pins can be configured as the control loop feedback path for both V_{OUT0} and V_{OUT1} by setting MFR_PWM_CONFIG[7] = 1_b. (See Figure 35).

The typical application schematic is shown in Figure 62 on the back page of this data sheet.

The LTM4686B can operate from input voltages between 4.5V and 5.75V (see Figure 62). Internal LDOs—3.3V (V_{DD33}), derived from $INTV_{CC}$, and 2.5V (V_{DD25}), derived from V_{DD33}—bias the LTM4686B's digital circuitry. Control IC bias (SV_{IN}) is routed independent of the inputs to the power stages (V_{IN0}, V_{IN1}); this enables step-down DC/DC conversion from less than 4.5V input (see Figure 31), so long as auxiliary power (~ 5V) is available to bias SV_{IN} and $INTV_{CC}$ (the module's control IC) appropriately. (See also Test Circuit 2). Furthermore, the inputs of the two

OPERATION

power stages are not connected together internal to the module; therefore, DC/DC step-down conversion from two different source power supplies can be performed.

Per Note 6 of the Electrical Characteristics section, the output current may require derating for some operating scenarios. Detailed derating guidance is provided in the Applications Information section.

The LTM4686B contains dual integrated constant frequency current mode control buck regulators (Channel 0 and Channel 1) whose built-in power MOSFETs are capable of fast switching speed. The factory NVM-default switching frequency clocks SYNC at 1MHz, to which the regulators synchronize their switching frequency. The default phase-interleaving angle between the channels is 180°. A pin-strapping resistor on $F_{SWPHCFG}$ configures the frequency of the SYNC clock (switching frequency) and the channel phase relationship of the channels to each other and with respect to the falling edge of the SYNC signal. (Not all possible combinations of switching frequency and phase-angle assignments are settable by resistor pin programming; see Table 4. Configure the LTM4686B's NVM to implement settings not available by resistor-pin strapping.) When a $F_{SWPHCFG}$ pin-strap resistor sets the channel phase relationship of the LTM4686B's channels, the SYNC clock is not driven by the module; instead, SYNC becomes strictly a high impedance input and channel switching frequency is then synchronized to SYNC provided by an externally-generated clock or sibling LTM4686B with pull-up resistor to V_{DD33}. Switching frequency and phase relationship can be altered via the I^2C interface, but only when switching action is off, i.e., when the module is not regulating either output. See the Applications Information section for details.

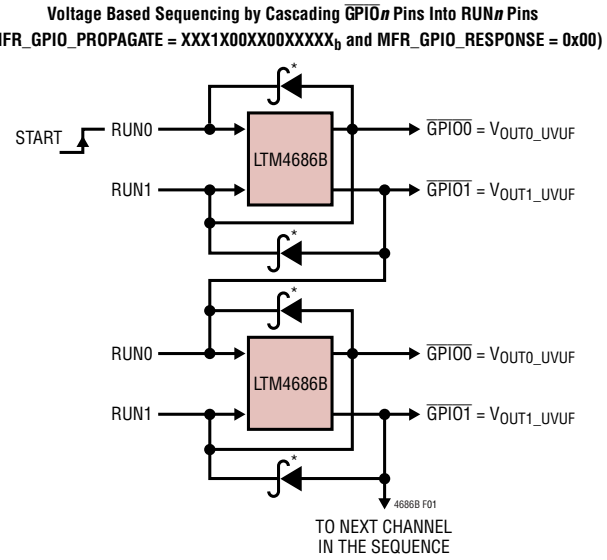
Internal feedback loop compensation for Regulator 0 is available by connecting COMP0a to COMP0b. (For Regulator 1, the connection is from COMP1a to COMP1b.) With current mode control and internal feedback loop compensation, the LTM4686B module has sufficient stability margins and good transient performance with a wide range of output capacitors—even all-ceramic MLCCs. Table 20 provides guidance on input and output capacitors recommended for many common operating conditions.

The Analog Devices, Inc. µModule Power Design Tool is available for transient and stability analysis. Furthermore, expert users who prefer to not make use of the module's internal feedback loop compensation—but instead, tailor the feedback loop compensation specifically for his/her application—may do so by not connecting COMP*n*a to COMP*n*b: the personalized loop compensation network can be applied externally, i.e., from COMP*n*a to SGND, and leaving COMP*n*b open circuit.

The LTM4686B has two general purpose input/output pins, named $\overline{\text{GPIO0}}$ and $\overline{\text{GPIO1}}$. The behavior of these pins is configurable via registers MFR_GPIO_PROPAGATE*n* and MFR_GPIO_RESPONSE*n*. The $\overline{\text{GPIO}}n$ pins are high impedance during NVM-download-to-RAM initialization. These pins are intended to perform one of two primary functions, or a hybrid of the two: behave as open-drain, active low fault/warning indicators; and/or, behave as auxiliary RUN pins for their respective channels. In the former case, the pins can be configured as interrupt pins, pulling active low when output under/overvoltage, input under/overvoltage, input/output overcurrent, overtemperature, and/or communication, memory or logic (CML) fault or warning events are detected by the LTM4686B. In the latter case, the $\overline{\text{GPIO}}n$ pins can be bussed to paralleled siblings (paralleled LTM4686B channels and/or modules), for purposes of coordinating orderly power-up and power-down, i.e., in unison. The LTM4686B DC/DC regulator does not feature a traditional "power good" (PGOOD) indicator pin to indicate when the output voltage is within a few percent of the target regulation point. However, the $\overline{\text{GPIO}}n$ pin can be configured as a PGOOD indicator—and this is, in fact, its factory-default NVM setting. Suitable for event-based sequencing of downstream rails, $\overline{\text{GPIO}}n$ is configured as the unfiltered output of the VOUT_UV_FAULT_LIMIT*n* comparator, with Bit 12 of MFR_GPIO_PROPAGATE*n* = "1_b"; Bits 9 and 10 of MFR_GPIO_PROPAGATE*n* are not set, since the propagation of power good in those latter instances is subject to supervisor filtering and comparator latency. If it is necessary to have the desired PGOOD polarity appear on the $\overline{\text{GPIO}}n$ pin immediately upon SV_{IN} power-up—given that the pin will initially be high impedance, until NVM contents have downloaded to RAM—a pull-down Schottky diode is needed between the RUN*n*

OPERATION

pin of the LTM4686B and the respective $\overline{\text{GPIO}}n$ pin. (See Figure 1). If the $\overline{\text{GPIO}}n$ pin is configured as a PGOOD indicator, the MFR_GPIO_RESPONSE*n* must be set to "ignore" (factory-default 0x00), or else the LTM4686B cannot start up due to the latch-off conditions imposed.



NOTE: RESISTOR OR RC PULL-UPS ON RUN*n* AND $\overline{\text{GPIO}}n$ PINS NOT SHOWN
*OPTIONAL SIGNAL SCHOTTKY DIODE. ONLY NEEDED WHEN ACCURATE PGOOD (POWER GOOD) INDICATION IS REQURED BY THE SYSTEM/USER IMMEDIATELY AT SV_{IN} POWER UP

Figure 1. Event (Voltage) Based Sequencing

The RUN*n* pin is a bidirectional open-drain pin. This means it should never be driven logic high from a low impedance source. Instead, simply provide a 10k pull-up resistor from the RUN*n* pins to V_{DD33}. The LTM4686B pulls its RUN*n* pin logic low during NVM-download-to-RAM initialization, when SV_{IN} is below the commanded undervoltage lockout voltage (VIN_ON, rising and VIN_OFF, falling), and subsequent to external stimulus pulling RUN low—for a minimum time dictated by MFR_RESTART_DELAY*n*. Bussing the respective RUN*n* and $\overline{\text{GPIO}}n$ pins to sibling LTM4686B modules enables coordinated power-up/power-down to be well orchestrated, i.e., performing turn-on and turn-off in a unified fashion.

When RUN*n* exceeds 1.35V, the LTM4686B initially idles for a time dictated by the TON_DELAY*n* register. After the TON_DELAY*n* time expires, the module begins ramping up the respective control loop's internal reference, starting from 0V. In the absence of a prebiased $V_{OUT}n$ condition, the output voltage is ramped linearly from 0V to the commanded target voltage, with a ramp-up time dictated by the TON_RISE*n* register. In the presence of a prebiased $V_{OUT}n$ condition, the output voltage is brought into regulation in the same manner as aforementioned, with the exception that inductor current is prevented from going negative (the module's controller is operated in discontinuous mode operation during start-up). In both cases, the output voltage reaches regulation in a consistent time, as measured with respect to RUN*n* toggling high. See start-up oscilloscope shots in the Typical Performance Characteristics section.

Pulling the RUN*n* pin below 0.8V turns off the DC/DC converter, i.e., forces the respective regulator into a shutdown state. Factory NVM-default settings configure the LTM4686B to turn off its power stage MOSFETs immediately, thereby becoming high impedance. The output voltage then decays according to whatever output capacitance and load impedance is present. Alternatively, NVM/register settings can configure the LTM4686B to actively discharge $V_{OUT}n$ when RUN*n* is pulled logic low, according to prescribed TOFF_DELAY*n* delay and TOFF_FALL*n* ramp-down times. See the Applications Information section for details. The LTM4686B does not feature an explicit, analog TRACK pin. Rail-to-rail tracking and sequencing is handled digitally, as explained previously.

Bussing the open-drain SHARE_CLK pins of all LTM4686Bs (and providing a pull-up resistor to V_{DD33}) provides a means for all LTM4686Bs in the system to synchronize their time-base (or "heartbeat") to the fastest SHARE_CLK clock. Sharing the heartbeat amongst all LTM4686B ensures that all rails are sequenced according to expectations; it negates timing errors that could otherwise materialize due to SHARE_CLK (time-base) tolerance and part-to-part variation.

Current sense information is derived from across the power inductors internal to the LTM4686B and made available to the internal control IC's current control loops and ADC sensors. Output current readback telemetry is available over I^2C (READ_IOUT*n* registers). Peak output current readback telemetry is available in the MFR_READ_IOUT_PEAK*n* registers.

OPERATION

Output power readback is computed by the LTM4686B according to:

READ_POUT*n* = READ_VOUT*n* • READ_IOUT*n*

Alternating excitation currents of 2µA and 30µA are sourced from the TSNS1a pin. Connecting TSNS1a to TSNS1b, temperature sensing of the Channel 1 power stage is realized by the LTM4686B digitizing the voltages that appear at the PNP transistor temperature sensor that resides at the TSNS1b pin. Analogous activity occurs on the TSNS0 node, from which Channel 0 power stage temperature is derived. The LTM4686B performs what is known in the industry as delta VBE (ΔVBE) computations and makes channel (power stage) temperature telemetry available over I^{2}C (READ_TEMPERATURE_1$_n$). The junction temperature of the control IC within the LTM4686B is also available over I^{2}C (READ_TEMPERATURE_2). Observed peak Channel temperatures can be read back in registers READ_MFR_TEMPERATURE_1_PEAK*n*. Observed peak temperature of the control IC can be read back in register MFR_READ_TEMPERATURE_2_PEAK.

For a fixed load current, the amplitude of the current sense information changes over temperature due to the temperature coefficient of copper (inductor DCR), which is approximately 3900ppm/°C. This would introduce significant current readback error over the operating range of the module if not for the fact that the LTM4686B's temperature readback information is used in conjunction with the perceived current sense signal to yield temperature-corrected current readback data.

If desired, it is possible to use only the temperature readback information derived by the TSNS0 pin to yield temperature-corrected current readback data for both Channels 0 and 1. This frees up the Channel 1 temperature sensor to monitor a temperature sensor external to the LTM4686B. This is achieved by setting MFR_PWM_MODE0[4] = 1_b (the NVM-factory default value is 0_b). This degrades the current readback accuracy of Channel 1—more so when Channel 0 and Channel 1 are not paralleled outputs. However, the TSNS1a pin becomes available to be connected to an external diode-connected small-signal PNP transistor (such as 2N3906) and 10nF X7R capacitor, i.e., an external temperature sensor, whose temperature readback data and peak value are available over I^{2}C (READ_TEMPERATURE_1_1, MFR_READ_TEMPERATURE_1_PEAK1). Implementation of the aforementioned is as follows: (1) local to the LTM4686B, electrically connect a 10nF X7R capacitor directly from TSNS1a to SGND; (2) differentially route a pair of traces from the LTM4686B's TSNS1a and SGND pins to the target PNP transistor; (3) electrically connect the emitter of the PNP transistor to TSNS1a; (4) electrically connect the collector and base of the PNP transistor to SGND.

Power stage duty cycle readback telemetry is available over I^{2}C (READ_DUTY_CYCLE*n* registers). Computed channel input current readback is computed by the LTM4686B as:

MFR_READ_IIN*n* = READ_DUTY_CYCLE*n* • READ_IOUT*n* + MFR_IIN_OFFSET*n*

Computed module input current readback is computed by the LTM4686B as:

READ_IIN = MFR_READ_IIN$_0$ + MFR_READ_IIN1

where MFR_IIN_OFFSET*n* is a register value representing the SV_{IN} input bias current. The SV_{IN} current is not digitized by the module. The factory NVM-default value of MFR_IIN_OFFSET*n* is 48.16mA, representing the contribution of current drawn by each of the module's channels on the SV_{IN} pin, when the power stages are operating in forced continuous mode at the factory-default switching frequency of 1MHz. See Table 8 in the Applications Information section for recommended MFR_IIN_OFFSET*n* setting vs Switching Frequency. The aforementioned method by which input current is calculated yields an accurate current readback value even at light load currents, but only as long as the module is configured for forced continuous operation (NVM-factory default). SV_{IN} and peak SV_{IN} readback telemetry is accessible via I^{2}C in the READ_VIN and MFR_VIN_PEAK registers, respectively.

The power stage switch nodes are brought out on the SW*n* pin for functional operation monitoring and for optional installation of a resistor-capacitor snubber circuit (terminated to GND) for reduced EMI.

The LTM4686B features a write protect (WP) pin. If WP is open circuit or logic high, I^{2}C writes are severely restricted:

OPERATION

only I^2C writes to the PAGE, OPERATION, CLEAR_FAULTS, MFR_CLEAR_PEAKS, and MFR_EE_UNLOCK commands are supported, with the exception that individual fault bits can be cleared by writing a "1_b" to the respective bits in the STATUS_* registers. Register reads are never restricted. Not to be confused with the WP pin, the LTM4686B features a WRITE_PROTECT register, which is also used to restrict I^2C writes to register contents. Refer to Appendix C: PMBus Command Details for details. The WP pin and the WRITE_PROTECT register provide a level of protection against accidental changes to RAM and EEPROM contents.

The LTM4686B supports all possible 7-bit slave addresses. The factory NVM-default slave address is 0x4F. The lower four bits of the LTM4686B's slave address can be altered from this default value by connecting a resistor from the ASEL pin to SGND. See Table 5 in the Applications Information section for details. Bits[6:4] can be altered by writing to the SLAVE_ADDRESS command. The value of the SLAVE_ADDRESS command can be stored to NVM, however, the lower four bits of the SLAVE_ADDRESS is always dictated by the ASEL resistor pin-strap setting.

Up to four LTM4686B modules (8 channels) can be paralleled, suitable for powering ~108A loads such as CPUs and GPUs. (See Figure 32) The LTM4686B can be paralleled with LTM4650 and other modules, as well (see Figure 33 and Figure 34).

EEPROM

The LTM4686B's control IC contains an internal EEPROM (nonvolatile memory, NVM) with Error Correction Coding (ECC) to store configuration settings and fault log information. EEPROM endurance retention and mass write operation time are specified in the Electrical Characteristics and Absolute Maximum Ratings sections. Write operations at $T_J < 0°C$ or at $T_J > 85°C$ are possible although the Electrical Characteristics are not guaranteed and the EEPROM retention characteristics may be degraded. Read operations performed at junction temperatures between –40°C and 125°C do not degrade the EEPROM. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log-specific EEPROM locations (partitions). If occasional writes to these registers occur above 85°C junction, the slight degradation in the data retention characteristics of the fault log does not undermine the usefulness of the function.

It is recommended that the EEPROM not be written when the control IC die temperature is greater than 85°C. If the die temperature exceeds 130°C, the LTM4686B's control IC disables all EEPROM write operations. EEPROM write operations are subsequently re-enabled when the die temperature drops below 125°C.

The degradation in EEPROM retention for temperatures >125°C can be approximated by calculating the dimensionless acceleration factor using Equation 1.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]} \quad (1)$$

where:

AF = acceleration factor

Ea = activation energy = 1.4eV

$k = 8.617 \bullet 10^{-5}$ eV/°K

T_{USE} = 125°C specified junction temperature

T_{STRESS} = actual junction temperature in °C

Example: Calculate the effect on retention when operating at a junction temperature of 130°C for 10 hours.

T_{STRESS} = 130°C

T_{USE} = 125°C

$AF = e^{[(1.4/8.617 \bullet 10^{-5}) \bullet (1/398 - 1/403)]} = 1.66$

The equivalent operating time at 125°C = 16.6 hours.

Thus the overall retention of the EEPROM was degraded by 6.6 hours as a result of operating at a junction temperature of 130°C for 10 hours. The effect of the overstress is negligible when compared to the overall EEPROM retention rating of 87,600 hours at a maximum junction temperature of 125°C.

OPERATION

The integrity of the EEPROM is checked with a CRC calculation each time its data is read, such as after a power-on reset or execution of a RESTORE_USER_ALL or MFR_RESET command. If CRC error occurs, the MFR bit is set in the STATUS_BYTE and STATUS_WORD commands. The NVM CRC error bit in the STATUS_MFR_SPECIFIC command is set and the $\overline{\text{ALERT}}$ and RUN pins are pulled low disabling the output as a safety measure. The device will only respond at special address 0x7C or global addresses 0x5A and 0x5B.

Internal EEPROM with CRC Protection and ECC

The LTM4686B contains internal EEPROM with Error Correction Coding (ECC) to store user configuration settings and fault log information. EEPROM endurance and retention for user space and fault log pages are specified in the Absolute Maximum Ratings and Electrical Characteristics table.

The integrity of the EEPROM memory is checked with a CRC calculation each time its data is to be read, such as after a power-on reset. A CRC error will prevent the controller from leaving the OFF state. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the $\overline{\text{ALERT}}$ and RUN pins will be pulled low. At that point the device will respond at special address 0x7C, which is only activated after an invalid CRC has been detected. The module will also respond to global addresses 0x5A and 0x5B, but all ADI PSM modules and ICs will respond to these addresses so users must be careful when using global addresses. EEPROM repair can be attempted by writing the desired configuration to the controller and executing a STORE_USER_ALL command followed by a CLEAR_FAULTS command. Contact the factory if EEPROM repair is unsuccessful.

See the Applications Information section and Analog Devices Application Note 145, or contact the factory for details on efficient in-system EEPROM programming, including bulk EEPROM programming, which the LTM4686B also supports.

SERIAL INTERFACE

The LTM4686B serial interface is a PMBus compliant slave device and can operate at any frequency between 10kHz and 400kHz. The address is configurable using either the EEPROM or an external resistor. In addition the LTM4686B always responds to the global broadcast address of 0x5A (7 bit) or 0x5B (7 bit). Address 0x5A is not paged and is performed on both channels. 0x5B respects the page command. Because address 0x5A does not support page, it can not be used for any paged reading commands.

The serial interface supports the following protocols defined in the PMBus specifications: 1) send command, 2) write byte, 3) write word, 4) group, 5) read byte, 6) read word and 7) read block 8) PAGE_PLUS_READ, 9) PAGE_PLUS_WRITE 10) SMBALERT_MASK read, 11) SMBALERT_MASK write. All read operations will return a valid PEC if the PMBus master requests it. If the PEC_REQUIRED bit is set in the MFR_CONFIG_ALL command, the PMBus write operations will not be acted upon until a valid PEC has been received by the LTM4686B.

Communication Protection

PEC write errors (if PEC_REQUIRED is active), attempts to access unsupported commands, or writing invalid data to supported commands will result in a CML fault. The CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_CML command, and the $\overline{\text{ALERT}}$ pin is pulled low.

DEVICE ADDRESSING

The LTM4686B offers four different types of addressing over the PMBus interface, specifically: 1) global, 2) device, 3) rail addressing and 4) alert response address (ARA).

Global addressing provides a means of the PMBus master to address all LTM4686B devices on the bus. The LTM4686B global address is fixed 0x5A (7 bit) or 0xB4 (8 bit) and cannot be disabled. Commands sent to the global address act the same as if PAGE is set to a value of 0xFF. Commands sent are written to both channels simultaneously. Global command 0x5B (7 bit) or 0xB6 (8 bit) is paged and allows channel specific command of all LTM4686B devices on the bus. Other ADI device types may respond at one or both of these global addresses; therefore do not read from global addresses.

OPERATION

Rail addressing provides a means for the bus master to simultaneously communicate with all channels connected together to produce a single output voltage (PolyPhase®). While similar to global addressing, the rail address can be dynamically assigned with the paged MFR_RAIL_ADDRESS command, allowing for any logical grouping of channels that might be required for reliable system control. Do not read from rail addresses because multiple ADI devices may respond.

Device addressing provides the standard means of the PMBus master communicating with a single instance of an LTM4686B. The value of the device address is set by a combination of the ASEL configuration pin and the MFR_ADDRESS command. When this addressing means is used, the PAGE command determines the channel being acted upon. Device addressing can be disabled by writing a value of 0x80 to the MFR_ADDRESS.

All four means of PMBus addressing require the user to employ disciplined planning to avoid addressing conflicts. Communication to LTM4686B devices at global and rail addresses should be limited to command write operations.

FAULT DETECTION AND HANDLING

A variety of fault and warning reporting and handling mechanisms are available. Fault and warning detection capabilities include:

- Input OV/FAULT Protection and UV Warning
- Average Input OC Warn
- Output OV/UV Fault and Warn Protection
- Output OC Fault and Warn Protection
- Internal and External Overtemperature Fault and Warn Protection
- External Undertemperature Fault Protection
- CML Fault (Communication, Memory or Logic)
- External Fault Detection via the Bidirectional $\overline{\text{GPIO}}n$ Pins.

In addition, the LTM4686B can map any combination of fault indicators to their respective $\overline{\text{GPIO}}n$ pin using the propagate $\overline{\text{GPIO}}n$ response commands, MFR_GPIO_PROPAGATE*n*. Typical usage of a $\overline{\text{GPIO}}$ pin is as a driver for an external crowbar device, overtemperature alert, overvoltage alert or as an interrupt to cause a microcontroller to poll the fault commands. Alternatively, the $\overline{\text{GPIO}}n$ pins can be used as inputs to detect external faults downstream of the controller that require an immediate response. The $\overline{\text{GPIO0}}$ and/or $\overline{\text{GPIO1}}$ pins can also be configured as power good outputs. Power good indicates the controller output is within the OV/UV fault thresholds. At power-up the pin will initially be three-state. If it is necessary to have the desired polarity on the pin at power-up in this configuration, attach a Schottky diode between the RUN pin of the propagated power good signal and the $\overline{\text{GPIO}}$ pin. The Cathode must be attached to RUN and the Anode to the $\overline{\text{GPIO}}$ pin (see Figure 1). If the $\overline{\text{GPIO}}$ pin is set to a power good status, the MFR_GPIO_RESPONSE must be ignore otherwise a latched off condition exists.

As described in the Soft-Start section, it is possible to control start-up through concatenated events. If $\overline{\text{GPIO}}n$ is used to drive the RUN pin of another controller, the unfiltered VOUT_UV fault limit should be mapped to the $\overline{\text{GPIO}}n$ pin.

Any fault or warning event will cause the $\overline{\text{ALERT}}$ pin to assert low unless the $\overline{\text{ALERT}}$ is masked by the SMBALERT_MASK command. The pin will remain asserted low until the CLEAR_FAULTS command is issued, the fault bit is written to a 1, the PMBus master successfully reads the device ARA register, bias power is cycled or a MFR_RESET or RESTORE_USER_ALL command is issued. Channel specific faults are cleared if the RUN pins are toggled OFF/ON or the part is commanded OFF/ON via PMBus. If bit 0 of MFR_CONFIG_ALL is set to a 1, toggling the RUN pins OFF/ON or commanding the part OFF/ON via PMBus clears all faults. The MFR_GPIO_PROPAGATE*n* command determines if the $\overline{\text{GPIO}}$ pins are pulled low when a fault is detected; however, the $\overline{\text{ALERT}}$ pin is always pulled low if a fault or warning is detected and the status bits are updated unless the $\overline{\text{ALERT}}$ pin is masked using the SMBALERT_MASK command.

Output and input fault event handling is controlled by the corresponding fault response byte as specified in Table 24 to Table 28. Shutdown recovery from these types of faults can either be autonomous or latched. For autonomous recovery, the faults are not latched, so if the fault condition is not present after the retry interval has elapsed, a new soft-start is attempted. If the fault persists, the controller

OPERATION

will continue to retry. The retry interval is specified by the MFR_RETRY_DELAY command and prevents damage to the regulator components by repetitive power cycling. The MFR_RETRY_DELAY must be greater than 120ms. It can not exceed 83.88 seconds.

Channel-to-channel fault dependencies can be created by connecting $\overline{\text{GPIO}}n$ pins together. In the event of an internal fault, one or more of the channels is configured to pull the bussed $\overline{\text{GPIO}}n$ pins low. The other channels are then configured to shut down when the $\overline{\text{GPIO}}n$ pins are pulled low. For autonomous group retry, the faulted channel is configured to release the $\overline{\text{GPIO}}n$ pin(s) after a retry interval, assuming the original fault has cleared. All the channels in the group then begin a soft-start sequence. If the fault response is LATCH_OFF, the $\overline{\text{GPIO}}n$ pin remains asserted low until either the RUN pin is toggled OFF/ON or the part is commanded OFF/ON. The toggling of the RUN either by the pin or OFF/ON command will clear faults associated with the channel. If it is desired to have all faults cleared when either RUN pin is toggled, set bit 0 of MFR_CONFIG_ALL to a 1.

The status of all faults and warnings is summarized in the STATUS_WORD and STATUS_BYTE commands.

RESPONSES TO V_{OUT} AND I_{OUT} FAULTS

V_{OUT} OV and UV conditions are monitored by comparators. The OV and UV limits are set in three ways.

- As a Percentage of the V_{OUT} if Using the Resistor Configuration Pins
- In EEPROM if Either Programmed at the Factory or Through the GUI
- By PMBus Command

The I_{IN} and I_{OUT} overcurrent monitors are performed by ADC readings and calculations. Thus these values are based on average currents and can have a nominal time latency of up to 90ms. The I_{OUT} calculation accounts for the power inductor DCR and the temperature coefficient of the inductor's copper winding. The input current is equal to the sum of output current times the respective channel duty cycle plus the input offset current for each channel. If this calculated input current exceeds the IIN_OC_WARN_LIMIT the $\overline{\text{ALERT}}$ pin is pulled low and the IIN_OC_WARN bit is asserted in the STATUS_INPUT register.

The LTM4686B provides the ability to ignore the fault, shut down and latch off or shut down and retry indefinitely (hiccup). The retry interval is set in MFR_RETRY_DELAY*n* and can be from 120ms to 83.88 seconds in 1ms increments. The shutdown for OV/UV and OC can be done immediately or after a user selectable deglitch time.

Output Overvoltage Fault Response

A programmable overvoltage comparator (OV) guards against transient overshoots as well as long-term overvoltages at the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared *regardless of the PMBus VOUT_OV_FAULT_RESPONSEn command byte value.* This hardware level fault response delay is typically 2µs from the overvoltage condition to BG asserted high. Using the VOUT_OV_FAULT_RESPONSE*n* command, the user can select any of the following behaviors:

- OV Pull-Down Only (OV cannot be ignored)
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely using the Time Interval Specified in MFR_RETRY_DELAY*n*

Either the Latch Off or Retry fault responses can be deglitched in increments of (0 to 7) • 10µs. See Table 24.

Output Undervoltage Response

The response to an undervoltage comparator output can be either:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely using the Time Interval Specified in MFR_RETRY_DELAY*n*

Either the Latch Off or Retry fault responses can be deglitched in increments of (0 to 7) • 10µs. See Table 25.

OPERATION

Peak Output Overcurrent Fault Response

Due to the current mode control algorithm, peak inductor current is always limited on a cycle by cycle basis. The value of the peak current limit is specified in the Electrical Characteristics table. The current limit circuit operates by limiting the COMP*n*a maximum voltage. DCR sensing is used so the COMP*n*a maximum voltage has a temperature dependency directly proportional to the TC of the DCR of the inductor. The LTM4686B automatically monitors the power stage temperature sensors and modifies the maximum allowed COMP*n*a to compensate for this term.

The overcurrent fault processing circuitry can execute the following behaviors:

- Current Limit Indefinitely
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely using the Time Interval Specified in MFR_RETRY_DELAY*n*

The overcurrent responses can be deglitched in increments of (0 to 7) • 16ms. See Table 26.

RESPONSES TO TIMING FAULTS

TON_MAX_FAULT_LIMIT*n* is the time allowed for V_{OUT} to rise and settle at start-up. The TON_MAX_FAULT_LIMIT*n* condition is predicated upon detection of the VOUT_UV_FAULT_LIMIT*n* as the output is undergoing a SOFT_START sequence. The TON_MAX_FAULT_LIMIT*n* time is started after TON_DELAY*n* has been reached and a SOFT_START sequence is started. The resolution of the TON_MAX_FAULT_LIMIT*n* is 10µs. If the VOUT_UV_FAULT_LIMIT*n* is not reached within the TON_MAX_FAULT_LIMIT*n* time, the response of this fault is determined by the value of the TON_MAX_FAULT_RESPONSE*n* command value. This response may be one of the following:

- Ignore
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely using the Time Interval Specified in MFR_RETRY_DELAY*n*

This fault response is not deglitched. A value of 0 in TON_MAX_FAULT_LIMIT*n* means the fault is ignored. The TON_MAX_FAULT_LIMIT*n* should be set longer than the TON_RISE*n* time. It is recommended TON_MAX_FAULT_LIMIT*n* always be set to a non-zero value, otherwise the output may never come up and no flag will be set to the user.

See Table 28.

RESPONSES TO SV_{IN} OV FAULTS

SV_{IN} overvoltage is measured with the ADC; therefore, the response is naturally deglitched by up to the 90ms typical response time of the ADC. The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely using the Time Interval Specified in MFR_RETRY_DELAY*n*

See Table 28.

RESPONSES TO OT/UT FAULTS

Internal Overtemperature Fault/Warn Response

An internal temperature sensor protects against EEPROM damage. Above 85°C, no writes to EEPROM are recommended. Above 130°C, the internal over temperature warn threshold is exceeded and the part disables EEPROM writes and does not re-enable until the temperature has dropped to 125°C. When the die temperature exceed 160°C the internal over temperature fault response is enabled and the PWM is disabled until the die temperature drops below 150°C. Temperature is measured by the ADC. Internal temperature faults cannot be ignored. Internal temperature limits cannot be adjusted by the user.

See Table 27.

External Overtemperature and Undertemperature Fault Response

Two temperature sensors within the LTM4686B are used to sense power stage temperature. The OT_FAULT_RESPONSE*n* and UT_FAULT_RESPONSE*n* commands

OPERATION

are used to determine the appropriate response to an overtemperature and undertemperature condition, respectively.

The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely using the Time Interval Specified in MFR_RETRY_DELAY*n*

See Table 28.

RESPONSES TO EXTERNAL FAULTS

When either $\overline{\text{GPIO}}n$ pin is pulled low, the OTHER bit is set in the STATUS_WORD command, the appropriate bit is set in the STATUS_MFR_SPECIFC command, and the $\overline{\text{ALERT}}$ pin is pulled low. Responses are not deglitched. Each channel can be configured to ignore or shut down then retry in response to its $\overline{\text{GPIO}}n$ pin going low by modifying the MFR_GPIO_RESPONSE*n* command. To avoid the $\overline{\text{ALERT}}$ pin asserting low when $\overline{\text{GPIO}}n$ is pulled low, assert bit 1 of MFR_CHAN_CONFIG*n*, or mask the $\overline{\text{ALERT}}$ using the SMBALERT_MASK command.

FAULT LOGGING

The LTM4686B has fault logging capability. Data is logged into memory in the order shown in Table 30. The data to be stored in the fault log is being continuously stored in internal volatile memory. When a fault event occurs, the recording into internal volatile memory is halted, the fault log information is available from the MFR_FAULT_LOG command, and the contents of the internal memory are copied into EEPROM. Fault logging is allowed at temperatures above 85°C; however, retention of 10 years is not guaranteed. When the die temperature exceeds 130°C the fault logging is delayed until the die temperature drops below 125°C. After the fault condition that created the fault log event has been removed, clear the fault before the fault log data is erased, or else the part will immediately issue another fault log.

When the LTM4686B powers-up, it checks the EEPROM for a valid fault log. If a valid fault log exists in EEPROM, the "Valid Fault Log" bit in the STATUS_MFR_SPECIFIC command will be set and an $\overline{\text{ALERT}}$ event will be generated. Also, fault logging will be blocked until the LTM4686B has received a MFR_FAULT_LOG_CLEAR command before fault logging will be re-enabled.

The information is stored in EEPROM in the event of any fault that disables the controller on either channel. An external $\overline{\text{GPIO}}n$ pulling low will not trigger a fault logging event.

BUS TIMEOUT PROTECTION

The LTM4686B implements a timeout feature to avoid hanging the serial interface. The data packet timer begins at the first START event before the device address write byte. Data packet information must be completed within 25ms or the LTM4686B will three-state the bus and ignore the given data packet. If more time is required, assert bit 3 of MFR_CONFIG_ALL to allow typical bus timeouts of 255ms. Data packet information includes the device address byte write, command byte, repeat start event (if a read operation), device address byte read (if a read operation), all data bytes and the PEC byte if applicable.

The LTM4686B allows longer PMBus timeouts for block read data packets. This timeout is proportional to the length of the block read. The additional block read timeout applies primarily to the MFR_FAULT_LOG command. In no circumstances will the timeout period be less than the $t_{TIMEOUT\_SMB}$ specification of 32ms (typical).

The user is encouraged to use as high a clock rate as possible to maintain efficient data packet transfer between all devices sharing the serial bus interface. The LTM4686B supports the full PMBus frequency range from 10kHz to 400kHz.

PMBus COMMAND SUMMARY

PMBUS COMMANDS

Table 1 lists supported PMBus commands and manufacturer specific commands. A complete description of these commands can be found in the “PMBus Power System Management Protocol Specification – Part II – Revision 1.2." Users are encouraged to reference this specification. Exceptions or manufacturer specific implementations are listed in Table 1.

All commands from 0xD0 through 0xFF not listed in this table are implicitly reserved by the manufacturer. Users should avoid blind writes within this range of commands to avoid undesired operation of the part. All commands from 0x00 through 0xCF not listed in this table are implicitly not supported by the manufacturer. Attempting to access non-supported or reserved commands may result in a CML command fault event. All output voltage settings and measurements are based on the VOUT_MODE setting of 0x14. This translates to an exponent of 2–12.

If PMBus commands are received faster than they are being processed, the part may become too busy to handle new commands. In these circumstances the part follows the protocols defined in the PMBus Specification v1.2, Part II, Section 10.8.7, to communicate that it is busy.

The part includes handshaking features to eliminate busy errors and simplify error handling software while ensuring robust communication and system behavior. Please refer to the PMBus Communication and Command Processing subsection in the Applications Information section for details.

Table 1. Summary of Supported Commands

PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTM4686B NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	PAGE
PAGE	0x00	Channel or page currently targeted for paged communications.	0x00, read/write, non-paged, not stored in NVM.	82
OPERATION*n*	0x01	Operating mode control. On/off, margin high and margin low.	0x80, read/write, paged, stored in user-editable NVM.	86
ON_OFF_CONFIG*n*	0x02	RUN*n* pin and On/Off Configuration.	0x1F, read/write, paged, stored in user-editable NVM.	85
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Default value not applicable, send byte only, non-paged, not stored in NVM.	109
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	Default value not applicable, write-only, non-paged, not stored in NVM.	82
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Default value not applicable, read/write, non-paged, not stored in NVM.	83
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	0x00, read/write, non-paged, stored in user-editable NVM.	83
STORE_USER_ALL	0x15	Store user operating memory to EEPROM (user-editable NVM).	Default value not applicable, send byte only, non-paged, not stored in NVM.	120
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Default value not applicable, send byte only, non-paged, not stored in NVM. Identical to MFR_RESET command (0xFD).	121
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	0xB0, read-only, non-paged, not stored in NVM.	108
SMBALERT_MASK*n*	0x1B	Mask $\overline{\text{ALERT}}$ activity.	Default mask values: STATUS_VOUT*n* = 0x00, STATUS_IOUT*n* = 0x00, STATUS_INPUT = 0x00, STATUS_TEMPERATURE*n* = 0x00, STATUS_CML = 0x00, STATUS_MFR_SPECIFIC*n* = 0x11. Read/write, paged as indicated, 10 bytes total, stored in NVM	110
VOUT_MODE*n*	0x20	Output voltage format/exponent.	0x14 (2^{-12}), read-only, paged, not stored in NVM.	90
VOUT_COMMAND*n*	0x21	Nominal output voltage set point.	0x1000 (1.000V), read/write, paged, stored in user-editable NVM.	91

PMBus COMMAND SUMMARY

Table 1. Summary of Supported Commands

PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTM4686B NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	PAGE
VOUT_MAX*n*	0x24	The upper limit on the commandable output voltage.	0x3A14 (3.630V), read/write, paged, stored in user-editable NVM.	90
VOUT_MARGIN_HIGH*n*	0x25	Margin high output voltage set point. Must be greater than VOUT_COMMAND*n*.	0x10CD (1.050V), read/write, paged, stored in user-editable NVM.	91
VOUT_MARGIN_LOW*n*	0x26	Margin low output voltage set point. Must be less than VOUT_COMMAND*n*.	0x0F33 (0.95V), read/write, paged, stored in user-editable NVM.	91
VOUT_TRANSITION_RATE*n*	0x27	The rate at which the output voltage changes when $V_{OUT}n$ is commanded to a new value via I^2C.	0x08B33 (25mV/ms), read/write, paged, stored in user-editable NVM.	97
FREQUENCY_SWITCH	0x33	The switching frequency setting.	0x03E8 (1MHz), read/write, non-paged, stored in user-editable NVM.	88
VIN_ON	0x35	The undervoltage lockout (UVLO)–rising threshold.	0xCA20 (4.250V) Voltage as monitored on the "SV_{IN}" pin, read/write, non-paged, stored in user-editable NVM.	89
VIN_OFF	0x36	The undervoltage lockout (UVLO)–falling threshold.	0xCA00 (4.000V) Voltage as monitored on the "SV_{IN}" pin, read/write, non-paged, stored in user-editable NVM.	89
IOUT_CAL_GAIN*n*	0x38	The ratio of the voltage at the control IC's current-sense pins to the sensed current, in mΩ, at 25°C.	Trimmed at ATE, read/write, paged, stored in factory-only NVM. Writes to this register not recommended.	93
VOUT_OV_FAULT_LIMIT*n*	0x40	Output overvoltage fault limit.	0x119A (1.100V), read/write, paged, stored in user-editable NVM.	90
VOUT_OV_FAULT_RESPONSE*n*	0x41	Action to be taken by the device when an output overvoltage fault is detected.	0x80 (immediate off; no retry), read/write, paged, stored in user-editable NVM.	100
VOUT_OV_WARN_LIMIT*n*	0x42	Output overvoltage warning threshold.	0x1133 (1.075V), read/write, paged, stored in user-editable NVM.	91
VOUT_UV_WARN_LIMIT*n*	0x43	Output undervoltage warning threshold.	0x0ECD (0.925V), read/write, paged, stored in user-editable NVM.	92
VOUT_UV_FAULT_LIMIT*n*	0x44	Output undervoltage fault limit.	0x0E66 (0.900V), read/write, paged, stored in user-editable NVM.	92
VOUT_UV_FAULT_RESPONSE*n*	0x45	Action to be taken by the device when an output undervoltage fault is detected.	0xB8 (non-latching shutdown; autonomous restart upon fault removal), read/write, paged, stored in user-editable NVM.	101
IOUT_OC_FAULT_LIMIT*n*	0x46	Output overcurrent fault threshold (cycle-by-cycle inductor peak current).	0xE240 (36A), read/write, paged, stored in user-editable NVM.	94
IOUT_OC_FAULT_RESPONSE*n*	0x47	Action to be taken by the device when an output overcurrent fault is detected.	0x00 (try to regulate through the fault condition/event; limit the cycle-by-cycle peak of the inductor current to not exceed the commanded IOUT_OC_FAULT_LIMIT), read/write, paged, stored in user-editable NVM.	103
IOUT_OC_WARN_LIMIT*n*	0x4A	Output overcurrent warning threshold (time-averaged inductor current).	0xDA90 (20.5A), read/write, paged, stored in user-editable NVM.	94
OT_FAULT_LIMIT*n*	0x4F	Overtemperature fault threshold.	0xF200 (128°C), read/write, paged, stored in user-editable NVM.	96

PMBus COMMAND SUMMARY

Table 1. Summary of Supported Commands

PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTM4686B NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	PAGE
OT_FAULT_RESPONSE*n*	0x50	Action to be taken by the device when an overtemperature fault is detected via TSNS*n*a.	0x80 (immediate off; no retry), read/write, paged, stored in user-editable NVM.	104
OT_WARN_LIMIT*n*	0x51	Overtemperature warning threshold.	0xEBE8 (125°C), read/write, paged, stored in user-editable NVM.	96
UT_FAULT_LIMIT*n*	0x53	Undertemperature fault threshold.	0xE530 (–45°C), read/write, paged, stored in user-editable NVM.	96
UT_FAULT_RESPONSE*n*	0x54	Response to undertemperature fault events.	0x80 (immediate off; no retry), read/write, paged, stored in user-editable NVM, read/write, paged, stored in user-editable NVM.	105
VIN_OV_FAULT_LIMIT	0x55	Input supply (SV_{IN}) overvoltage fault limit.	0xCB00 (6.000V), read/write, non-paged, stored in user-editable NVM.	89
VIN_OV_FAULT_RESPONSE*n*	0x56	Response to input overvoltage fault events.	0x80 (immediate off; no retry), read/write, paged, stored in user-editable NVM.	99
VIN_UV_WARN_LIMIT	0x58	Input undervoltage warning threshold.	0xCA0C (4.094V) Voltage as measured on the "SV_{IN}" pin, read/write, non-paged, stored in user-editable NVM.	89
IIN_OC_WARN_LIMIT	0x5D	Input supply overcurrent warning threshold.	0xDBC0 (30A), read/write, non-paged, stored in user-editable NVM.	93
TON_DELAY*n*	0x60	Time from RUN*n* and/or OPERATION*n* on to output rail turn-on.	0x0000 (0ms), read/write, paged, stored in user-editable NVM.	97
TON_RISE*n*	0x61	Time from when the output voltage reference starts to rise until it reaches its commanded setting.	0xC200 (2ms), read/write, paged, stored in user-editable NVM.	97
TON_MAX_FAULT_LIMIT*n*	0x62	Turn-on watchdog timeout fault threshold (time permitted for $V_{OUT}n$ to reach or exceed VOUT_UV_FAULT_LIMIT*n* after turn-on command is received).	0xD280 (10ms), read/write, paged, stored in user-editable NVM.	97
TON_MAX_FAULT_RESPONSE*n*	0x63	Action to be taken by the device when a TON_MAX_FAULT*n* event is detected.	0xB8 (non-latching shutdown; autonomous restart upon fault removal), read/write, paged, stored in user-editable NVM.	102
TOFF_DELAY*n*	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL*n* ramp.	0x0000 (0ms), read/write, paged, stored in user-editable NVM.	97
TOFF_FALL*n*	0x65	Time from when the output voltage reference starts to fall until it reaches 0V.	0xC280 (2.5ms), read/write, paged, stored in user-editable NVM.	98
TOFF_MAX_WARN_LIMIT*n*	0x66	Turn-off watchdog timeout fault threshold (time permitted for $V_{OUT}n$ to decay to or below 12.5% of the commanded $V_{OUT}n$ value at the time of receiving a turn-off command).	0xF320 (200ms), read/write, paged, stored in user-editable NVM.	98
STATUS_BYTE*n*	0x78	One byte summary of the unit's fault condition.	Default value not applicable, read/write, paged, not stored in NVM.	111
STATUS_WORD*n*	0x79	Two byte summary of the unit's fault condition.	Default value not applicable, read/write, paged, not stored in NVM.	111
STATUS_VOUT*n*	0x7A	Output voltage fault and warning status.	Default value not applicable, read/write, paged, not stored in NVM.	112

PMBus COMMAND SUMMARY

Table 1. Summary of Supported Commands

PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTM4686B NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	PAGE
STATUS_IOUT*n*	0x7B	Output current fault and warning status.	Default value not applicable, read/write, paged, not stored in NVM.	112
STATUS_INPUT	0x7C	Input supply (SV_{IN}) fault and warning status.	Default value not applicable, read/write, non-paged, not stored in NVM.	112
STATUS_ TEMPERATURE$_n$	0x7D	TSNS*n*a$^-$ sensed temperature fault and warning status for READ_TEMERATURE_1$_n$.	Default value not applicable, read/write, paged, not stored in NVM.	113
STATUS_CML	0x7E	Communication and memory fault and warning status.	Default value not applicable, read/write, non-paged, not stored in NVM.	113
STATUS_MFR_ SPECIFIC*n*	0x80	Manufacturer specific fault and state information.	Default value not applicable, read/write, paged, not stored in NVM.	113
READ_VIN	0x88	Measured input supply (SV_{IN}) voltage.	Default value not applicable, read-only, non-paged, not stored in NVM.	117
READ_IIN	0x89	Calculated total input supply current.	Default value not applicable, read-only, non-paged, not stored in NVM.	117
READ_VOUT*n*	0x8B	Measured output voltage.	Default value not applicable, read-only, paged, not stored in NVM.	117
READ_IOUT*n*	0x8C	Measured output current.	Default value not applicable, read-only, paged, not stored in NVM.	117
READ_ TEMPERATURE_1$_n$	0x8D	Measurement of TSNS*n*a$^-$ sensed temperature.	Default value not applicable, read-only, paged, not stored in NVM.	117
READ_ TEMPERATURE_2	0x8E	Measured control IC junction temperature.	Default value not applicable, read-only, non-paged, not stored in NVM.	118
READ_DUTY_CYCLE*n*	0x94	Measured duty cycle of MT*n*.	Default value not applicable, read-only, paged, not stored in NVM.	118
READ_POUT*n*	0x96	Calculated output power.	Default value not applicable, read-only, paged, not stored in NVM.	118
PMBUS_REVISION	0x98	PMBus revision supported by this device.	0x22 (Revision 1.2 of Part I and Revision 1.2 of Part II of PMBus Specification documents), read-only, non-paged, not stored in NVM.	108
MFR_ID	0x99	Manufacturer identification, in ASCII	“LTC”, read-only, non-paged.	108
MFR_MODEL	0x9A	Manufacturer’s part number, in ASCII	“LTM4686 ”, read-only, non-paged. Note: The MFR_MODEL value is “LTM4686 ”. The value consists of 8 ASCII characters and the last character is a blank space punctuation character (“ ”), i.e., ASCII code 0x20 or 32d.	109
MFR_SERIAL	0x9E	Serial number of this specific unit.	Up to nine bytes of custom-formatted data that identify the unit’s configuration, read-only, non-paged.	109
MFR_VOUT_MAX*n*	0xA5	Maximum allowed output voltage.	0x5B34 (5.700V) on both channels. Read-only, paged, not stored in user-editable NVM.	92
USER_DATA_00	0xB0	OEM reserved data.	Read/write, non-paged, stored in user-editable NVM. Recommended against altering.	108
USER_DATA_01*n*	0xB1	OEM reserved data.	Read/write, paged, stored in user-editable NVM. Recommended against altering.	108
USER_DATA_02	0xB2	OEM reserved data.	Read/write, non-paged, stored in user-editable NVM. Recommended against altering.	108
USER_DATA_03*n*	0xB3	User-editable words available for the user.	0x0000, read/write, paged, stored in user-editable NVM.	108
USER_DATA_04	0xB4	A user-editable word available for the user.	0x0000, read/write, non-paged, stored in user-editable NVM.	108
MFR_INFO	0xB6	Manufacturing specific information	Default value not applicable, read only, non-paged, not stored in NVM. Bit 5 is 0_b when ECC has made a correction to data derived from the EEPROM user space.	116

PMBus COMMAND SUMMARY

Table 1. Summary of Supported Commands

PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTM4686B NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	PAGE
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	Default value not applicable, read/write, non-paged, not stored in NVM.	126
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	Default value not applicable, read/write, non-paged, not stored in NVM.	126
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	Default value not applicable, read/write, non-paged, not stored in NVM.	126
MFR_CHAN_CONFIG_*$_n$	0xD0	Channel-specific configuration bits.	0x1D, read/write, paged, stored in user-editable NVM. Register is named “MFR_CHAN_CONFIG” and referred to as “MFR_CHAN_CONFIG_LTM468X” in LTpowerPlay.	84
MFR_CONFIG_ALL_*	0xD1	Global configuration bits, i.e., common to both V_{OUT} channels 0 and 1.	0x09, read/write, non-paged, stored in user-editable NVM. Bit 4 configures whether the SYNC drive circuit is active (0_b) or inactive (1_b); Bit 3 configures whether the Stuck PMBus Timer Timeout is 150ms for Block Reads and 32ms for Non-Block Reads (0_b) or 250ms for all Reads (1_b). Register is named "MFR_CONFIG_ALL_LTM468X” in LTpowerPlay.	85
MFR_GPIO_PROPAGATE_*$_n$	0xD2	Configuration bits for propagating faults to the $\overline{\text{GPIO}}n$ pins.	0x7993, read/write, paged, stored in user-editable NVM. Register is named “MFR_GPIO_PROPAGATE” and referred to as “MFR_GPIO_PROPAGATE_LTM468X” in LTpowerPlay.	106
MFR_PWM_MODE_*$_n$	0xD4	Configuration for the PWM engine of each V_{OUT} channel.	0xC3, read/write, paged, stored in user-editable NVM. Bit 1 commands whether the output is in high range (0_b) or low range (1_b). Bit 0 commands whether the output is operating in Forced Continuous Conduction Mode (1_b) or Discontinuous Mode (0_b). Command is named MFR_PWM_MODE and referred to as MFR_PWM_MODE_LTM468X in LTpowerPlay.	87
MFR_GPIO_RESPONSEn	0xD5	Action to be taken by the device when the $\overline{\text{GPIO}}n$ pin is asserted low by circuitry external to the unit.	0x00 (none; ignore), read/write, paged, stored in user-editable NVM.	107
MFR_OT_FAULT_RESPONSE	0xD6	Action to be taken by the device when a control IC junction overtemperature fault is detected.	0xC0 (make the respective output’s power stage high impedance, i.e., three-stated; autonomous restart upon fault removal), read-only, non-paged, not stored in user-editable NVM.	104
MFR_IOUT_PEAKn	0xD7	Maximum measured value of READ_IOUTn since the last MFR_CLEAR_PEAKS.	Default value not applicable, read-only, paged, not stored in NVM.	119
MFR_ADC_CONTROL	0xD8	ADC telemetry parameter for repeated fast ADC readback.	0x00, read/write, not paged, not stored in NVM. Allows telemetry readback rates up to 125Hz instead of 10Hz, nominal.	119
MFR_ADC_TELEMETRY_STATUS	0xDA	ADC status during short-loop.	Default value not applicable, read/write, not paged, not stored in NVM. ADC status indicating most recently digitized telemetry when engaged in short round-robin loop (MFR_ADC_CONTROL = 0x0D)	120
MFR_RETRY_DELAYn	0xDB	Retry interval during fault-retry mode.	0xFABC (350ms), read/write, paged, stored in user-editable NVM.	99
MFR_RESTART_DELAYn	0xDC	Minimum interval (nominal) the RUNn pin is pulled logic low by internal circuitry.	0xF320 (200ms), read/write, paged, stored in user-editable NVM.	98
MFR_VOUT_PEAKn	0xDD	Maximum measured value of READ_VOUTn since the last MFR_CLEAR_PEAKS.	Default value not applicable, read-only, paged, not stored in NVM.	118
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since the last MFR_CLEAR_PEAKS.	Default value not applicable, read-only, non-paged, not stored in NVM.	118

PMBus COMMAND SUMMARY

Table 1. Summary of Supported Commands

PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTM4686B NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	PAGE
MFR_ TEMPERATURE_1_ PEAK*n*	0xDF	Maximum value of TSNS*n*a measured temperature since the last MFR_CLEAR_PEAKS.	Default value not applicable, read-only, paged, not stored in NVM.	118
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Default value not applicable, send byte only, non-paged, not stored in NVM.	110
MFR_PADS	0xE5	Digital status of the I/O pads.	Default value not applicable, read-only, non-paged, not stored in NVM.	114
MFR_ADDRESS	0xE6	LTM4686B's I^2C slave address, right-justified.	0x4F, read/write, non-paged, stored in user-editable NVM. Bits[6:4] represent the user-configurable upper 3 bits of the 7-bit slave address of the device. Bits[3:0] are dictated by the ASEL resistor pin-strap setting. Setting this command to 0x80 disables device-specific addressing.	84
MFR_SPECIAL_ID	0xE7	Manufacturer code representing IC silicon and revision	0x477X, read-only, non-paged.	109
MFR_IIN_OFFSET$_n$	0xE9	Coefficient used in calculations of READ_IIN and MFR_READ_IIN$_n$, representing the contribution of input current drawn by the control IC, including the MOSFET drivers.	0x9315 (0.04816A), read/write, paged, stored in user-editable NVM.	92
MFR_FAULT_LOG_ STORE	0xEA	Commands a transfer of the fault log from RAM to EEPROM. This causes the part to behave as if a channel has faulted off.	Default value not applicable, send byte only, non-paged, not stored in NVM.	126
MFR_FAULT_LOG_ CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	Default value not applicable, send byte only, non-paged, not stored in NVM.	126
MFR_READ_IIN$_n$	0xED	Calculated input current, by channel.	Default value not applicable, read-only, paged, not stored in NVM.	117
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	Default value not applicable, read-only, non-paged, stored in fault-log NVM.	125
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI PSM ICs/modules.	Default value not applicable, read-only, non-paged, not stored in NVM.	114
MFR_COMPARE_ USER_ALL	0xF0	Compares current command contents (RAM) with NVM.	Default value not applicable, send byte only, non-paged, not stored in NVM.	121
MFR_ TEMPERATURE_2_ PEAK	0xF4	Maximum measured control IC junction temperature since last MFR_CLEAR_PEAKS.	Default value not applicable, read-only, non-paged, not stored in NVM.	118
MFR_PWM_ CONFIG_*	0xF5	Configuration bits for setting the phase interleaving angles of Channels 0 and 1, SHARE_CLK behavior in UVLO, and using the fully differential amplifier to regulate paralleled output channels.	0x10, read/write, non-paged, stored in user-editable NVM. When bit 7 is 0_b, Channel 1's output is regulated by the V_{OSNS1} and SGND feedback signals. When bit 7 is 1_b, Channel 1's output is regulated by the V_{OSNS0}+ and V_{OSNS0}– feedback signals. Only set bit 7 to 1_b for PolyPhase rail applications. The command is named MFR_PWM_CONFIG and referred to as MFR_PWM_CONFIG_LTM468X in LTpowerPlay.	88
MFR_IOUT_CAL_ GAIN_TC*n*	0xF6	Temperature coefficient of the current sensing element.	0x0F14 (3860ppm/°C), read/write, paged, stored in user-editable NVM.	93
MFR_TEMP_1_GAIN*n*	0xF8	Sets the slope of the temperature sensors that interface to TSNS*n*a.	0x3FAE (0.995, in custom units), read/write, paged, stored in user-editable NVM.	95

PMBus COMMAND SUMMARY

Table 1. Summary of Supported Commands

PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTM4686B NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	PAGE
MFR_TEMP_1_ OFFSET*n*	0xF9	Sets the offset of the TSNS*na* temperature sensor with respect to –273.1°C.	0x8000 (0.0), read/write, paged, stored in NVM.	95
MFR_RAIL_ ADDRESS*n*	0xFA	Common address for PolyPhase outputs to adjust common parameters.	0x80, read/write, paged, stored in NVM.	84
MFR_RESET	0xFD	Commanded reset without requiring a power down.	Default value not applicable, send byte only, non-paged, not stored in NVM. Identical to RESTORE_USER_ALL.	86

APPLICATIONS INFORMATION

Table 2. $V_{OUTnCFG}$ Pin Strapping Look-Up Table for the LTM4686B's Output Voltage, Coarse Setting (Not Applicable if MFR_CONFIG_ALL[6] = 1_b)

$R_{VOUTnCFG}$* (kΩ)	V_{OUTn} (V) SETTING COARSE	MFR_PWM_MODE*n*[1] BIT
Open	NVM	NVM
32.4	See Table 3	See Table 3
22.6	3.3	0
18.0	3.1	0
15.4	2.9	0
12.7	2.7	0
10.7	2.5	0, if V_{TRIMn} > 0mV 1, if V_{TRIMn} ≤ 0mV
9.09	2.3	1
7.68	2.1	1
6.34	1.9	1
5.23	1.7	1
4.22	1.5	1
3.24	1.3	1
2.43	1.1	1
1.65	0.9	1
0.787	0.7	1
0	0.5	1

*$R_{VOUTnCFG}$ value indicated is nominal. Select $R_{VOUTnCFG}$ from a resistor vendor such that its value is always within 3% of the value indicated in the table. Take into account resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect $R_{VOUTnCFG}$'s value over time. All such effects must be taken into account in order for resistor pin strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET or RESTORE_USER_ALL, over the lifetime of one's product.

Table 3. $V_{TRIMnCFG}$ Pin Strapping Look-Up Table for the LTM4686B's Output Voltage, Fine Adjustment Setting (Not Applicable if MFR_CONFIG_ALL[6] = 1_b)

$R_{VTRIMnCFG}$* (kΩ)	V_{TRIM} (mV) FINE ADJUSTMENT TO V_{OUTn} SETTING WHEN $R_{VOUTnCFG}$ ≠ 32.4kΩ	VOUT_COMMAND*n* SETTING (V) WHEN $R_{VOUTnCFG}$ = 32.4kΩ	MFR_PWM_MODE*n*[1] BIT
Open	0	NVM	0, if VOUT_OV_FAULT_LIMIT*n* > 2.75V 1, if VOUT_OV_FAULT_LIMIT*n* ≤ 2.75V
32.4	99		
22.6	86.625		
18.0	74.25		
15.4	61.875		
12.7	49.5		
10.7	37.125	Do Not Use	0
9.09	24.75	Do Not Use	0
7.68	12.375	Do Not Use	0
6.34	–12.375	Do Not Use	0
5.23	–24.75	Do Not Use	0
4.22	–37.125	Do Not Use	0
3.24	–49.5	Do Not Use	0
2.43	–61.875	Do Not Use	0
1.65	–74.25	Do Not Use	0
0.787	–86.625	3.50	0
0	–99	3.46	0

*$R_{VTRIMnCFG}$ value indicated is nominal. Select $R_{VTRIMnCFG}$ from a resistor vendor such that its value is always within 3% of the value indicated in the table. Take into account resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect $R_{VTRIMnCFG}$'s value over time. All such effects must be taken into account in order for resistor pin strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET or RESTORE_USER_ALL, over the lifetime of one's product.

APPLICATIONS INFORMATION

Table 4. $F_{SWPHCFG}$ Pin Strapping Look-Up Table to Set the LTM4686B's Switching Frequency and Channel Phase-Interleaving Angle (Not Applicable if MFR_CONFIG_ALL[6] = 1_b)

$R_{FSWPHCFG}$* (kΩ)	SWITCHING FREQUENCY (kHz)	θ_{SYNC} TO θ_0	θ_{SYNC} TO θ_1	BITS [2:0] OF MFR_PWM_CONFIG	BIT [4] OF MFR_CONFIG_ALL
Open	NVM; LTM4686B Default = 1000	NVM; LTM4686B Default = 0°	NVM; LTM4686B Default = 180°	NVM; LTM4686B Default = 000_b	NVM; LTM4686B Default = 0_b
15.4	575	0°	180°	000_b	0_b
12.7	650	0°	180°	000_b	0_b
10.7	750	0°	180°	000_b	0_b
9.09	1000	0°	180°	000_b	0_b
7.68	500	120°	240°	100_b	0_b
6.34	500	90°	270°	001_b	0_b
5.23	Sync Slave**	0°	240°	010_b	1_b
4.22	Sync Slave**	0°	120°	011_b	1_b
3.24	Sync Slave**	60°	240°	101_b	1_b
2.43	Sync Slave**	120°	300°	110_b	1_b
1.65	Sync Slave**	90°	270°	001_b	1_b
0.787	Sync Slave**	0°	180°	000_b	1_b
0	Sync Slave**	120°	240°	100_b	1_b

* $R_{FSWPHCFG}$ value indicated is nominal. Select $R_{FSWPHCFG}$ from a resistor vendor such that its value is always within 3% of the value indicated in the table. Take into account resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect $R_{FSWPHCFG}$'s value over time. All such effects must be taken into account in order for resistor pin-strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET or RESTORE_USER_ALL, over the lifetime of one's product.

** The "Sync Slave" setting results in MFR_CONFIG_ALL[4] being set to 1_b and FREQUENCY_SWITCH being set according to user-configurable EEPROM contents corresponding to Command 0x33 (factory default: 1MHz). In this configuration, the module's switching frequency synchronizes to the SYNC signal, provided that the SYNC pin is driven in a manner consistent with specifications (see Switching Frequency and Phase subsection of the Applications Information section for details).

APPLICATIONS INFORMATION

Table 5. ASEL Pin Strapping Look-Up Table to Set the LTM4686B's MFR_ADDRESS (Applicable Regardless of MFR_CONFIG_ALL[6] Setting)

R_{ASEL}* (kΩ)	SLAVE ADDRESS
Open	MFR_ADDRESS[6:0]_R/W
32.4	MFR_ADDRESS[6:4]_1111_R/W
22.6	MFR_ADDRESS[6:4]_1110_R/W
18.0	MFR_ADDRESS[6:4]_1101_R/W
15.4	MFR_ADDRESS[6:4]_1100_R/W
12.7	MFR_ADDRESS[6:4]_1011_R/W
10.7	MFR_ADDRESS[6:4]_1010_R/W
9.09	MFR_ADDRESS[6:4]_1001_R/W
7.68	MFR_ADDRESS[6:4]_1000_R/W
6.34	MFR_ADDRESS[6:4]_0111_R/W
5.23	MFR_ADDRESS[6:4]_0110_R/W
4.22	MFR_ADDRESS[6:4]_0101_R/W
3.24	MFR_ADDRESS[6:4]_0100_R/W
2.43	MFR_ADDRESS[6:4]_0011_R/W
1.65	MFR_ADDRESS[6:4]_0010_R/W
0.787	MFR_ADDRESS[6:4]_0001_R/W
0	MFR_ADDRESS[6:4]_0000_R/W

where:

R/W = Read/Write bit in control byte.
All PMBus device addresses listed in the specification are 7 bits wide unless otherwise noted.
Note: The LTM4686B will always respond to slave address 0x5A and 0x5B regardless of the NVM or ASEL resistor configuration values.

*R_{ASEL} value indicated is nominal. Select R_{ASEL} from a resistor vendor such that its value is always within 3% of the value indicated in the table. Take into account resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect R_{ASEL}'s value over time. All such effects must be taken into account in order for resistor pin-strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET or RESTORE_USER_ALL, over the lifetime of one's product.

Table 6. LTM4686B MFR_ADDRESS Command Examples Expressed in 7- and 8-Bit Addressing

DESCRIPTION	HEX DEVICE ADDRESS 7 BIT	8 BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	R/W
Rail[4]	0x5A	0xB4	0	1	0	1	1	0	1	0	0
Global[4]	0x5B	0xB6	0	1	0	1	1	0	1	1	0
Default	0x4F	0x9E	0	1	0	0	1	1	1	1	0
Example 1	0x40	0x80	0	1	0	0	0	0	0	0	0
Example 2	0x41	0x82	0	1	0	0	0	0	0	1	0
Disabled[2,3]			1	0	0	0	0	0	0	0	0

Note 1: This table can be applied to the MFR_RAIL_ADDRESS*n* command, but not the MFR_ADDRESS command.

Note 2: A disabled value in one command does not disable the device, nor does it disable the Global address.

Note 3: A disabled value in one command does not inhibit the device from responding to device addresses specified in other commands.

Note 4: It is not recommended to write the value 0x00, 0x0C (7 bit), 0x5A (7 bit), 0x5B (7 bit), or 0x7C (7 bit) to the MFR_RAIL_ADDRESS*n* or MFR_ADDRESS commands.

APPLICATIONS INFORMATION

V_{IN} TO V_{OUT} STEP-DOWN RATIOS

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage. Each output of the LTM4686B is capable of 95% duty cycle at 500kHz, but the V_{IN} to V_{OUT} minimum dropout is still a function of its load current and will limit output current capability related to high duty cycle on the topside switch. Minimum on-time $t_{ON(MIN)}$ is another consideration in operating at a specified duty cycle while operating at a certain frequency due to the fact that $t_{ON(MIN)} < D/f_{SW}$, where D is duty cycle and f_{SW} is the switching frequency. $t_{ON(MIN)}$ is specified in the electrical parameters as 45ns. See Note 6 in the Electrical Characteristics section for output current guideline.

INPUT CAPACITORS

The LTM4686B module should be connected to a low AC-impedance DC source. For the regulator input four 22µF input ceramic capacitors are used to handle the RMS ripple current. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated with Equation 2.

$$D_n = \frac{V_{OUT_n}}{V_{IN_n}} \quad (2)$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated with Equation 3.

$$I_{CINn(RMS)} = \frac{I_{OUTn(MAX)}}{\eta\%} \bullet \sqrt{D_n \bullet (1-D_n)} \quad (3)$$

In the above equation, $\eta\%$ is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor, or a Polymer capacitor.

OUTPUT CAPACITORS

The LTM4686B is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range for each output is from 400µF to 700µF. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spikes is required. Table 20 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 5A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 20 matrix, and the Analog Devices, Inc. µModule Power Design Tool will be provided for stability analysis. Multiphase operation reduces effective output ripple as a function of the number of phases. Analog Devices Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The Analog Devices, Inc. µModule Power Design Tool can calculate the output ripple reduction as the number of implemented phases increases by N times. A small value 10Ω resistor can be placed in series from V_{OUTn} to the V_{OSNS0}^+ or V_{OSNS1} pin to allow for a bode plot analyzer to inject a signal into the control loop and validate the regulator stability.

LIGHT LOAD CURRENT OPERATION

The LTM4686B has two modes of operation: high efficiency, discontinuous conduction mode or forced continuous conduction mode. The mode of operation is configured by bit 0 of the MFR_PWM_MODE*n* command (discontinuous conduction is always the start-up mode, forced continuous is the default running mode).

APPLICATIONS INFORMATION

If a channel is enabled for discontinuous mode operation, the inductor current is not allowed to reverse. The reverse current comparator, I_{REV}, turns off the bottom MOSFET (MB*n*) just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller can operate in discontinuous (pulse-skipping)operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined solely by the voltage on the COMP*n*a pin. In this mode, the efficiency at light loads is lower than discontinuous mode operation. However, continuous mode exhibits lower output ripple and less interference with audio circuitry. Forced continuous conduction mode may result in reverse inductor current, which can cause the input supply to boost. The VIN_OV_FAULT_LIMIT can detect this (if SV_{IN} is connected to V_{IN0} and/or V_{IN1}) and turn off the offending channel. However, this fault is based on an ADC read and can nominally take up to 90ms to detect. If there is a concern about the input supply boosting, keep the part in discontinuous conduction operation.

SWITCHING FREQUENCY AND PHASE

The switching frequency of the LTM4686B's channels is established by its analog phase-locked-loop (PLL) locking on to the clock present at the module's SYNC pin. The clock waveform on the SYNC pin can be generated by the LTM4686B's internal circuitry when an external pull-up resistor to 3.3V (e.g., V_{DD33}) is provided, in combination with the LTM4686B control IC's FREQUENCY_SWITCH command being set to one of the following supported values: 500kHz, 575kHz, 650kHz, 750kHz, 1MHz (see Table 8 for hexadecimal values). In this configuration, the module is called a "sync master": using the factory-default setting of MFR_CONFIG_ALL[4] = 0_b, SYNC becomes a bidirectional open-drain pin, and the LTM4686B pulls SYNC logic low for nominally 500ns at a time, at the prescribed clock rate. The SYNC signal can be bused to other LTM4686B modules (configured as "sync slaves"), for purposes of synchronizing switching frequencies of multiple modules within a system—but only one LTM4686B should be configured as a "sync master"; the other LTM4686B(s) should be configured as "sync slaves".

There are two recommended ways to configure an LTM4686B as a "sync slave":

- Apply an appropriate pin-strap resistor setting on the $F_{SWPHCFG}$ pin (see Table 4), and use the factory-default setting MFR_CONFIG_ALL[6] = 0_b. This configures MFR_CONFIG_ALL[4] = 1_b and FREQUENCY_SWITCH according to EEPROM settings (0x03E8 factory default, corresponding to 1MHz). The LTM4686B's SYNC pin thus becomes a high impedance input and the module synchronizes its frequency to that of the externally applied clock, provided that the frequency of the externally applied clock exceeds ~45% of the target frequency (FREQUENCY_SWITCH). If the SYNC clock is absent, the module responds by operating at its target frequency, indefinitely. If and when the SYNC clock is restored, the module automatically phase-locks to the SYNC clock as normal.
- Set FREQUENCY_SWITCH to 0x0000 and MFR_CONFIG_ALL[4] = 1_b. Using MFR_CONFIG_ALL[4] = 1_b, the LTM4686B's SYNC pin becomes a high impedance input, only—i.e., it does not drive SYNC low. The module synchronizes its frequency to that of the clock applied to its SYNC pin. The only shortcoming of this approach is: in the absence of an externally applied clock, the switching frequency of the module will default to the low end of its frequency-synchronization capture range.

The FREQUENCY_SWITCH command can be altered via I^2C commands, but only when switching action is disengaged, i.e., the module's outputs are turned off. The FREQUENCY_SWITCH command takes on the value stored in NVM at SV_{IN} power-up, but is overridden according to a resistor pin-strap applied between the $F_{SWPHCFG}$ pin and SGND only if the module is configured to respect resistor pin-strap settings (MFR_CONFIG_ALL[6] = 0_b). Table 4 highlights available resistor pin-strap and corresponding FREQUENCY_SWITCH settings.

APPLICATIONS INFORMATION

The relative phasing of all active channels in a PolyPhase rail should be optimally phased. The relative phasing of each rail is 360°/n, where n is the number of phases in the rail. MFR_PWM_CONFIG[2:0] configures channel relative phasing with respect to the SYNC pin. Phase relationship values are indicated with 0° corresponding to the falling edge of SYNC being coincident with the turn-on of the top MOSFETs, MT*n*.

The MFR_PWM_CONFIG command can be altered via I^2C commands, but only when switching action is disengaged, i.e., the module's outputs are turned off. The MFR_PWM_CONFIG command takes on the value stored in NVM at SV_{IN} power-up, but is overridden according to a resistor pin-strap applied between the $F_{SWPHCFG}$ pin and SGND only if the module is configured to respect resistor pin-strap settings (MFR_CONFIG_ALL[6] = 0_b). Table 4 highlights available resistor pin-strap and corresponding MFR_PWM_CONFIG[2:0] settings.

Some combinations of FREQUENCY_SWITCH and MFR_PWM_CONFIG[2:0] are not available by resistor pin-strapping the $F_{SWPHCFG}$ pin. All combinations of supported values for FREQUENCY_SWITCH and MFR_PWM_CONFIG[2:0] can be configured by NVM programming—or, I^2C transactions, provided switching action is disengaged, i.e., the module's outputs are turned off.

Care must be taken to minimize capacitance on SYNC to assure that the pull-up resistor versus the capacitor load has a low enough time constant for the application to form a "clean" clock. (See "Open-Drain Pins", later in this section.)

When an LTM4686B is configured as a sync slave, it is permissible for external circuitry to drive the SYNC pin from a current-limited source (less than 10mA), rather than using a pull-up resistor. Any external circuitry must not drive high with arbitrarily low impedance at SV_{IN} power-up, because the SYNC output can be low impedance until NVM contents have been downloaded to RAM.

Recommended LTM4686B switching frequencies of operation for many common V_{IN}-to-V_{OUT} applications are indicated in Table 7. When the two channels of an LTM4686B are stepping input voltage(s) down to output voltages whose recommended switching frequencies in Table 7 are significantly different, operation at the higher of the two recommended switching frequencies is preferable, but minimum on-time must be considered. (See Minimum On-Time Considerations section.) For example, consider an application in which it is desired for an LTM4686B to step-down $5V_{IN}$ to $0.6V_{OUT}$ on Channel 0, and $5V_{IN}$ to $3.3V_{OUT}$ on Channel 1: according to Table 7, the recommended switching frequency is 500kHz and 1MHz, respectively. However, the switching frequency setting of the LTM4686B is common to both channels. Based on the aforementioned guidance, operation at 1MHz would be preferred—in order to keep inductor ripple currents reasonable. The on-time for a $5V_{IN}$-to-$0.6V_{OUT}$ condition at 1MHz is 120ns, thus meeting the 90ns guardband recommendation. Therefore, for this particular example, the recommended switching frequency becomes 1MHz.

Table 7. Recommended Switching Frequency for Various V_{IN}-to-V_{OUT} Step-Down Scenarios

	$2.5V_{IN}$	**$3.3V_{IN}$**	**$5V_{IN}$**
$0.6V_{OUT}$	425kHz	425kHz	500kHz
$0.7V_{OUT}$	500kHz	500kHz	575kHz
$0.8V_{OUT}$	500kHz	575kHz	650kHz
$0.9V_{OUT}$	575kHz	575kHz	650kHz
$1V_{OUT}$	575kHz	650kHz	750kHz
$1.2V_{OUT}$	575kHz	750kHz	1MHz
$1.5V_{OUT}$	575kHz	750kHz	1MHz
$1.8V_{OUT}$	575kHz	750kHz	1MHz
$2.5V_{OUT}$	N/A	650kHz	1MHz
$3.3V_{OUT}$	N/A	N/A	1MHz

The current drawn by the SV_{IN} pin of the LTM4686B is not digitized or computed. A value representing the estimated SV_{IN} current is located in the MFR_IIN_OFFSET*n* command, and is used in the computations of input current readback telemetry, namely READ_IIN and and MFR_READ_IIN*n*. The recommended setting of MFR_IIN_OFFSET*n* is found in Table 8. The same value should be used for MFR_IIN_OFFSET0 and MFR_IIN_OFFSET1 (i.e., Pages 0x00 and 0x01).

APPLICATIONS INFORMATION

Table 8. Recommended MFR_IIN_OFFSET*n* Setting vs Switching Frequency Setting

SWITCHING FREQUENCY (kHz)	FREQUENCY_ SWITCH COMMAND VALUE (HEX.)	RECOMMENDED MFR_IIN_ OFFSET*n* SETTING (mA)	RECOMMENDED MFR_IIN_ OFFSET*n* SETTING (HEX.)
500	0xFBE8	29.56	0x8BC9
575	0x023F	32.35	0x9212
650	0x028A	35.14	0x9240
750	0x02EE	38.86	0x927D
1000	0x03E8	48.16	0x9315
Sync. to External Clock, f_{SYNC}	N/A	$0.0372 \bullet f_{SYNC} + 10.96$	*

*See Appendix C: PMBus Command Details, L11 data format.

MINIMUM ON-TIME CONSIDERATIONS

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTM4686B is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure Equation 6.

$$t_{ON(MIN)} < \frac{V_{OUTn}}{V_{INn} \bullet f_{OSC}} \quad (6)$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTM4686B is 45ns, nominal, guardband to 90ns.

VARIABLE DELAY TIME, SOFT-START AND OUTPUT VOLTAGE RAMPING

The LTM4686B must enter its run state prior to soft-start. The RUN*n* pins are released after the part initializes and SV_{IN} is greater than the VIN_ON threshold. If multiple LTM4686Bs are used in an application, they should be configured to share the same RUN*n* pins. They all hold their respective RUN*n* pins low until all devices initialize and SV_{IN} exceeds the VIN_ON threshold for all devices. The SHARE_CLK pin assures all the devices connected to the signal use the same time base.

After the RUN*n* pin releases, the controller waits for the user-specified turn-on delay (TON_DELAY*n*) prior to initiating an output voltage ramp. Multiple LTM4686Bs and other ADI parts can be configured to start with variable delay times. To work correctly, all devices use the same timing clock (SHARE_CLK) and all devices must share the RUN*n* pin. This allows the relative delay of all parts to be synchronized. The actual variation in the delay will be dependent on the highest clock rate of the devices connected to the SHARE_CLK pin (all Analog Devices, ICs are configured to allow the fastest SHARE_CLK signal to control the timing of all devices). The SHARE_CLK signal can be ±5% in frequency, thus the actual time delays will have some variance.

Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set point. The rise time of the voltage ramp can be programmed using the TON_RISE*n* command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting TON_RISE*n* to any value less than 0.250ms. The LTM4686B performs the necessary math internally to assure the voltage ramp is controlled to the desired slope. However, the voltage slope can not be any faster than the fundamental limits of the power stage. The number of steps in the ramp is equal to TON_RISE/0.1ms. Therefore, the shorter the TON_RISE*n* time setting, the more jagged the soft-start ramp appears.

The LTM4686B PWM always operates in discontinuous mode during the TON_RISE*n* operation. In discontinuous mode, the bottom MOSFET (MB*n*) is turned off as soon as reverse current is detected in the inductor. This allows the regulator to start up into a prebiased load.

There is no analog tracking feature in the LTM4686B; however, two outputs can be given the same TON_RISE*n* and TON_DELAY*n* times to achieve ratiometric rail tracking. Because the RUN*n* pins are released at the same time and both units use the same time base (SHARE_CLK), the outputs track very closely. If the circuit is in a PolyPhase configuration, all timing parameters must be the same.

APPLICATIONS INFORMATION

Coincident rail tracking can be achieved by setting two outputs to have the same turn-on/off slew rates, identical turn-on delays, and appropriately chosen turn-off delays (see Equation 7 through Equation 9).

$$\frac{VOUT\_COMMAND_{RAIL1}}{TON\_RISE_{RAIL1}} = \frac{VOUT\_COMMAND_{RAIL2}}{TON\_RISE_{RAIL2}}$$

and (7)

$$\frac{VOUT\_COMMAND_{RAIL1}}{TOFF\_FALL_{RAIL1}} = \frac{VOUT\_COMMAND_{RAIL2}}{TOFF\_FALL_{RAIL2}}$$

and

$$TON\_DELAY_{RAIL1} = TON\_DELAY_{RAIL2}$$

and (if $VOUT\_COMMAND_{RAIL2} \geq VOUT\_COMMAND_{RAIL1}$)

$$TOFF\_DELAY_{RAIL1} = TOFF\_DELAY_{RAIL2} + \left(1 - \frac{VOUT\_COMMAND_{RAIL1}}{VOUT\_COMMAND_{RAIL2}}\right) \bullet TOFF\_FALL_{RAIL2} \quad (8)$$

or else ($VOUT\_COMMAND_{RAIL2} < VOUT\_COMMAND_{RAIL1}$)

$$TOFF\_DELAY_{RAIL2} = TOFF\_DELAY_{RAIL1} + \left(1 - \frac{VOUT\_COMMAND_{RAIL2}}{VOUT\_COMMAND_{RAIL1}}\right) \bullet TOFF\_FALL_{RAIL1} \quad (9)$$

The described method of start-up sequencing is time based. For concatenated events it is possible to control the RUN pin based on the $\overline{GPIO}n$ pin of a different controller (see Figure 1). The $\overline{GPIO}n$ pin can be configured to release when the output voltage of the converter is greater than the VOUT_UV_FAULT_LIMIT*n*. It is recommended to use the unfiltered V_{OUT} UV fault limit because there is little appreciable time delay between the converter crossing the UV threshold and the $\overline{GPIO}n$ pin releasing. The unfiltered output can be enabled by the MFR_GPIO_PROPAGATE*n*[12] setting. (Refer to the MFR section of the PMBus commands in Appendix C: PMBus Command Details). The unfiltered signal may have some glitching as the V_{OUT} signal transitions through the comparator threshold. A small digital filter of 250µs internally deglitches the $\overline{GPIO}n$ pins. If the TON_RISE time is greater than 100ms, the deglitch filter should be complimented with an externally applied capacitor between $\overline{GPIO}n$ and ground—to further filter the waveform. The RC time-constant of the filter should be set sufficiently fast to assure no appreciable delay is incurred. For most applications, a value of 300µs to 500µs will provide sufficient filtering without significantly delaying the trigger event.

DIGITAL SERVO MODE

For maximum accuracy in the regulated output voltage, enable the digital servo loop by asserting bit 6 of the MFR_PWM_MODE*n* command. In digital servo mode, the LTM4686B adjusts the regulated output voltage based on the ADC voltage reading. Every 90ms the digital servo loop steps the LSB of the DAC (nominally 1.375mV or 0.6875mV depending on the voltage range bit, MFR_PWM_MODE*n*[1]) until the output is at the correct ADC reading. At power-up this mode engages after TON_MAX_FAULT_LIMIT*n* unless the limit is set to 0 (infinite). If the TON_MAX_FAULT_LIMIT*n* is set to 0 (infinite), the servo begins after TON_RISE*n* is complete and $V_{OUT}n$ has exceeded VOUT_UV_FAULT_LIMIT*n* and IOUT_OC*n* is not present. This same point in time is when the output changes from discontinuous to the mode commanded by MFR_PWM_MODE*n*[0]. Refer to Figure 2 for details on the $V_{OUT}n$ waveform under time based sequencing.

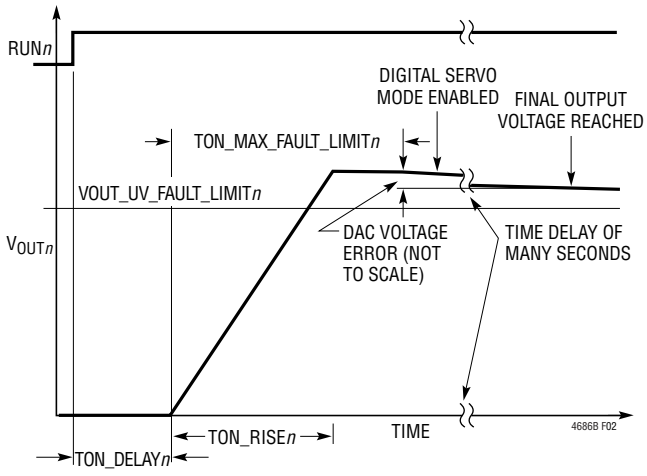


Figure 2. Timing Controlled V_{OUT} Rise

APPLICATIONS INFORMATION

If the TON_MAX_FAULT_LIMIT*n* is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE*n* is set to ignore (0x00), the servo begins:

1. After the TON_RISE$_n$ sequence is complete
2. After the TON_MAX_FAULT_LIMIT*n* time is reached; and
3. After the VOUT_UV_FAULT_LIMIT*n* has been exceed or the IOUT_OC_FAULT_LIMIT*n* is no longer active.

If the TON_MAX_FAULT_LIMIT*n* is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE*n* is not set to ignore (0X00), the servo begins:

1. After the TON_RISE$_n$ sequence is complete;
2. After the TON_MAX_FAULT_LIMIT*n* time has expired and both VOUT_UV_FAULT*n* and IOUT_OC_FAULT*n* are not present.

The maximum rise time is limited to 1.3 seconds.

In a PolyPhase configuration it is recommended only one of the control loops have the digital servo mode enabled. This will assure the various loops do not work against each other due to slight differences in the reference circuits.

SOFT OFF (SEQUENCED OFF)

In addition to a controlled start-up, the LTM4686B also supports controlled turn-off. The TOFF_DELAY*n* and TOFF_FALL$_n$ functions are shown in Figure 3. TOFF_FALL*n* is processed when the RUN*n* pin goes low or if the module is commanded off. If the module faults off or $\overline{\text{GPIO}}$*n* is pulled low externally and the module is programmed to respond to this (MFR_GPIO_RESPONSE*n* = 0xC0), the output three-states (becomes high impedance) rather than exhibiting a controlled ramp. The output then decays as a function of the load.

The output voltage operates as shown in Figure 3 so long as the part is in forced continuous mode and the TOFF_FALL*n* time is sufficiently slow that the power stage can achieve the desired slope. The TOFF_FALL*n* time can only be met if the power stage and controller can sink sufficient current to assure the output is at zero volts by the end of the fall time interval. If the TOFF_FALL*n* time is set shorter than the time required to discharge the load capacitance, the output will not reach the desired zero volt state. At the end of TOFF_FALL*n*, the controller ceases to sink current and V_{OUTn} decays at the natural rate determined by the load impedance. If the controller is in discontinuous mode, the controller does not pull negative current and the output becomes pulled low by the load, not the power stage. The maximum fail time is limited to 1.3 seconds. The number of steps in the ramp is equal to TOFF_FALL/0.1ms.Therefore, the shorter the TOFF_FALL*n* setting, the more jagged the TOFF_FALL*n* ramp appears.

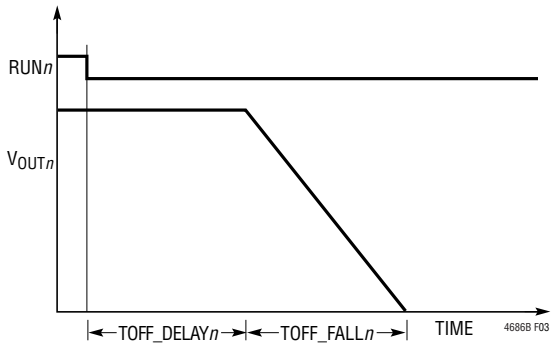


Figure 3. TOFF_DELAY*n* and TOFF_FALL*n*

UNDERVOLTAGE LOCKOUT

The LTM4686B is initialized by an internal threshold-based UVLO where SV_{IN} must be approximately 4V and $INTV_{CC}$, V_{DD33}, V_{DD25} must be within approximately 20% of the regulated values. In addition, V_{DD33} must be within approximately 7% of the targeted value before the LTM4686B releases its RUN*n* pins. After the part has initialized, an additional comparator monitors SV_{IN}. The VIN_ON threshold must be exceeded before the power sequencing can begin. When SV_{IN} drops below the VIN_OFF threshold, the LTM4686B ceases PWM action and SV_{IN} must increase above the VIN_ON threshold before the controller will restart. The normal start-up sequence will be allowed after the VIN_ON threshold is crossed.

It is possible to program the contents of the NVM in the application if the V_{DD33} supply is externally driven. This activates the digital portion of the LTM4686B without engaging the high voltage sections. PMBus communications are valid in this supply configuration. If SV_{IN} has not been applied to the LTM4686B, MFR_COMMON[3] will

APPLICATIONS INFORMATION

be asserted low, indicating that NVM has not initialized. If this condition is detected, the part will only respond to addresses 0x5A and 0x5B. To initialize the part issue the following set of commands: global address 0x5B command 0xBD data 0x2B followed by global address 0x5B command 0xBD and data 0xC4. The part will now respond to the correct address. Configure the part as desired then issue a STORE_USER_ALL. When SV_{IN} is applied a MFR_RESET or RESTORE_USER_ALL, command must be issued to allow the PWM to be enabled and valid ADC conversions to be read.

FAULT DETECTION AND HANDLING

The LTM4686B $\overline{GPIO}n$ pins are configurable to indicate a variety of faults including OV/UV, OC, OT, timing faults, peak overcurrent faults. In addition the $\overline{GPIO}n$ pins can be pulled low by external sources to indicate to the LTM4686B the presence of a fault in some other portion of the system. The fault response is configurable via PMBus Command Code names with a _RESPONSE suffix and allows the following options:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY*n*

Refer to Appendix C and the PMBus specification for more details.

The OV response is automatic and rapid. If an OV is detected, MT*n* is turned off and BG*n* is turned on, until the OV condition clears.

Fault logging is available on the LTM4686B. The fault logging is configurable to automatically store data when a fault occurs that causes the unit to fault off. The header portion of the fault logging table contains peak values. It is possible to read these values at any time. This data will be useful while troubleshooting the fault.

If the LTM4686B internal temperature is in excess of 85°C or below 0°C, the write into the NVM is not recommended. The data will still be held in RAM, unless the 3.3V supply UVLO threshold is reached. If the die temperature exceeds 130°C all NVM communication is disabled until the die temperature drops below 125°C, with the exception of the RESTORE_USER_ALL command, which is valid at any temperature.

OPEN-DRAIN PINS

Note that up to nine pull-up resistors are required for proper operation of the LTM4686B:

- Three for the SMBus/I^2C interface (the SCL, SDA, and $\overline{ALERT}$ pins); two, only if the system SMBus host does not make use of the $\overline{ALERT}$ interrupt. (These are 5V tolerant).
- One each for the RUN0 and RUN1 pins (or, just one to RUN0 and RUN1, if RUN0 and RUN1 are electrically connected together). (These are 5V tolerant).
- One each for $\overline{GPIO0}$ and $\overline{GPIO1}$ (or, just one to $\overline{GPIO0}$ and $\overline{GPIO1}$, if $\overline{GPIO0}$ and $\overline{GPIO1}$ are electrically connected together). (These are 3.3V tolerant).
- One on SHARE_CLK, required, for the LTM4686B to establish a heartbeat time base for timing-related operations and functions (output voltage ramp-up timing, voltage margining transition timing, SYNC open-drain drive frequency). (SHARE CLK is 3.3V tolerant).
- One on SYNC, in order for the LTM4686B to phase lock to the frequency generated by the open-drain output of its digital engine. EXCEPTION: in some applications, it is desirable to drive the LTM4686B's SYNC pin with a hard-driven (low impedance) external clock. This is the only scenario where the LTM4686B does not require a pull-up resistor on SYNC. However, be aware that the SYNC pin can be low impedance during NVM initialization, i.e., during download of EEPROM contents to RAM (for ~50ms [Note 12] after SV_{IN} power is applied). Therefore, the hard-driven clock signal should only be applied to the LTM4686B SYNC pin through a series resistor whose impedance limits current into the SYNC pin during NVM initialization to less than 10mA. If FREQUENCY_SWITCH = 0x0000, any clock signal should be provided prior to the RUN*n* pins toggle from logic low to logic high, or else the switching frequency of the LTM4686B will start off at the low end of its PLL-capture range until the SYNC clock becomes established. (SYNC is 3.3V tolerant).

APPLICATIONS INFORMATION

All the above pins interface to pull-down transistors within the module that can sink 3mA at 0.4V. The low threshold on the pins is 0.8V; thus, plenty of margin on the digital signals with 3mA of current. For 3.3V pins, 3mA of current is a 1.1k resistor. Unless there are transient speed issues associated with the RC time constant of the resistor pull-up and parasitic capacitance to ground, a 10k resistor or larger is generally recommended.

For high speed signals such as the SDA, SCL and SYNC, a lower value resistor may be required. The RC time constant should be set to 1/3 to 1/5 the required rise time to avoid timing issues. For a 100pF load and a 400kHz PMBus communication rate, the rise time must be less than 300ns. The resistor pull-up on the SDA and SCL pins with the time constant set to 1/3 the rise time is give by Equation 4.

$$R_{PULLUP} = \frac{t_{RISE}}{3 \bullet 100pF} = 1k \quad (4)$$

Be careful to minimize parasitic capacitance on the SDA and SCL pins to avoid communication problems. To estimate the loading capacitance, monitor the signal in question and measure how long it takes for the desired signal to reach approximately 63% of the output value. This is one time constant.

The SYNC pin interfaces to a pull-down transistor within the module whose output is held low for nominally 500ns per switching period. If the internal oscillator is set for 500kHz and the load is 100pF and a 3x time constant is required, the resistor calculation is given by Equation 5.

$$R_{PULLUP} = \frac{2\mu s - 500ns}{3 \bullet 100pF} = 5k \quad (5)$$

The closest 1% resistor is 4.99k.

If timing errors are occurring or if the SYNC frequency is not as fast as desired, monitor the waveform and determine if the RC time constant is too long for the application. If possible reduce the parasitic capacitance. If not reduce the pull up resistor sufficiently to assure proper timing.

PHASE-LOCKED LOOP AND FREQUENCY SYNCHRONIZATION

The LTM4686B has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. The PLL is locked to the falling edge of the SYNC pin. The phase relationship between channel 0, channel 1 and the falling edge of SYNC is controlled by the lower 3 bits of the MFR_PWM_CONFIG command. For PolyPhase applications, it is recommended all the phases be spaced evenly. Thus for a 2-phase system the signals should be 180° out of phase and a 4-phase system should be spaced 90°.

The phase detector is an edge-sensitive digital type that provides a known phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. The PLL lock range is guaranteed between 450kHz and 1.05MHz.

The PLL has a lock detection circuit. If the PLL should lose lock during operation, bit 4 of the STATUS_MFR_SPECIFIC command is asserted and the $\overline{\text{ALERT}}$ pin is pulled low. The fault can be cleared by writing a 1 to the bit. If the user does not wish to see the PLL_FAULT, even if a synchronization clock is not available at power up, bit 3 of the MFR_CONFIG_ALL command must be asserted.

If the SYNC signal is not clocking in the application, the PLL runs at the lowest free running frequency of the VCO. This will be well below the intended PWM frequency of the application and may cause undesirable operation of the converter.

If the PWM (SW*n*) signal appears to be running at too high a frequency, monitor the SYNC pin. Extra transitions on the falling edge will result in the PLL trying to lock on to noise instead of the intended signal. Review routing of digital control signals and minimize crosstalk to the SYNC signal to avoid this problem. Multiple LTM4686Bs are required to share the SYNC pin in PolyPhase configurations; for other configurations, it is optional. If the SYNC

APPLICATIONS INFORMATION

pin is shared between LTM4686Bs, only one LTM4686B can be programmed with a frequency output. All the other LTM4686Bs must be configured for external clock (MFR_CONFIG_ALL[4] = 1_b, and/or see Table 4).

R_{CONFIG} PIN-STRAPS (EXTERNAL RESISTOR CONFIGURATION PINS)

The LTM4686B default NVM is programmed to respect the RCONFIG pins. If a user wishes the output voltage, PWM frequency and phasing and the address to be set without programming the part or purchasing specially programmed parts, the RCONFIG pins can be used to establish these parameters—provided MFR_CONFIG_ALL[6] = 0_b. The RCONFIG pins only require a resistor terminating to SGND of the LTM4686B. The RCONFIG pins are only monitored at initial power up and during a reset (MFR_RESET or RESTORE_USER_ALL) so modifying their values perhaps using a DAC after the part is powered will have no effect. To assure proper operation, the value of RCONFIG resistors applied to the LTM4686B pin-strapping pins must not deviate more than ±3% away from the target nominal values indicated in lookup Table 2 to Table 5, over the lifetime of the product. Thin film, 1% tolerance (or better), ±50ppm/°C-T.C.R. rated (or better) resistors from vendors such as KOA Speer, Panasonic, Vishay and Yageo are good candidates. Noisy clock signals should not be routed near these pins. Note that bits [3:0] of MFR_ADDRESS are dictated by the ASEL pin-strap resistor regardless of the setting of MFR_CONFIG_ALL[6].

VOLTAGE SELECTION

When an output voltage is set using the RCONFIG pins on VOUT*n*_CFG and VTRIM*n*_CFG (MFR_CONFIG_ALL[6] = 0_b), the following parameters are set as a percentage of the output voltage:

- VOUT_OV_FAULT_LIMIT +10%
- VOUT_OV_WARN +7.5%
- VOUT_MAX +7.5%
- VOUT_MARGIN_HI +5%
- VOUT_MARGIN_LO –5%
- VOUT_UV_WARN –6.5%
- VOUT_UV_FAULT_LIMIT –7%

CONNECTING THE USB TO THE I^2C/SMBus/PMBus CONTROLLER TO THE LTM4686B IN SYSTEM

The ADI USB to I^2C/SMBus/PMBus controller can be interfaced to the LTM4686B on the user's board for programming, telemetry and system debug. The controller, when used in conjunction with LTpowerPlay, provides a powerful way to debug an entire power system. Faults are quickly diagnosed using telemetry, fault status registers and the fault log. The final configuration can be quickly developed and stored to the LTM4686B EEPROM.

Figure 4 and Figure 5 illustrate the application schematics for powering, programming and communicating with one or more LTM4686Bs via the ADI I^2C/SMBus/PMBus controller regardless of whether or not system power is present. If system power is not present the dongle will power the LTM4686B through the V_{DD33} supply pin. To initialize the part when SV_{IN} is not applied and the V_{DD33} pin is powered use global address 0x5B command 0xBD data 0x2B followed by address 0x5B command 0xBD data 0xC4. The part can now be communicated with, and the project file updated. To write the updated project file to the NVM issue a STORE_USER_ALL command. When SV_{IN} is applied, a MFR_RESET or RESTORE_USER_ALL must be issued to allow the PWM to be enabled and valid ADCs to be read.

Because of the controllers limited current sourcing capability, only the LTM4686Bs, their associated pull-up resistors and the I^2C pull-up resistors should be powered from the ORed 3.3V/3.4V supply. In addition, any device sharing the I^2C bus connections with the LTM4686B must not have body diodes between the SDA/SCL pins and their respective V_{DD} node because this will interfere with bus communication in the absence of system power. In Figure 4, the dongle will not bias the LTM4686Bs when SV_{IN} is present. It is recommended the RUN*n* pins be held low to avoid providing power to the load until the part is fully configured.

APPLICATIONS INFORMATION

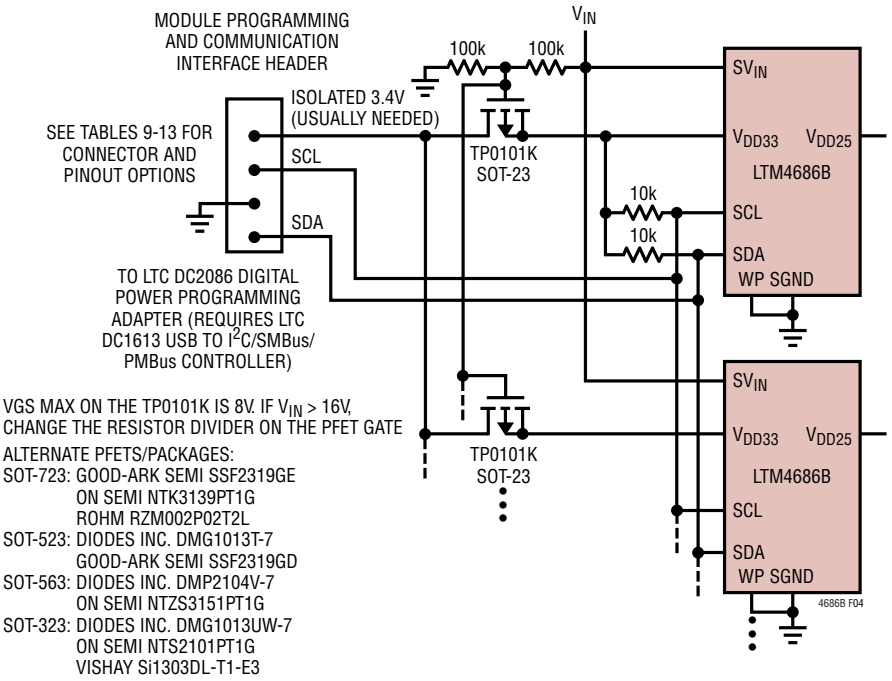


Figure 4. Circuit Suitable for Programming EEPROM/NVM of LTM4686B and Other ADI PSM Modules/ICs in Vast Systems, Even When V_{IN} Power is Absent, 0°C < T_J ≤ 85°C

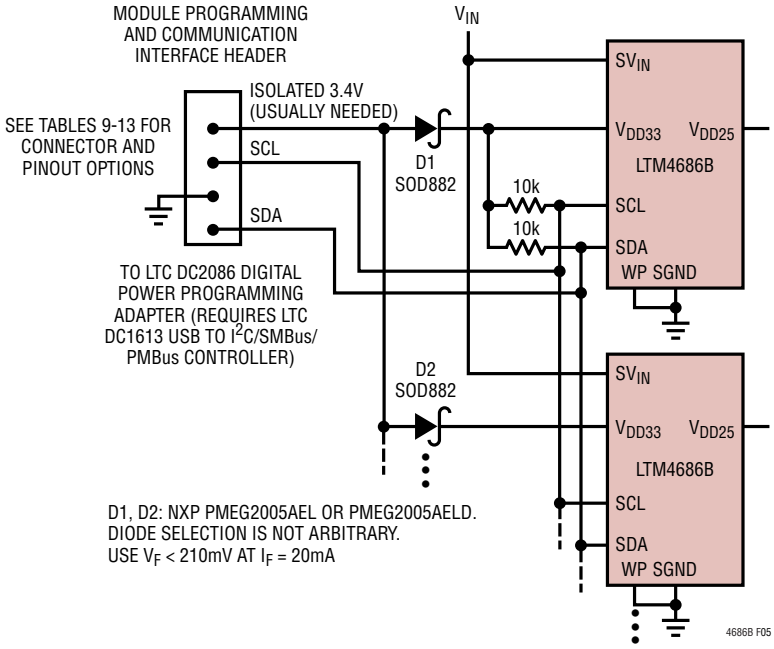


Figure 5. Circuit Suitable for Programming EEPROM/NVM of LTM4686B and Other ADI PSM Modules/ICs in Vast Systems, Even When V_{IN} Power is Absent, T_A > 20°C and T_J < 85°C

APPLICATIONS INFORMATION

The ADI controller/adapter I^2C connections are opto-isolated from the PC USB. The 3.3V/3/4V from the controller/adapter and the LTM4686B V_{DD33} pin must be driven to each LTM4686B with a separate PFET or diode, according to Figure 4 and Figure 5. Only when SV_{IN} is not applied is it permissible for the V_{DD33} pins to be electrically in parallel because the $INTV_{CC}$ LDO is off. The DC1613's 3.3V current limit is 100mA but typical V_{DD33} currents are under 15mA. The V_{DD33} does back drive the $INTV_{CC}$ pin. Normally this is not an issue if SV_{IN} is open. The DC2086 is capable of delivering 3.4V at 2A.

Using a 4-pin header in Figure 4 or Figure 5 maximizes flexibility to alter the LTM4686B's NVM contents at any stage of the user's product development and production cycles. If the LTM4686B's NVM is "pre-programmed", i.e., contains its finalized configuration, prior to being soldered to the user's PCB/motherboard—or, if other means have been provided for altering the LTM4686B's NVM contents in the user's system—then the 3.3V/3.4V pin on the header is not needed, and a 3-pin header is sufficient to establish GUI communications. The LTM4686B can be purchased with customized NVM contents; consult factory for details. Alternatively, the NVM contents of the LTM4686B can be configured in a mass production environment by designing for it in ICT (in-circuit test), or by providing a means of applying SV_{IN} while holding the LTM4686B's RUN pins low. Communication to the module must be made possible via the SCL and SDA pins/nets in all NVM programming scenarios. Recommended headers are found in Table 9 and Table 10.

Table 9. 4-Pin Headers, 2mm Pin-to-Pin Spacing, Gold Flash or Plating, Compatible with DC2086 Cables

MOUNTING STYLE	INSERTION ANGLE	INTERFACE STYLE	VENDOR	PART NUMBER	PINOUT STYLE (SEE Table 11)
Surface Mount	Vertical	Shrouded and Keyed Header	Hirose	DF3DZ-4P-2V(51) DF3DZ-4P-2V(50) DF3Z-4P-2V(50)	Type A
		Non Shrouded, Non-Keyed Header	3M	951104-2530-AR-PR	Type A and B Supported. Reversible/Not Keyed
	Right Angle	Shrouded and Keyed Header	Hirose	DF3DZ-4P-2H(51) DF3DZ-4P-2H(50)	Type A
		Non Shrouded. Cable-to-Header/PCB Mechanics Yield Keying Effect	FCI	10112684-G03-04ULF	Type B. Keying Achieved by PCB Surface
Through-Hole	Vertical	Shrouded and Keyed Header	Hirose	DF3-4P-2DSA(01)	Type A
		Non Shrouded, Non-Keyed Header	Harwin	M22-2010405	Type A and B Supported. Reversible/Not Keyed
			Samtec	TMM-104-01-LS	
			Sullins	NRPN041PAEN-RC	
	Right Angle	Shrouded and Keyed Header	Hirose	DF3-4P-2DS(01)	Type A
		Non Shrouded. Cable-to-Header/PCB Mechanics Yield Keying Effect	Norcomp	27630402RP2	Type B. Keying Achieved by Intentional PCB Interference
			Harwin	M22-2030405	
			Samtec	TMM-104-01-L-S-RA	

APPLICATIONS INFORMATION

Table 10. 3-Pin Headers, 2mm Pin-to-Pin Spacing, Gold Flash or Plating, Compatible with DC2086 Cables

MOUNTING STYLE	INSERTION ANGLE	INTERFACE STYLE	VENDOR	PART NUMBER	PINOUT STYLE (SEE Table 12)
Surface Mount	Vertical	Shrouded and Keyed Header	Hirose	DF3DZ-3P-2V(51) DF3DZ-3P-2V(50) DF3Z-3P-2V(50)	Type A
		Non Shrouded, Non-Keyed Header	3M	951103-2530-AR-PR	Type A and B Supported. Reversible/Not Keyed
	Right Angle	Shrouded and Keyed Header	Hirose	DF3DZ-3P-2H(51) DF3DZ-3P-2H(50)	Type A
		Non Shrouded. Cable-to-Header/PCB Mechanics Yield Keying Effect	FCI	10112684-G03-03LF	Type B. Keying Achieved by PCB Surface
Through-Hole	Vertical	Shrouded and Keyed Header	Hirose	DF3-3P-2DSA(01)	Type A
		Non Shrouded, Non-Keyed Header	Harwin	M22-2010305	Type A and B Supported. Reversible/Not Keyed
			Samtec	TMM-103-01-LS	
			Sullins	NRPN031PAEN-RC	
	Right Angle	Shrouded and Keyed Header	Hirose	DF3-3P-2DS(01)	Type A
		Non Shrouded. Cable-to-Header/PCB Mechanics Yield Keying Effect	Norcomp	27630302RP2	Type B. Keying Achieved by Intentional PCB Interference
			Harwin	M22-2030305	
			Samtec	TMM-103-01-L-S-RA	

Table 11. Recommended 4-Pin Header Pinout (Pin Numbering Scheme Adheres to Hirose Conventions). Interfaces to DC2086 Cables

PIN NUMBER	PINOUT STYLE "A" (SEE TABLE 9)	PINOUT STYLE "B" (SEE TABLE 9)
1	SDA	Isolated 3.3V/3.4V
2	GND	SCL
3	SCL	GND
4	Isolated 3.3V/3.4V	SDA

Table 12. Recommended 3-Pin Header Pinout (Pin Numbering Scheme Adheres to Hirose Conventions). Interfaces to DC2086 Cables

PIN NUMBER	PINOUT STYLE "A" (SEE TABLE 10)	PINOUT STYLE "B" (SEE TABLE 10)
1	SDA	SCL
2	GND	GND
3	SCL	SDA

Table 13. 4-Pin Male-to-Male Shrouded and Keyed Adapter (Optional; Eases Creation of Adapter Cables, if Deviating from Recommended Connectors/Connector Pinouts); Interfaces to DC2086 Cables

VENDOR	PART NUMBER	WEBSITE
Hirose	DF3-4EP-2A	www.hirose.com, www.hirose.co.jp

APPLICATIONS INFORMATION

LTpowerPlay: AN INTERACTIVE GUI FOR DIGITAL POWER SYSTEM MANAGEMENT

LTpowerPlay is a powerful Windows-based development environment that supports Analog Devices, digital power ICs including the LTM4686B. The software supports a variety of different tasks. LTpowerPlay can be used to evaluate Analog Devices, ICs by connecting to a demo board or the user application. LTpowerPlay can also be used in an offline mode (with no hardware present) in order to build multiple IC configuration files that can be saved and reloaded at a later time. LTpowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program or tweak the power system or to diagnose power issues when bringing up rails. LTpowerPlay utilizes Analog Devices, USB-to-I^{2}C/SMBus/PMBus controller to communication with one of the many potential targets including the DC3089 (single LTM4686B), DC1811 (single LTM4676A) or DC1989B (dual, triple, quad LTM4676A) demo boards, or a customer target system. The software also provides an automatic update feature to keep the revisions current with the latest set of device drivers and documentation. A great deal of context sensitive help is available with LTpowerPlay along with several tutorial demos.

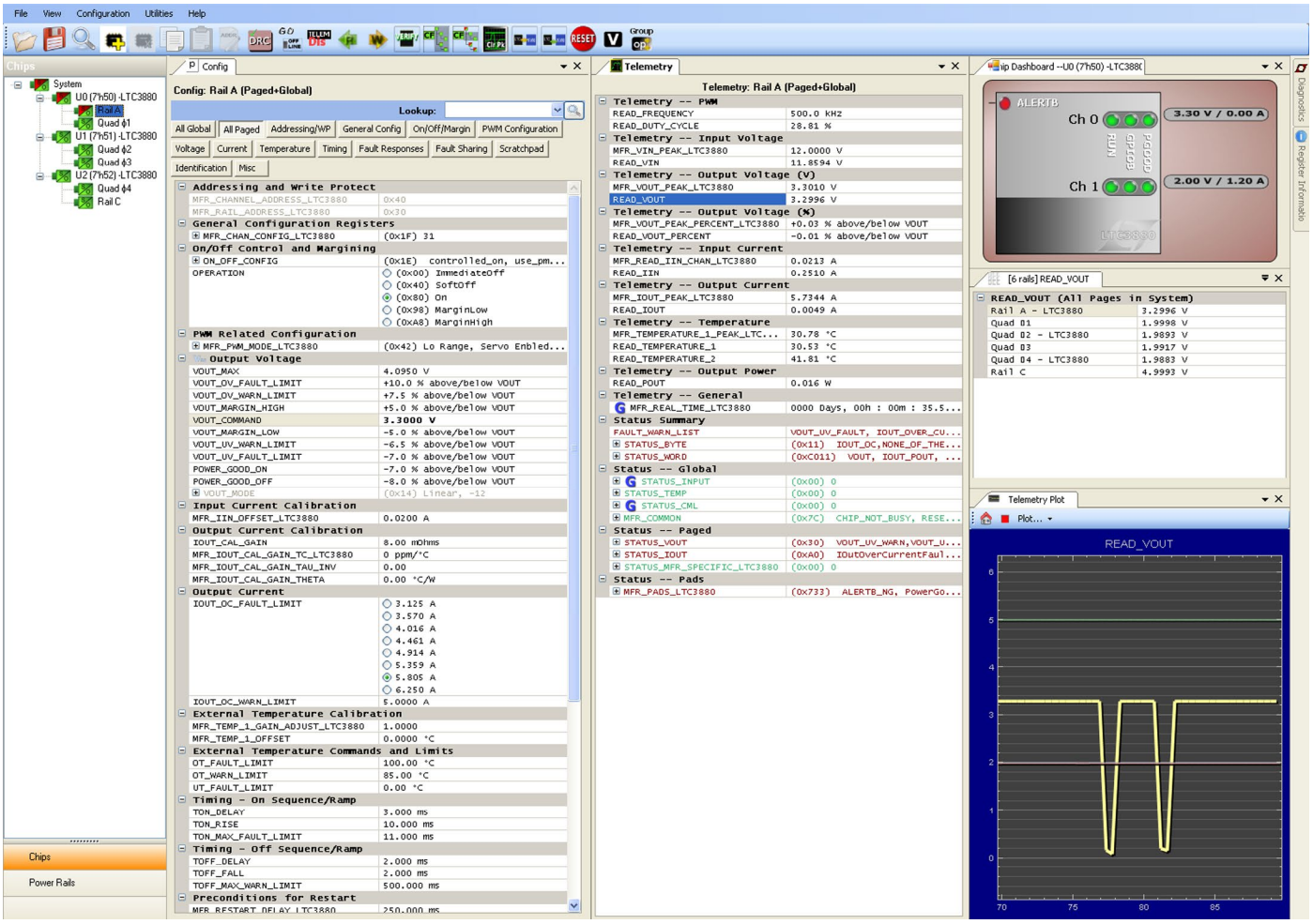


Figure 6. LTpowerPlay

APPLICATIONS INFORMATION

PMBus COMMUNICATION AND COMMAND PROCESSING

The LTM4686B has one deep buffer to hold the last data written for each supported command prior to processing as shown in Figure 7; Write Command Data Processing. When the part receives a new command from the bus, it copies the data into the Write Command Data Buffer, indicates to the internal processor that this command data needs to be fetched, and converts the command to its internal format so that it can be executed.

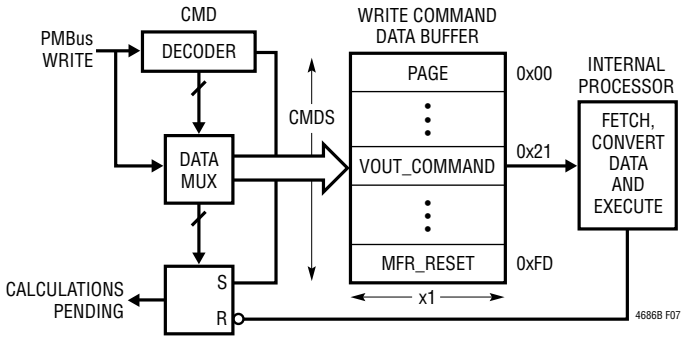


Figure 7. Write Command Data Processing

Two distinct parallel blocks manage command buffering and command processing (fetch, convert, and execute) to ensure the last data written to any command is never lost. Command data buffering handles incoming PMBus writes by storing the command data to the Write Command Data Buffer and marking these commands for future processing. The internal processor runs in parallel and handles the sometimes slower task of fetching, converting and executing commands marked for processing.

Some computationally intensive commands (e.g., timing parameters, temperatures, voltages and currents) have internal processor execution times that may be long relative to PMBus timing. If the part is busy processing a command, and new command(s) arrive, execution may be delayed or processed in a different order than received. The part indicates when internal calculations are in process via bit 5 of MFR_COMMON ('calculations not pending'). When the part is busy calculating, bit 5 is cleared. When this bit is set, the part is ready for another command. An example polling loop is provided in Figure 7 which ensures that commands are processed in order while simplifying error handling routines.

When the part receives a new command while it is busy, it will communicate this condition using standard PMBus protocol. Depending on part configuration it may either NACK the command or return all ones (0xFF) for reads. It may also generate a BUSY fault and $\overline{\text{ALERT}}$ notification, or stretch the SCL clock low. For more information refer to PMBus Specification v1.2, Part II, Section 10.8.7 and SMBus v2.0 section 4.3.3. Clock stretching can be enabled by asserting bit 1 of MFR_CONFIG_ALL. Clock stretching will only occur if enabled and the bus communication speed exceeds 100kHz.

PMBus busy protocols are well accepted standards, but can make writing system level software somewhat complex. The part provides three 'hand shaking' status bits which reduce complexity while enabling robust system level communication.

The three hand shaking status bits are in the MFR_COMMON register. When the part is busy executing an internal operation, it will clear bit 6 of MFR_COMMON ('module not busy'). When the part is busy specifically because it is in a transitional V_{OUT} state (margining hi/lo, power off/on, moving to a new output voltage set point, etc.) it will clear bit 4 of MFR_COMMON ('output not in transition'). When internal calculations are in process, the part will clear bit 5 of MFR_COMMON ('calculations not pending'). These three status bits can be polled with a PMBus read byte of the MFR_COMMON register until all three bits are set. A command immediately following the status bits being set will be accepted without NACKing or generating a BUSY fault/$\overline{\text{ALERT}}$ notification. The part can NACK commands for other reasons, however, as required by the PMBus spec (for instance, an invalid command or data). An example of a robust command write algorithm for the VOUT_COMMAND*n* register is provided in Figure 8.

```
// wait until bits 6, 5, and 4 of MFR_COMMON are all set
do
{
      mfrCommonValue = PMBUS_READ_BYTE(0xEF);
      partReady = (mfrCommonValue & 0x68) == 0x68;
}while (!partReady)

// now the part is ready to receive the next command
PMBUS_WRITE_WORD(0x21, 0x2000); //write VOUT_COMMAND to 2V
```

4686B F08

Figure 8. Example of a Command Write of VOUT_COMMAND

APPLICATIONS INFORMATION

It is recommended that all command writes (write byte, write word, etc.) be preceded with a polling loop to avoid the extra complexity of dealing with busy behavior and unwanted $\overline{\text{ALERT}}$ notification. A simple way to achieve this is by creating SAFE_WRITE_BYTE() and SAFE_WRITE_WORD() subroutines. The above polling mechanism allows one's software to remain clean and simple while robustly communicating with the part. For a detailed discussion of these topics and other special cases please refer to the Analog Devices Application Note section.

When communicating using bus speeds at or below 100kHz, the polling mechanism shown here provides a simple solution that ensures robust communication without clock stretching. At bus speeds in excess of 100kHz, it is strongly recommended that the part be configured to enable clock stretching. This requires a PMBus master that supports clock stretching. System software that detects and properly recovers from the standard PMBus NACK/BUSY faults as described in the PMBus Specification v1.2, Part II, Section 10.8.7 is required to communicate above 100kHz without clock stretching. Clock stretching will not extend the PMBus speed beyond the specified 400kHz.

THERMAL CONSIDERATIONS AND OUTPUT CURRENT DERATING

The thermal resistances reported in the Pin Configuration section of this data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder

APPLICATIONS INFORMATION

joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 9; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4686B, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4686B and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 and JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4686B with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves provided in later sections of this data sheet, along with well-correlated JESD51-12-defined θ values provided in the Pin Configuration section of this data sheet.

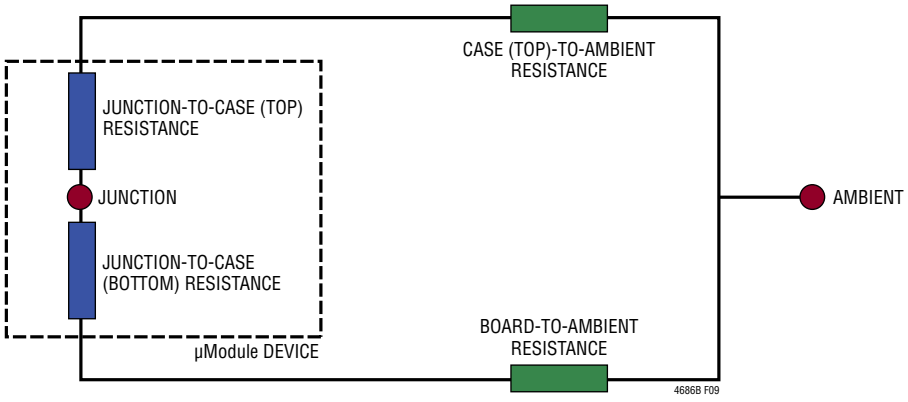


Figure 9. Graphical Representation of JESD51-12 Thermal Coefficients

APPLICATIONS INFORMATION

The power loss curves in Figure 10 to Figure 13 can be used in coordination with the load current derating curves in Figure 14 to Figure 27 for calculating an approximate θ_{JA} thermal resistance for the LTM4686B with various heat sinking and air flow conditions. These thermal resistances represent demonstrated performance of the LTM4686B on DC3089A hardware; a 4-layer FR4 PCB measuring 99mm × 133mm × 1.6mm using outer and inner copper weights of 2oz and 1oz, respectively. The power loss curves are taken at room temperature, and are increased with multiplicative factors with ambient temperature. These approximate factors are listed in Table 14. (Compute the factor by interpolation, for intermediate temperatures.) The derating curves are plotted with the LTM4686B's paralleled outputs initially sourcing up to 28A and the ambient temperature at 25°C. The output voltages are 0.6V, 1V, 1.8V, and 3.3V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without air flow, and with and without a heat sink attached with thermally conductive adhesive tape. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power while increasing ambient temperature.

The decreased output current decreases the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 22, the load current is derated to 24A at 70°C ambient with no airflow and no heat sink and the room temperature (25°C) power loss for this $3.3V_{IN}$ to $1.8V_{OUT}$ at $24A_{OUT}$ condition is ~5W. A ~5.75W loss is calculated by multiplying the ~5W room temperature loss from the $3.3V_{IN}$ to $1.8V_{OUT}$ power loss curve at 24A (Figure 12), with the 1.15 multiplying factor at 70°C ambient (from Table 14). If the 70°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 50°C divided by ~5.75W yields a thermal resistance, θ_{JA}, of ~8.9°C/W—in good agreement with Table 17. Table 15, Table 16, Table 17 and Table 18 provide equivalent thermal resistances for 0.6V, 1V, 1.8V and 3.3V outputs with and without air flow and heat sinking. The derived thermal resistances in Table 15, Table 16, Table 17 and Table 18 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with ambient temperature multiplicative factors from Table 14.

Table 14. Power Loss Multiplicative Factors vs Ambient Temperature

AMBIENT TEMPERATURE	POWER LOSS MULTIPLICATIVE FACTOR
Up to 40°C	1.00
50°C	1.05
60°C	1.10
70°C	1.15
80°C	1.20
90°C	1.25
100°C	1.30
110°C	1.35
120°C	1.40

APPLICATIONS INFORMATION-DERATING CURVES

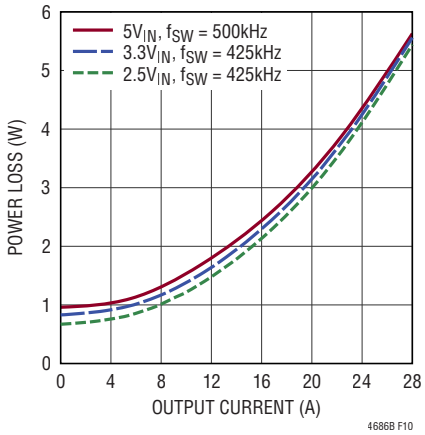


Figure 10. 0.6V_{OUT} Power Loss Curves

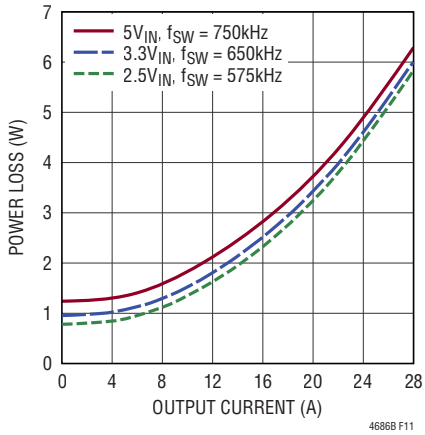


Figure 11. 1V_{OUT} Power Loss Curves

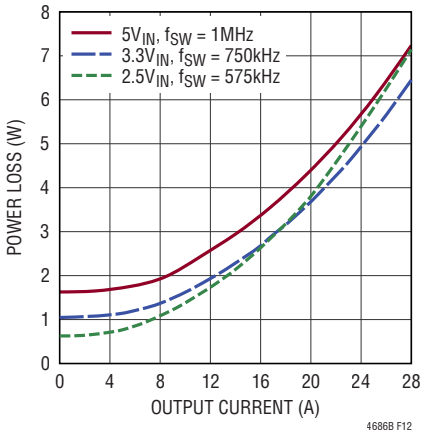


Figure 12. 1.8V_{OUT} Power Loss Curves

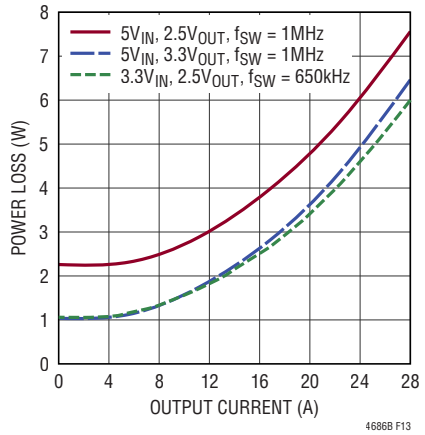


Figure 13. 3.3V_{OUT} and 2.5V_{OUT} Power Loss Curves

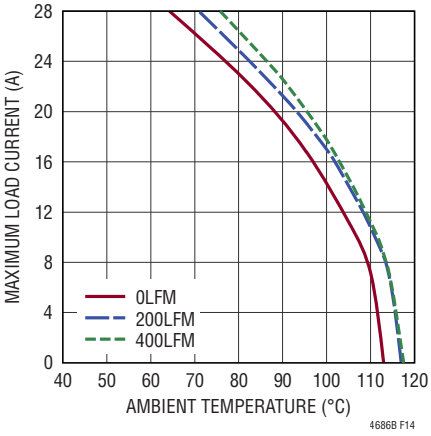


Figure 14. 3.3V to 0.6V Derating Curve, No Heat Sink

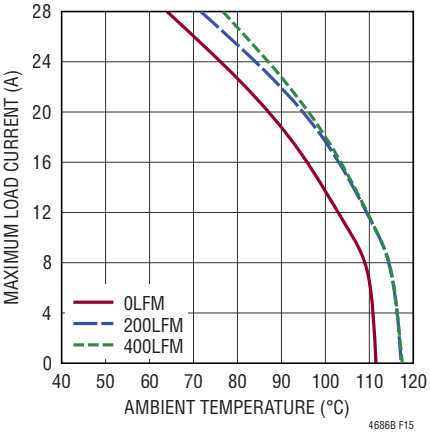


Figure 15. 5V to 0.6V Derating Curve, No Heat Sink

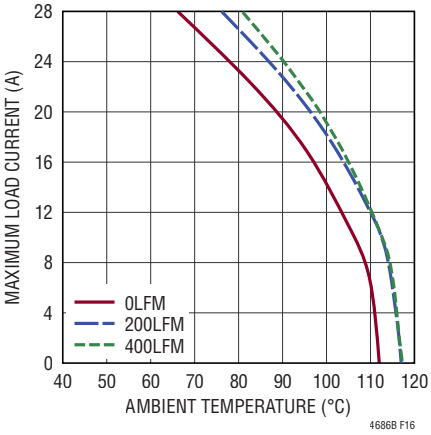


Figure 16. 3.3V to 0.6V Derating Curve with Heat Sink

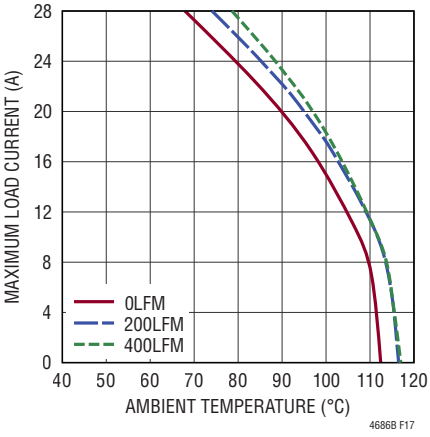


Figure 17. 5V to 0.6V Derating Curve with Heat Sink

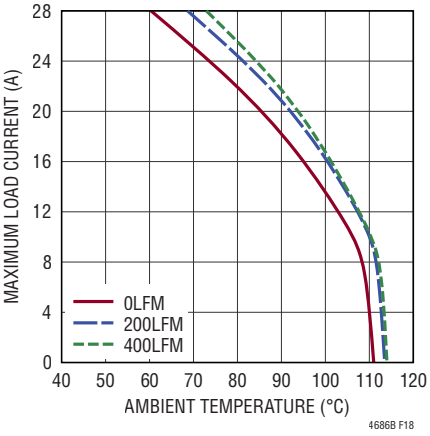


Figure 18. 3.3V to 1V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION-DERATING CURVES

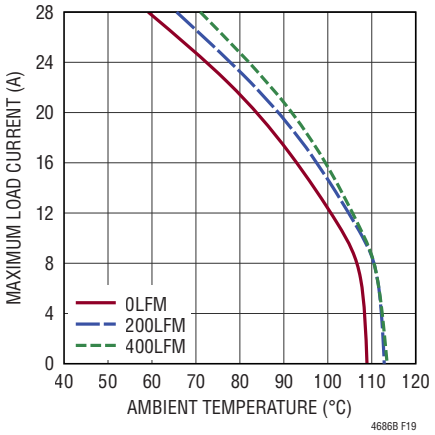


Figure 19. 5V to 1V Derating Curve, No Heat Sink

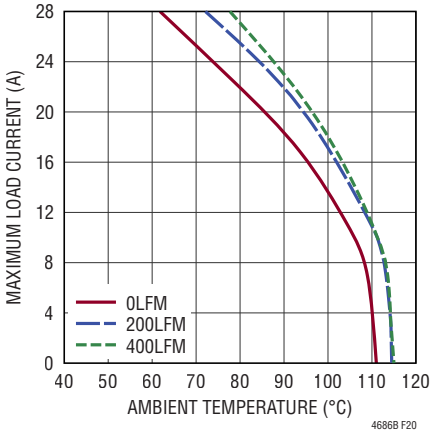


Figure 20. 3.3V to 1V Derating Curve with Heat Sink

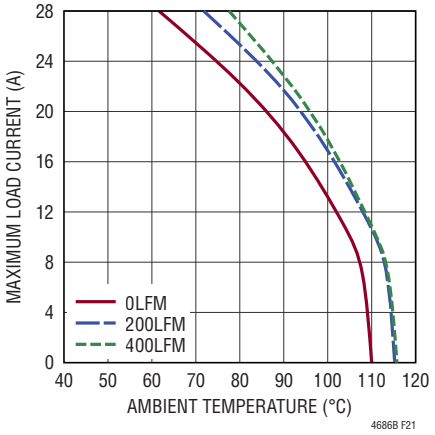


Figure 21. 5V to 1V Derating Curvewith Heat Sink

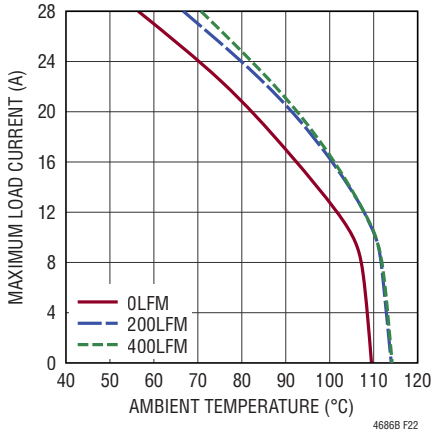


Figure 22. 3.3V to 1.8V Derating Curve, No Heat Sink

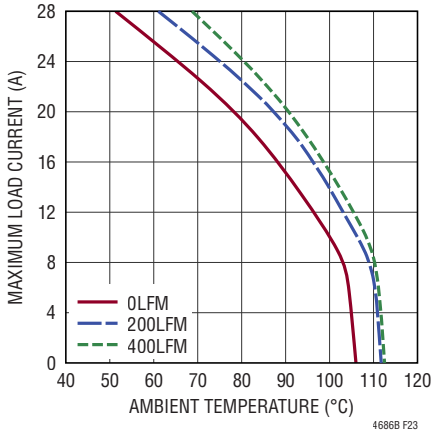


Figure 23. 5V to 1.8V Derating Curve, No Heat Sink

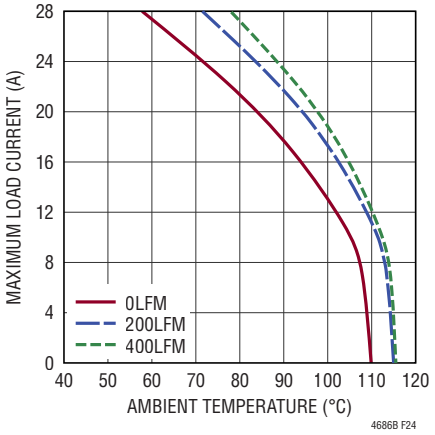


Figure 24. 3.3V to 1.8V Derating Curve with Heat Sink

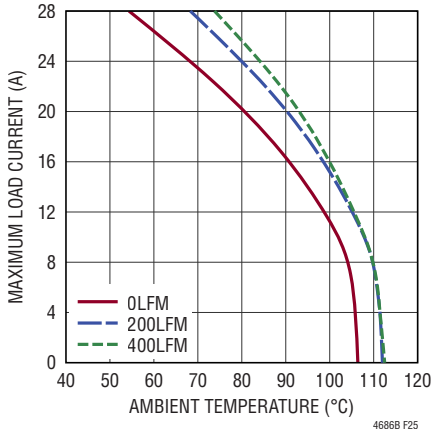


Figure 25. 5V to 1.8V Derating Curve with Heat Sink

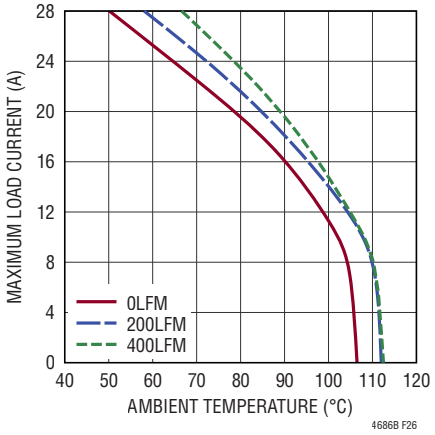


Figure 26. 5V to 3.3V Derating Curve, No Heat Sink

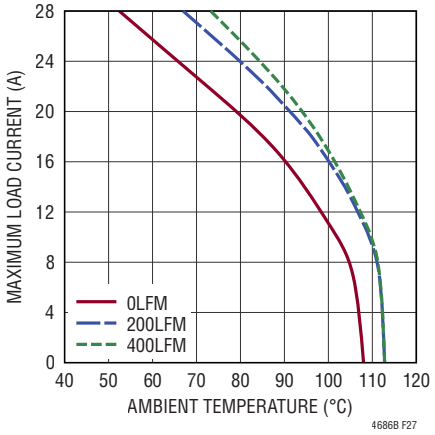


Figure 27. 5V to 3.3V Derating Curve with Heat Sink

APPLICATIONS INFORMATION

Table 15. 0.6V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 14, Figure 15	3.3, 5	Figure 10	0	None	8.5
Figure 14, Figure 15	3.3, 5	Figure 10	200	None	7.3
Figure 14, Figure 15	3.3, 5	Figure 10	400	None	6.7
Figure 16, Figure 17	3.3, 5	Figure 10	0	BGA Heat Sink	8.0
Figure 16, Figure 17	3.3, 5	Figure 10	200	BGA Heat Sink	6.7
Figure 16, Figure 17	3.3, 5	Figure 10	400	BGA Heat Sink	6.3

Table 16. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 18, Figure 19	3.3, 5	Figure 11	0	None	8.4
Figure 18, Figure 19	3.3, 5	Figure 11	200	None	7.1
Figure 18, Figure 19	3.3, 5	Figure 11	400	None	6.4
Figure 20, Figure 21	3.3, 5	Figure 11	0	BGA Heat Sink	8.0
Figure 20, Figure 21	3.3, 5	Figure 11	200	BGA Heat Sink	6.4
Figure 20, Figure 21	3.3, 5	Figure 11	400	BGA Heat Sink	5.9

Table 17. 1.8V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 22, Figure 23	3.3, 5	Figure 12	0	None	8.7
Figure 22, Figure 23	3.3, 5	Figure 12	200	None	7.0
Figure 22, Figure 23	3.3, 5	Figure 12	400	None	6.2
Figure 24, Figure 25	3.3, 5	Figure 12	0	BGA Heat Sink	8.3
Figure 24, Figure 25	3.3, 5	Figure 12	200	BGA Heat Sink	6.2
Figure 24, Figure 25	3.3, 5	Figure 12	400	BGA Heat Sink	5.6

Table 18. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 26	5	Figure 13	0	None	10.1
Figure 26	5	Figure 13	200	None	8.1
Figure 26	5	Figure 13	400	None	7.4
Figure 27	5	Figure 13	0	BGA Heat Sink	9.8
Figure 27	5	Figure 13	200	BGA Heat Sink	6.9
Figure 27	5	Figure 13	400	BGA Heat Sink	6.0

Table 19. Heat Sink and Thermally Conductive Adhesive Tape Part Numbers

MANUFACTURER	PART NUMBER	WEBSITE
Cool Innovations	3-0504035UT411	www.coolinnovations.com
Chomerics	T411	www.chomerics.com

APPLICATIONS INFORMATION

Table 20. LTM4686B Channel Output Voltage Response vs Component Matrix. 7A Load-Stepping at 7A/µs. Typical Measured Values

C_{OUTH} VENDORS	PART NUMBER	C_{OUTL} VENDORS	PART NUMBER
AVX	12106D107MAT2A (100µF, 6.3V, 1210 Case Size)	Panasonic POSCAP	6TPF330M9L (330µF, 6.3V, 9mΩ ESR, D3L Case Size)
Murata	GRM32ER60J107ME20L (100µF, 6.3V, 1210 Case Size)	Panasonic POSCAP	6TPD470M (470µF, 6.3V, 10mΩ ESR, D4D Case Size)
Taiyo Yuden	JMK325BJ107MM-T (100µF, 6.3V, 1210 Case Size)	Panasonic POSCAP	2R5TPE470M9** (470µF, 2.5V, 9mΩ ESR, D2E Case Size)
TDK	C3225X5R0J107MT (100µF, 6.3V, 1210 Case Size)	Panasonic POSCAP	6TPF470MAH (470µF, 6.3V, 10mΩ ESR, D4 Case Size)

V_{OUTn} (V)	V_{INn} (V)	REF. CIRCUIT*	C_{OUTHn} CERAMIC OUTPUT CAP (µF)	C_{OUTLn} BULK OUTPUT CAP (µF)	CONNECT COMP*na* TO COMP*nb*? (INTERNAL LOOP COMP)	R_{THn} (EXT LOOP COMP) (kΩ)	C_{THn} (EXT LOOP COMP) (nF)	f_{SW} (kHz)	$F_{SWPHCFG}$ PIN-STRAP, RESISTOR TO SGND (TABLE 4) (kΩ)	$V_{OUTn\ CFG}$ PIN-STRAP RESISTOR TO SGND (TABLE 2) (kΩ)	$V_{TRIMnCFG}$ PIN-STRAP, RESISTOR TO SGND (TABLE 3) (kΩ)	TRANSIENT DROOP (0A TO 7A) (mV)	PK-PK DEVIATION (0A TO 7A TO 0A) (mV)	RECOVERY TIME (µs)
0.9	5	Test Ckt. 1	100 ×4	None	Yes, cf. Figure 62	N/A	N/A	650	12.7	1.65	None	36	75	80
0.9	5	Test Ckt. 1	100 ×3	470	Yes, cf. Figure 62	N/A	N/A	650	12.7	1.65	None	35	70	45
1	5	Test Ckt. 1	100 ×4	None	Yes, cf. Figure 62	N/A	N/A	750	10.7	2.43	0	35	77	80
1	5	Test Ckt. 1	100 ×3	470	Yes, cf. Figure 62	N/A	N/A	750	10.7	2.43	0	32	67	60
1.2	5	Test Ckt. 1	100 ×4	None	Yes, cf. Figure 62	N/A	N/A	1000	None	3.24	0	35	76	60
1.2	5	Test Ckt. 1	100 ×3	470	Yes, cf. Figure 62	N/A	N/A	1000	None	3.24	0	31	68	60
1.5	5	Test Ckt. 1	100 ×4	None	Yes, cf. Figure 62	N/A	N/A	1000	None	4.22	None	36	74	60
1.5	5	Test Ckt. 1	100 ×3	470	Yes, cf. Figure 62	N/A	N/A	1000	None	4.22	None	31	67	60
1.8	5	Test Ckt. 1	100 ×4	None	Yes, cf. Figure 62	N/A	N/A	1000	None	6.34	0	37	79	60
1.8	5	Test Ckt. 1	100 ×3	470	Yes, cf. Figure 62	N/A	N/A	1000	None	6.34	0	31	68	60
2.5	5	Test Ckt. 1	100 ×4	None	Yes, cf. Figure 62	N/A	N/A	1000	None	10.7	None	34	77	70
2.5	5	Test Ckt. 1	100 ×3	470	Yes, cf. Figure 62	N/A	N/A	1000	None	10.7	None	29	68	70
3.3	5	Test Ckt. 1	100 ×4	None	Yes, cf. Figure 62	N/A	N/A	1000	None	22.6	None	79	170	70
3.3	5	Test Ckt. 1	100 ×3	470	Yes, cf. Figure 62	N/A	N/A	1000	None	22.6	None	64	135	70

*For all conditions: C_{INH} input capacitance is 10µF × 2, per channel (V_{IN0}, V_{IN1}). C_{INL} bulk input capacitance of 150µF is optional if V_{IN} has very low input impedance.

**2.5V-rated output capacitor is suitable for output voltages up to 1.8V.

APPLICATIONS INFORMATION

EMI PERFORMANCE

The SW*n* pin provides access to the midpoint of the power MOSFETs in LTM4686B's power stages.

Connecting an optional series RC network from SW*n* to GND can dampen high frequency (~30MHz+) switch node ringing caused by parasitic inductances and capacitances in the switched-current paths. The RC network is called a snubber circuit because it dampens (or "snubs") the resonance of the parasitics, at the expense of higher power loss.

To use a snubber, choose first how much power to allocate to the task and how much PCB real estate is available to implement the snubber. For example, if PCB space allows a low inductance 1W resistor to be used—derated conservatively to 600mW (P_{SNUB})—then the capacitor in the snubber network (C_{SW}) is computed by Equation 10.

$$C_{SW} = \frac{P_{SNUB}}{V_{INn(MAX)}^2 \bullet f_{SW}} \quad (10)$$

where $V_{INn(MAX)}$ is the maximum input voltage that the input to the power stage (V_{INn}) will see in the application, and f_{SW} is the DC/DC converter's switching frequency of operation. C_{SW} should be NPO, C0G or X7R-type (or better) material.

The snubber resistor (R_{SW}) value is then given by Equation 11.

$$R_{SW} = \sqrt{\frac{5nH}{C_{SW}}} \quad (11)$$

The snubber resistor should be low ESL and capable of withstanding the pulsed currents present in snubber circuits. A value between 0.7Ω and 4.2Ω is normal.

SAFETY CONSIDERATIONS

The LTM4686B modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

The fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage, thus the internal bottom MOSFET will turn on indefinitely trying to protect the load. Under this fault condition, the input voltage will source very large currents to ground through the failed internal top MOSFET and enabled internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation. The device does support over current and overtemperature protection.

LAYOUT CHECKLIST/EXAMPLE

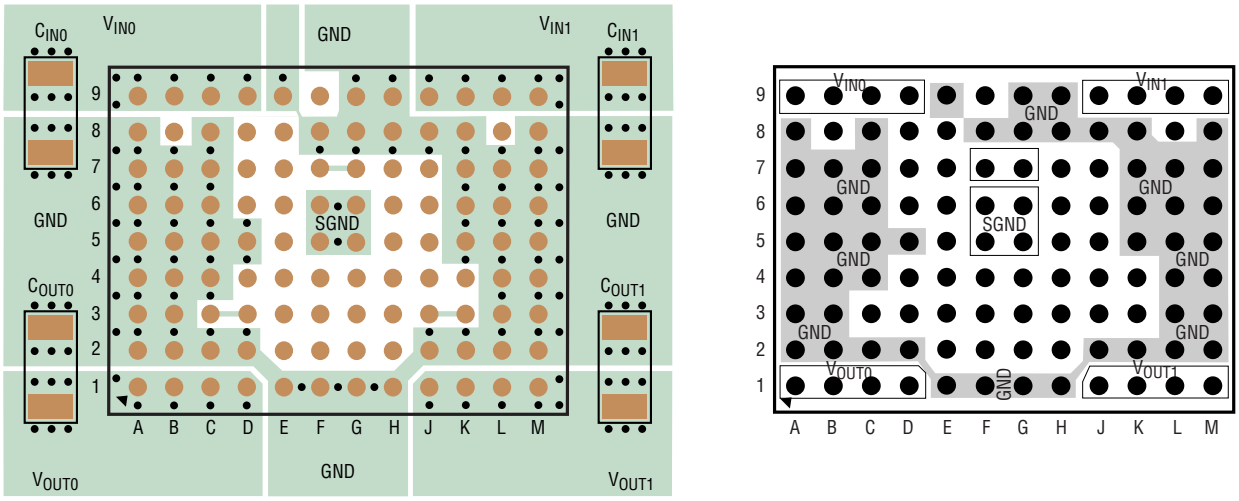
The high integration of LTM4686B makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{INn}, GND and V_{OUTn}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{INn}, GND and V_{OUTn} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

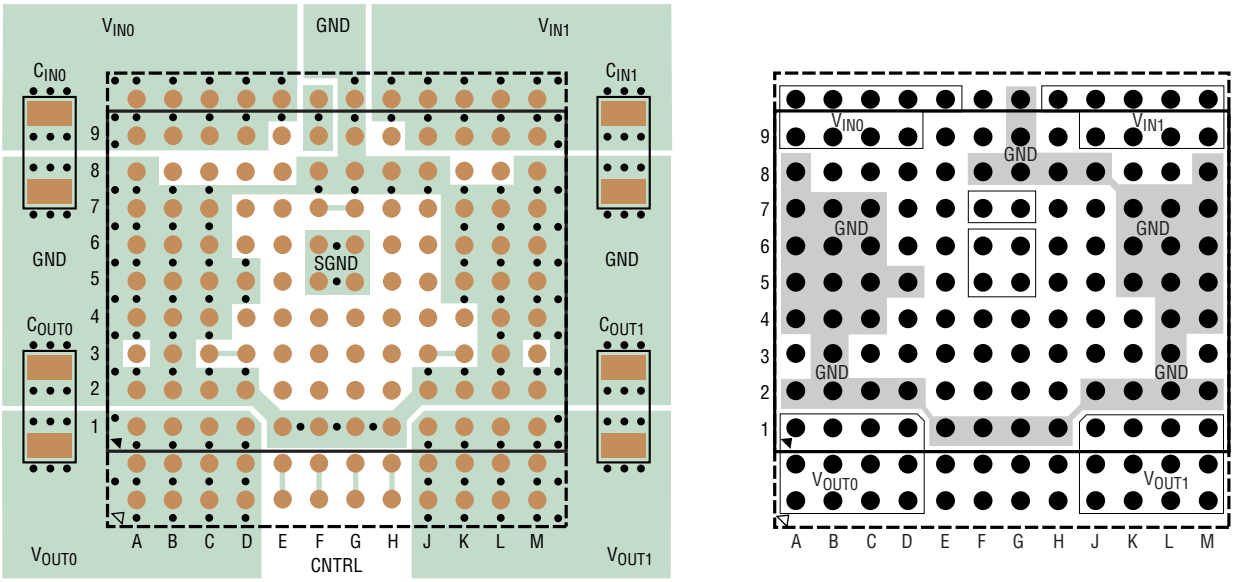
APPLICATIONS INFORMATION

- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4686B.
- For parallel modules, tie the V_{OUTn}, $V_{OSNS0}^{+}/V_{OSNS}^{-}$ and/or V_{OSNS1}/SGND voltage-sense differential pair lines, RUN*n*, $\overline{GPIO}$*n*, COMP*n*a, SYNC and SHARE_CLK pins together—as shown in Figure 32.
- Bring out test points on the signal pins for monitoring.

Figure 28a shows a good example of the LTM4686B's recommended layout. For flexibility, the LTM4686B is drop-in pin-compatible to its taller, larger dual 13A LTM4676A and dual 18A LTM4677 sibling modules—as seen in the layout recommended by Figure 28b.



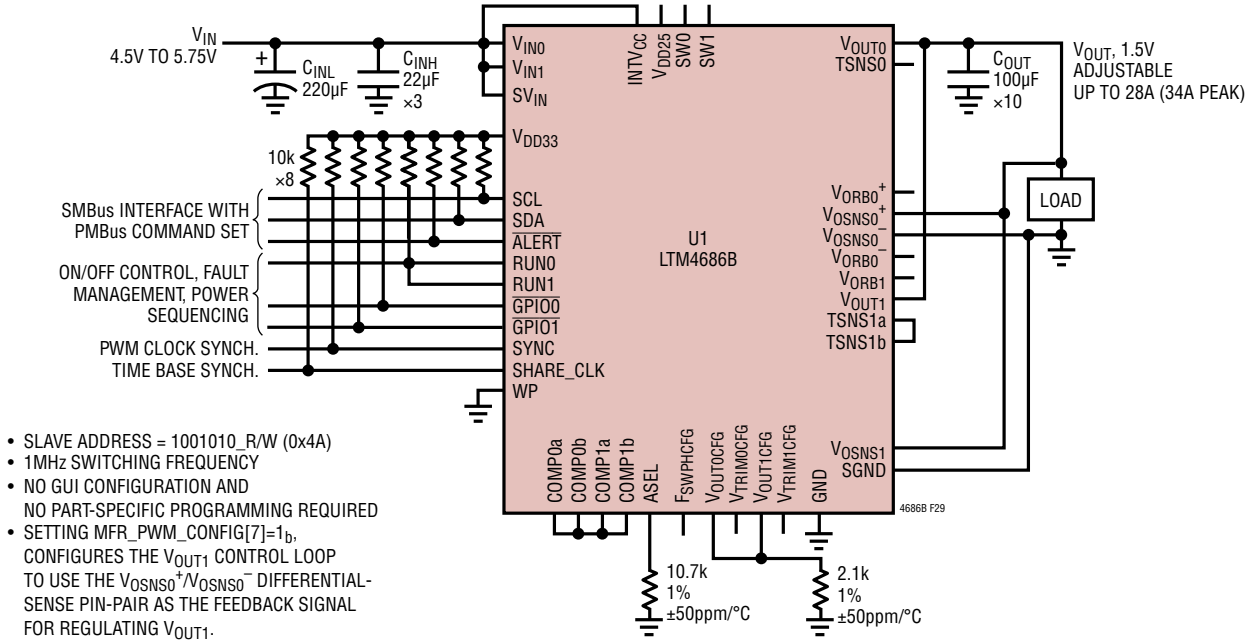
(a) PCB Layout for LTM4686B, LTM4686 and LTM4675, Package Top View



(b) PCB Layout to Accommodate Any of LTM4686B or LTM4686 or LTM4675 or LTM4676A or LTM4677 Modules 4686B F28ab

Figure 28. Recommended PCB Layout Package Top View

TYPICAL APPLICATIONS



- SLAVE ADDRESS = 1001010_R/W (0x4A)
- 1MHz SWITCHING FREQUENCY
- NO GUI CONFIGURATION AND NO PART-SPECIFIC PROGRAMMING REQUIRED
- SETTING MFR_PWM_CONFIG[7]=1_b, CONFIGURES THE V_{OUT1} CONTROL LOOP TO USE THE V_{OSNS0}^+/V_{OSNS0}^- DIFFERENTIAL-SENSE PIN-PAIR AS THE FEEDBACK SIGNAL FOR REGULATING V_{OUT1}.

Figure 29. 28A, 1.5V Output DC/DC µModule Regulator with I²C/SMBus/PMBus Serial Interface

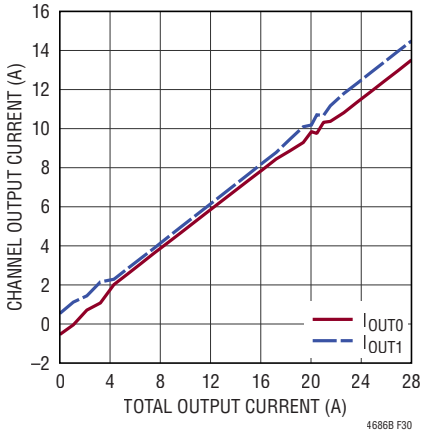


Figure 30. Current Sharing Performance of the LTM4686B's Channels at $5V_{IN}$

TYPICAL APPLICATIONS

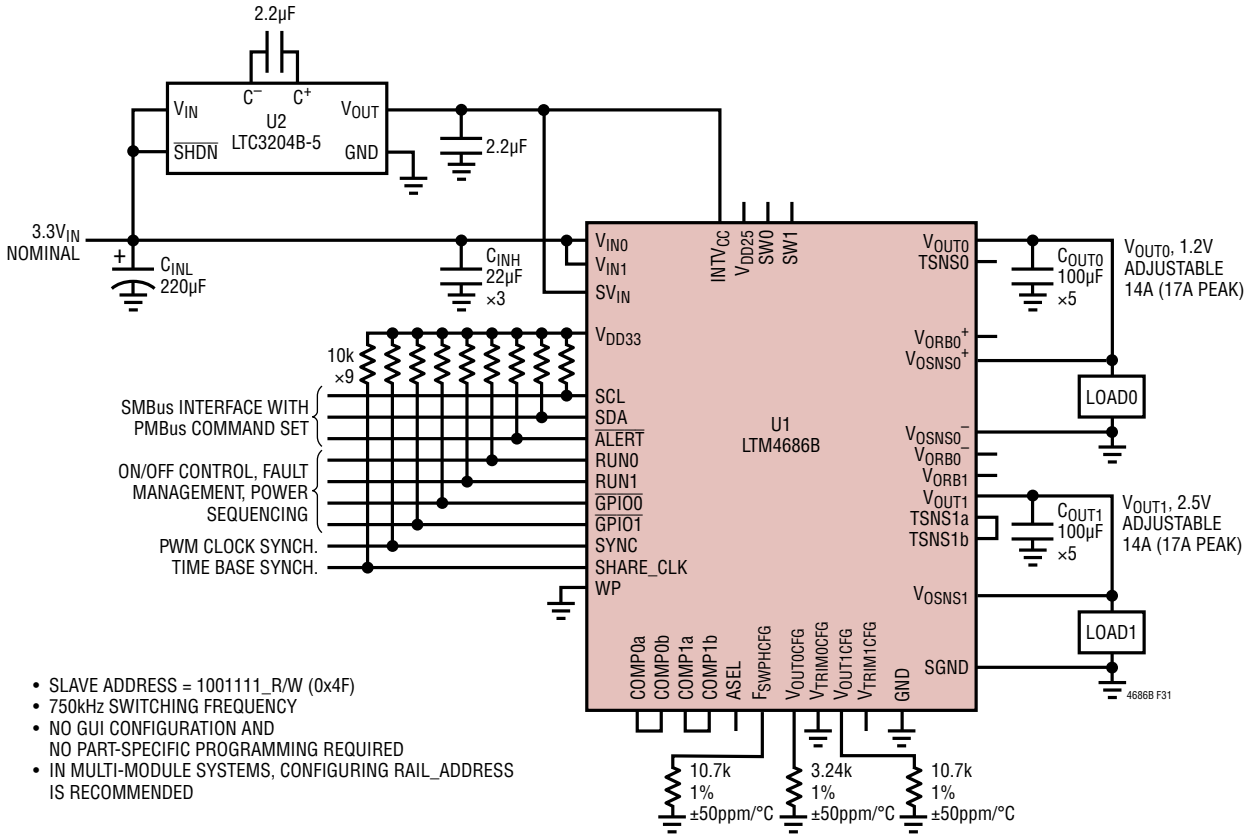


Figure 31. 14A, 1.2V and 2.5V Outputs Generated from 3.3V Power Input and Providing I²C/SMBus/PMBus Serial Interface

TYPICAL APPLICATIONS

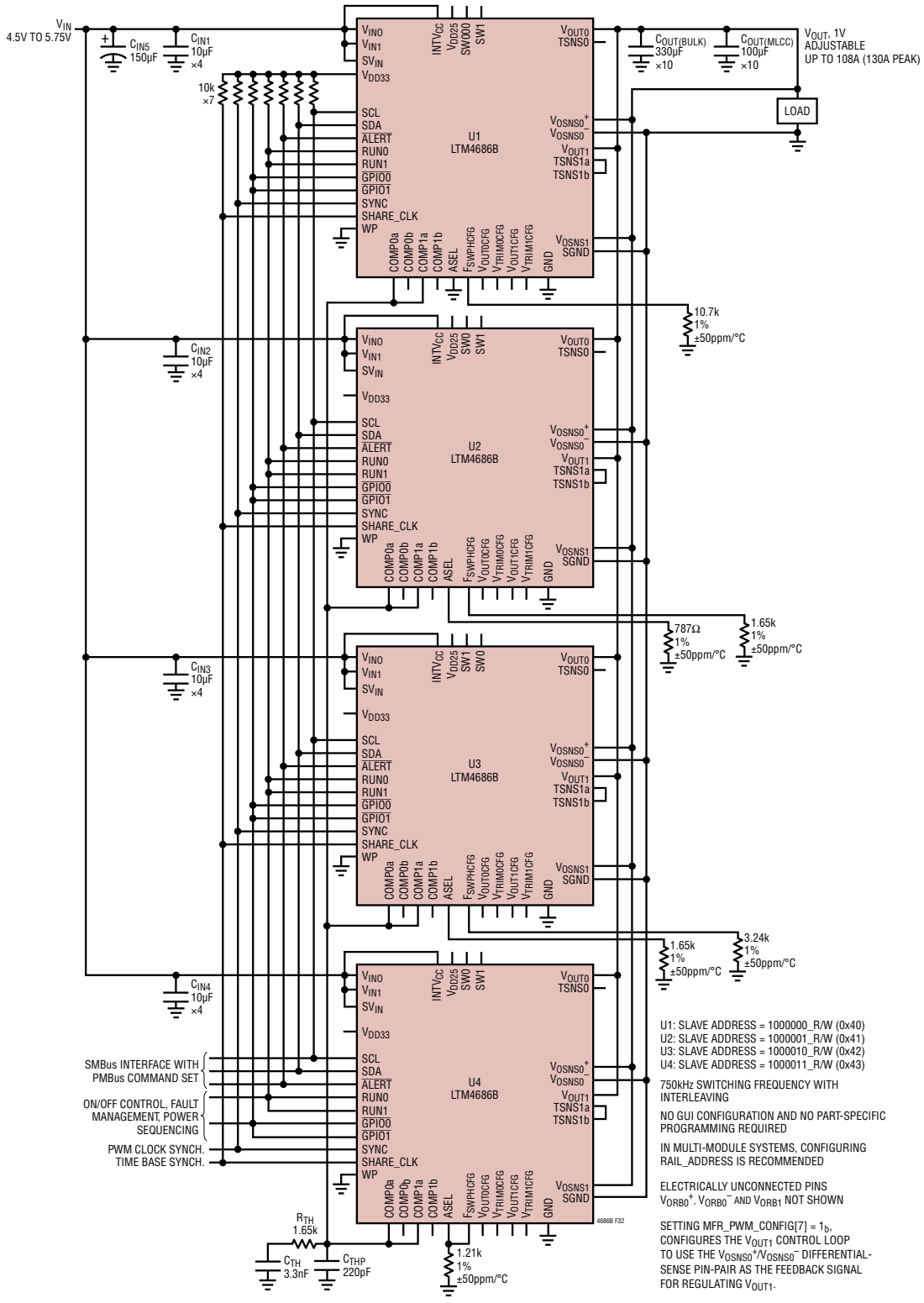
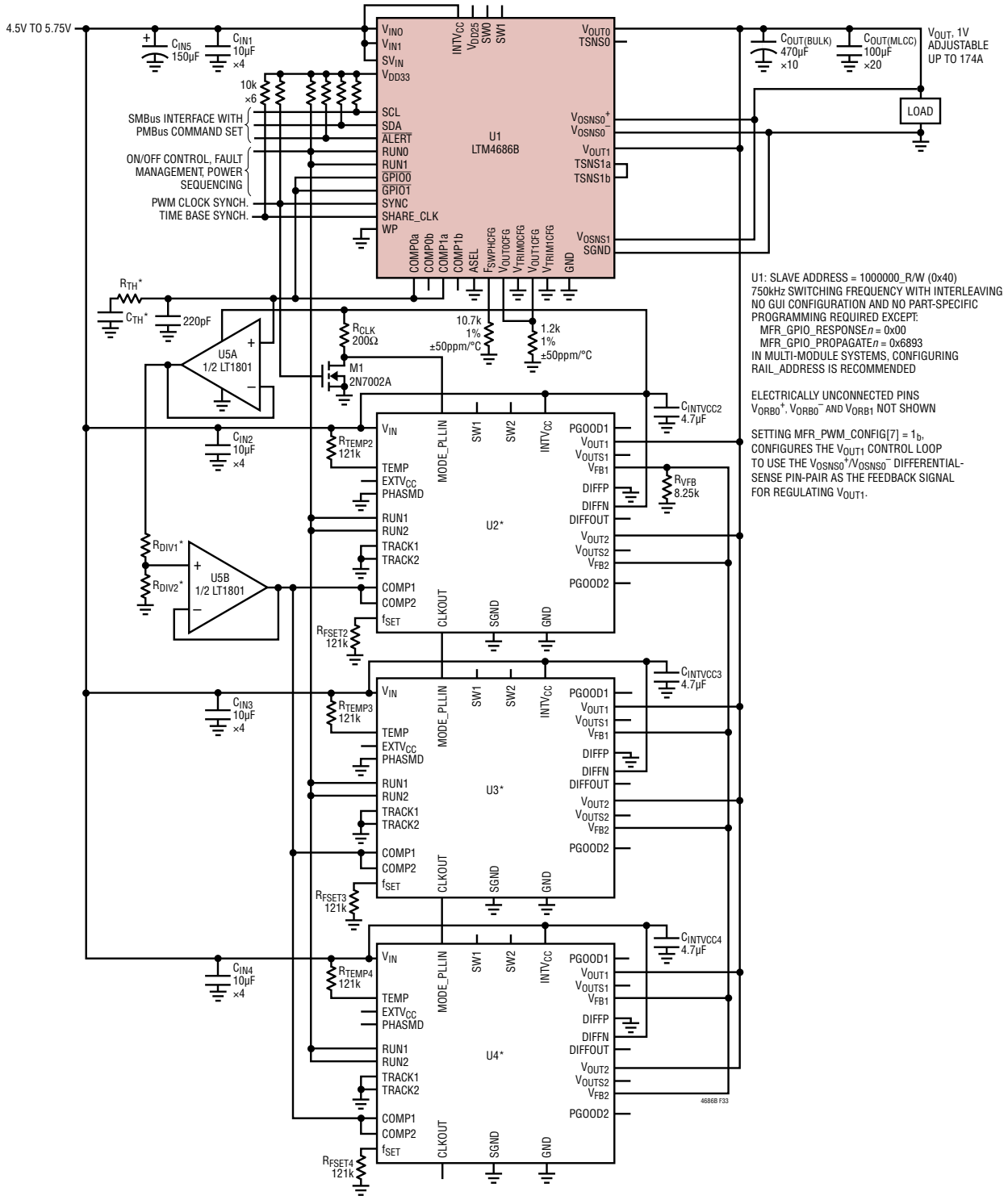


Figure 32. Four Paralleled LTM4686B Producing 1V$_{OUT}$ at Up to 108A. Integrated Power System Management Features Accessible Over 2-Wire I^{2}C/SMBus/PMBus Serial Interface. Evaluated on DC1989B-C, Custom-Stuffed with LTM4686B Modules

TYPICAL APPLICATIONS



U1: SLAVE ADDRESS = 1000000_R/W (0x40)
750kHz SWITCHING FREQUENCY WITH INTERLEAVING
NO GUI CONFIGURATION AND NO PART-SPECIFIC PROGRAMMING REQUIRED EXCEPT:
MFR_GPIO_RESPONSE*n* = 0x00
MFR_GPIO_PROPAGATE*n* = 0x6893
IN MULTI-MODULE SYSTEMS, CONFIGURING RAIL_ADDRESS IS RECOMMENDED

ELECTRICALLY UNCONNECTED PINS V_{ORB0}^+, V_{ORB0}^- AND V_{ORB1} NOT SHOWN

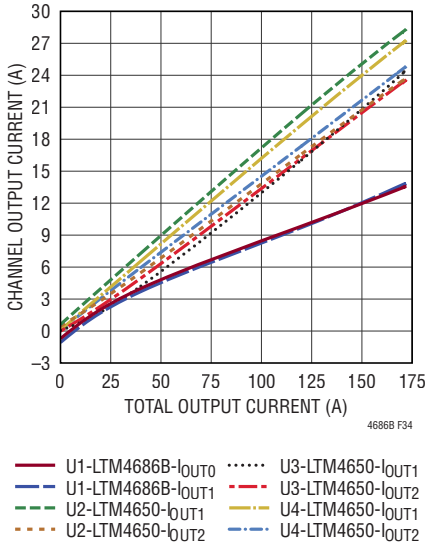
SETTING MFR_PWM_CONFIG[7] = 1_b, CONFIGURES THE V_{OUT1} CONTROL LOOP TO USE THE V_{OSNS0}^+/V_{OSNS0}^- DIFFERENTIAL-SENSE PIN-PAIR AS THE FEEDBACK SIGNAL FOR REGULATING V_{OUT1}.

*STUFFING OPTIONS

DEMO BOARD	OUTPUT CURRENT	U1	U2, U3, U4	R_{DIV1}	R_{DIV2}	R_{TH}	C_{TH}
DC2481A-B	UP TO 174A	LTM4686B	LTM4650	1.05k	10k	2k	6.8nF

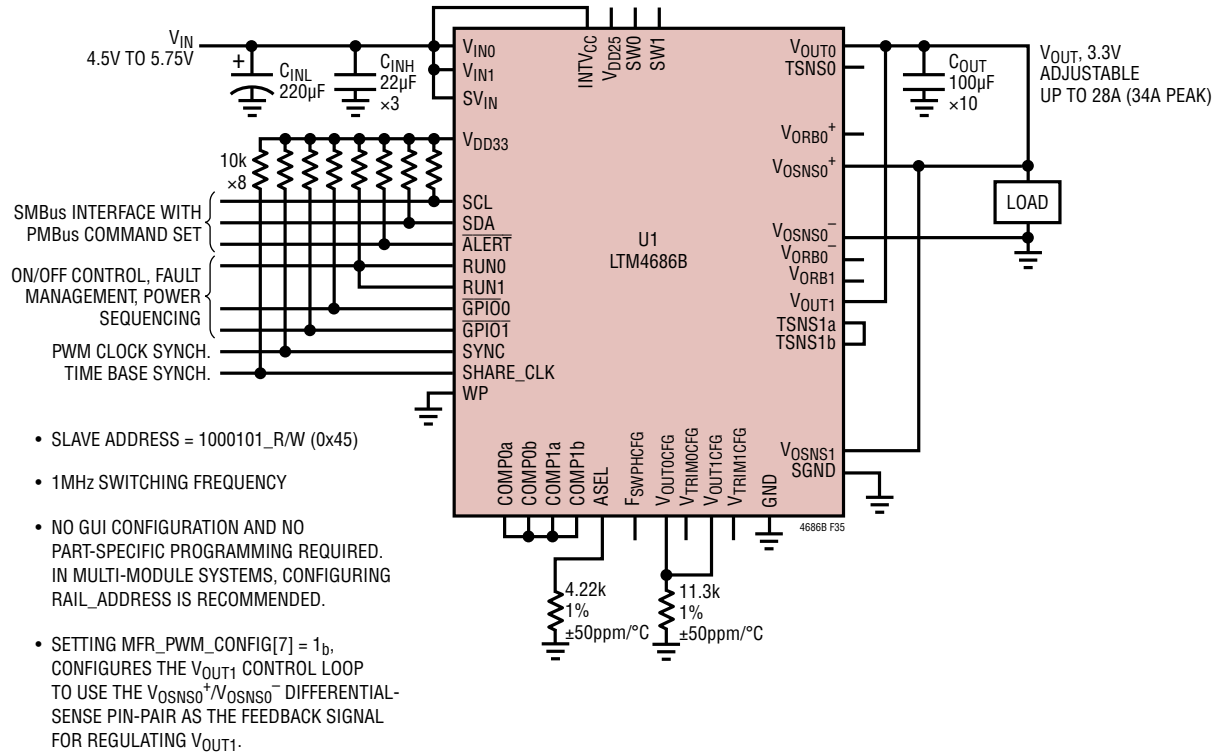
Figure 33. One LTM4686B Operating In Parallel with 3xLTM4650 (See Demo Board DC2481A-B, Custom-Stuffed with LTM4686B Module for U1) Producing 1V_{OUT} at up to 174A. Power System Management Features Accessible Through LTM4686B. See Figure 34. Contact Sales Support for Adapting Circuit for LTM4686B Use with LTM4631, LTM4620A, LTM4630

TYPICAL APPLICATIONS



LTM4686B Paralleled with 3× LTM4650 (Up to 174A Output)

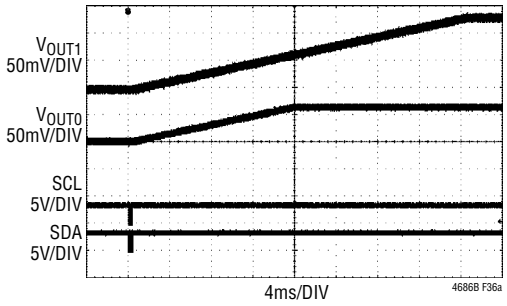
Figure 34. Current Sharing Performance of Figure 33 Circuit at $5V_{IN}$



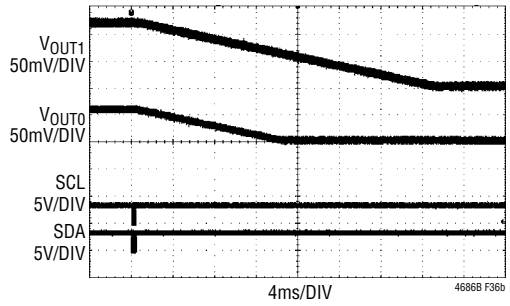
- SLAVE ADDRESS = 1000101_R/W (0x45)
- 1MHz SWITCHING FREQUENCY
- NO GUI CONFIGURATION AND NO PART-SPECIFIC PROGRAMMING REQUIRED. IN MULTI-MODULE SYSTEMS, CONFIGURING RAIL_ADDRESS IS RECOMMENDED.
- SETTING MFR_PWM_CONFIG[7] = 1_b, CONFIGURES THE V_{OUT1} CONTROL LOOP TO USE THE V_{OSNS0}^+/V_{OSNS0}^- DIFFERENTIAL-SENSE PIN-PAIR AS THE FEEDBACK SIGNAL FOR REGULATING V_{OUT1}.

Figure 35. 28A, 3.3V Output DC/DC µModule Regulator with Serial Interface

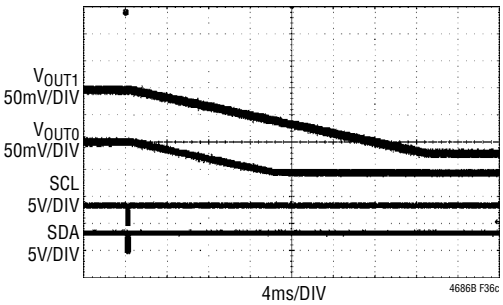
TYPICAL APPLICATIONS



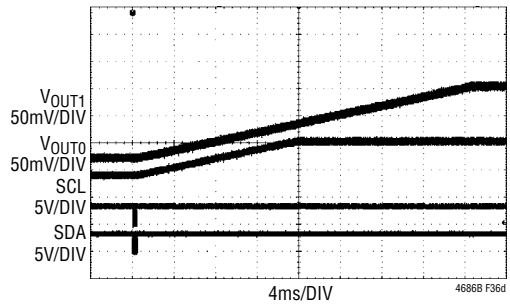
(a) PMBus Operation (Reg. 0x01): 0x80 → 0xA8 (Margin High)



(b) PMBus Operation (Reg. 0x01): 0xA8 → 0x80 (Margin Off)



(c) PMBus Operation (Reg. 0x01): 0x80 → 0x98 (Margin Low)



(d) PMBus Operation (Reg. 0x01): 0x98 → 0x80 (Margin Off)

Figure 36. Output Voltage Margining, Figure 62 Circuit, VOUT_COMMAND0 = 1.20V, VOUT_COMMAND1 = 2.50V

APPENDIX A

SIMILARITY BETWEEN PMBUS, SMBUS AND I²C 2-WIRE INTERFACE

The PMBus 2-wire interface is an incremental extension of the SMBus. SMBus is built upon I²C with some minor differences in timing, DC parameters and protocol. The PMBus/SMBus protocols are more robust than simple I²C byte commands because PMBus/SMBus provide time-outs to prevent bus errors and optional packet error checking (PEC) to ensure data integrity. In general, a master device that can be configured for I²C communication can be used for PMBus communication with little or no change to hardware or firmware. Repeat start (restart) is not supported by all I²C controllers but is required for SMBus/PMBus reads. If a general purpose I²C controller is used, check that repeat start is supported.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.2: Paragraph 5: Transport.

For a description of the differences between SMBus and I²C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B—Differences Between SMBus and I²C.

PMBus data format terminology and abbreviations used in ADI data sheets (see Appendix C: PMBus Command Details, for example), application notes, and the LTpowerPlay GUI are indicated in Table 21.

Table 21. Data Format Terminology

PMBus TERMINOLOGY	MEANING	TERMINOLOGY FOR: SPECS, GUI, APPLICATION NOTES	ABBREVIATIONS FOR SUMMARY COMMAND TABLE
Linear	Linear	Linear_5s_11s	L11
Linear (for Voltage Related Commands)	Linear	Linear_16u	L16
Direct	Direct-Manufacturer Customized	DirectMfr	CF
Hex		Hex	I16
ASCII		ASCII	ASC
	Register Fields	Reg	Reg

Handshaking features are included to ensure robust system communication. Please refer to the PMBus Communication and Command Processing subsection of the Applications Information section for further details.

APPENDIX B

PMBUS SERIAL DIGITAL INTERFACE

The LTM4686B communicates with a host (master) using the standard PMBus serial bus interface. The Timing Diagram, Figure 37, shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTM4686B is a slave device. The master can communicate with the LTM4686B using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following PMBus protocols are supported:

- Write Byte, Write Word, Send Byte, Block Write
- Read Byte, Read Word, Block Read
- Block Write – Block Read Process Call
- Alert Response Address

Figure 39 to Figure 55 illustrate the aforementioned PMBus protocols. All transactions support PEC (parity error check) and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the PMBus timeout may be extended when reading the fault log.

Figure 38 is a key to the protocol diagrams in this section. PEC is optional.

A value shown below a field in the following figures is a mandatory value for that field.

The data formats implemented by PMBus are:

- Master transmitter transmits to slave receiver. The transfer direction in this case is not changed.
- Master reads slave immediately after the first byte. At the moment of the first acknowledgment (provided by the slave receiver) the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.
- Combined format. During a change of direction within a transfer, the master repeats both a start condition and the slave address but with the R/$\overline{W}$ bit reversed. In this case, the master receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

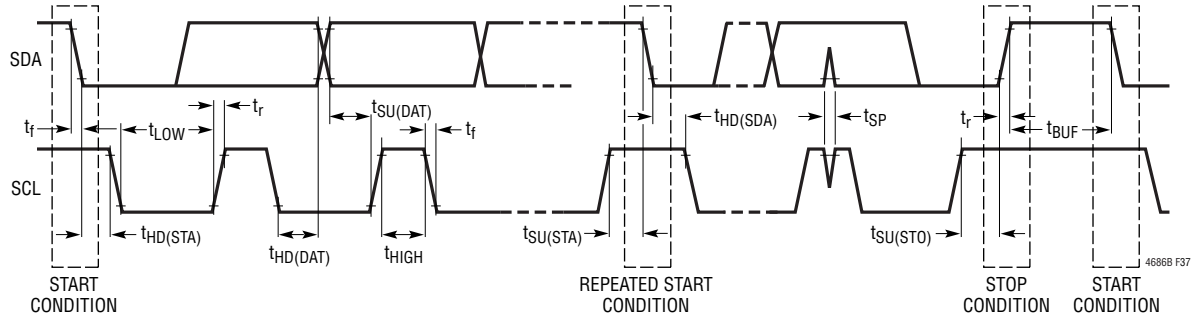


Figure 37. Timing Diagram

APPENDIX B

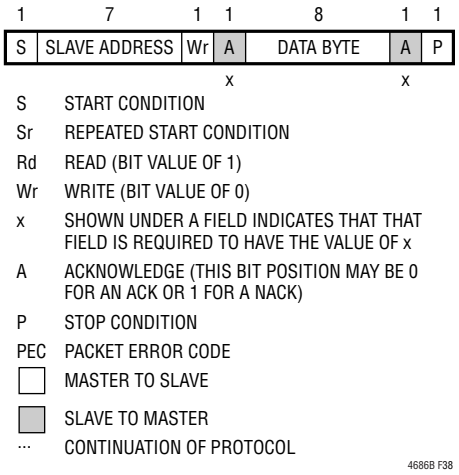


Figure 38. PMBus Packet Protocol Diagram Element Key

Figure 39. Quick Command Protocol

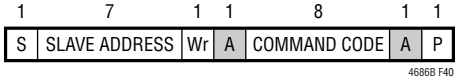


Figure 40. Send Byte Protocol

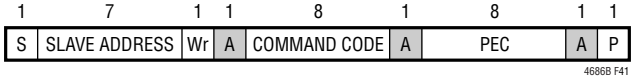


Figure 41. Send Byte Protocol with PEC

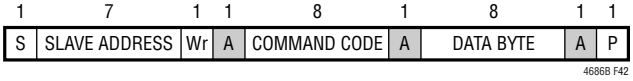


Figure 42. Write Byte Protocol

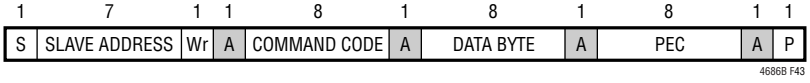


Figure 43. Write Byte Protocol with PEC

APPENDIX B

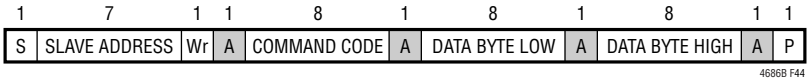


Figure 44. Write Word Protocol

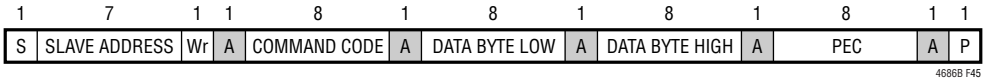


Figure 45. Write Word Protocol with PEC

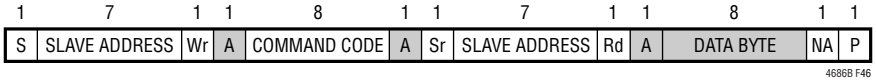


Figure 46. Read Byte Protocol

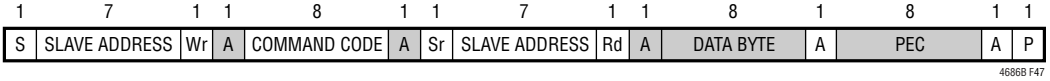


Figure 47. Read Byte Protocol with PEC

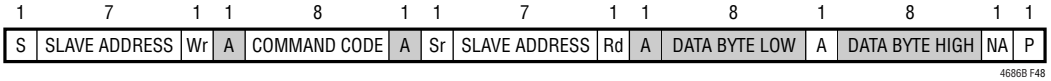


Figure 48. Read Word Protocol

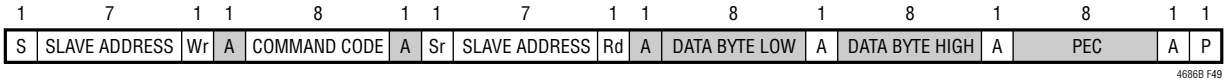


Figure 49. Read Word Protocol with PEC

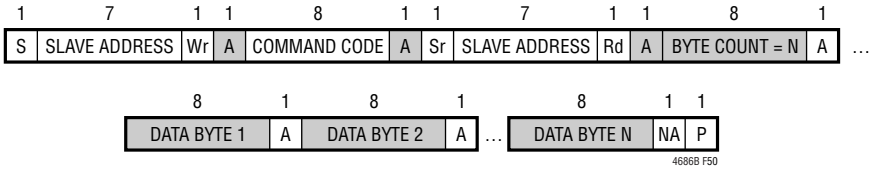


Figure 50. Block Read Protocol

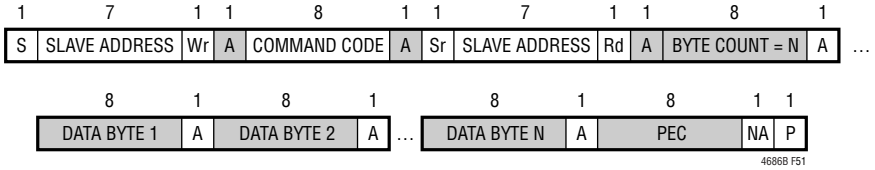


Figure 51. Block Read Protocol with PEC

APPENDIX B

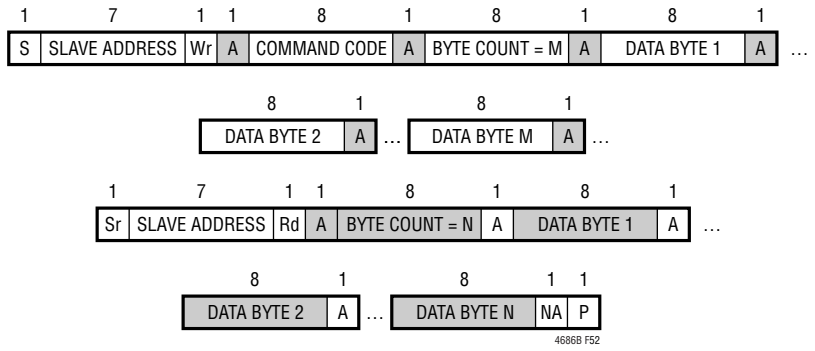


Figure 52. Block Write – Block Read Process Call

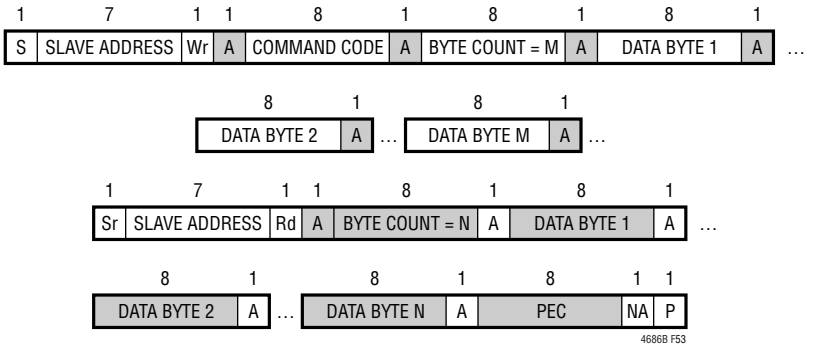


Figure 53. Block Write – Block Read Process Call with PEC

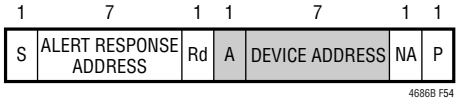


Figure 54. Alert Response Address Protocol

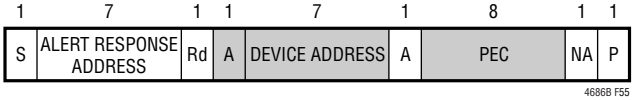


Figure 55. Alert Response Address Protocol with PEC

APPENDIX C: PMBUS COMMAND DETAILS

ADDRESSING AND WRITE PROTECT

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
PAGE	0x00	Channel (page) presently selected for any paged command.	R/W Byte	N	Reg			0x00
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	W Block	N				
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Block R/W Process	N				
WRITE_PROTECT	0x10	Protect the device against unintended PMBus modifications.	R/W Byte	N	Reg		Y	0x00
MFR_ADDRESS	0xE6	Specify right-justified 7-bit device address.	R/W Byte	N	Reg		Y	0x4F
MFR_RAIL_ADDRESS	0xFA	Specify unique right-justified 7-bit address for channels comprising a PolyPhase output.	R/W Byte	Y	Reg		Y	0x80

Related commands: MFR_COMMON.

PAGE

The PAGE command provides the ability to configure, control and monitor both PWM channels through only one physical address, either the MFR_ADDRESS or GLOBAL device address. Each PAGE contains the operating memory for one PWM channel.

Pages 0x00 and 0x01 correspond to channel 0 and channel 1, respectively, in this device.

Setting PAGE to 0xFF applies any following paged commands to both outputs. With PAGE set to 0xFF the LTM4686B will respond to read commands as if PAGE were set to 0x00 (channel 0 results).

This command has one data byte.

PAGE_PLUS_WRITE

The PAGE_PLUS_WRITE command provides a way to set the page within a device, send a command and then send the data for the command, all in one communication packet. Commands allowed by the present write protection level may be sent with PAGE_PLUS_WRITE.

The value stored in the PAGE command is not affected by PAGE_PLUS_WRITE. If PAGE_PLUS_WRITE is used to send a non-paged command, the Page Number byte is ignored.

This command uses Write Block protocol. An example of the PAGE_PLUS_WRITE command with PEC sending a command that has two data bytes is shown in Figure 56.

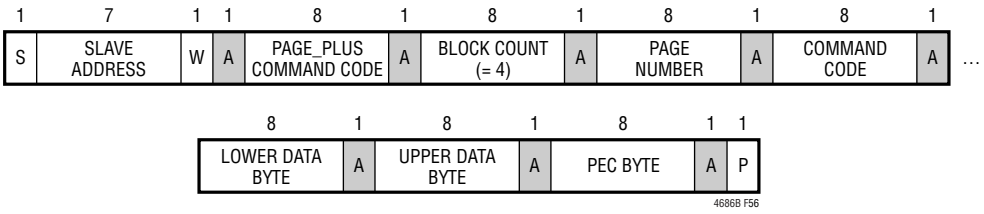


Figure 56. Example of PAGE_PLUS_WRITE

APPENDIX C: PMBUS COMMAND DETAILS

PAGE_PLUS_READ

The PAGE_PLUS_READ command provides the ability to set the page within a device, send a command and then read the data returned by the command, all in one communication packet .

The value stored in the PAGE command is not affected by PAGE_PLUS_READ. If PAGE_PLUS_READ is used to access data from a non-paged command, the Page Number byte is ignored.

This command uses Block Write – Block Read Process Call protocol. An example of the PAGE_PLUS_READ command with PEC is shown in Figure 57.

NOTE: PAGE_PLUS commands cannot be nested. A PAGE_PLUS command cannot be used to read or write another PAGE_PLUS command. If this is attempted, the LTM4686B will NACK the entire PAGE_PLUS packet and issue a CML fault for Invalid/Unsupported Data.

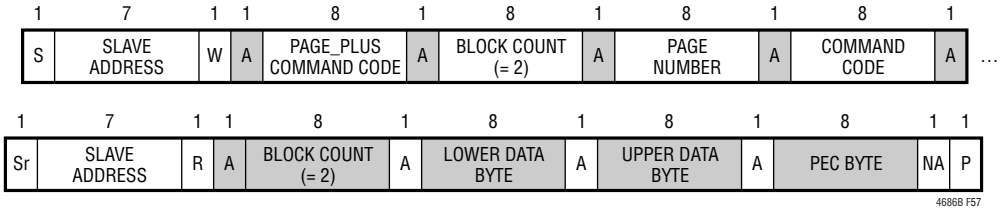


Figure 57. Example of PAGE_PLUS_READ

WRITE_PROTECT

The WRITE_PROTECT command is used to control writing to the LTM4686B device. This command does not indicate the status of the WP pin which is defined in the MFR_COMMON command. The WP pin takes precedence over the value of this command unless the WRITE_PROTECT command is more stringent.

BYTE	MEANING
0x80	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK and STORE_USER_ALL command
0x40	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, STORE_USER_ALL, OPERATION and CLEAR_FAULTS command. individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS registers.
0x20	Disable all writes except to the WRITE_PROTECT, OPERATION, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, CLEAR_FAULTS, PAGE, ON_OFF_CONFIG, VOUT_COMMAND and STORE_USER_ALL. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS registers.
0x10	Reserved, must be 0
0x08	Reserved, must be 0
0x04	Reserved, must be 0
0x02	Reserved, must be 0
0x01	Reserved, must be 0

Enable writes to all commands when WRITE_PROTECT is set to 0x00.

This command has one data byte.

APPENDIX C: PMBUS COMMAND DETAILS

If WP pin is high, PAGE, OPERATION, MFR_CLEAR_PEAKS, MFR_EE_UNLOCK and CLEAR_FAULTS commands are supported. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS registers.

MFR_ADDRESS

The MFR_ADDRESS command byte sets the 7 bits of the PMBus slave address for this device.

Setting this command to a value of 0x80 disables device addressing. The GLOBAL device address, 0x5A and 0x5B, cannot be deactivated. If RCONFIG is set to ignore (MFR_CONFIG_ALL[6] = 1_b), the ASEL pin is still used to determine the LSB of the channel address. If the ASEL pin is open, the LTM4686B will use the MFR_ADDRESS stored in EEPROM. Values of 0x5A, 0x5B, 0x0C, and 0x7C are not recommended.

This command has one data byte.

MFR_RAIL_ADDRESS

The MFR_RAIL_ADDRESS command enables direct device address access to the PAGE activated channel. The value of this command should be common to all devices attached to a single power supply rail.

The user should only perform command writes to this address. If a read is performed from this address and the rail devices do not respond with EXACTLY the same value, the LTM4686B will detect bus contention and set a CML communications fault.

Setting this command to a value of 0x80 disables rail device addressing for the channel.

This command has one data byte.

GENERAL CONFIGURATION REGISTERS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_CHAN_CONFIG	0xD0	Configuration bits that are channel specific.	R/W Byte	Y	Reg		Y	0x1D
MFR_CONFIG_ALL	0xD1	Configuration bits that are common to all pages.	R/W Byte	N	Reg		Y	0x09

MFR_CHAN_CONFIG

General purpose configuration command common to multiple ADI products.

BIT	MEANING
7	Reserved
6	Reserved
5	Reserved
4	Disable RUN Low. When asserted the RUN pin is not pulsed low if commanded OFF
3	Short Cycle. When asserted the output will immediate off if commanded ON while waiting for TOFF_DELAY or TOFF_FALL. TOFF_MIN of 120ms is honored then the part will command ON.
2	SHARE_CLOCK control, if SHARE_CLOCK is held low, the output is disabled
1	No $\overline{\text{GPIO}}$ $\overline{\text{ALERT}}$, $\overline{\text{ALERT}}$ is not pulled low if $\overline{\text{GPIO}}$ is pulled low externally. Assert this bit if either POWER_GOOD or VOUT_UVUF are propagated on $\overline{\text{GPIO}}$
0	Disables the V_{OUT} decay value requirement for MFR_RETRY_TIME processing. When this bit is set to a 0, the output must decay to less than 12.5% of the programmed value for any action that turns off the rail including a fault, an OFF/ON command, or a toggle of RUN from high to low to high.

This command has one data byte.

APPENDIX C: PMBUS COMMAND DETAILS

MFR_CONFIG_ALL

General purpose configuration command common to multiple ADI products

BIT	MEANING
7	Enable Fault Logging
6	Ignore Resistor Configuration Pins
5	Disable CML fault for Quick Command message
4	Disable SYNC out
3	Enable 255ms Time Out
2	A valid PEC required for PMBus writes to be accepted. If this bit is not set, the part will accept commands with invalid PEC.
1	Enable the use of PMBus clock stretching
0	Enables a low to high transition on either RUN pin to issue a CLEAR_FAULTS command

This command has one data byte.

ON/OFF/MARGIN

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1F
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x80
MFR_RESET	0xFD	Commanded reset without requiring a power-down. Identical to RESTORE_USER_ALL.	Send Byte	N				NA

ON_OFF_CONFIG

The ON_OFF_CONFIG command configures the combination of RUN*n* pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.

Table 22. Supported Values

VALUE	MEANING
0x1F	OPERATION value and RUN*n* pin must both command the device to start/run. Device executes immediate off when commanded off.
0x1E	OPERATION value and RUN*n* pin must both command the device to start/run. Device uses TOFF_ command values when commanded off.
0x17	RUN*n* pin control with immediate off when commanded off. OPERATION on/off control ignored.
0x16	RUN*n* pin control using TOFF_ command values when commanded off. OPERATION on/off control ignored.

Note: A high on the RUN*n* pin is always required to start power conversion. Power conversion will always stop with a low on RUN*n*.

Programming an unsupported ON_OFF_CONFIG value will generate a CML fault and the command will be ignored.

This command has one data byte.

APPENDIX C: PMBUS COMMAND DETAILS

OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the input from the RUN*n* pins. It is also used to cause the unit to set the output voltage to the upper or lower MARGIN VOLTAGEs. The unit stays in the commanded operating mode until a subsequent OPERATION command or change in the state of the RUN*n* pin instructs the device to change to another mode. If the part is stored in the MARGIN_LOW/HIGH state, the next MFR_RESET or RESTORE_USER_ALL or SV_{IN} power cycle will ramp to that state. If the OPERATION command is modified, for example ON is changed to MARGIN_LOW, the output will move at a fixed slope set by the VOUT_TRANSITION_RATE. The default operation command is sequence off.

Margin High (Ignore Faults) and Margin Low (Ignore Faults) operations are not supported by the LTM4686B.

The part defaults to the Sequence Off state.

This command has one data byte.

Table 23. OPERATION Command Detail Register OPERATION Data Contents When On_Off_Config_Use_PMBus Enables Operation_Control

SYMBOL	ACTION	VALUE
BITS		
FUNCTION	Turn off immediately	0x00
	Turn on	0x80
	Margin Low	0x98
	Margin High	0xA8
	Sequence off	0x40

OPERATION Data Contents When On_Off_Config is Configured Such That OPERATION Command Is Not Used to Command Channel On or Off

SYMBOL	ACTION	VALUE
BITS		
FUNCTION	Output at Nominal	0x80
	Margin Low	0x98
	Margin High	0xA8

Note: Attempts to write a reserved value will cause a CML fault.

MFR_RESET

This command provides a means by which the user can perform a reset of the LTM4686B. Identical to RESTORE_USER_ALL.

This write-only command has no data bytes.

PWM CONFIG

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_PWM_MODE	0xD4	Configuration for the PWM engine of each channel.	R/W Byte	Y	Reg		Y	0xC3
MFR_PWM_CONFIG	0xF5	Set numerous parameters for the DC/DC controller including phasing.	R/W Byte	N	Reg		Y	0x10
FREQUENCY_SWITCH	0x33	Switching frequency of the controller.	R/W Word	N	L11	kHz	Y	1000 0x03E8

APPENDIX C: PMBUS COMMAND DETAILS

MFR_PWM_MODE

The MFR_PWM_MODE command allows the user to program the PWM controller to use, discontinuous (pulse-skipping mode), or forced continuous conduction mode.

BIT	MEANING
7	Range of I_{LIMIT} 0 – Low Current Range 1 – High Current Range
6	Enable Servo Mode
5	Reserved
4	Page 0 Only: Use of TSNS1a-Sensed Temperature Telemetry 0 – Temperature sensed via TSNS1a is used to temperature-correct the current-sense information digitized by Channel 1. 1 – Temperature sensed via TSNS0 is used to temperature-correct the current-sense information digitized by Channel 1. Telemetry obtained from the thermal sensor connected to TSNS1a can be external to the module, if desired.
3	Reserved
2	Reserved
1	Voltage Range 0 – Hi Voltage Range 3.6 volts max 1 – Lo Voltage Range 2.75 volts max
0	PWM Mode 0 – Discontinuous Mode 1 – Continuous Mode

Whenever the channel is ramping on, the PWM mode will be discontinuous, regardless of the value of this command.

Bit [7] of this command determines if the part is in high range or low range of the IOUT_OC_FAULT_LIMIT command. Changing this bit value changes the PWM loop gain and compensation. Changing this bit value whenever an output is active may have detrimental system results.

Bit [6] The LTM4686B will not servo while the part is OFF, ramping on or ramping off. When set to a one, the output servo is enabled. The output set point DAC will be slowly adjusted to minimize the difference between the READ_VOUT_ADC and the VOUT_COMMAND (or the appropriate margined value).

Bit [1] of this command determines if the part is in high range or low voltage range. Changing this bit value changes the PWM loop gain and compensation. This bit value cannot be changed when an output is active.

This command has one data byte.

APPENDIX C: PMBUS COMMAND DETAILS

MFR_PWM_CONFIG

The MFR_PWM_CONFIG command sets the switching frequency phase offset with respect to the falling edge of the SYNC signal. The part must be in the OFF state to process this command. Either the RUN pins must be low or the part must be commanded off. If the part is in the RUN state and this command is written, the command will be ignored and a BUSY fault will be asserted. Bit 7 allows remote differential voltage sensing for PolyPhase rail applications.

BIT	MEANING
7	EA Connection 0 – Independent EA and Channel Outputs 1 – EA1 uses EA0 input for PolyPhase operation
6	Reserved.
5	Reserved
4	Share Clock Enable : If this bit is 1, the SHARE_CLK pin will not be released until SV_{IN} > VIN_ON. The SHARE_CLK pin will be pulled low when SV_{IN} < VIN_OFF. If this bit is 0, the SHARE_CLK pin will not be pulled low when SV_{IN} < VIN_OFF except for the initial application of SV_{IN}.
3	Reserved

BIT [2:0]	CHANNEL 0 (DEGREES)	CHANNEL 1 (DEGREES)
000b	0	180
001b	90	270
010b	0	240
011b	0	120
100b	120	240
101b	60	240
110b	120	300

Do not assert Bit [7] unless it is a PolyPhase application and both V_{OUT} pins are tied together and both COMP*n*a pins are tied together.

This command has one data byte.

FREQUENCY_SWITCH

The FREQUENCY_SWITCH command sets the switching frequency, in kHz, of a PMBus device. See Table 7 for recommended values.

Supported Frequencies:

VALUE [15:0]	RESULTING FREQUENCY (TYP)
0x0000	External Oscillator
0xFBE8	500kHz
0x023F	575kHz
0x028A	650kHz
0x02EE	750kHz
0x03E8	1000kHz

APPENDIX C: PMBUS COMMAND DETAILS

The part must be in the OFF state to process this command. Either the RUN pins must be low or the part must be commanded off. If the part is in the RUN state and this command is written, the command will be ignored and a BUSY fault will be asserted. When the part is commanded off and the frequency is changed, a PLL_UNLOCK status may be detected as the PLL locks onto the new frequency.

This command has two data bytes and is formatted in Linear_5s_11s format.

VOLTAGE

Input Voltage (SV_{IN}) and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VIN_OV_FAULT_ LIMIT	0x55	Input supply (SV_{IN}) overvoltage fault limit.	R/W Word	N	L11	V	Y	6.000 0xCB00
VIN_UV_WARN_LIMIT	0x58	Input supply (SV_{IN}) undervoltage warning limit.	R/W Word	N	L11	V	Y	4.094 (0xCA0C)
VIN_ON	0x35	Input voltage (SV_{IN}) at which the unit should start power conversion.	R/W Word	N	L11	V	Y	4.250 (0xCA20)
VIN_OFF	0x36	Input voltage (SV_{IN}) at which the unit should stop power conversion.	R/W Word	N	L11	V	Y	4.000 (0xCA00)

VIN_OV_FAULT_LIMIT

The VIN_OV_FAULT_LIMIT command sets the value of the measured (SV_{IN}) input voltage, in volts, that causes an input overvoltage fault. The fault is detected with the A/D converter resulting in latency up to 90ms, typical.

This command has two data bytes and is formatted in Linear_5s_11s format.

VIN_UV_WARN_LIMIT

The VIN_UV_WARN_LIMIT command sets the value of the SV_{IN} input voltage that causes an SV_{IN} input undervoltage warning. The warning is detected with the A/D converter resulting in latency up to 90ms, typical.

This command has two data bytes and is formatted in Linear_5s_11s format.

VIN_ON

The VIN_ON command sets the SV_{IN} input voltage, in volts, at which the unit should start power conversion.

This command has two data bytes and is formatted in Linear_5s_11s format.

VIN_OFF

The VIN_OFF command sets the SV_{IN} input voltage, in volts, at which the unit should stop power conversion.

This command has two data bytes and is formatted in Linear_5s_11s format.

APPENDIX C: PMBUS COMMAND DETAILS

Output Voltage and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VOUT_MODE	0x20	Output voltage format and exponent (2^{-12}).	R Byte	Y	Reg			2^{-12} 0x14
VOUT_MAX	0x24	Upper limit on the commanded output voltage including VOUT_MARGIN_HIGH.	R/W Word	Y	L16	V	Y	3.630 0x3A14
VOUT_OV_FAULT_ LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.100V 0x119A
VOUT_OV_WARN_ LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075V 0x1133
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point. Must be greater than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	1.050V 0x10CD
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	L16	V	Y	1.000V 0x1000
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point. Must be less than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.950V 0x0F33
VOUT_UV_WARN_ LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925V 0x0ECD
VOUT_UV_FAULT_ LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	L16	V	Y	0.900V 0x0E66
MFR_VOUT_MAX	0xA5	Maximum allowed output voltage including VOUT_OV_FAULT_LIMIT.	R Word	Y	L16	V		5.7 0x5B34

VOUT_MODE

The data byte for VOUT_MODE command, used for commanding and reading output voltage, consists of a 3-bit mode (only linear format is supported) and a 5-bit parameter representing the exponent used in output voltage Read/Write commands.

This read-only command has one data byte.

VOUT_MAX

The VOUT_MAX command sets an upper limit on any voltage, including VOUT_MARGIN_HIGH, the unit can command regardless of any other commands or combinations. The maximum allowed value of this command is 5.7 volts. The maximum output voltage the LTM4686B can produce is 3.6 volts including VOUT_MARGIN_HIGH. However, the VOUT_OV_FAULT_LIMIT can be commanded as high as 4.0 volts. The LTM4686B is not specified for operation above $3.6V_{OUT}$.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_OV_FAULT_LIMIT

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage measured at the sense pins, in volts, which causes an output overvoltage fault.

If the VOUT_OV_FAULT_LIMIT is modified and the switcher is active, allow 10ms after the command is modified to assure the new value is being honored. The part indicates if it is busy making a calculation. Monitor bits 5 and 6 of MFR_COMMON. Either bit is low if the part is busy. If this wait time is not met, and the VOUT_COMMAND is modified

APPENDIX C: PMBUS COMMAND DETAILS

above the old overvoltage limit, an OV condition might temporarily be detected resulting in undesirable behavior and possible damage to the switcher.

If VOUT_OV_FAULT_RESPONSE is set to OV_PULLDOWN, the $\overline{GPIO}$ pin will not assert if VOUT_OV_FAULT is propagated. The LTM4686B will pull the TG low and assert the BG bit as soon as the overvoltage condition is detected.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_OV_WARN_LIMIT

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage measured at the sense pins, in volts, which causes an output voltage high warning. The READ_VOUT value will be used to determine if this limit has been exceeded.

In response to the VOUT_OV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the V_{OUT} bit in the STATUS_WORD
- Sets the V_{OUT} Overvoltage Warning bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{ALERT}$ pin, unless masked.

This condition is detected by the ADC so the response time may be up to 90ms, typical.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_MARGIN_HIGH

The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed, in volts, when the OPERATION command is set to “Margin High”. The value must be greater than VOUT_COMMAND. The maximum guaranteed value on VOUT_MARGIN_HIGH is 3.6V.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_COMMAND

The VOUT_COMMAND consists of two bytes and is used to set the output voltage, in volts. The maximum guaranteed value on V_{OUT} is 3.6V.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_MARGIN_LOW

The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed, in volts, when the OPERATION command is set to “Margin Low”. The value must be less than VOUT_COMMAND.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

APPENDIX C: PMBUS COMMAND DETAILS

This command has two data bytes and is formatted in Linear_16u format.

VOUT_UV_WARN_LIMIT

The VOUT_UV_ WARN_LIMIT command reads the value of the output voltage measured at the sense pins, in volts, which causes an output voltage low warning.

In response to the VOUT_UV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the V_{OUT} bit in the STATUS_WORD
- Sets the V_{OUT} Undervoltage Warning bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked.

This condition is detected by the ADC so the response time may be up to 90ms, typical.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_UV_FAULT_LIMIT

The VOUT_UV_FAULT_LIMIT command reads the value of the output voltage measured at the sense pins, in volts, which causes an output undervoltage fault.

This command has two data bytes and is formatted in Linear_16u format.

MFR_VOUT_MAX

The MFR_VOUT_MAX command is the maximum output voltage in volts for each channel including VOUT_OV_FAULT_LIMIT. If the output voltages are set to high range (Bit 1 of MFR_PWM_MODE set to a 0) MFR_VOUT_MAX for channel 0 and 1 is 5.7V. If the output voltages are set to low range (Bit 1 of MFR_PWM_MODE set to a 1) the MFR_VOUT_MAX for both channels is 2.75V. Entering VOUT_COMMAND values greater than this will result in a CML fault and the output voltage setting will be clamped to the maximum level.

This read-only command has 2 data bytes and is formatted in Linear_16u format.

CURRENT

Input Current Calibration

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_IIN_OFFSET	0xE9	Coefficient used to add to the input current to account for the IQ of the part.	R/W Word	Y	L11	A	Y	0.04816 0x9315

MFR_IIN_OFFSET

The MFR_IIN_OFFSET command allows the user to set an input current representing the quiescent current of each channel. For accurate results at low output current, the part should be in continuous conduction mode. (MFR_PWM_MODE[0] = 1_b). See Table 8 for recommended values.

This command has 2 data bytes and is formatted in Linear_5s_11s format.

APPENDIX C: PMBUS COMMAND DETAILS

Output Current Calibration

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IOUT_CAL_GAIN	0x38	The ratio of the voltage at the current sense pins to the sensed current.	R/W Word	Y	L11	mΩ	Factory-Only NVM	Trimmed, 1.41mΩ typical
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient of the current sensing element.	R/W Word	Y	CF		Y	3860 0x0F14

IOUT_CAL_GAIN

The IOUT_CAL_GAIN command is nominally used to set the resistance value of the current sense element, in milliohms. (See also MFR_IOUT_CAL_GAIN_TC). Writes to this register result in a NACK and do not impact output current readback telemetry.

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_IOUT_CAL_GAIN_TC

The MFR_IOUT_CAL_GAIN_TC command allows the user to program the temperature coefficient of the IOUT_CAL_GAIN inductor DCR in ppm/°C.

This command has two data bytes and is formatted in 16-bit 2's complement integer ppm. N = –32768 to 32767 • 10^{-6}. Nominal temperature is 27°C. The IOUT_CAL_GAIN is multiplied by:

[1.0 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERATURE_1–27)]. DCR sensing will have a typical value of 3900.

The IOUT_CAL_GAIN and MFR_IOUT_CAL_GAIN_TC impact all current parameters including: READ_IOUT, READ_IIN, IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT. Writes to this register are not recommended; use the factory-default value.

Input Current

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IIN_OC_WARN_LIMIT	0x5D	Input overcurrent warning limit.	R/W Word	N	L11	A	Y	30 0xDBC0

IIN_OC_WARN_LIMIT

The IIN_OC_WARN_LIMIT command sets the value of the input current, in amperes, that causes a warning indicating the input current is high. The READ_IIN value will be used to determine if this limit has been exceeded.

In response to the IIN_OC_WARN_LIMIT being exceeded, the device:

- Sets the OTHER bit in the STATUS_BYTE
- Sets the INPUT bit in the upper byte of the STATUS_WORD
- Sets the IIN Overcurrent Warning bit in the STATUS_INPUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This condition is detected by the ADC so the response time may be up to 90ms, typical.

This command has two data bytes and is formatted in Linear_5s_11s format.

APPENDIX C: PMBUS COMMAND DETAILS

Output Current

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	36 0xE240
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	20.5 0xDA90

IOUT_OC_FAULT_LIMIT

The IOUT_OC_FAULT_LIMIT command sets the value of the peak output current limit, in amperes. When the controller is in current limit, the overcurrent detector will indicate an overcurrent fault condition. The programmed overcurrent fault limit value is rounded up to the nearest one of the following set of discrete values:

25mV/IOUT_CAL_GAIN	Low Range (1.5x Nominal Loop Gain)
28.6mV/IOUT_CAL_GAIN	MFR_PWM_MODE [7] = 0
32.1mV/IOUT_CAL_GAIN	
35.7mV/IOUT_CAL_GAIN	
39.3mV/IOUT_CAL_GAIN	
42.9mV/IOUT_CAL_GAIN	
46.4mV/IOUT_CAL_GAIN	
50mV/IOUT_CAL_GAIN	
37.5mV/IOUT_CAL_GAIN	High Range (Nominal Loop Gain)
42.9mV/IOUT_CAL_GAIN	MFR_PWM_MODE [7] = 1
48.2mV/IOUT_CAL_GAIN	
53.6mV/IOUT_CAL_GAIN	
58.9mV/IOUT_CAL_GAIN	
64.3mV/IOUT_CAL_GAIN	
69.6mV/IOUT_CAL_GAIN	
75mV/IOUT_CAL_GAIN	

Note: This is the peak of the current waveform. The READ_IOUT command returns the average current. The peak output current limits are adjusted with temperature based on the MFR_IOUT_CAL_GAIN_TC using the equation:

IOUT_OC_FAULT_LIMIT = IOUT_CAL_GAIN • (1 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERTURE_1-27.0)).

The LTpowerPlay GUI automatically convert the voltages to currents.

The I_{OUT} range is set with bit 7 of the MFR_PWM_MODE command.

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

This command has two data bytes and is formatted in Linear_5s_11s format.

IOUT_OC_WARN_LIMIT

This command sets the value of the output current that causes an output overcurrent warning in amperes. The READ_IOUT value will be used to determine if this limit has been exceeded.

APPENDIX C: PMBUS COMMAND DETAILS

In response to the IOUT_OC_WARN_LIMIT being exceeded, the device:

• Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE

• Sets the IOUT bit in the STATUS_WORD

• Sets the IOUT Overcurrent Warning bit in the STATUS_IOUT command, and

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked.

This condition is detected by the ADC so the response time may be up to 90ms, typical.

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

This command has two data bytes and is formatted in Linear_5s_11s format

TEMPERATURE

Power Stage DCR Temperature Calibration

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_TEMP_1_GAIN	0xF8	Sets the slope of the power stage temperature sensor.	R/W Word	Y	CF		Y	0.995 0x3FAE
MFR_TEMP_1_OFFSET	0xF9	Sets the offset of the power stage temperature sensor with respect to –273.1°C.	R/W Word	Y	L11	C	Y	0 0x8000

MFR_TEMP_1_GAIN

The MFR_TEMP_1_GAIN command will modify the slope of the power stage temperature sensor to account for non-idealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in 16-bit 2's complement integer. N = 8192 to 32767. The effective adjustment is $N \bullet 2^{-14}$. The nominal value is 1.

MFR_TEMP_1_OFFSET

The MFR_TEMP_1_OFFSET command will modify the offset of the power stage temperature sensor to account for non-idealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in Linear_5s_11s format. The part starts the calculation with a value of –273.15 so the default adjustment value is zero.

Power Stage Temperature Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
OT_FAULT_LIMIT	0x4F	Power stage overtemperature fault limit.	R/W Word	Y	L11	C	Y	128 0xF200
OT_WARN_LIMIT	0x51	Power stage overtemperature warning limit.	R/W Word	Y	L11	C	Y	125 0xEBE8
UT_FAULT_LIMIT	0x53	Power stage undertemperature fault limit.	R/W Word	Y	L11	C	Y	–45 0xE530

APPENDIX C: PMBUS COMMAND DETAILS

OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the value of the power stage temperature, in degrees Celsius, which causes an overtemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

This condition is detected by the ADC so the response time may be up to 90ms, typical.

This command has two data bytes and is formatted in Linear_5s_11s format.

OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the value of the power stage temperature, in degrees Celsius, which causes an overtemperature warning. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

In response to the OT_WARN_LIMIT being exceeded, the device:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the Overtemperature Warning bit in the STATUS_TEMPERATURE command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked.

This condition is detected by the ADC so the response time may be up to 90ms, typical.

This command has two data bytes and is formatted in Linear_5s_11s format.

UT_FAULT_LIMIT

The UT_FAULT_LIMIT command sets the value of the power stage temperature, in degrees Celsius, which causes an undertemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

This condition is detected by the ADC so the response time may be up to 90ms, typical.

This command has two data bytes and is formatted in Linear_5s_11s format.

TIMING

Timing: On Sequence/Ramp

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	L11	ms	Y	0.0 0x0000
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the V_{OUT} commanded value.	R/W Word	Y	L11	ms	Y	2.0 0xC200
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for V_{OUT} to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	L11	ms	Y	10 0xD280
VOUT_TRANSITION_RATE	0x27	Rate the output changes when V_{OUT} commanded to a new value.	R/W Word	Y	L11	V/ms	Y	0.025 0x8B33

APPENDIX C: PMBUS COMMAND DETAILS

TON_DELAY

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received until the output voltage starts to rise. Values from 0ms to 83 seconds are valid.

This command has two data bytes and is formatted in Linear_5s_11s format.

TON_RISE

The TON_RISE command sets the time, in milliseconds, from the time the output starts to rise to the time the output enters the regulation band. Values from 0 to 1.3 seconds are valid. The part will be in discontinuous mode during TON_RISE events. If TON_RISE is less than 0.25ms, the LTM4686B digital slope will be bypassed. The output voltage transition will be controlled by the analog performance of the PWM switcher. The maximum allowed slope is 4V/ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

TON_MAX_FAULT_LIMIT

The TON_MAX_FAULT_LIMIT command sets the value, in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit.

A data value of 0ms means that there is no limit and that the unit can attempt to bring up the output voltage indefinitely. The maximum limit is 83 seconds.

This command has two data bytes and is formatted in Linear_5s_11s format.

VOUT_TRANSITION_RATE

When a PMBus device receives either a VOUT_COMMAND or OPERATION (Margin High, Margin Low) that causes the output voltage to change this command set the rate in V/ms at which the output voltage changes. This commanded rate of change does not apply when the unit is commanded on or off.

This command has two data bytes and is formatted in Linear_5s_11s format.

Timing: Off Sequence/Ramp

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	L11	ms	Y	0.0 0x0000
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	L11	ms	Y	2.5 0xC280
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the unit to decay below 12.5%.	R/W Word	Y	L11	ms	Y	200 0xF320

TOFF_DELAY

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received until the output voltage starts to fall. Values from 0 to 83 seconds are valid.

This command is excluded from fault events.

This command has two data bytes and is formatted in Linear_5s_11s format.

APPENDIX C: PMBUS COMMAND DETAILS

TOFF_FALL

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-off delay time until the output voltage is commanded to zero. It is the ramp time of the V_{OUT} DAC. When the V_{OUT} DAC is zero, the part will three-state.

The part will maintain the mode of operation programmed. For defined TOFF_FALL times, the user should set the part to continuous conduction mode. Loading the max value indicates the part will ramp down at the slowest possible rate. The minimum supported fall time is 0.25ms. A value less than 0.25ms will result in a 0.25ms ramp. The maximum fall time is 1.3 seconds. The maximum allowed slope is 4V/ms.

In discontinuous conduction mode, the controller will not draw current from the load and the fall time will be set by the output capacitance and load current.

This command has two data bytes and is formatted in Linear_5s_11s format.

TOFF_MAX_WARN_LIMIT

The TOFF_MAX_WARN_LIMIT command sets the value, in milliseconds, on how long the unit can attempt to turn off the output until a warning is asserted. The output is considered off when the V_{OUT} voltage is less than 12.5% of the programmed VOUT_COMMAND value. The calculation begins after TOFF_FALL is complete. TOFF_MAX_WARN is not enabled in VOUT_DECAY is disabled.

A data value of 0ms means that there is no limit and that the unit can attempt to turn off the output voltage indefinitely. Other than 0, values from 120ms to 524 seconds are valid.

This command has two data bytes and is formatted in Linear_5s_11s format.

Precondition for Restart

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_RESTART_ DELAY	0xDC	Delay from actual RUN active edge to virtual RUN active edge.	R/W Word	Y	L11	ms	Y	200 0xF320

MFR_RESTART_DELAY

This command specifies the minimum RUN off time in milliseconds. This device will pull the RUN pin low for this length of time once a falling edge of RUN has been detected. The minimum recommended value is 136ms.

Note: The restart delay is different than the retry delay. The restart delay pulls run low for the specified time, after which a standard start-up sequence is initiated. The minimum restart delay should be equal to TOFF_DELAY + TOFF_FALL + 136ms. Valid values are from 136ms to 65.52 seconds in 16ms increments. To assure a minimum off time, set the MFR_RESTART_DELAY 16ms longer than the desired time. The output rail can be off longer than the MFR_RESTART_DELAY after the RUN pin is pulled high if the output decay bit 1 is enabled in MFR_CHAN_CONFIG and the output takes a long time to decay below 12.5% of the programmed value.

This command has two data bytes and is formatted in Linear_5s_11s format.

APPENDIX C: PMBUS COMMAND DETAILS

FAULT RESPONSE

Fault Responses All Faults

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_RETRY_ DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	Y	L11	ms	Y	350 0xFABC

MFR_RETRY_DELAY

This command sets the time in milliseconds between restarts if the fault response is to retry the controller at specified intervals. This command value is used for all fault responses that require retry. The retry time starts once the fault has been detected by the offending channel. Valid values are from 120ms to 83.88 seconds in 1ms increments.

Note: The retry delay time is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG.

This command has two data bytes and is formatted in Linear_5s_11s format.

Fault Responses Input Voltage (SV_{IN})

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an SV_{IN} input supply overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80

VIN_OV_FAULT_RESPONSE

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an (SV_{IN}) input overvoltage fault. The data byte is in the format given in Table 28.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD
- Sets the SV_{IN} Overvoltage Fault bit in the STATUS_INPUT command, and
- Notifies the host by asserting $\overline{ALERT}$ pin, unless masked.

This command has one data byte.

APPENDIX C: PMBUS COMMAND DETAILS

Fault Responses Output Voltage

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
TON_MAX_FAULT_ RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8

VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. The data byte is in the format given in Table 24.

The device also:

- Sets the VOUT_OV bit in the STATUS_BYTE
- Sets the V_{OUT} bit in the STATUS_WORD
- Sets the V_{OUT} Overvoltage Fault bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked.

The only value recognized for this command are:

0x80–The device shuts down (disables the output) and the unit does not attempt to retry. The output remains disabled until the fault is cleared (PMBus, Part II, Section 10.7).

0xB8–The device shuts down (disables the output) and device attempts retry continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.

0x4n The device shuts down and the unit does not attempt to retry. The output remains disabled until the part is commanded OFF then ON or the RUN pin is asserted low then high or MFR_RESET or RESTORE_USER_ALL through the command or removal of SV_{IN}. The OV fault must remain active for a period of n • 10µs, where n is a value from 0 to 7.

0x78+n The device shuts down and the unit attempts to retry continuously until either the fault condition is cleared or the part is commanded OFF then ON or the RUN pin is asserted low then high or MFR_RESET or RESTORE_USER_ALL through the command or removal of SV_{IN}. The OV fault must remain active for a period of n • 10µs, where n is a value from 0 to 7.

Any other value will result in a CML fault and the write will be ignored.

This command has one data byte.

APPENDIX C: PMBUS COMMAND DETAILS

Table 24. VOUT_OV_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4686B: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN*n* pin, the OPERATION command, or the combined action of the RUN*n* pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTM4686B.	00	Part performs OV pull down only (i.e., turns off the top MOSFET and turns on lower MOSFET while V_{OUT} is > VOUT_OV_FAULT)
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000–110	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN*n* pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	XXX	The delay time in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. Only valid for deglitched off state

VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output undervoltage fault. The data byte is in the format given in Table 25.

The device also:

• Sets the V_{OUT} bit in the STATUS_WORD

• Sets the V_{OUT} undervoltage fault bit in the STATUS_VOUT command

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked.

The UV fault and warn are masked until the following criteria are achieved:

1) The TON_MAX_FAULT_LIMIT has been reached
2) The TON_DELAY sequence has completed
3) The TON_RISE sequence has completed
4) The VOUT_UV_FAULT_LIMIT threshold has been reached
5) The IOUT_OC_FAULT_LIMIT is not present

The UV fault and warn are masked whenever the channel is not active.

The UV fault and warn are masked during TON_RISE and TOFF_FALL sequencing.

This command has one data byte.

APPENDIX C: PMBUS COMMAND DETAILS

Table 25. VOUT_UV_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4686B: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command • The output is commanded through the RUN*n* pin, the OPERATION command, or the combined action of the RUN*n* pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTM4686B	00	The PMBus device continues operation without interruption. (Ignores the fault functionally)
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
		10	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000–110	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN*n* pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	XXX	The delay time in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. Only valid for deglitched off state.

TON_MAX_FAULT_RESPONSE

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to a TON_MAX fault. The data byte is in the format given in Table 28.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the V_{OUT} bit in the STATUS_WORD
- Sets the TON_MAX_FAULT bit in the STATUS_VOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked.
- A value of 0 disables the TON_MAX_FAULT_RESPONSE. It is not recommended to use 0.

This command has one data byte.

Fault Responses Output Current

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00

APPENDIX C: PMBUS COMMAND DETAILS

IOUT_OC_FAULT_RESPONSE

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an output overcurrent fault. The data byte is in the format given in Table 26.

The device also:

- Sets the IOUT_OC bit in the STATUS_BYTE
- Sets the I_{OUT} bit in the STATUS_WORD
- Sets the I_{OUT} Overcurrent Fault bit in the STATUS_IOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked.

This command has one data byte.

Table 26. IOUT_OC_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4686B: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command • The output is commanded through the RUN*n* pin, the OPERATION command, or the combined action of the RUN*n* pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTM4686B.	00	The LTM4686B continues to operate indefinitely while maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage (known as constant-current or brick-wall limiting).
		01	Not supported.
		10	The LTM4686B continues to operate, maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage, for the delay time set by bits [2:0]. If the device is still operating in current limit at the end of the delay time, the device responds as programmed by the Retry Setting in bits [5:3].
		11	The LTM4686B shuts down immediately and responds as programmed by the Retry Setting in bits [5:3].
5:3	Retry Setting	000–110	The unit does not attempt to restart. The output remains disabled until the fault is cleared by cycling the RUN*n* pin or removing bias power.
		111	The device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN*n* pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	XXX	The number of delay time units in 16ms increments. This delay time is used to determine the amount of time a unit is to continue operating after a fault is detected before shutting down. Only valid for deglitched off state.

Fault Responses IC Temperature

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_OT_FAULT_RESPONSE	0xD6	Action to be taken by the device when an internal overtemperature fault is detected.	R Byte	N	Reg			0xC0

APPENDIX C: PMBUS COMMAND DETAILS

MFR_OT_FAULT_RESPONSE

The MFR_OT_FAULT_RESPONSE command byte instructs the device on what action to take in response to an internal overtemperature fault. The data byte is in the format given in Table 27.

The LTM4686B also:

- Sets the MFR bit in the STATUS_WORD, and
- Sets the Overtemperature Fault bit in the STATUS_MFR_SPECIFIC command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked.

This command has one data byte.

Table 27. Data Byte Contents MFR_OT_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4686B: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command • The output is commanded through the RUN*n* pin, the OPERATION command, or the combined action of the RUN*n* pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTM4686B	00	Not supported. Writing this value will generate a CML fault.
		01	Not supported. Writing this value will generate a CML fault
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared.
		001–111	Not supported. Writing this value will generate CML fault.
2:0	Delay Time	XXX	Not supported. Value ignored

Fault Responses Power Stage Temperature

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
OT_FAULT_ RESPONSE	0x50	Action to be taken by the device when a power stage overtemperature fault is detected,	R/W Byte	Y	Reg		Y	0x80
UT_FAULT_ RESPONSE	0x54	Action to be taken by the device when a power stage undertemperature fault is detected.	R/W Byte	Y	Reg		Y	0x80

OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to a power stage overtemperature fault. The data byte is in the format given in Table 28.

The device also:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the Overtemperature Fault bit in the STATUS_TEMPERATURE command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked.

APPENDIX C: PMBUS COMMAND DETAILS

This condition is detected by the ADC so the response time may be up to 90ms, typical.

This command has one data byte.

UT_FAULT_RESPONSE

The UT_FAULT_RESPONSE command instructs the device on what action to take in response to a power stage under-temperature fault. The data byte is in the format given in Table 28.

The device also:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the Undertemperature Fault bit in the STATUS_TEMPERATURE command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked.

This condition is detected by the ADC so the response time may be up to 90ms, typical.

This command has one data byte.

Table 28. Data Byte Contents: TON_MAX_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE, OT_FAULT_RESPONSE, UT_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4686B: • Sets the corresponding fault bit in the status commands, and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command • The output is commanded through the RUN*n* pin, the OPERATION command, or the combined action of the RUN*n* pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTM4686B	00	The PMBus device continues operation without interruption.
		01	Not supported. Writing this value will generate a CML fault.
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000–110	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN*n* pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	XXX	Not supported. Values ignored

FAULT SHARING

Fault Sharing Propagation

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_GPIO_ PROPAGATE$_n$	0xD2	Configuration that determines which faults are propagated to the $\overline{\text{GPIO}}_n$ pins.	R/W Word	Y	Reg		Y	0x7993

APPENDIX C: PMBUS COMMAND DETAILS

MFR_GPIO_PROPAGATE

The MFR_GPIO_PROPAGATE command enables the faults that can cause the $\overline{GPIO}_n$ pin to assert low. The command is formatted as shown in Table 29. Faults can only be propagated to the $\overline{GPIO}_n$ if they are programmed to respond to faults.

This command has two data bytes.

Table 29. $\overline{GPIO}n$ Propagate Fault Configuration. The $\overline{GPIO0}$ and $\overline{GPIO1}$ pins are designed to provide electrical notification of selected events to the user. Some of these events are common to both output channels. Others are specific to an output channel. They can also be used to share faults between channels.

BIT(S)	SYMBOL	OPERATION
B[15]	V_{OUT} disabled while not decayed.	This is used in a PolyPhase configuration when bit 0 of the MFR_CHAN_CONFIG is a zero. If the channel is turned off, by toggling the RUN pin or commanding the part OFF, and then the RUN is reasserted or the part is commanded back on before the output has decayed, V_{OUT} will not restart until the 12.5% decay is honored. The $\overline{GPIO}n$ pin is asserted during this condition if bit 15 is asserted.
B[14]	Mfr_gpio_propagate_short_CMD_cycle	0: No action 1: Asserts low if commanded off then on before the output has sequenced off. Re-asserts high 120ms after sequence off.
b[13]	Mfr_gpio_propagate_ton_max_fault	0: No action if a TON_MAX_FAULT fault is asserted 1: Associated output will be asserted low if a TON_MAX_FAULT fault is asserted $\overline{GPIO0}$ is associated with page 0 TON_MAX_FAULT faults $\overline{GPIO1}$ is associated with page 1 TON_MAX_FAULT faults
b[12]	Mfr_gpio0_propagate_vout_uvuf, Mfr_gpio1_propagate_vout_uvuf	Unfiltered VOUT_UV_FAULT_LIMIT comparator output $\overline{GPIO0}$ is associated with channel 0 $\overline{GPIO1}$ is associated with channel 1
b[11]	Mfr_gpio0_propagate_int_ot, Mfr_gpio1_propagate_int_ot	0: No action if the MFR_OT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the MFR_OT_FAULT_LIMIT fault is asserted
b[10]	Mfr_pwrgd1_en*	0: No action if channel 1 POWER_GOOD is not true 1: Associated output will be asserted low if channel 1 POWER_GOOD is not true If this bit is asserted, the GPIO_FAULT_RESPONSE must be ignore. If the GPIO_FAULT_RESPONSE is not set to ignore, the part will latch off and never be able to start.
b[9]	Mfr_pwrgd0_en*	0: No action if channel 0 POWER_GOOD is not true 1: Associated output will be asserted low if channel 0 POWER_GOOD is not true If this bit is asserted, the GPIO_FAULT_RESPONSE must be ignore. If the GPIO_FAULT_RESPONSE is not set to ignore, the part will latch off and never be able to start.
b[8]	Mfr_gpio0_propagate_ut, Mfr_gpio1_propagate_ut	0: No action if the UT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the UT_FAULT_LIMIT fault is asserted $\overline{GPIO0}$ is associated with page 0 UT faults $\overline{GPIO1}$ is associated with page 1 UT faults
b[7]	Mfr_gpio0_propagate_ot, Mfr_gpio1_propagate_ot	0: No action if the OT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the OT_FAULT_LIMIT fault is asserted $\overline{GPIO0}$ is associated with page 0 OT faults $\overline{GPIO1}$ is associated with page 1 OT faults
b[6]	Reserved	
b[5]	Reserved	
b[4]	Mfr_gpio0_propagate_input_ov, Mfr_gpio1_propagate_input_ov	0: No action if the VIN_OV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VIN_OV_FAULT_LIMIT fault is asserted

APPENDIX C: PMBUS COMMAND DETAILS

Table 29. $\overline{GPIO}n$ Propagate Fault Configuration. The $\overline{GPIO0}$ and $\overline{GPIO1}$ pins are designed to provide electrical notification of selected events to the user. Some of these events are common to both output channels. Others are specific to an output channel. They can also be used to share faults between channels.

BIT(S)	SYMBOL	OPERATION
b[3]	Reserved	
b[2]	Mfr_gpio0_propagate_iout_oc, Mfr_gpio1_propagate_iout_oc	0: No action if the IOUT_OC_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the IOUT_OC_FAULT_LIMIT fault is asserted $\overline{GPIO0}$ is associated with page 0 OC faults $\overline{GPIO1}$ is associated with page 1 OC faults
b[1]	Mfr_gpio0_propagate_vout_uv, Mfr_gpio1_propagate_vout_uv	0: No action if the VOUT_UV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VOUT_UV_FAULT_LIMIT fault is asserted $\overline{GPIO0}$ is associated with page 0 UV faults $\overline{GPIO1}$ is associated with page 1 UV faults
b[0]	Mfr_gpio0_propagate_vout_ov, Mfr_gpio1_propagate_vout_ov	0: No action if the VOUT_OV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VOUT_OV_FAULT_LIMIT fault is asserted $\overline{GPIO0}$ is associated with page 0 OV faults $\overline{GPIO1}$ is associated with page 1 OV faults

*The PWRGD status is designed as an indicator and not to be used for power supply sequencing.

Fault Sharing Response

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_GPIO_RESPONSE	0xD5	Action to be taken by the device when the $\overline{GPIO}_n$ pin is asserted low.	R/W Byte	Y	Reg		Y	0x00

MFR_GPIO_RESPONSE

This command determines the controller's response to the $\overline{GPIO}_n$ pin being pulled low by an external source.

VALUE	MEANING
0xC0	GPIO_INHIBIT The LTM4686B will three-state the output in response to the $\overline{GPIO}_n$ pin pulled low.
0x00	GPIO_IGNORE The LTM4686B continues operation without interruption.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the MFR bit in the STATUS_WORD
- Sets the GPIOB bit in the STATUS_MFR_SPECIFIC command, and
- Notifies the host by asserting $\overline{ALERT}$ pin, unless masked. The $\overline{ALERT}$ pin pulled low can be disabled by setting bit[1] of MFR_CHAN_CFG.

This command has one data byte.

APPENDIX C: PMBUS COMMAND DETAILS

SCRATCHPAD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
USER_DATA_00	0xB0	OEM reserved. Typically used for part serialization.	R/W Word	N	Reg		Y	NA
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA
USER_DATA_02	0xB2	OEM reserved. Typically used for part serialization.	R/W Word	N	Reg		Y	NA
USER_DATA_03	0xB3	A NVM word available for the user.	R/W Word	Y	Reg		Y	0x0000
USER_DATA_04	0xB4	A NVM word available for the user.	R/W Word	N	Reg		Y	0x0000

USER_DATA_00 through *USER_DATA_04*

These commands are nonvolatile memory locations for customer storage. The customer has the option to write any value to the USER_DATA_nn at any time. However, the LTpowerPlay software and contract manufacturers use some of these commands for inventory control. Modifying the reserved USER_DATA_nn commands may lead to undesirable inventory control and incompatibility with these products.

These commands have 2 data bytes and are in register format.

IDENTIFICATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.2.	R Byte	N	Reg			0x22
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0
MFR_ID	0x99	The manufacturer ID of the LTM4686B in ASCII.	R String	N	ASC			LTC
MFR_MODEL	0x9A	Manufacturer part number in ASCII.	R String	N	ASC			“LTM4686 ”*
MFR_SERIAL	0x9E	Serial number of this specific unit in ASCII.	R Block	N	CF			NA
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTM4686B.	R Word	N	Reg			0x477X

* The MFR_MODEL value is “LTM4686 ”. The value consists of 8 ASCII characters and the last character is a blank space punctuation character (" "), i.e., ASCII code 0x20 or 32d.

PMBus_REVISION

The PMBUS_REVISION command indicates the revision of the PMBus to which the device is compliant. The LTM4686B is PMBus Version 1.2 compliant in both Part I and Part II.

This read-only command has one data byte.

CAPABILITY

This command provides a way for a host system to determine some key capabilities of a PMBus device.

The LTM4686B supports packet error checking, 400kHz bus speeds, and $\overline{\text{ALERT}}$ pin.

This read-only command has one data byte.

MFR_ID

The MFR_ID command indicates the manufacturer ID of the LTM4686B using ASCII characters.

This read-only command is in block format.

APPENDIX C: PMBUS COMMAND DETAILS

MFR_MODEL

The MFR_MODEL command indicates the manufacturer's part number of the LTM4686B using ASCII characters. The MFR_MODEL value is "LTM4686 ". The value consists of 8 ASCII characters and the last character is a blank space punctuation character (" "), i.e., ASCII code 0x20 or 32d.

This read-only command is in block format.

MFR_SERIAL

The MFR_SERIAL command contains up to 9 bytes of custom formatted data used to uniquely identify the LTM4686B configuration.

This read-only command is in block format.

MFR_SPECIAL_ID

The 16-bit word representing the part name. The 0x477 prefix denotes the part is an LTM4686B genre, whereas the X suffix is adjustable by the manufacturer.

This read-only command has 2 data bytes.

FAULT WARNING AND STATUS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				NA
SMBALERT_MASK	0x1B	Mask $\overline{\text{ALERT}}$ Activity.	Block R/W	Y	Reg		Y	See CMD Details
MFR_CLEAR_PEAKS	0xE3	Clears all peaks values.	Send Byte	N				NA
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			NA
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			NA
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			NA
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			NA
STATUS_INPUT	0x7C	Input supply (SV_{IN}) fault and warning status.	R/W Byte	N	Reg			NA
STATUS_ TEMPERATURE	0x7D	TSNS*n*a^{-} sensed fault and warning status for READ_TEMERATURE_1.	R/W Byte	Y	Reg			NA
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			NA
STATUS_MFR_ SPECIFIC	0x80	Manufacturer specific fault and state information.	R/W Byte	Y	Reg			NA
MFR_PADS	0xE5	Digital status of the I/O pads.	R Word	N	Reg			NA
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI ICs/modules.	R Byte	N	Reg			NA
MFR_INFO	0xB6	Manufacturing Specific Information	R Word	N	Reg			NA

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status commands simultaneously. At the same time, the device negates (clears, releases) its $\overline{\text{ALERT}}$ pin signal output if the device is asserting the $\overline{\text{ALERT}}$ pin signal. If the fault is still present when the bit is cleared, the fault bit will remain

APPENDIX C: PMBUS COMMAND DETAILS

set and the host notified by asserting the $\overline{\text{ALERT}}$ pin low. CLEAR_FAULTS can take up to 10µs to process. If a fault occurs within that time frame it may be cleared before the status register is set.

This write-only command has no data bytes.

The CLEAR_FAULTS does not cause a unit that has latched off for a fault condition to restart. Units that have shut down for a fault condition are restarted when:

- The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or
- MFR_RESET or RESTORE_USER_ALL command is issued.
- Bias power is removed and reapplied to the integrated circuit

MFR_CLEAR_PEAKS

The MFR_CLEAR_PEAKS command clears the MFR_*_PEAK data values. A MFR_RESET or RESTORE_USER_ALL will initiate this command.

This write-only command has no data bytes.

SMBALERT_MASK

The SMBALERT_MASK command can be used to prevent a particular status bit or bits from asserting $\overline{\text{ALERT}}$ as they are asserted.

Figure 58 shows an example of the Write Word format used to set an $\overline{\text{ALERT}}$ mask, in this case without PEC. The bits in the mask byte align with bits in the specified status register. For example, if the STATUS_TEMPERATURE command code is sent in the first data byte, and the mask byte contains 0x40, then a subsequent External Overtemperature Warning would still set bit 6 of STATUS_TEMPERATURE but not assert $\overline{\text{ALERT}}$. All other supported STATUS_TEMPERATURE bits would continue to assert $\overline{\text{ALERT}}$ if set.

Figure 59 shows an example of the Block Write – Block Read Process Call protocol used to read back the present state of any supported status register, again without PEC.

SMBALERT_MASK cannot be applied to STATUS_BYTE, STATUS_WORD, MFR_COMMON or MFR_PADS. Factory default masking for applicable status registers is shown below. Providing an unsupported command code to SMBALERT_MASK will generate a CML for Invalid/Unsupported Data.

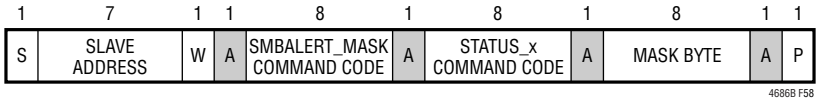


Figure 58. Example of Setting SMBALERT_MASK

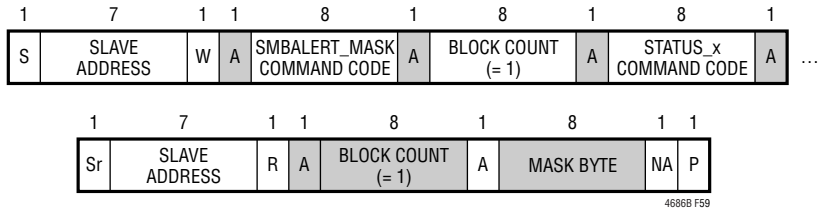


Figure 59. Example of Reading SMBALERT_MASK

APPENDIX C: PMBUS COMMAND DETAILS

SMBALERT_MASK Default Setting: (Refer Also to Summary of the Status Registers, Figure 60)

STATUS RESISTER	ALERT Mask Value	MASKED BITS
STATUS_VOUT*n*	0x00	None
STATUS_IOUT*n*	0x00	None
STATUS_TEMPERATURE*n*	0x00	None
STATUS_CML	0x00	None
STATUS_INPUT	0x00	None
STATUS_MFR_SPECIFIC*n*	0x11	Bit 4 (internal PLL unlocked), bit 0 ($\overline{\text{GPIO}}n$ pulled low by external device)

STATUS_BYTE

The STATUS_BYTE command returns a one-byte summary of the most critical faults.

STATUS_BYTE Message Contents:

BIT	STATUS BIT NAME	MEANING
7	BUSY	A fault was declared because the LTM4686B was unable to respond.
6	OFF	This bit is set if the channel is not providing power to its output, regardless of the reason, including simply not being enabled.
5	VOUT_OV	An output overvoltage fault has occurred.
4	IOUT_OC	An output overcurrent fault has occurred.
3	VIN_UV	Not supported (LTM4686B returns 0).
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	NONE OF THE ABOVE	A fault Not listed in bits[7:1] has occurred.

This command has one data byte

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

STATUS_WORD

The STATUS_WORD command returns a two-byte summary of the channel's fault condition. The low byte of the STATUS_WORD is the same as the STATUS_BYTE command.

STATUS_WORD High Byte Message Contents:

BIT	STATUS BIT NAME	MEANING
15	V_{OUT}	An output voltage fault or warning has occurred.
14	I_{OUT}	An output current fault or warning has occurred.
13	INPUT	An SV_{IN} input voltage fault or warning has occurred.
12	MFR_SPECIFIC	A fault or warning specific to the LTM4686B has occurred.
11	POWER_GOOD#	The POWER_GOOD state is false if this bit is set.
10	FANS	Not supported (LTM4686B returns 0).
9	OTHER	Not supported (LTM4686B returns 0).
8	UNKNOWN	Not supported (LTM4686B returns 0).

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has two data bytes.

APPENDIX C: PMBUS COMMAND DETAILS

STATUS_VOUT

The STATUS_VOUT command returns one byte of V_{OUT} status information.

STATUS_VOUT Message Contents:

BIT	MEANING
7	V_{OUT} overvoltage fault.
6	V_{OUT} overvoltage warning.
5	V_{OUT} undervoltage warning.
4	V_{OUT} undervoltage fault.
3	VOUT_MAX warning.
2	TON_MAX fault.
1	TOFF_MAX warning.
0	Not supported by the LTM4686B (returns 0).

$\overline{ALERT}$ can be asserted if any of bits[7:1] are set. These may be cleared by writing a 1 to their bit position in STATUS_VOUT, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_IOUT

The STATUS_IOUT command returns one byte of I_{OUT} status information.

STATUS_IOUT Message Contents:

BIT	MEANING
7	I_{OUT} overcurrent fault.
6	Not supported (LTM4686B returns 0).
5	I_{OUT} overcurrent warning.
4:0	Not supported (LTM4686B returns 0).

$\overline{ALERT}$ can be asserted if any supported bits are set. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_IOUT, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_INPUT

The STATUS_INPUT command returns one byte of V_{IN} (SV_{IN}) status information.

STATUS_INPUT Message Contents:

BIT	MEANING
7	SV_{IN} overvoltage fault.
6	Not supported (LTM4686B returns 0).
5	SV_{IN} undervoltage warning.
4	Not supported (LTM4686B returns 0).
3	Unit off for insufficient SV_{IN} voltage.
2	Not supported (LTM4686B returns 0).
1	Input over current warning.
0	Not supported (LTM4686B returns 0)

$\overline{ALERT}$ can be asserted if bit 7 is set. Bit 7 may be cleared by writing it to a 1, in lieu of a CLEAR_FAULTS command.

APPENDIX C: PMBUS COMMAND DETAILS

This command has one data byte.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns one byte of sensed power stage temperature status information.

STATUS_TEMPERATURE Message Contents:

BIT	MEANING
7	External overtemperature fault.
6	External overtemperature warning.
5	Not supported (LTM4686B returns 0).
4	External undertemperature fault.
3:0	Not supported (LTM4686B returns 0).

$\overline{\text{ALERT}}$ can be asserted if any supported bits are set. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_TEMPERATURE, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_CML

The STATUS_CML command returns one byte of status information on received commands, internal memory and logic.

STATUS_CML Message Contents:

BIT	MEANING
7	Invalid or unsupported command received.
6	Invalid or unsupported data received.
5	Packet error check failed.
4	Memory fault detected.
3	Processor fault detected.
2	Reserved (LTM4686B returns 0).
1	Other communication fault.
0	Other memory or logic fault.

$\overline{\text{ALERT}}$ can be asserted if any supported bits are set. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_CML, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC commands returns one byte with the manufacturer specific status information. Each channel has a copy of the same information. Only bit 0 is page specific. The format for this byte is:

BIT	MEANING
7	Internal Temperature Fault Limit Exceeded.
6	Internal Temperature Warn Limit Exceeded.
5	NVM CRC Fault.
4	PLL is Unlocked
3	Fault Log Present
2	V_{DD33} UV or OV Fault
0	$\overline{\text{GPIO}}_n$ Pin Asserted Low by External Device (paged)

APPENDIX C: PMBUS COMMAND DETAILS

If any of these bits are set, the MFR bit in the STATUS_WORD will be set.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command. Exception: The fault log present bit can only be cleared by issuing the MFR_FAULT_LOG_CLEAR command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

MFR_PADS

This command provides the user a means of directly reading the digital status of the I/O pins of the device. The bit assignments of this command are as follows:

BIT	ASSIGNED DIGITAL PIN
15	V_{DD33} OV Fault
14	V_{DD33} UV Fault
13	Reserved
12	Reserved
11	ADC Values Invalid, Occurs During Start-Up
10	SYNC Output Disabled Due to External Clock
9	PowerGood1
8	PowerGood0
7	Device Driving RUN1 Low
6	Device Driving RUN0 Low
5	RUN1
4	RUN0
3	Device Driving $\overline{\text{GPIO1}}$ Low
2	Device Driving $\overline{\text{GPIO0}}$ Low
1	$\overline{\text{GPIO1}}$
0	$\overline{\text{GPIO0}}$

A 1 indicates the condition is true.

This read-only command has two data bytes.

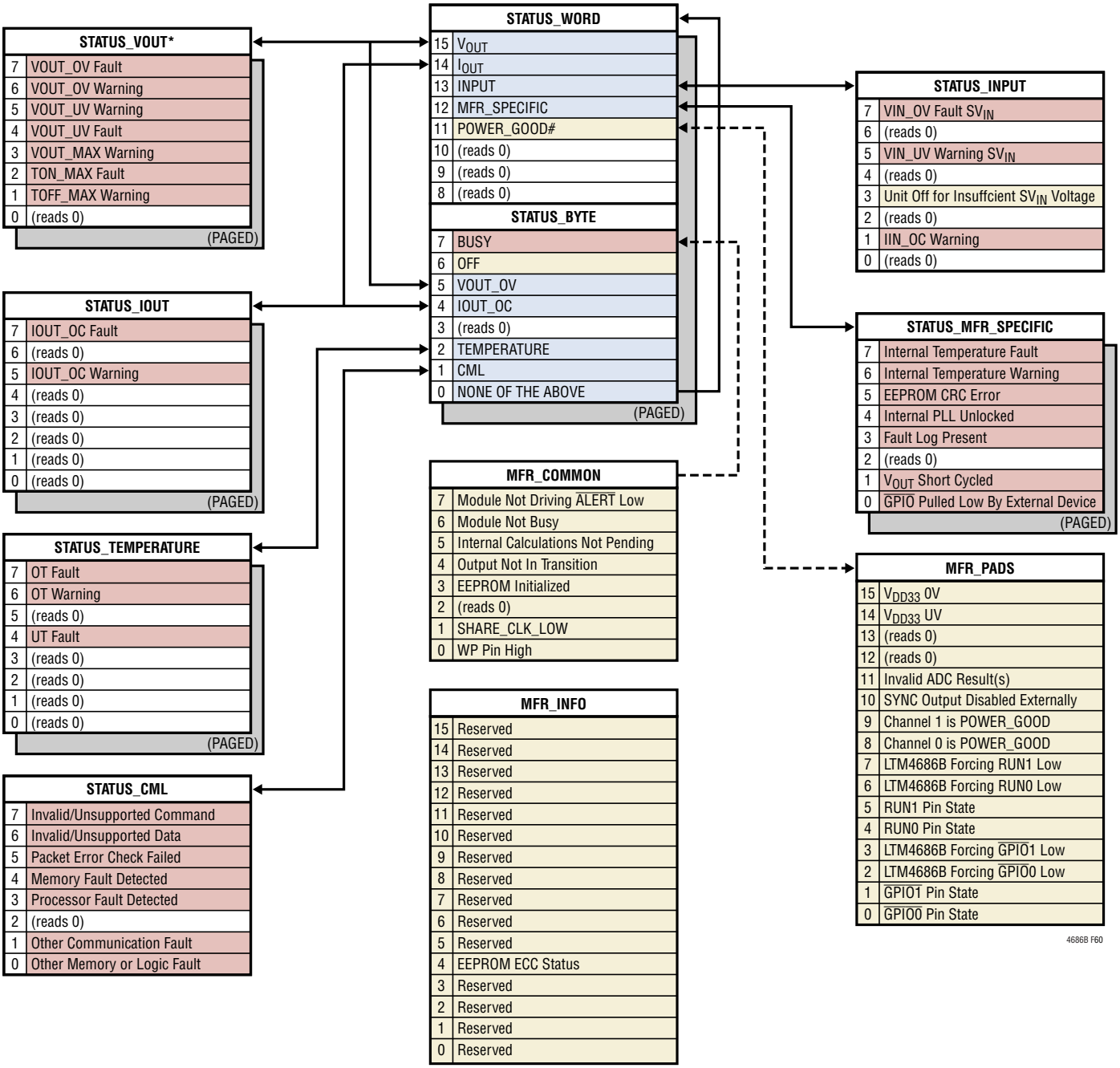
MFR_COMMON

The MFR_COMMON command contains bits that are common to all ADI digital power and telemetry products.

BIT	MEANING
7	MODULE NOT DRIVING $\overline{\text{ALERT}}$ LOW
6	MODULE NOT BUSY
5	CALCULATIONS NOT PENDING
4	OUTPUT NOT IN TRANSITION
3	NVM Initialized
2	Reserved
1	SHARE_CLK Timeout
0	WP Pin Status

This read-only command has one data byte.

APPENDIX C: PMBUS COMMAND DETAILS



DESCRIPTION	MASKABLE	GENERATES ALERT	BIT CLEARABLE
General Fault or Warning Event	Yes	Yes	Yes
Dynamic	No	No	No
Status Derived from Other Bits	No	Not Directly	No

Figure 60. Summary of the Status Registers

APPENDIX C: PMBUS COMMAND DETAILS

MFR_INFO

The MFR_INFO command contains additional status bits that are LTM4686B-specific and may be common to multiple ADI PSM products.

MFR_INFO Data Contents

BIT	MEANING
15:6	Reserved.
5	EEPROM ECC status. 0: Corrections have been made in the EEPROM user space. 1: No corrections have been made in the EEPROM user space.
4:0	Reserved

EEPROM ECC status is updated after each RESTORE_USER_ALL or RESET command, a power-on reset or an EEPROM bulk read operation. This read-only command has two data bytes.

TELEMETRY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
READ_VIN	0x88	Measured input supply (SV_{IN}) voltage.	R Word	N	L11	V		NA
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	L16	V		NA
READ_IIN	0x89	Calculated input supply current.	R Word	N	L11	A		NA
MFR_READ_IIN	0xED	Calculated input current per channel.	R Word	Y	L11	A		NA
READ_IOUT	0x8C	Measured output current.	R Word	Y	L11	A		NA
READ_TEMPERATURE_1	0x8D	Power stage temperature sensor. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	C		NA
READ_TEMPERATURE_2	0x8E	Control IC die temperature. Does not affect any other registers.	R Word	N	L11	C		NA
READ_DUTY_CYCLE	0x94	Duty cycle of the top gate control signal.	R Word	Y	L11	%		NA
READ_POUT	0x96	Calculated output power.	R Word	Y	L11	W		NA
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		NA
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.	R Word	N	L11	V		NA
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of power stage temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.	R Word	Y	L11	C		NA
MFR_TEMPERATURE_2_PEAK	0xF4	Maximum measured value of control IC die temperature (READ_TEMPERATURE_2) since last MFR_CLEAR_PEAKS.	R Word	N	L11	C		NA
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		NA
MFR_ADC_CONTROL	0xD8	ADC telemetry parameter selected for repeated fast ADC read back.	R/W Byte	N	Reg			0x00
MFR_ADC_TELEMETRY_STATUS	0xDA	ADC telemetry status indicating which parameter is most recently converted when the short round robin ADC loop is enabled	R/W Byte	N	Reg			NA

APPENDIX C: PMBUS COMMAND DETAILS

READ_VIN

The READ_VIN command returns the measured SV_{IN} input voltage, in volts.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_VOUT

The READ_VOUT command returns the measured output voltage in the same format as set by the VOUT_MODE command.

This read-only command has two data bytes and is formatted in Linear_16u format.

READ_IIN

The READ_IIN command returns the input current in Amperes. Note: Input current is calculated from READ_IOUT current and the READ_DUTY_CYCLE value from both outputs plus the MFR_IIN_OFFSET. For accurate values at low currents the part must be in continuous conduction mode. The greatest source of error if DCR sensing is used, is the accuracy of the inductor parasitic DC resistance (DCR) at room temperature IOUT_CAL_GAIN.

$READ\_IIN = MFR\_READ\_IIN_{\_PAGE0} + MFR\_READ\_IIN_{\_PAGE1}$

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_READ_IIN

The MFR_READ_IIN command is a paged reading of the input current that applies the paged MFR_IIN_OFFSET parameter. This calculation is similar to READ_IIN except the paged values are used.

$MFR\_READ\_IIN = MFR\_IIN\_OFFSET + (I_{OUT} \bullet DUTY\_CYCLE)$

This command has 2 data bytes and is formatted in Linear_5s_11s format.

READ_IOUT

The READ_IOUT command returns the average output current in amperes. The IOUT value is a function of:

a) the differential voltage derived from the power inductor ΔI_{SNSn}

b) the IOUT_CAL_GAIN value

c) the MFR_IOUT_CAL_GAIN_TC value, and

d) READ_TEMPERATURE_1 value

e) The MFR_TEMP_1_GAIN and the MFR_TEMP_1_OFFSET

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the temperature, in degrees Celsius, of the external sense element.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

APPENDIX C: PMBUS COMMAND DETAILS

READ_TEMPERATURE_2

The READ_TEMPERATURE_2 command returns the temperature, in degrees Celsius, of the internal sense element.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_DUTY_CYCLE

The READ_DUTY_CYCLE command returns the duty cycle of controller, in percent.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_POUT

The READ_POUT command is a paged reading of the DC/DC converter output power in Watts. The POUT is calculated based on the most recent correlated output voltage and current readings.

This command has 2 data bytes and is formatted in Linear_5s_11s format.

MFR_VOUT_PEAK

The MFR_VOUT_PEAK command reports the highest voltage, in volts, reported by the READ_VOUT measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_16u format.

MFR_VIN_PEAK

The MFR_VIN_PEAK command reports the highest voltage, in volts, reported by the READ_VIN measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_TEMPERATURE_1_PEAK

The MFR_TEMPERATURE_1_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_1 measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_TEMPERATURE_2_PEAK

The MFR_TEMPERATURE_2_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_2 measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

APPENDIX C: PMBUS COMMAND DETAILS

MFR_IOUT_PEAK

The MFR_IOUT_PEAK command reports the highest current, in amperes, reported by the READ_IOUT measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_ADC_CONTROL

The MFR_ADC_CONTROL command determines the ADC read back selection. A default value of 0 in the command runs the standard telemetry loop with all parameters updated in a round robin fashion with a typical latency of 90ms. The user can command a non-zero value to monitored a single parameter with an approximate update rate of 8ms. This command has a latency of up to two ADC conversions or approximately 16ms (power stage temperature conversions may have a latency of up to three ADC conversion or approximately 24ms). Selecting a value of 0x0D will enable a short round robin loop. This commanded value runs a short telemetry loop only selecting V_{OUT0}, I_{OUT0}, V_{OUT1} and I_{OUT1} in a round robin manner. The round robin typical latency is 27ms. It is recommended the part remain in standard telemetry mode except for special cases where fast ADC updates of a single parameter is required. The part should be commanded to monitor the desired parameter for a limited period of time (say, less than a second) then set the command back to standard round robin mode. If this command is set to any value except standard round robin telemetry (0) all warnings and faults associated with telemetry other than the selected parameter are effectively disabled and voltage servoing is disabled. When round robin is reasserted, all warnings and faults and servo mode are re-enabled.

COMMANDED VALUE	TELEMETRY SELECTED
0x00	Standard ADC Round Robin Telemetry
0x01	SV_{IN}
0x02	Reserved
0x03	Reserved
0x04	Internal IC Temperature
0x05	Channel 0 V_{OUT}
0x06	Channel 0 I_{OUT}
0x07	Reserved
0x08	Channel 0 Power Stage-Sensed Temperature
0x09	Channel 1 V_{OUT}
0x0A	Channel 1 I_{OUT}
0x0B	Reserved
0x0C	Channel 1 Power Stage or TSNS1a-Sensed Temperature
0x0D	ADC Short Round Robin
0x0E – 0xFF	Reserved

If a reserved command value is entered, the part will default to Internal IC Temperature and issue a CML[6] fault. CML[6] faults will continue to be issued by the LTM4686B until a valid command value is entered.

This read/write command has 1 data byte and is formatted in register format.

APPENDIX C: PMBUS COMMAND DETAILS

MFR_ADC_TELEMETRY_STATUS

The MFR_ADC_TELEMETRY_STATUS command provides the user the means to determine the most recent ADC conversion when the MFR_ADC_CONTROL short round robin loop is enabled using command 0xD8 value 0x0D. The bit assignments of this command are as follows:

BIT	TELEMETRY DATA AVAILABLE
7	Reserved returns 0
6	Reserved returns 0
5	Reserved returns 0
4	Reserved returns 0
3	Channel 1 I_{OUT} readback (I_{OUT1})
2	Channel 1 V_{OUT} readback (V_{OUT1})
1	Channel 0 I_{OUT} readback (I_{OUT0})
0	Channel 0 V_{OUT} readback (V_{OUT0})

Write to MFR_ADC_TELEMETRY_STATUS with data bits set to 1 clear the respective bits.

This read/write command has 1 data byte and is formatted in register format.

NVM (EEPROM) MEMORY COMMANDS

Store/Restore

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				NA
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM. Identical to MFR_RESET.	Send Byte	N				NA
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with NVM.	Send Byte	N				NA

STORE_USER_ALL

The STORE_USER_ALL command instructs the PMBus device to copy the nonvolatile user contents of the Operating Memory to the matching locations in the nonvolatile User NVM memory (EEPROM).

The 10 year data retention can only be guaranteed when STORE_USER_ALL is executed at $0°C \le T_J \le 85°C$. Executing this command at junction temperatures above 85°C or below 0°C is not recommended because data retention cannot be guaranteed for that condition. If the die temperature exceeds 130°C, the STORE_USER_ALL command is disabled. The command is re-enabled when the IC temperature drops below 125°C.

Communication with the LTM4686B and programming of the EEPROM can be initiated when VDD33 is available and SV_{IN} is not applied. To enable the part in this state, using global address 0x5B write 0x2B followed by 0xC4. The part can now be communicated with, and the project file updated. To write the updated project file to the EEPROM issue a STORE_USER_ALL command. When SV_{IN} is applied, a MFR_RESET or RESTORE_USER_ALL must be issued to allow the PWM to be enabled and valid ADCs to be read.

This write-only command has no data bytes.

APPENDIX C: PMBUS COMMAND DETAILS

RESTORE_USER_ALL

The RESTORE_USER_ALL command provides an alternate means by which the user can perform a MFR_RESET of the LTM4686B.

This write-only command has no data bytes.

MFR_COMPARE_USER_ALL

The MFR_COMPARE_USER_ALL command instructs the PMBus device to compare current command contents with what is stored in nonvolatile memory. If the compare operation detects differences, a CML bit 0 fault will be generated.

MFR_COMPARE_USER_ALL commands are disabled if the die exceeds 130°C and are not re-enabled until the die temperature drops below 125°C.

This write-only command has no data bytes.

Fault Log Operation

A conceptual diagram of the fault log is shown in Figure 61. The fault log provides telemetry recording capability to the LTM4686B. During normal operation the contents of the status registers, the output voltage readings, temperature readings as well as peak values of these quantities are stored in a continuously updated buffer in RAM. The operation is similar to a strip chart recorder. When a fault occurs, the contents are written into EEPROM for nonvolatile storage. The EEPROM fault log is then locked. The part can be powered down with the fault log available for reading at a later time. As a consequence of adding ECC, the area in the EEPROM available for fault log is reduced. When reading the fault log from RAM all 6 events of cyclical data remain. However, when the fault log is read from EEPROM (after a reset), the last 2 events are lost. The read length of 147 bytes remains the same, but the fifth and sixth events are a repeat of the fourth event.

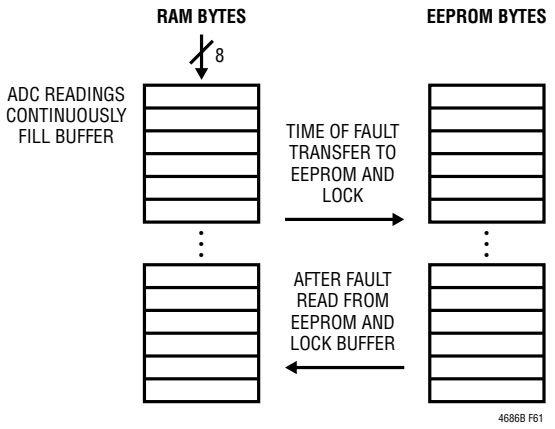


Figure 61. Fault Log Conceptual Diagram

APPENDIX C: PMBUS COMMAND DETAILS

Table 30. Fault Logging

This table outlines the format of the block data from a read block data of the MFR_FAULT_LOG command.

Data Format Definitions				LIN 11 = PMBus = Rev 1.2, Part 2, section 7.1
				LIN 16 = PMBus Rev 1.2, Part 2, section 8. Mantissa portion only
				BYTE = 8 bits interpreted per definition of this command
DATA	**BITS**	**DATA FORMAT**	**BYTE NUM**	**BLOCK READ COMMAND**
Block Length		BYTE	147	The MFR_FAULT_LOG command is a fixed length of 147 bytes The block length will be zero if a data log event has not been captured
HEADER INFORMATION				
Fault Log Preface	[7:0]	ASC	0	Returns LTxx beginning at byte 0 if a partial or complete fault log exists. Word xx is a factory identifier that may vary part to part.
	[7:0]		1	
	[15:8]	Reg	2	
	[7:0]		3	
Fault Source	[7:0]	Reg	4	Refer to Table 31.
MFR_REAL_TIME	[7:0]	Reg	5	48 bit share-clock counter value when fault occurred (200µs resolution).
	[15:8]		6	
	[23:16]		7	
	[31:24]		8	
	[39:32]		9	
	[47:40]		10	
MFR_VOUT_PEAK (PAGE 0)	[15:8]	L16	11	Peak READ_VOUT on Channel 0 since last power-on or CLEAR_PEAKS command.
	[7:0]		12	
MFR_VOUT_PEAK (PAGE 1)	[15:8]	L16	13	Peak READ_VOUT on Channel 1 since last power-on or CLEAR_PEAKS command.
	[7:0]		14	
MFR_IOUT_PEAK (PAGE 0)	[15:8]	L11	15	Peak READ_IOUT on Channel 0 since last power-on or CLEAR_PEAKS command.
	[7:0]		16	
MFR_IOUT_PEAK (PAGE 1)	[15:8]	L11	17	Peak READ_IOUT on Channel 1 since last power-on or CLEAR_PEAKS command.
	[7:0]		18	
MFR_VIN_PEAK	[15:8]	L11	19	Peak READ_VIN since last power-on or CLEAR_PEAKS command.
	[7:0]		20	
READ_TEMPERATURE1 (PAGE 0)	[15:8]	L11	21	Channel 0 power stage during last event.
	[7:0]		22	
READ_TEMPERATURE1 (PAGE 1)	[15:8]	L11	23	Channel 1 power stage or TSNS1a⁻ sensed temperature 1 during last event.
	[7:0]		24	
READ_TEMPERATURE2	[15:8]	L11	25	Internal temperature sensor during last event.
	[7:0]		26	

APPENDIX C: PMBUS COMMAND DETAILS

Table 30. Fault Logging

This table outlines the format of the block data from a read block data of the MFR_FAULT_LOG command.

CYCLICAL DATA				
EVENT n **(Data at Which Fault Occurred; Most Recent Data)**				Event "n" represents one complete cycle of ADC reads through the MUX at time of fault. Example: If the fault occurs when the ADC is processing step 15, it will continue to take readings through step 25 and then store the header and all 6 event pages to EEPROM
READ_VOUT (PAGE 0)	[15:8]	LIN 16	27	
	[7:0]	LIN 16	28	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	29	
	[7:0]	LIN 16	30	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	31	
	[7:0]	LIN 11	32	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	33	
	[7:0]	LIN 11	34	
READ_VIN	[15:8]	LIN 11	35	
	[7:0]	LIN 11	36	
READ_IIN	[15:8]	LIN 11	37	
	[7:0]	LIN 11	38	
STATUS_VOUT (PAGE 0)		BYTE	39	
STATUS_VOUT (PAGE 1)		BYTE	40	
STATUS_WORD (PAGE 0)	[15:8]	WORD	41	
	[7:0]	WORD	42	
STATUS_WORD (PAGE 1)	[15:8]	WORD	43	
	[7:0]	WORD	44	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	45	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	46	
EVENT n–1 **(data measured before fault was detected)**				
READ_VOUT (PAGE 0)	[15:8]	LIN 16	47	
	[7:0]	LIN 16	48	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	49	
	[7:0]	LIN 16	50	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	51	
	[7:0]	LIN 11	52	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	53	
	[7:0]	LIN 11	54	
READ_VIN	[15:8]	LIN 11	55	
	[7:0]	LIN 11	56	
READ_IIN	[15:8]	LIN 11	57	
	[7:0]	LIN 11	58	

APPENDIX C: PMBUS COMMAND DETAILS

Table 30. Fault Logging

This table outlines the format of the block data from a read block data of the MFR_FAULT_LOG command.

STATUS_VOUT (PAGE 0)		BYTE	59	
STATUS_VOUT (PAGE 1)		BYTE	60	
STATUS_WORD (PAGE 0)	[15:8]	WORD	61	
	[7:0]	WORD	62	
STATUS_WORD (PAGE 1)	[15:8]	WORD	63	
	[7:0]	WORD	64	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	65	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	66	
*				
*				
*				
EVENT n–5 (Oldest Recorded Data)				
READ_VOUT (PAGE 0)	[15:8]	LIN 16	127	
	[7:0]	LIN 16	128	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	129	
	[7:0]	LIN 16	130	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	131	
	[7:0]	LIN 11	132	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	133	
	[7:0]	LIN 11	134	
READ_VIN	[15:8]	LIN 11	135	
	[7:0]	LIN 11	136	
READ_IIN	[15:8]	LIN 11	137	
	[7:0]	LIN 11	138	
STATUS_VOUT (PAGE 0)		BYTE	139	
STATUS_VOUT (PAGE 1)		BYTE	140	
STATUS_WORD (PAGE 0)	[15:8]	WORD	141	
	[7:0]	WORD	142	
STATUS_WORD (PAGE 1)	[15:8]	WORD	143	
	[7:0]	WORD	144	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	145	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	146	

APPENDIX C: PMBUS COMMAND DETAILS

Table 31. Explanation of Position_Fault Values

POSITION_FAULT VALUE	SOURCE OF FAULT LOG
0xFF	MFR_FAULT_LOG_STORE
0x00	TON_MAX_FAULT Channel 0
0x01	VOUT_OV_FAULT Channel 0
0x02	VOUT_UV_FAULT Channel 0
0x03	IOUT_OC_FAULT Channel 0
0x05	OT_FAULT Channel 0
0x06	UT_FAULT Channel 0
0x07	VIN_OV_FAULT Channel 0
0x0A	MFR_OT_FAULT Channel 0
0x10	TON_MAX_FAULT Channel 1
0x11	VOUT_OV_FAULT Channel 1
0x12	VOUT_UV_FAULT Channel 1
0x13	IOUT_OC_FAULT Channel 1
0x15	OT_FAULT Channel 1
0x16	UT_FAULT Channel 1
0x17	VIN_OV_FAULT Channel 1
0x1A	MFR_OT_FAULT Channel 1

Fault Logging

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	R Block	N	CF		Y	NA
MFR_FAULT_LOG_ STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging.	Send Byte	N				NA

MFR_FAULT_LOG

The MFR_FAULT_LOG command allows the user to read the contents of the FAULT_LOG after the first fault occurrence since the last MFR_FAULT_LOG_CLEAR command was last written. The contents of this command are stored in non-volatile memory, and are cleared by the MFR_FAULT_LOG_CLEAR command. The length and content of this command are listed in Table 30. If the user accesses the MFR_FAULT_LOG command and no fault log is present, the command will return a data length of 0. If a fault log is present, the MFR_FAULT_LOG will always return a block of data 147 bytes long. If a fault occurs within the first second of applying power, some of the earlier pages in the fault log may not contain valid data.

NOTE: The approximate transfer time for this command is 3.4ms using a 400kHz clock.

This read-only command is in block format.

APPENDIX C: PMBUS COMMAND DETAILS

MFR_FAULT_LOG_STORE

The MFR_FAULT_LOG_STORE command forces the fault log operation to be written to EEPROM just as if a fault event occurred. This command will generate a MFR_SPECIFIC fault if the “Enable Fault Logging” bit is set in the MFR_CONFIG_ALL command.

If the die temperature exceeds 130°C, the MFR_FAULT_LOG_STORE command is disabled until the IC temperature drops below 125°C.

Up-Time Counter is in the Fault Log header. The counter is the time since the last module reset (MFR_RESET, RESTORE_USER_ALL, or SV_{IN} – power cycle) in 200µs increments. This is a 48-bit binary counter.

This write-only command has no data bytes.

MFR_FAULT_LOG_CLEAR

The MFR_FAULT_LOG_CLEAR command will erase the fault log file stored values. It will also clear bit 3 in the STATUS_MFR_SPECIFIC command. After a clear is issued, the status can take up to 8ms to clear.

This write-only command is send bytes.

Block Memory Write/Read

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA

All the (EEPROM) commands are disabled if the die temperature exceeds 130°C. (EEPROM) commands are re-enabled when the die temperature drops below 125°C.

MFR_EE_xxxx

MFR_EE_XXXX commands are used to facilitate bulk programming of the internal EEPROM. Contact the factory for more details.

PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

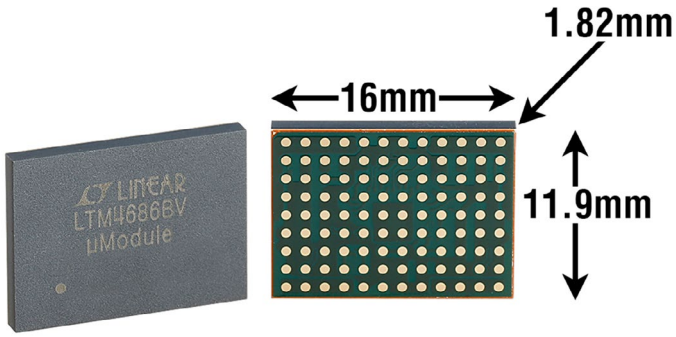
Table 32. LTM4686B LGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT0}	B1	V_{OUT0}	C1	V_{OUT0}	D1	V_{OUT0}	E1	GND	F1	GND
A2	GND	B2	GND	C2	GND	D2	GND	E2	$\overline{GPIO0}$	F2	$\overline{GPIO1}$
A3	GND	B3	GND	C3	TSNS0	D3	TSNS0	E3	$\overline{ALERT}$	F3	RUN0
A4	GND	B4	GND	C4	GND	D4	SDA	E4	SCL	F4	RUN1
A5	GND	B5	GND	C5	GND	D5	GND	E5	SYNC	F5	SGND
A6	GND	B6	GND	C6	GND	D6	COMP0b	E6	COMP0a	F6	SGND
A7	GND	B7	GND	C7	GND	D7	V_{OSNS0}^{+}	E7	V_{OSNS0}^{-}	F7	$INTV_{CC}$
A8	GND	B8	SW0	C8	GND	D8	V_{ORB0}^{+}	E8	V_{ORB0}^{-}	F8	GND
A9	V_{IN0}	B9	V_{IN0}	C9	V_{IN0}	D9	V_{IN0}	E9	GND	F9	SV_{IN}

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	GND	J1	V_{OUT1}	K1	V_{OUT1}	L1	V_{OUT1}	M1	V_{OUT1}
G2	ASEL	H2	$F_{SWPHCFG}$	J2	GND	K2	GND	L2	GND	M2	GND
G3	$V_{OUT0CFG}$	H3	$V_{TRIM0CFG}$	J3	TSNS1a	K3	TSNS1b	L3	GND	M3	GND
G4	$V_{OUT1CFG}$	H4	$V_{TRIM1CFG}$	J4	V_{DD25}	K4	WP	L4	GND	M4	GND
G5	SGND	H5	SHARE_CLK	J5	V_{DD33}	K5	GND	L5	GND	M5	GND
G6	SGND	H6	COMP1a	J6	COMP1b	K6	GND	L6	GND	M6	GND
G7	$INTV_{CC}$	H7	V_{OSNS1}	J7	V_{ORB1}	K7	GND	L7	GND	M7	GND
G8	GND	H8	GND	J8	GND	K8	GND	L8	SW1	M8	GND
G9	GND	H9	GND	J9	V_{IN1}	K9	V_{IN1}	L9	V_{IN1}	M9	V_{IN1}

PACKAGE PHOTOS

Part marking is either ink mark or laser mark



PACKAGE DESCRIPTION

LGA Package
108-Lead (16mm × 11.9mm × 1.82mm)
(Reference DWG # 05-08-1563)

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.72	1.82	1.92	
b	0.60	0.63	0.66	
D		16.00		
E		11.90		
e		1.27		
F		13.97		
G		10.16		
H1		0.32 REF		
H2		1.50 REF		
aaa			0.15	
bbb			0.10	
eee			0.15	
TOTAL NUMBER OF LGA PADS: 108				

TYPICAL APPLICATION

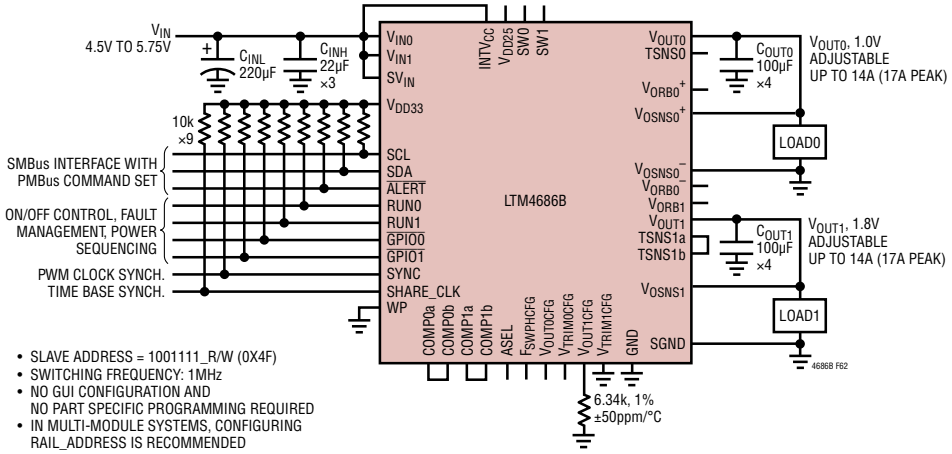
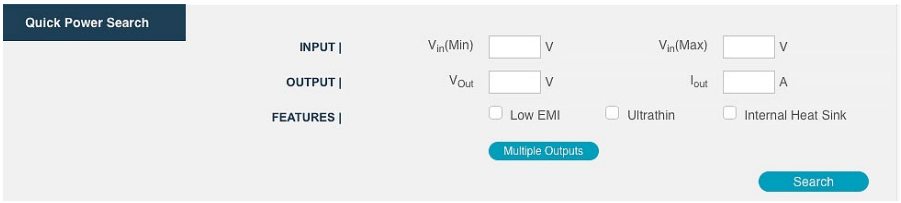


Figure 62. 14A, 1V and 14A, 1.8V Output DC/DC µModule Regulator with Serial Interface

DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4686/ LTM4686-1	Ultrathin Dual 10A or Single 20A µModule Regulator with Digital Power System Management	$4.5V \le V_{IN} \le 17V$ (LTM4686), $2.375V \le V_{IN} \le 17V$ with 5V Bias (LTM4686-1), $0.6V \le V_{OUT} \le 3.6V$, 11.9mm × 16mm × 1.82mm LGA
LTM4631	Ultrathin Dual 10A or Single 20A µModule Regulator Non-PMBus	$4.5V \le V_{IN} \le 15V$, $0.6V \le V_{OUT} \le 1.8V$, 16mm × 16mm × 1.91mm LGA
LTM4673	Dual 12A and Dual 5A, Quad Output µModule Regulator with Digital Power System Management	$4.5V \le V_{IN} \le 15V$, $0.6V \le V_{OUT} \le 3.3V$ (12A Rails), $0.6V \le V_{OUT} \le 5.5V$ (5A Rails), 16mm × 16mm × 4.72mm BGA
LTM4675	Dual 9A or Single 18A Step-Down µModule Regulator with Digital Power System Management	$4.5V \le V_{IN} \le 17V$, $0.5V \le V_{OUT} \le 5.5V$, 11.9mm × 16mm × 3.51mm BGA
LTM4676A	Dual 13A or Single 26A Step-Down µModule Regulator with Digital Power System Management	$4.5V \le V_{IN} \le 26.5V$, $0.5V \le V_{OUT} \le 5.5V$, 16mm × 16mm × 5.01mm BGA
LTM4677	Dual 18A or Single 36A Step-Down µModule Regulator with Digital Power System Management	$4.5V \le V_{IN} \le 16V$, $0.6V \le V_{OUT} \le 1.8V$, 16mm × 16mm × 5.01mm BGA