Low Profile Quad 31.25A or Single 125A µModule Regulator with Digital Power System Management

FEATURES

- **Quad Digitally Adjustable Analog Loops with Digital Interface for Control and Monitoring**
- **Wide Input Voltage Range: 4.5V to 16V**
- **Output Voltage Range: 0.7V to 1.35V**
- **±0.5% DC Output Accuracy at 0.75V**
- **±4.5% Current Readback Accuracy: 0°C to 125°C**
- **Optimized for Low Output Voltage Ranges**
- **400kHz PMBus-Compliant I²C Serial Interface**
- **Supports Telemetry Polling Rates Up to 125Hz**
- **Integrated 16-Bit ΔΣ ADC**
- **Parallel and Current Share Multiple Modules**
- 15mm × 22mm × 5.71mm BGA Package

Readable Data

- Input and Output Voltages, Currents, and Temperatures
- Running Peak Values, Uptime, Faults and Warnings
- Onboard EEPROM Fault Log Record

Writable Data and Configurable Parameters

- Output Voltage, Voltage Sequencing and Margining
- Digital Soft-Start/Stop Ramp, Program Analog Loop
- OV/UV/OT, UVLO, Frequency and Phasing

APPLICATIONS

- Multi-Rail Processor Power, Configurable Core Power

DESCRIPTION

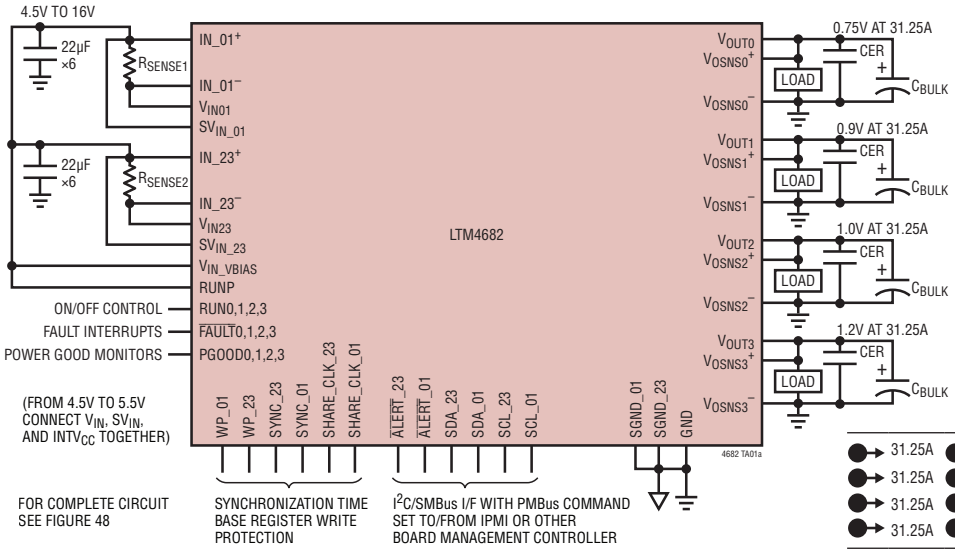
The LTM®4682 is a quad 31.25A or single 125A step-down power µModule® (power micromodule) DC/DC regulator featuring remote configurability and telemetry monitoring of power management parameters over PMBus. The LTM4682 is comprised of digitally programmable analog control loops, and is optimized for higher bandwidth and transient response.

The LTM4682's 2-wire serial interface allows outputs to be margined, tuned, and ramped up and down at programmable slew rates with sequencing delay times. True input current sense, output currents, output voltages, output power, temperatures, uptime, and peak values are readable. Custom configuration of the EEPROM contents is not required. At start-up, output voltages, switching frequency, and channel phase angle assignments can be set by pin-strapping resistors. The LTpowerPlay® graphical user interface (GUI), the DC1613A USB-to-PMBus converter, and evaluation kits are available.

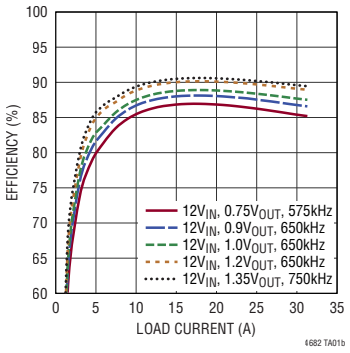
The LTM4682 is offered in a 15mm × 22mm × 5.71mm BGA package available with an SnPb or a RoHS-compliant terminal finish.

TYPICAL APPLICATION

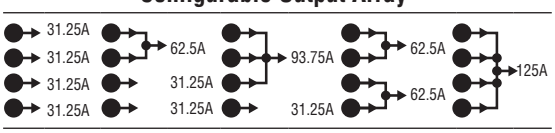
Quad 31.25A µModule Regulator with Digital Interface for Control and Monitoring



Single Channel Efficiency vs Load Current



Configurable Output Array



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ABSOLUTE MAXIMUM RATINGS

(Note 1)

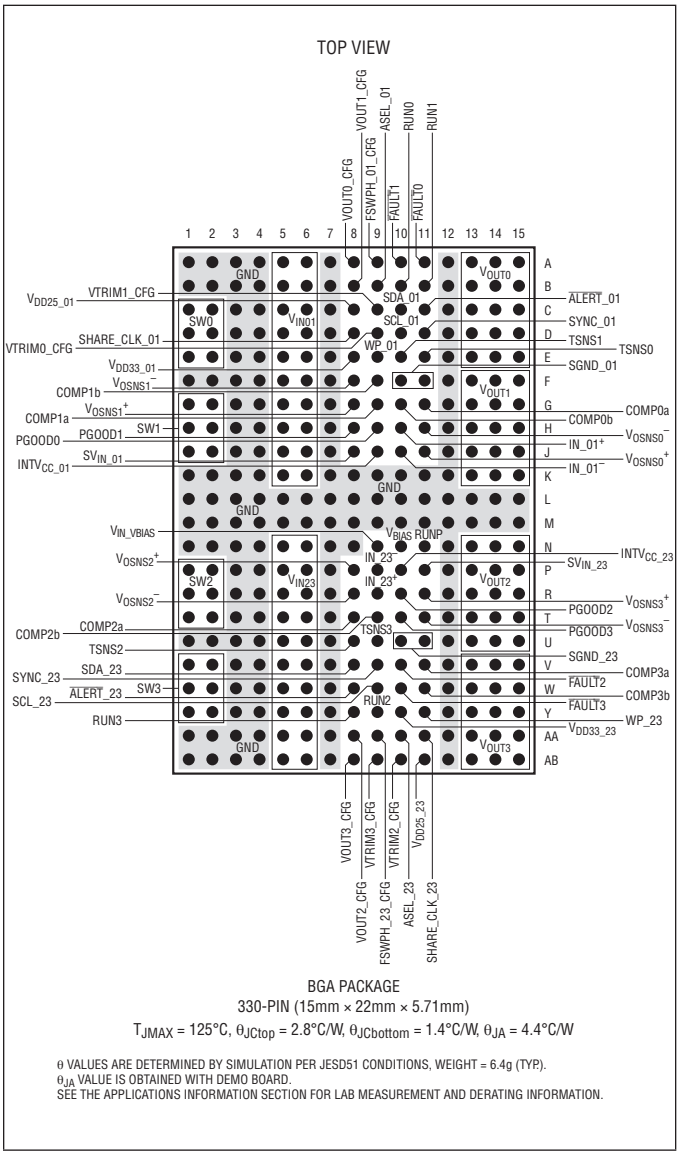
Terminal Voltages

V_{INnn} (Note 4), SV_{IN_nn}, $I_{IN\_nn}^{+}$, $I_{IN\_nn}^{-}$,
V_{IN_VBIAS}, RUNP ..... –0.3V to 18V
($SV_{IN\_nn} – I_{IN\_nn}^{+}$), ($I_{IN\_nn}^{+} – I_{IN\_nn}^{-}$) ..... –0.3V to 0.3V
SW*n* ..... –1V to 18V, –5V to 18V Transient
$INTV_{CC\_nn}$, V_{BIAS} ..... –0.3V to 6V
$V_{OUT}n$ ..... –0.3V to 2.0V
$V_{OSNS}n^{+}$ ..... –0.3V to 2.0V
$V_{OSNS}n^{-}$ ..... –0.3V to 0.3V
RUN*n*, SDA_*nn*, SCL_*nn*, $\overline{\text{ALERT}}$_*nn* ..... –0.3V to 5.5V
FSWPH_*nn*_CFG, VOUT*n*_CFG,
VTRIM*n*_CFG, ASEL_*nn* ..... –0.3V to 2.75V
$\overline{\text{FAULT}}n$, SYNC_*nn*, SHARE_CLK_*nn*,
WP_*nn*, PGOOD*n* ..... –0.3V to 3.6V
COMP*n*a, COMP*n*b ..... –0.3V to 2.7V
TSNS*n* ..... –0.3V to 0.8V
n = 0, 1, 2, 3 and *nn* = 01, 23
V_{DD33_nn} and V_{DD25_nn} Are Outputs Not to Be Driven.

Temperatures

Internal Operating Temperature Range
(Notes 2, 15, 16) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Package Body Temperature ... 245°C

PIN CONFIGURATION



BGA PACKAGE
330-PIN (15mm × 22mm × 5.71mm)
T_{JMAX} = 125°C, θ_{JCtop} = 2.8°C/W, $\theta_{JCbottom}$ = 1.4°C/W, θ_{JA} = 4.4°C/W

θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS, WEIGHT = 6.4g (TYP).
θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
SEE THE APPLICATIONS INFORMATION SECTION FOR LAB MEASUREMENT AND DERATING INFORMATION.

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH*	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4682EY#PBF	SAC305 (RoHS)	LTM4682Y	e1	BGA	4	–40°C to 125°C
LTM4682IY#PBF	SAC305 (RoHS)	LTM4682Y	e1	BGA	4	–40°C to 125°C
LTM4682IY	SnPb (63/37)	LTM4682Y	e0	BGA	4	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 12V, RUN*n* = 3.3V, RUNP = 12V, FREQUENCY_SWITCH = 575kHz and V_{OUTn} commanded to 0.75V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{INnn}	Input DC Voltage	Test Circuit 1 Test Circuit 2, VIN_OFF < VIN_ON = 4V	● ●	5.75 4.5		16 5.75	V V
V_{OUTn}	Range of Output Voltage Regulation for Each Channel	V_{OUTn} Differentially Sensed on V_{OSNSn}^+/V_{OSNSn}^- Pin-Pair, Commanded by Serial Bus or with Resistors Present at Start-Up on V_{OUTn_CFG}	●	0.7		1.35	V V
$V_{OUTn(DC)}$	Output Voltage, Total Variation with Line and Load for Each Channel	Digital Servo Engaged (MFR_PWM_MODE*n*[6] = 1b) Digital Servo Disengaged (MFR_PWM_MODE*n*[6] = 0b) V_{OUTn} Commanded to 0.75V, V_{OUTn} Low Range (MFR_PWM_MODE*n*[1] = 1b) (Notes 5, 6)	●	0.745 0.742	0.750 0.750	0.755 0.758	V V
V_{UVLO}	Undervoltage Lockout Threshold, When V_{IN} < 4.3V	V_{INTVCC_nn} Falling V_{INTVCC_nn} Rising			3.55 3.90		V V
Input Specifications							
$I_{INRUSH(VINnn)}$	Input Inrush Current at Start-Up	Test Circuit 1, V_{OUTn} = 0.75V, V_{IN} = 12V; No Load Besides Capacitors; TON_RISE*n* = 3ms			200		mA
$I_{Q(SVINnn)}$	Input Supply Bias Current	Forced Continuous Mode, MFR_PWM_MODE*n*[0] = 1b RUN*n* = RUNP = 3.3V Shutdown, RUN*n* = RUNP = 0V			 40 25		 mA mA
$I_{S(VINnn,PSM)}$	Input Supply Current in Pulse-Skipping Mode Operation	Pulse-Skipping Mode, MFR_PWM_MODE*n*[0] = 0b, I_{OUTn} = 100mA			10		mA
$I_{S(VINnn,FCM)}$	Input Supply Current in Forced-Continuous Mode Operation	Forced Continuous Mode, MFR_PWM_MODE*n*[0] = 1b 12V to 0.75V, I_{OUTn} = 31.25A, V_{BIAS} = Off			 2.3		 A
$I_{S(VINnn,SHUTDOWN)}$	Input Supply Current in Shutdown	Shutdown, RUN*n* = 0V, RUNP = 0V, V_{BIAS} = Off			300		µA
Output Specifications							
I_{OUTn}	Output Continuous Current Range Each Channel	(Note 6) Utilizing MFR_PWM_MODE[7] = 1 and Using ~I_{OUT} = 42A for IOUT_OC_FAULT_LIMIT, See the IOUT_OC_FAULT_LIMIT in the PMBus Command Details Section		0		31.25	A
$\frac{\Delta V_{OUTn(LINE)}}{V_{OUTn}}$	Line Regulation Accuracy Each Channel	Digital Servo Engaged (MFR_PWM_MODE*n*[6] = 1b) Digital Servo Disengaged (MFR_PWM_MODE*n*[6] = 0b) SV_{IN} and V_{INn} Electrically Shorted Together and $INTV_{CC}$ Open Circuit, I_{OUTn} = 0A, 5.75V ≤ V_{IN} ≤ 16V, V_{OUT} Low Range (MFR_PWM_MODE*n*[1] = 1b), FREQUENCY_SWITCH = 575kHz (Note 5)	 ●		0.03 0.03	 ±0.2	%/V %/V
$\frac{\Delta V_{OUTn(LOAD)}}{V_{OUTn}}$	Load Regulation Accuracy Each Channel	Digital Servo Engaged (MFR_PWM_MODE*n*[6] = 1b) Digital Servo Disengaged (MFR_PWM_MODE*n*[6] = 0b) 0A ≤ I_{OUTn} ≤ 31.25A, V_{OUT} Low Range, (MFR_PWM_MODE*n*[1] = 1b) (Notes 5, 6)	 ●		0.03 0.2	 0.5	% %
$V_{OUTn(AC)}$	Output Voltage Ripple				10		mV_{P-P}
f_S (Each Channel)	V_{OUTn} Ripple Frequency	FREQUENCY_SWITCH Set to 575kHz (0x023F)	●	535	575	605	kHz
$\Delta V_{OUTn(START)}$	Turn-On Overshoot	TON_RISE*n* = 3ms (Note 12)			8		mV
t_{START}	Turn-On Start-Up Time	Time from V_{IN} Toggling from 0V to 12V to Rising Edge PGOOD*n*. TON_DELAY*n* = 0ms, TON_RISE*n* = 3ms	●		35		ms
$t_{DELAY(0ms)}$	Turn-On Delay Time	Time from First Rising Edge of RUN*n* to Rising Edge of PGOOD*n* . TON_DELAY*n* = 0ms, TON_RISE*n* = 3ms, V_{IN} Having Been Established for at Least 70ms		2.75	3.3	3.8	ms
$\Delta V_{OUTn(LS)}$	Peak Output Voltage Deviation for Dynamic Load Step	Load: 0A to 10A and 10A to 0A at 10A/µs, V_{OUTn} = 0.75V, V_{IN} = 12V (Note 12) See Transient Graph			35		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 12V, RUN*n* = 3.3V, RUNP = 12V, FREQUENCY_SWITCH = 575kHz and V_{OUT}*n* commanded to 0.75V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SETTLE}	Settling Time for Dynamic Load Step per Channel	Load: 0A to 10A and 10A to 0A at 10A/µs, V_{OUT}*n* = 0.75V, V_{IN} = 12V (Note 12) See the Transient Graphs in the Typical Performance Characteristics section.			30		µs
I_{OUT}*n*(OCL_PK)	Output Current Limit, Peak High Range per Channel	Cycle-by-Cycle Inductor Peak Current Limit Inception, Utilizing MFR_PWM_MODE[7] = 1, Using ~I_{OUT} = 42A for IOUT_OC_FAULT_LIMIT, See the IOUT_OC_FAULT_LIMIT in the PMBus Command Details Section			45		A
I_{OUT}*n*(OCL_AVG)	Output Current Limit, Time Averaged per Channel	Time-Averaged Output Inductor Current Limit Inception Threshold, Commanded by IOUT_OC_FAULT_LIMIT*n* (Note 12) Utilizing MFR_PWM_MODE[7] = 1, Using ~I_{OUT} = 42A, See the IOUT_OC_FAULT_LIMIT in the PMBus Command Details Section			40 See the $I_{OUT-RB-ACC}$ Specification (Output Current Readback Accuracy)		A
Control Section							
V_{FBCM}*n*	Channel 0 to Channel 3 Feedback Input Common Mode Range	V_{OSNS}*n*$^-$ Valid Input Range (Referred to SGND) V_{OSNS}*n*$^+$ Valid Input Range (Referred to SGND)	● ●	–0.1		0.3 2.0	V V
$V_{OUT-RNGL}$	Full-Scale Command Voltage, Range Low (0.7V to 2.75V) per Channel (Note 14)	V_{OUT}*n* Commanded to 2.750V, MFR_PWM_MODE*n*[1] = 1b Set Point Accuracy Resolution LSB Step Size		 –0.5 	2.75 12 0.688	 +0.5 	V % Bits mV
R_{VSNS}*n*$^+$	V_{OSNS}*n*$^+$ Impedance to SGND	0.5V ≤ V_{VOSNS}*n*$^+$ – V_{SGND} ≤ 1.5V			50		kΩ
$t_{ON(MIN)}$	Minimum On-Time	(Note 8) per Channel			85		ns
R_{COMP}*n*	Resolution Compensation Resistor $R_{TH(MAX)}$ Compensation Resistor $R_{TH(MIN)}$	MFR_PWM_CONFIG[4:0] = 0 to 31 (See Figure 1, in the Note Section)			5 62 0		Bits kΩ kΩ
g_{m}*n*	Resolution Error Amplifier $g_{m(MAX)}$ Error Amplifier $g_{m(MIN)}$ LSB Step Size	V_{COMP}*n* = 1.35V, MFR_PWM_CONFIG[7:5] = 0 to 7			3 5.76 1 0.68		Bits mmho mmho mmho
Analog OV/UV (Overvoltage/Undervoltage) Output Voltage Supervisor Comparators (VOUT_OV/UV_FAULT_LIMIT and VOUT_OV/UV_WARN_LIMIT Monitors)							
N_{OV/UV_COMP}	Resolution, Output Voltage Supervisors	(Notes 13, 14)			9		Bits
V_{OV-RNG}	Output OV Comparator Threshold Detection Range	High Range Scale, Not Needed, Output Limited to 1.35V Low Range Scale, MFR_PWM_MODE*n*[1] = 1b (Note 14)		 0.7		 2.7	 V
V_{OUSTP}	Output OV and UV Comparator Threshold Programming LSB Step Size	(Note 14) Low Range Scale, MFR_PWM_MODE*n*[1] = 1b			 5.6		 mV
$V_{OV-ACC-}$*n*	Output OV Comparator Threshold Accuracy Channel 0 to Channel 3 (Note 13)	0.7V ≤ V_{VOSNS}*n*$^+$ – V_{VOSNS}*n*$^-$ ≤ 1.35V, MFR_PWM_MODE[1] = 1b	●			±3	%
V_{UV-RNG}*n*	Output UV Comparator Threshold Detection Range	High Range Scale, Not Needed, Output Limited to 1.35V Low Range Scale, MFR_PWM_MODE*n*[1] = 1b		 0.7		 2.7	V V
V_{UV-ACC}*n*	Output UV Comparator Threshold Accuracy Channel 0 to Channel 3 (Note 13)	0.7V ≤ V_{VOSNS}*n*$^+$ – V_{VOSNS}*n*$^-$ ≤ 1.35V, MFR_PWM_MODE[1] = 1b	●			±3	%
$t_{PROP-OV}$	Output OV Comparator Response Times	Overdrive to 10% Above Programmed Threshold				100	µs
$t_{PROP-UV}$	Output UV Comparator Response Times	Underdrive to 10% Below Programmed Threshold				100	µs

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog OV/UV SV_{IN_nn} Input Voltage Supervisor Comparators (Threshold Detectors for VIN_ON and VIN_OFF)							
$N_{SVIN-OV/UV-COMP}$	SV_{IN_nn} OV/UV Comparator Threshold-Programming Resolution	(Note 14)			9		Bits
$SV_{IN-OU-RANGE}$	SV_{IN_nn} OV/UV Comparator Threshold-Programming Range	Limited to Abs Max = 18V	●	4.5		18	V
$SV_{IN-OU-STP}$	SV_{IN_nn} OV/UV Comparator Threshold-Programming LSB Step Size	(Note 14)			76		mV
$SV_{IN-OU-ACC}$	SV_{IN_nn} OV/UV Comparator Threshold Accuracy	9V < SV_{IN} ≤ 16V 4.5V ≤ SV_{IN} ≤ 9V	● ●			±3 ±270	% mV
$t_{PROP-SVIN-HIGH-VIN}$	SV_{IN_nn} OV/UV Comparator Response Time, High V_{IN} Operating Configuration	Test Circuit 1, and: VIN_ON = 9V, SV_{IN} Driven from 8.775V to 9.225V VIN_OFF = 9V, SV_{IN} Driven from 9.225V to 8.775V	 ● ●			 100 100	 µs µs
$t_{PROP-SVIN-LOW-VIN}$	SV_{IN_nn} OV/UV Comparator Response Time, Low V_{IN} Operating Configuration	Test Circuit 2, and: VIN_ON = 4.5V, SV_{IN} Driven from 4.225V to 4.725V VIN_OFF = 4.5V, SV_{IN} Driven from 4.725V to 4.225V	 ● ●			 100 100	 µs µs
Channel*n* Output Voltage Readback (READ_VOUT*n*)							
N_{VO-RB}	Output Voltage Readback Resolution and LSB Step Size	(Note 14)			16 244		Bits µV
$V_{O-F/S}$	Output Voltage Full-Scale Digitizable Range	V_{RUN}*n* = 0V (Note 14), Limited to 1.35V Max Operating			8		V
$V_{O-RB-ACC}$	Output Voltage Readback Accuracy	Channel *n*: 0.7V ≤ $V_{VOSNS}^+ - V_{VOSNS}^-$ < 1.35V	●	–7		7	mV
$t_{CONVERT-VO-RB}$	Output Voltage Readback Update Rate	MFR_ADC_CONTROL = 0x00 (Notes 9, 14) MFR_ADC_CONTROL = 0x01 through 0x0C (Notes 9, 14) MFR_ADC_CONTROL Section			90 8		ms ms ms
Input Voltage (SV_{IN_nn}) Readback (READ_VIN)							
$N_{SVIN-RB}$	Input Voltage Readback Resolution and LSB Step Size	(Notes 10, 14) Limited to Abs Max = 18V			10 15.625		Bits mV
$SV_{IN-F/S}$	Input Voltage Full-Scale Digitizable Range	(Notes 11, 14) Limited to 16V Operating			43		V
$SV_{IN-RB-ACC}$	Input Voltage Readback Accuracy	READ_VIN, 4.5V ≤ SV_{IN} ≤ 16V	●		Within ±2% of Reading		
$t_{CONVERT-SVIN-RB}$	Input Voltage Readback Update Rate	MFR_ADC_CONTROL = 0x00 (Notes 9, 14) MFR_ADC_CONTROL = 0x01 (Notes 9, 14)			90 8		ms ms
Channel*n* Output Current (READ_IOUT*n*), Duty Cycle (READ_DUTY_CYCLE*n*), and Computed Input Current (MFR_READ_IIN*n*) Readback							
N_{IO-RB}	Output Current Readback Resolution and LSB Step Size	(Notes 10, 14)			10 34.1		Bits mA
$I_{OUT-F/S}$	Output Current Full-Scale Digitizable Range	(Note 14) Utilizing MFR_PWM_MODE[7] = 1, Using IOUT_OC_FAULT_LIMIT = 61A, See the IOUT_OC_FAULT_LIMIT in the PMBus Command Details Section			54		A
$I_{OUT-RB-ACC}$	Output Current, Readback Accuracy	READ_IOUT*n*, Channel 0 to Channel 3, 0 ≤ I_{OUT}*n* ≤ 25A, Forced Continuous Mode, MFR_PWM_MODE*n*[0] = 1b See Histograms in Typical Performance Characteristics Section, (Note 12)	●		Within 1.5A of Reading		
$I_{OUT-RB(31.25A)}$	Full Load Output Current Readback	(Note 12), See Histograms in Typical Performance Characteristics			31.25		A
$t_{CONVERT-IO-RB}$	Output Current Readback Update Rate	MFR_ADC_CONTROL = 0x00 (Notes 9, 14) MFR_ADC_CONTROL = 0x06 (CH0,2 I_{OUT}) or 0x0A (CH1,3 I_{OUT}) (Notes 9, 14) See MFR_ADC_CONTROL SECTION			90 8		ms ms

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current Readback							
N	Resolution	(Note 10)			10		Bits
V_{IINSTP}	LSB Step Size Full-Scale Range = 16mV LSB Step Size Full-Scale Range = 32mV LSB Step Size Full-Scale Range = 64mV	Gain = 8, 0V ≤ $\lvert V_{IIN}^+ - V_{IIN}^- \rvert$ ≤ 5mV Gain = 4, 0V ≤ $\lvert V_{IIN}^+ - V_{IIN}^- \rvert$ ≤ 20mV Gain = 2, 0V ≤ $\lvert V_{IIN}^+ - V_{IIN}^- \rvert$ ≤ 50mV			15.26 30.52 61		µV µV µV
I_{IN_TUE}	Total Unadjusted Error	Gain = 8, 2.5mV ≤ $\lvert V_{IIN}^+ - V_{IIN}^- \rvert$ (Note 7) Gain = 4, 4mV ≤ $\lvert V_{IIN}^+ - V_{IIN}^- \rvert$ (Note 7) Gain = 2, 6mV ≤ $\lvert V_{IIN}^+ - V_{IIN}^- \rvert$ (Note 7)			2 1.3 1.2		% % %
V_{OS}	Zero-Code Offset Voltage	(Note 14)				±50	µV
$t_{CONVERT}$	Update Rate	(Notes 9,15), See MFR_ADC_CONTROL Section for Faster Update Rates			90		ms
Supply Current Readback (Note 15)							
N	Resolution	(Note 10)			10		Bits
$V_{ICHIPSTP}$	LSB Step Size Full-Scale Range = 256mV	Onboard 1Ω Resistor			244		µV
I_{CHIP_RB}	I_{CHIP} Readback	SV_{IN_nn} Current			50		mA
$t_{CONVERT}$	Update Rate	(Notes 9,14), See MFR_ADC_CONTROL Section for Faster Update Rates			90		ms
Temperature Readback (T0, T1)							
T_{RES-RB}	Temperature Readback Resolution	Channel *n*, and Controller (Note 14)			0.25		°C
T0_TUE	External Temperature Total Unadjusted Readback Error	Supporting Only ΔV_{BE} Sensing			2.5		°C
T1_TUE	Internal TSNS TUE	V_{RUNn} = 0.0, f_{SYNC} = 0kHz (Note 7)			±1		°C
$t_{CONVERT}$	Update Rate	(Note 9) MFR_ADC_CONTROL = 0x04, 0x0c, or 0x08 (Notes 9, 14)			90 8		ms ms
$INTV_{CC\_nn}$ Regulator/V_{BIAS}							
V_{INTVCC_nn}	Internal V_{CC} Voltage No Load	6V ≤ SV_{IN_nn} ≤ 16V	●	5.25	5.5	5.75	V
V_{LDO_INT}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA, 6V ≤ SV_{IN_nn} ≤ 16V			0.5	±2	%
V_{IN_VBIAS}	Input Range for V_{IN_VBIAS}			4.5		16	V
RUNP	V_{BIAS} Enable	RUNP Rising			0.8	0.85	V
V_{BIAS}	5.5V Internal Regulator	7V ≤ V_{IN_VBIAS} ≤ 16V, V_{SVIN_nn} > 7V		5.25	5.5	5.75	V
SV_{IN_THR}	V_{SVIN_nn} Threshold to Enable V_{BIAS} Switchover	SV_{IN_nn} Rising			7	7.5	V
SV_{IN_THF}	V_{SVIN_nn} Threshold to Disable V_{BIAS} Switchover	SV_{IN_nn} Falling			6.5		V
V_{DD33_nn} Regulator							
$V_{VDD33nn}$	Internal V_{DD33} Voltage	V_{INTVCC_nn} > 4.5V		3.2	3.3	3.4	V
I_{LIM}	V_{DD33} Current Limit	V_{DD33_nn} = GND, V_{IN_nn} = $INTV_{CC\_nn}$ = 4.5V			100		mA
V_{VDD33_OV}	V_{DD33} Overvoltage Threshold	(Note 14)			3.5		V
V_{VDD33_UV}	V_{DD33} Undervoltage Threshold	(Note 14)			3.1		V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD25_nn} Regulator							
$V_{VDD25nn}$	Internal V_{DD25} Voltage				2.5		V
I_{LIM}	V_{DD25} Current Limit	V_{DD25_nn} = GND, V_{IN_nn} = $INTV_{CC\_nn}$ = 4.5V			80		mA
Oscillator and Phase-Locked Loop (PLL)							
f_{RANGE}	PLL SYNC Range	Synchronized with Falling Edge of SYNC		250		1000	kHz
f_{OSC}	Oscillator Frequency Accuracy	Frequency Switch = 250kHz to 1000kHz (Note 14)	●			±7.5	%
$V_{TH(SYNC\_nn)}$	SYNC Input Threshold (Note 14)	V_{SYNC} Falling V_{SYNC} Rising			1 1.5		V V
$V_{OL(SYNC\_nn)}$	SYNC Low Output Voltage	I_{LOAD} = 3mA (Note 14)			0.2	0.4	V
$I_{LEAK(SYNC\_nn)}$	SYNC Leakage Current in Subordinate Mode	0V ≤ V_{SYNC_nn} ≤ 3.6V				±5	µA
θSYNC-θ0, -θ2	SYNC to Ch0, Ch2 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of SW0, SW2	MFR_PWM_CONFIG[2:0] = 0,2,3 MFR_PWM_CONFIG[2:0] = 5 MFR_PWM_CONFIG[2:0] = 1 MFR_PWM_CONFIG[2:0]= 4,6			0 60 90 120		Deg Deg Deg Deg
θSYNC-θ1, -θ3	SYNC to Ch1, Ch3 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of SW1, SW3	MFR_PWM_CONFIG[2:0] = 3 MFR_PWM_CONFIG[2:0] = 0 MFR_PWM_CONFIG[2:0] = 2,4,5 MFR_PWM_CONFIG[2:0] = 1 MFR_PWM_CONFIG[2:0] = 6			120 180 240 270 300		Deg Deg Deg Deg Deg
EEPROM Characteristics							
Endurance	(Note 15)	0°C ≤ T_J ≤ 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Note 15)	T_J < 125°C	●	10			Years
Mass_Write	Mass Write Operation Time	STORE_USER_ALL, 0°C < T_J < 85°C During EEPROM Write Operation			440	4100	ms
Leakage Current SDA_*nn*, SCL_*nn*, $\overline{\text{ALERT}}$_*nn*, RUN*n*							
I_{OL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V	●			±5	µA
Leakage Current $\overline{\text{FAULT}}$*n*, PGOOD*n*							
I_{GL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 3.6V	●			±2	µA
Digital Inputs SCL_*nn*, SDA_*nn*, RUN*n*							
V_{IH}	Input High Threshold Voltage		●			1.35	V
V_{IL}	Input Low Threshold Voltage		●	0.8			V
V_{HYST}	Input Hysteresis	SCL, SDA			0.08		V
C_{PIN}	Input Capacitance					10	pF
Digital Input WP_*nn* (Note 14) (Note 14)							
I_{PUWP}	Input Pull-Up Current	WP			10		µA
Open-Drain Outputs SCL_*nn*, SDA_*nn*, $\overline{\text{FAULT}}$*n*, $\overline{\text{ALERT}}$_*nn*, RUN*n*, SHARE_CLK_*nn*, PGOOD*n*							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA				0.4	V
Digital Inputs SHARE_CLK_*nn*, WP_*nn* (Note 14)							
V_{IH}	Input High Threshold Voltage		●		1.5	1.8	V
V_{IL}	Input Low Threshold Voltage		●	0.6	1		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 12V, RUN*n* = 3.3V, RUNP = 12V, FREQUENCY_SWITCH = 575kHz and V_{OUT}*n* commanded to 0.75V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Filtering of $\overline{\text{FAULT}}$*n* (Note 14)							
I_{FLTG}	Input Digital Filtering $\overline{\text{FAULT}}$*n*				3		µs
Digital Filtering of PGOOD*n* (Note 14)							
I_{FLTG}	Output Digital Filtering PGOOD*n*				100		µs
Digital Filtering of RUN*n* (Note 14)							
I_{FLTG}	Input Digital Filtering RUN				10		µs
PMBus Interface Timing Characteristics (Note 14)							
f_{SCL}	Serial Bus Operating Frequency		●	10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3			µs
$t_{HD(STA)}$	Hold Time After Repeated Start Condition After This Period, the First Clock is Generated		●	0.6			µs
$t_{SU(STA)}$	Repeated Start Condition Setup Time		●	0.6		10000	µs
$t_{SU(ST0)}$	Stop Condition Setup Time		●	0.6			µs
$t_{HD(DAT)}$	Date Hold Time Receiving Data Transmitting Data		 ● ●	 0 0.3		 0.9	 µs µs
$t_{SU(DAT)}$	Data Setup Time Receiving Data		 	 0.1			 µs
$t_{TIMEOUT\_SMB}$	Stuck PMBus Timer Non-Block Reads Stuck PMBus Timer Block Reads	Measured from the Last PMBus Start Event			32 255		ms
t_{LOW}	Serial Clock Low Period		●	1.3		10000	µs
t_{HIGH}	Serial Clock High Period		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4682 is tested under pulsed-load conditions such that $T_J \approx T_A$. The LTM4682E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4682I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The T_J is calculated from the ambient temperature T_A and the power dissipation P_D according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with the board layout, the rated package thermal resistance, and other environmental factors.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: The two power inputs—V_{IN01} and V_{IN23}—and their respective power outputs—$V_{OUT0,1}$ and $V_{OUT2,3}$—are tested independently in production. A shorthand notation is used in this document that allows these parameters to be referred to by V_{INnn} and V_{OUTn}, where *n* is permitted to take on a value of 0 to 3. This italicized *n* notation and convention is extended to encompass all such pin names, as well as register names with channel-specific, i.e., paged data. For example, VOUT_COMMAND*n* refers to the VOUT_COMMAND command code data located in Pages 0 and 1, which in turn relate to Channel 0,2 ($V_{OUT0,2}$) and Channel 1,3 ($V_{OUT1,3}$). Registers containing non-page-specific data, i.e., whose data is global to the module, or applies to all of the module's channels lack the italicized *n*, e.g., FREQUENCY_SWITCH.

ELECTRICAL CHARACTERISTICS

Note 5: V_{OUTn} (DC) and line and load regulation tests are performed in production with digital servo disengaged (MFR_PWM_MODE*n*[6] = 0b), and low V_{OUTn} range selected MFR_PWM_MODE*n*[1] = 1b. The digital servo control loop is exercised in production (setting MFR_PWM_MODE*n*[6] = 1b). However, the convergence of the output voltage to its final settling value is not necessarily observed in the final test—due to potentially long-time constants involved—and is instead guaranteed by the output voltage readback accuracy specification. Evaluation in application demonstrates capability; see the Typical Performance Characteristics section.

Note 6: See the Thermal Considerations and Output Current Derating section for V_{IN}, V_{OUT}, and T_A, located in the Applications Information section.

Note 7: Part tested with PWM disabled. Evaluation in application demonstrates capability. The TUE(%) = ADC Gain Error (%) + 100 (zero-code offset + ADC Linearity Error)/Actual Value.

Note 8: Minimum on-time is tested at wafer sort.

Note 9: The data conversion is done by default in a round-robin fashion. All input signals are continuously converted for a typical latency of 90ms. Setting MFR_ADC_CONTRL value to be 0 to 12, LTM4682 can do fast data conversion with only 8ms to 10ms. See the PMBus Command Summary section for details.

Note 10: The following telemetry parameters are formatted in PMBus-defined Linear Data Format, in which each register contains a word comprised of 5 most significant bits—representing a signed exponent, to be raised to the power of 2—and 11 least significant bits—representing a signed mantissa: input voltage (on SV_{IN_nn}), accessed through the READ_VIN command code; output currents (I_{OUTn}), accessed through the READ_IOUT*n* command codes; module input current (I_{VIN_nn} + I_{VIN_nn} + I_{SVIN_nn}), accessed through the READ_IIN command code; channel input currents (I_{VIN_nn} + 1/2 • I_{SVIN_nn}), accessed through the MFR_READ_IIN*n* command codes; and duty cycles of Channel 0 and Channel 1 switching power stages, accessed through the READ_DUTY_CYCLE*n* command codes. This data format limits the resolution of telemetry readback data to 10 bits even though the internal ADC is 16 bits and the LTM4682's internal calculations use 32-bit words.

Note 11: The absolute maximum rating for the SV_{IN_nn} pin is 18V. The input voltage telemetry (READ_VIN) is obtained by digitizing a voltage scaled down from the SV_{IN_nn} pin.

Note 12: These typical parameters are based on bench measurements and are not production tested.

Note 13: Channel 0 to Channel 3 OV/UV comparator threshold accuracy for 0.7V to 1.35V are 3%.

Note 14: Tested at IC-level ATE.

Note 15: The LTM4682's EEPROM temperature range for valid write commands is 0°C to 85°C. To achieve guaranteed EEPROM data retention, execution of the STORE_USER_ALL command—i.e., uploading RAM contents to NVM—outside this temperature range is not recommended. However, as long as the LTM4682's EEPROM temperature is less than 130°C, the LTM4682 will obey the STORE_USER_ALL command. Only when EEPROM temperature exceeds 130°C, the LTM4682 will not act on any STORE_USER_ALL transactions; instead, the LTM4682 NACKs the serial command and asserts its relevant CML (communications, memory, logic) fault bits. The EEPROM temperature can be queried before commanding STORE_USER_ALL; see the Applications Information section.

Note 16: The LTM4682 includes overtemperature protection that is intended to protect the device during momentary overload conditions. The junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

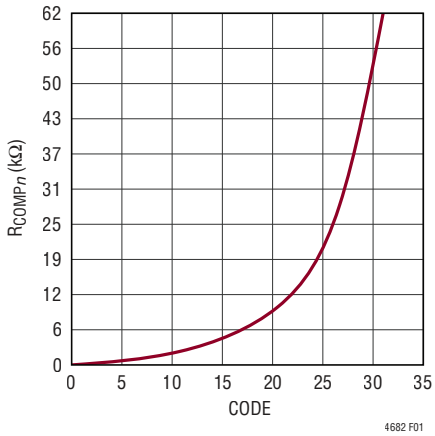
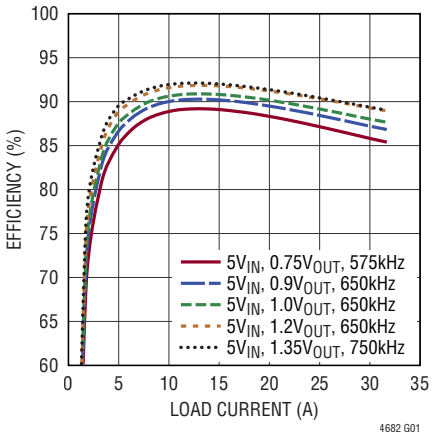


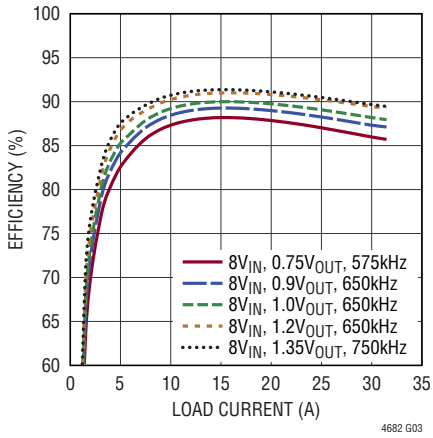
Figure 1. Programmable R_{COMPn}

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

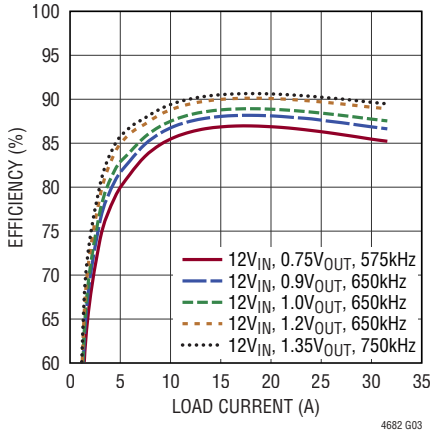
Single Channel Efficiency, $5V_{IN}$, $V_{IN} = SV_{IN} = INTV_{CC} = 5V$, RUNP = 0V, Continuous-Conduction Mode



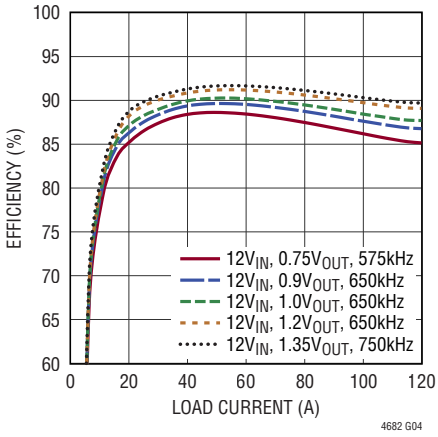
Single Channel Efficiency, $8V_{IN}$, $V_{IN} = SV_{IN} = V_{IN\_VBIAS} = 8V$, RUNP = 8V, Continuous-Conduction Mode



Single Channel Efficiency, $12V_{IN}$, $V_{IN} = SV_{IN} = V_{IN\_VBIAS} = RUNP = 12V$, Continuous-Conduction Mode



Quad Channel Single Output Efficiency $V_{IN} = SV_{IN} = V_{IN\_VBIAS} = RUNP = 12V$, Continuous-Conduction Mode



TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Single Channel Load Transient Response (0A) to (10A) Load Step, 10A/µs, 12V_{IN} to 0.7V_{OUT}, f_{SW} = 575kHz

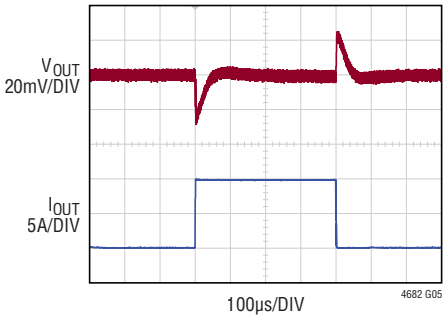


FIGURE 48 CIRCUIT
C_{OUT} = 470µF ×3 POSCAP, 100µF ×4 CERAMIC
R_{COMP} = 15k, EA-g_m = 3.02mS
COMPna = 2.2nF, COMPnb = 150pF
I_{LIM} RANGE HIGH, V_{OUT} RANGE LOW

Single Channel Load Transient Response (0A) to (10A) Load Step, 10A/µs, 12V_{IN} to 0.85V_{OUT}, f_{SW} = 650kHz

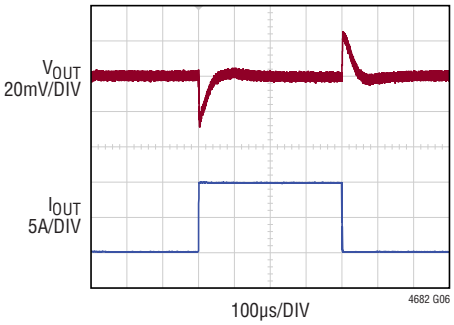


FIGURE 48 CIRCUIT
C_{OUT} = 470µF ×3 POSCAP, 100µF ×4 CERAMIC
R_{COMP} = 15k, EA-g_m = 3.02mS
COMPna = 2.2nF, COMPnb = 150pF
I_{LIM} RANGE HIGH, V_{OUT} RANGE LOW

Single Channel Load Transient Response (0A) to (10A) Load Step, 10A/µs, 12V_{IN} to 1V_{OUT}, f_{SW} = 650kHz

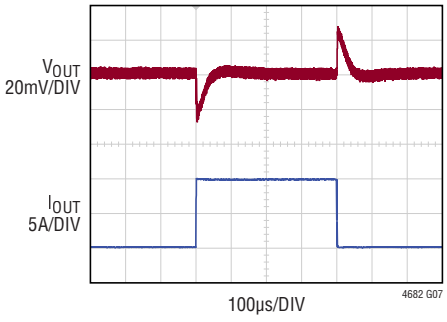


FIGURE 48 CIRCUIT
C_{OUT} = 470µF ×3 POSCAP, 100µF ×4 CERAMIC
R_{COMP} = 15k, EA-g_m = 3.02mS
COMPna = 2.2nF, COMPnb = 150pF
I_{LIM} RANGE HIGH, V_{OUT} RANGE LOW

Single Channel Load Transient Response (0A) to (10A) Load Step, 10A/µs, 12V_{IN} to 1.2V_{OUT}, f_{SW} = 650kHz

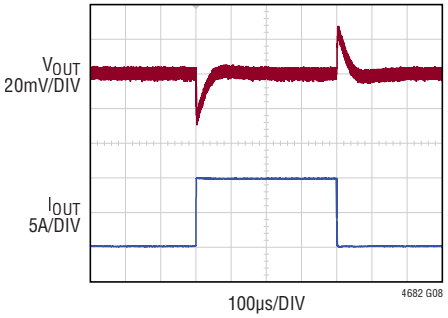


FIGURE 48 CIRCUIT
C_{OUT} = 470µF ×3 POSCAP, 100µF ×4 CERAMIC
R_{COMP} = 15k, EA-g_m = 3.02mS
COMPna = 2.2nF, COMPnb = 150pF
I_{LIM} RANGE HIGH, V_{OUT} RANGE LOW

Single Channel Load Transient Response (0A) to (10A) Load Step, 10A/µs, 12V_{IN} to 1.35V_{OUT}, f_{SW} = 750kHz

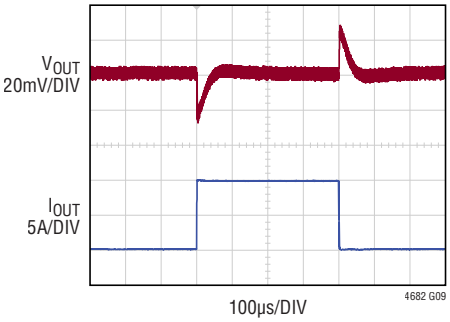


FIGURE 48 CIRCUIT
C_{OUT} = 470µF ×3 POSCAP, 100µF ×4 CERAMIC
R_{COMP} = 15k, EA-g_m = 3.02mS
COMPna = 2.2nF, COMPnb = 150pF
I_{LIM} RANGE HIGH, V_{OUT} RANGE LOW

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Quad Output Concurrent Rail, Start-Up, Prebias

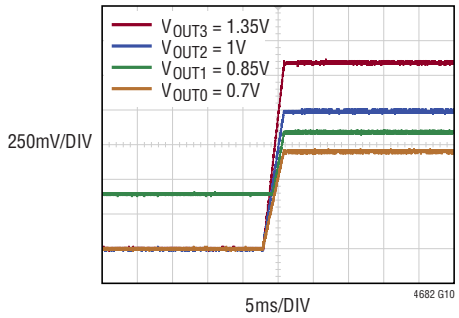


FIGURE 48 CIRCUIT, $12V_{IN}$, 30A ON V_{OUT0} NO LOAD ON OTHER OUTPUTS AND 400mV PREBIAS ON V_{OUT1}

Quad Output Concurrent Rail, Shutdown, Prebias

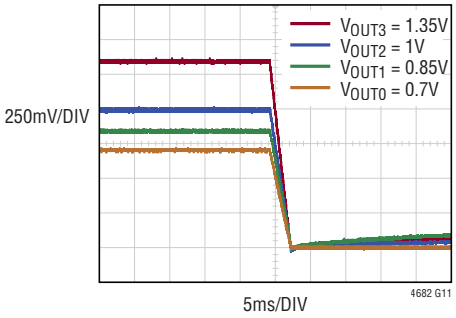


FIGURE 48 CIRCUIT, $12V_{IN}$, 30A ON V_{OUT0} NO LOAD ON OTHER OUTPUTS AND 400mV PREBIAS ON V_{OUT1}

Single Phase Single Output 12V to 0.75V, No Load Short-Circuit Protection

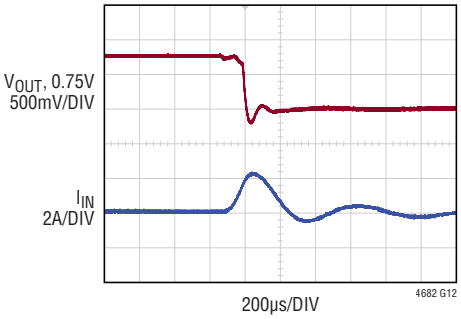


FIGURE 48 CIRCUIT, $12V_{IN}$, NO LOAD ON V_{OUT0} PRIOR TO APPLICATION OF SHORT-CIRCUIT USE OF HIGH RANGE OF I_{LIMIT} SYSTEM SHORT-CIRCUIT USING LOW IMPEDANCE COPPER ACROSS OUTPUT (HARD SHORT)

Single Phase Single Output 12V to 0.75V, 31.25A Load Short-Circuit Protection

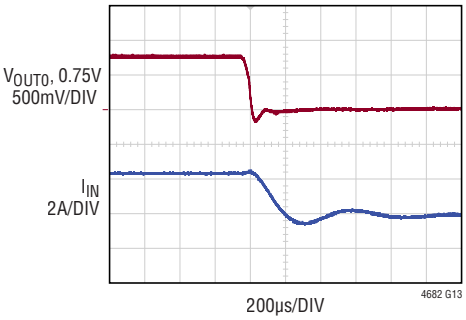
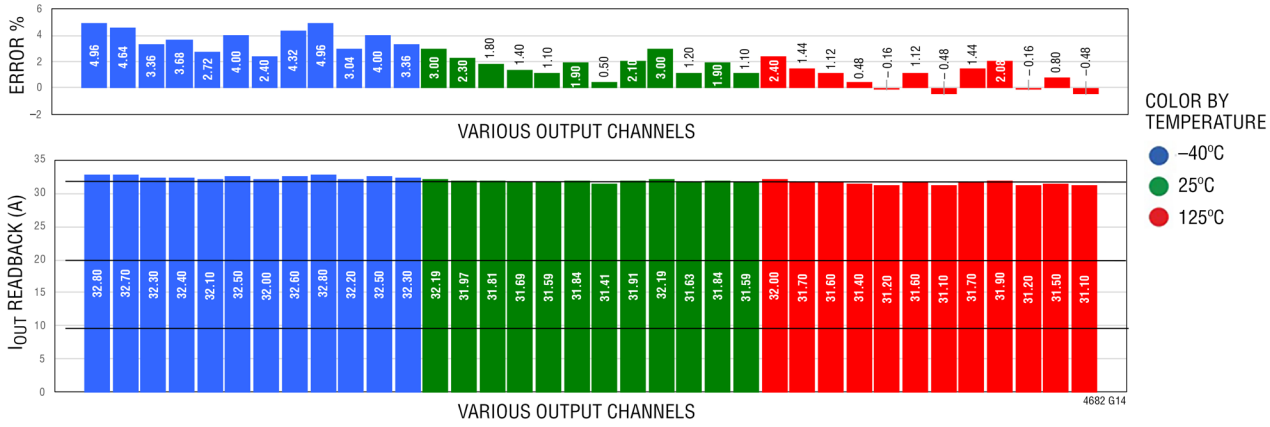


FIGURE 48 CIRCUIT, $12V_{IN}$, 31.25A LOAD ON V_{OUT0} PRIOR TO APPLICATION OF SHORT-CIRCUIT USE OF HIGH RANGE OF I_{LIMIT} SYSTEM SHORT-CIRCUIT USING LOW IMPEDANCE COPPER ACROSS OUTPUT (HARD SHORT)

V_{IN} = SV_{IN} = 12V, V_{OUT} = 0.75V, FREQ = 575kHz, I_{OUT} = 31.25A

I_OUT READBACK AT 31.25A



PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

GND (A1-A4, A7, A12, B1-B4, B7, B12, C3-C4, C7, C12, D3-D4, D7, D12, E3-E4, E7, E12, F1-F4, F7, F12, G3-G4, G7, G12, H3-H4, H7, H12, J3-J4, J7, J12, K1-K4, K7-K12, L1-L15, M1-M15, N1-N4, N7-N8, N12, P3-P4, P7, P12, R3-R4, R7, R12, T3-T4, T7, T12, U1-U4, U7, U12, V3-V4, V7, V12, W3-W4, W7, W12, Y3-Y4, Y7, Y12, AA1-AA4, AA7, AA12, AB1-AB4, AB7, AB12): Power Ground of the LTM4682. Power return for V_{IN01} V_{IN23} $V_{OUT0,1}$ and $V_{OUT2,3}$. Return input and output capacitors to this point.

V_{IN01} (A5-A6, B5-B6, C5-C6, D5-D6, E5-E6, F5-F6, G5-G6, H5-H6, J5-J6, K5-K6): Positive Power Input to Channels 0 and 1 Switching Stages. Provide sufficient decoupling capacitance in the form of multilayer ceramic capacitors (MLCCs) and low ESR electrolytic (or equivalent) to handle reflected input current ripple from the step-down switching stage. The MLCCs capacitors should be placed as close to the LTM4682 as physically possible. See the Layout Checklist/Example section in the Applications Information section.

VOUT0_CFG (A8): Output Voltage Select Pin for V_{OUT0}, Coarse Setting. If the VOUT0_CFG and VTRIM0_CFG pins are both left open—or, if the LTM4682 is configured to ignore pin-strap (R_{CONFIG}) resistors, i.e., MFR_CONFIG_ALL[6] = 1b—then the LTM4682s target V_{OUT0} output voltage setting (VOUT_COMMAND0) and associated power-good and OV/UV warning and fault thresholds are dictated at SV_{IN_01} power-up according to the LTM4682's nonvolatile (NVM) contents. A resistor divider connected to 2.5V and to SGND (see Table 1)—in combination with resistor pin settings on VTRIM0_CFG, and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0b—can be used to configure the LTM4682's Channel 0 output to power-up to a VOUT_COMMAND value (and associated output voltage monitoring and protection/fault-detection thresholds) different from those of NVM contents. (See the Applications Information section.) Connecting resistor(s) from VOUT0_CFG to SGND and, or VTRIM0_CFG to SGND allows a convenient way to configure multiple LTM4682s with identical NVM contents for different output voltage settings all without graphical user interface (GUI) intervention or the need to custom-preprogram module NVM contents. Minimize capacitance especially when the pin is left open, to ensure accurate detection of the pin state. Note that the use of R_{CONFIG}s on VOUT0_CFG/VTRIM0_CFG can affect the V_{OUT0} range setting (MFR_PWM_MODE0[1]) and loop gain. For addressed ASEL_01, Page 0x00 corresponds to Channel 0 and Page 0x01 corresponds to Channel 1. See PAGE description section.

FSWPH_01_CFG (A9): Switching Frequency, Channel Phase-Interleaving Angle and Phase Relationship to SYNC Configuration Pin for Channels 0 and 1. If this pin is left open—or, if the LTM4682 is configured to ignore pin-strap (R_{CONFIG}) resistors, i.e., MFR_CONFIG_ALL[6] = 1b—then LTM4682's switching frequency (FREQUENCY_SWITCH) and channel phase relationships (with respect to the SYNC clock; MFR_PWM_CONFIG[2:0]) are dictated at SV_{IN_01} power-up according to the LTM4682's NVM contents for Channels 0 and 1. Default factory values are: 575kHz operation; Channel 0 at 0°; and Channel 1 at 180°C (convention throughout this document: a phase angle of 0° means the channel's switch node rises coincident with the falling edge of the SYNC pulse). Connecting a resistor divider from 2.5V to SGND (and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0b) allows a convenient way to configure multiple LTM4682s with identical NVM contents for different switching frequencies of operation and phase interleaving angle settings of intra- and extra-module-paralleled channels—all, without GUI intervention or the need to custom pre-program module NVM contents. See the Applications Information section. Minimize capacitance—especially when the pin is left open—to ensure accurate detection of the pin state.

$\overline{FAULT}$0, $\overline{FAULT}$1, $\overline{FAULT}$2, $\overline{FAULT}$3 (A11, A10, V10, W10): Digital Programmable $\overline{FAULT}$ Inputs and Outputs. Open-drain output. A pull-up resistor to 3.3V is required in the application.

V_{OUT0} (A13-A15, B13-B15, C13-C15, D13-D15, E13-E15): Channel 0 Output Voltage. Place the recommended

PIN FUNCTIONS

output capacitors from this shape to GND. See the Layout Checklist/Example section.

VOUT2_CFG (AA8): Output Voltage Select Pin for V_{OUT2}, Coarse Setting. If the VOUT2_CFG and VTRIM2_CFG pins are both left open—or, if the LTM4682 is configured to ignore pin-strap (R_{CONFIG}) resistors, i.e., MFR_CONFIG_ALL[6] = 1b—then the LTM4682s target V_{OUT2} output voltage setting (VOUT_COMMAND2) and associated power-good and OV/UV warning and fault thresholds are dictated at SV_{IN_23} power-up according to the LTM4682's NVM contents. A resistor divider connected to 2.5V and to SGND to this pin—in combination with resistor pin settings on VTRIM2_CFG, and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0b—can be used to configure the LTM4682's Channel 2 output to power-up to a VOUT_COMMAND value (and associated output voltage monitoring and protection/fault-detection thresholds) different from those of NVM contents. See the Applications Information section. Connecting resistor(s) from VOUT2_CFG to SGND and/or VTRIM2_CFG to SGND in this manner allows a convenient way to configure multiple LTM4682s with identical NVM contents for different output voltage settings all without GUI intervention or the need to custom-preprogram module NVM contents. Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that the use of R_{CONFIG}s on VOUT2_CFG/VTRIM2_CFG can affect the V_{OUT2} range setting (MFR_PWM_MODE0[1]) and loop gain. For addressed ASEL_23, Page 0x00 corresponds to Channel 2 and Page 0x01 corresponds to Channel 3. See PAGE description section.

FSWPH_23_CFG (AA9): Switching Frequency, Channel Phase-Interleaving Angle and Phase Relationship to SYNC Configuration Pin for Channels 2 and 3. If this pin is left open—or, if the LTM4682 is configured to ignore pin-strap (R_{CONFIG}) resistors, i.e., MFR_CONFIG_ALL[6] = 1b—then LTM4682's switching frequency (FREQUENCY_SWITCH) and channel phase relationships (with respect to the SYNC clock; MFR_PWM_CONFIG[2:0]) are dictated at SV_{IN_23} power-up according to the LTM4682's NVM contents for Channels 2 and 3. Default factory values are 575kHz operation; Channel 2 at 0°; and Channel 3 at 180°C (convention throughout this document: a phase angle of 0° means the channel's switch node rises coincident with the falling edge of the SYNC pulse). Connecting a resistor divider from 2.5V to SGND (and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0b) allows a convenient way to configure multiple LTM4682s with identical NVM contents for different switching frequencies of operation and phase interleaving angle settings of intra- and extra-module-paralleled channels—all, without GUI intervention or the need to custom pre-program module NVM contents. See the Applications Information section. Minimize capacitance, especially, when the pin is left open, to ensure accurate detection of the pin state.

ASEL_23 (AA10): Serial Bus Address Configuration Pin for Channels 2 and 3 Controller. On any given I^2C/SMBus serial bus segment, every device must have its unique subordinate address. If this pin is left open, the LTM4682 powers up to its default subordinate address of 0x4F (hexadecimal), i.e., 1001111b (industry-standard convention is used throughout this document: 7-bit subordinate addressing). The lower 4 bits of the LTM4682's subordinate address can be altered from this default value by connecting a resistor from this pin to SGND. Minimize capacitance—especially when the pin is left open—to ensure accurate detection of the pin state. It is recommended to use a resistor to set the address. The ASEL_23 address will be used to address Channels 2 and 3, and a different ASEL_01 address will be used to address Channels 0 and 1. For addressed ASEL_23, Page 0x00 corresponds to Channel 2 and Page 0x01 corresponds to Channel 3. See PAGE description section. The GUI will represent Channel 2 as U1:B0 and Channel 3 as U1:B1. See the LTpowerPlay Screen Shot (Figure 31).

VOUT3_CFG (AB8): Output Voltage Select Pin for V_{OUT3}, Coarse Setting. If the VOUT3_CFG and VTRIM3_CFG pins are both left open—or, if the LTM4682 is configured to ignore pin-strap (R_{CONFIG}) resistors, i.e., MFR_CONFIG_ALL[6] = 1b, then the LTM4682s target V_{OUT3} output voltage setting (VOUT_COMMAND3) and associated power-good and OV/UV warning and fault thresholds are dictated at SV_{IN_23} power-up according to the LTM4682's NVM contents. A resistor divider connected to 2.5V and

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to SGND to this pin—in combination with resistor pin settings on VTRIM3_CFG, and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0b—can be used to configure the LTM4682's Channel 3 output to power-up to a VOUT_COMMAND value (and associated output voltage monitoring and protection/fault-detection thresholds) different from those of NVM contents. See the Applications Information section. Connecting resistor(s) from VOUT3_CFG to SGND and/or VTRIM3_CFG to SGND in this manner allows a convenient way to configure multiple LTM4682s with identical NVM contents for different output voltage settings all without GUI intervention or the need to custom-preprogram module NVM contents. Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that the use of R_{CONFIG}s on VOUT3_CFG/VTRIM3_CFG can affect the V_{OUT3} range setting (MFR_PWM_MODE1[1]) and loop gain. For addressed ASEL_23, Page 0x00 corresponds to Channel 2 and Page 0x01 corresponds to Channel 3. See PAGE description section.

VTRIM3_CFG (AB9): Output Voltage Select Pin for V_{OUT3}, Fine Setting. Works in combination with VOUT3_CFG to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 3, at SV_{IN_23} power-up. See VOUT3_CFG and the Applications Information section. A resistor divider from 2.5V to SGND connected to the pin will set the TRIM value (see Table 2). Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that the use of R_{CONFIG}s on VOUT3_CFG/VTRIM3_CFG can affect the V_{OUT3} range setting (MFR_PWM_MODE0[1]) and loop gain. For addressed ASEL_23, Page 0x00 corresponds to Channel 2 and Page 0x01 corresponds to Channel 3. See PAGE description section.

VTRIM2_CFG (AB10): Output Voltage Select Pin for V_{OUT2}, Fine Setting. Works in combination with VOUT2_CFG to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 2, at SV_{IN_23} power-up. See VOUT2_CFG and the Applications Information section. A resistor divider from 2.5V to SGND connected to the pin will set the TRIM value. See Table 2. Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that the use of R_{CONFIG}s on VOUT2_CFG/VTRIM2_CFG can affect the V_{OUT2} range setting (MFR_PWM_MODE0[1]) and loop gain. For addressed ASEL_23, Page 0x00 corresponds to Channel 2 and Page 0x01 corresponds to Channel 3. See PAGE description section.

V_{DD25_23} (AB11): Internally Generated 2.5V Power Supply Output Pin for Channels 2 and 3 Circuits. Do not load this pin with external current. This pin is used strictly to bias internal logic and provides current for the internal pull-up resistors connected to the configuration-programming pins. No external decoupling is required.

VOUT1_CFG (B8): Output Voltage Select Pin for V_{OUT1}, Coarse Setting. If the VOUT1_CFG and VTRIM1_CFG pins are both left open—or, if the LTM4682 is configured to ignore pin-strap (R_{CONFIG}) resistors, i.e., MFR_CONFIG_ALL[6] = 1b—then the LTM4682s target V_{OUT1} output voltage setting (VOUT_COMMAND1) and associated power-good and OV/UV warning and fault thresholds are dictated at SV_{IN_01} power-up according to the LTM4682's NVM contents. A resistor divider connected to 2.5V and to SGND to this pin—in combination with resistor pin settings on VTRIM1_CFG, and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0b—can be used to configure the LTM4682's Channel 1 output to power-up to a VOUT_COMMAND value (and associated output voltage monitoring and protection/fault-detection thresholds) different from those of NVM contents. See the Applications Information section. Connecting resistor(s) from VOUT1_CFG to SGND and/or VTRIM1_CFG to SGND in this manner allows a convenient way to configure multiple LTM4682s with identical NVM contents for different output voltage settings all without GUI intervention or the need to custom-preprogram module NVM contents. Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that the use of R_{CONFIG}s on VOUT1_CFG/VTRIM1_CFG can affect the V_{OUT1} range setting (MFR_PWM_MODE1[1]) and loop gain. For addressed ASEL_01, Page 0x00 corresponds to Channel 0 and Page 0x01 corresponds to Channel 1. See PAGE description section.

ASEL_01 (B9): Serial Bus Address Configuration Pin for Channels 0 and 1 Controller. On any given I^2C/SMBus

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serial bus segment, every device must have its unique subordinate address. If this pin is left open, the LTM4682 powers up to its default subordinate address of 0x4E (hexadecimal), i.e., 1001110b (industry-standard convention is used throughout this document: 7-bit subordinate addressing). The lower 4 bits of the LTM4682's subordinate address can be altered from this default value by connecting a resistor from this pin to SGND. Minimize capacitance—especially when the pin is left open—to ensure accurate detection of the pin state. It is recommended to use a resistor to set the address. The ASEL_01 address will be used to address Channels 0 and 1, and a different ASEL_23 address will be used to address Channels 2 and 3. For addressed ASEL_01, Page 0x00 corresponds to Channel 0 and Page 0x01 corresponds to Channel 1. See PAGE description section. The GUI will represent Channel 0 as U0:A0 and Channel 1 as U0:A1. See the LTpowerPlay Screen Shot (Figure 31).

RUN0, RUN1 (B10, B11 Respectively): Enable Run Input for Channels 0 and 1, Respectively. Open-drain input and output. The logic high on these pins enables the respective outputs of the LTM4682. These open-drain output pins hold the pin low until the LTM4682 is out of reset and SV_{IN_01} is detected to exceed V_{IN_ON}. A pull-up resistor to 3.3V is required in the application. The LTM4682 pulls RUN0 and/or RUN1 low, as appropriate, when a global fault and/or channel-specific fault occurs whose fault response is configured to latch off and cease regulation; issuing a CLEAR_FAULTS command through I^2C or power-cycling SV_{IN_01} is necessary to restart the module, in such cases. Do not pull RUN logic high with a low impedance source. The $INTV_{CC}$ is active when SVIN_01 is above UVLO. This provides power to the V_{DD33} and V_{DD25} to allow programming the EEPROM.

SW0 (C1-C2, D1-D2, E1-E2): Switching Node of Channel 0 Step-Down Converter Stage. Used for test purposes or EMI-snubbing. It may be routed a short distance to a local test point to monitor the switching action of Channel 0, if desired, but do not route near any sensitive signals. Otherwise, leave electrically isolated (open).

V_{DD25_01} (C8): Internally Generated 2.5V Power Supply Output Pin for Channels 0 and 1 Circuits. Do not load this pin with external current; it is used strictly to bias internal logic and provides current for the internal pull-up resistors connected to the configuration-programming pins. No external decoupling is required.

VTRIM1_CFG (C9): Output Voltage Select Pin for V_{OUT1}, Fine Setting. Works in combination with VOUT1_CFG to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 1, at SV_{IN_01} power-up. See VOUT1_CFG and the Applications Information section. A resistor divider from 2.5V to SGND connected to the pin will set the TRIM value. See Table 2. Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that the use of R_{CONFIG}s on VOUT1_CFG/VTRIM1_CFG can affect the V_{OUT1} range setting (MFR_PWM_MODE1[1]) and loop gain. For addressed ASEL_01, Page 0x00 corresponds to Channel 0 and Page 0x01 corresponds to Channel 1. See PAGE description section.

SDA_01, SDA_23 (C10, V8): Serial Bus Data Open-Drain Input and Output. A pull-up resistor to 3.3V is required in the application. The SDA_01 is for Channels 0 and 1, and SDA_23 is for Channels 2 and 3.

$\overline{\text{ALERT}}$_01, $\overline{\text{ALERT}}$_23 (C11, W8): Open-Drain Digital Output. A pull-up resistor to 3.3V is required in the application only if SMBALERT interrupt detection is implemented in one's SMBus system.

SHARE_CLK_01, SHARE_CLK_23 (D8, AA11): Share Clock, Bidirectional Open-Drain Clock Sharing Pin. Nominally 100kHz. Used for synchronizing the time base between multiple LTM4682s (and any other Analog Devices ICs with a SHARE_CLK pin)—to realize well-defined rail sequencing and rail tracking. Connect the SHARE_CLK pins of all such devices together. All devices with a SHARE_CLK pin will synchronize to the fastest clock. A pull-up resistor to 3.3V is only required when synchronizing the time base between devices.

VTRIM0_CFG (D9): Output Voltage Select Pin for V_{OUT0}, Fine Setting. Works in combination with VOUT0_CFG to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 0, at SV_{IN_01} power-up. See VOUT0_CFG and

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the Applications Information section. A resistor divider from 2.5V to SGND connected to the pin will set the TRIM value. See Table 2. Minimize capacitance especially when the pin is left open to ensure accurate detection of the pin state. Note that the use of R_{CONFIG}s on VOUT0_CFG/VTRIM0_CFG can affect the V_{OUT0} range setting (MFR_PWM_MODE0[1]) and loop gain. For addressed ASEL_01, Page 0x00 corresponds to Channel 0 and Page 0x01 corresponds to Channel 1. See PAGE command description section.

SCL_01, SCL_23 (D10, W9): Serial Bus Clock Open-Drain Input (Can Be an Input and Output, if Clock Stretching is Enabled). A pull-up resistor to 3.3V is required in the application for digital communication to the SMBus main device(s) that nominally drive this clock. The LTM4682 will never encounter scenarios where it would need to engage clock stretching unless SCL communication speeds exceed 100kHz—and even then, LTM4682 will not clock stretch unless clock stretching is enabled using setting MFR_CONFIG_ALL[1] = 1b. The factory-default NVM configuration setting has MFR_CONFIG_ALL[1] = 0b: clock stretching disabled. If communication on the bus at clock speeds above 100kHz is required, the user's SMBus main device(s) need to implement clock stretching support to ensure solid serial bus communications, and only then should MFR_CONFIG_ALL[1] be set to 1b. When clock stretching is enabled, SCL becomes a bidirectional, open-drain output pin on the LTM4682.

SYNC_01, SYNC_23 (D11,V9): External Clock Synchronization Input and Open-Drain Output Pin. If an external clock is present at this pin, the switching frequency will be synchronized to the external clock. If the main clock mode is enabled, this pin will pull low at the switching frequency with a 500ns pulse to the ground. A resistor pull-up to 3.3V is required in the application if the LTM4682 is the main device.

V_{DD33_01} (E8): Internally Generated 3.3V Power Supply Output Pin for Channels 0 and 1 Circuits. This pin should only be used to provide external current for the pull-up resistors required for $\overline{FAULT}n$, SHARE_CLK_*nn*, and SYNC_*nn*, and may be used to provide external current for pull-up resistors on RUN*n*, SDA_*nn*, SCL_*nn*, $\overline{ALERT}$_*nn* and PGOOD*n*. Where *nn* is either 0,1 or 2,3 channels, and *n* is the actual channel. No external decoupling is required. V_{DD33_01} is powered from V_{BIAS} and programming RUN*n* improves efficiency.

WP_01, WP_23 (E9, Y11): Write Protect Pin, Active High. An internal 10µA current source pulls this pin to V_{DD33}. If WP is open circuit or logic high, only I^2C writes to PAGE, OPERATION, CLEAR_FAULTS, MFR_CLEAR_PEAKS and MFR_EE_UNLOCK are supported. Additionally, Individual faults can be cleared by writing 1b's to bits of interest in registers prefixed with STATUS. If WP is low, I^2C writes are unrestricted. V_{OSNS0}^- (H11): Channel 0 negative differential voltage sense input. See V_{OSNS0}^+.

TSNS0, TSNS1, TSNS2, TSNS3 (E11, E10, U8, U9): Power Stage Temperature Monitors for the 4 Channels. See the Applications Information section.

V_{OSNS1}^- (F8): Channel 1 Negative Differential Voltage Sense Input. See V_{OSNS1}^+.

SGND01, SGND23 (F10-F11, U10-U11): SGND is the signal ground return path of the LTM4682 internal controllers. SGND is not internally connected to GND. Connect SGND to GND local to the LTM4682. See the Layout Checklist/Example section.

V_{OUT1} (F13-F15, G13-G15, H13-H15, J13-J15, K13-K15): Channel 1 Output Voltage. Place the recommended output capacitors from this shape to GND. See the Layout Checklist/Example section.

SW1 (G1-G2, H1-H2, J1-J2): Switching Node of Channel 1 Step-Down Converter Stage. Used for test purposes or EMI-snubbing. It may be routed a short distance to a local test point to monitor the switching action of Channel 1, if desired, but do not route near any sensitive signals. Otherwise, leave it open.

V_{OSNS1}^+ (G8): Channel 1 Positive Differential Voltage Sense Input. Together, V_{OSNS1}^+ and V_{OSNS1}^- serve to Kelvin-sense the V_{OUT1} output voltage at V_{OUT1}'s point of load (POL) and provide the differential feedback signal directly to Channel 1's feedback loop. Command V_{OUT1}'s

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target regulation voltage by serial bus. Its initial command value at SV_{IN_01} power-up is dictated by NVM contents (factory default: 0.75V)—or, optionally, may be set by configuration resistors; see VOUT1_CFG, VTRIM1_CFG and the Applications Information section.

COMP0b, COMP1b, COMP2b, COMP3b (G10, F9, T9, W11): Current Control Threshold and Error Amplifier Compensation Nodes. Each associated channel's current comparator tripping threshold increases with its compensation voltage. Each channel has a 22pF to SGND.

COMP0a, COMP1a, COMP2a, COMP3a (G11, G9, T8, V11): Loop Compensation Nodes. The internal PWM loop compensation resistors R_{COMPn} of the LTM4682 can be adjusted using bit[4:0] of the MFR_PWM_COMP command. The transconductance of the LTM4682 PWM error amplifier can be adjusted using bit[7:5] of the MFR_PWM_COMP command. These two loop compensation parameters can be programmed when the device is in operation. See the Programmable Loop Compensation subsection in the Applications Information section for further details. See Figure 1.

PGOOD0, PGOOD1, PGOOD2, PGOOD3 (H9, H8, R10, T10): Power Good Indicator Outputs. The open-drain logic output is pulled to the ground when the output exceeds the UV and OV regulation window. The output is deglitched by an internal 100µs filter. A pull-up resistor to 3.3V is required in the application.

$I_{IN\_01}^+$ (H10): Positive Current Sense Amplifier Input. If the input current sense amplifier is not used, this pin must be shorted to the $I_{IN\_01}^-$ and SV_{IN_01} pin. See the Applications Information section for more details about the input current sensing.

V_{OSNS0}^- (H11): Channel 0 Negative Differential Voltage Sense Input. See V_{OSNS0}^+.

SV_{IN_01} (J8): Input Supply for LTM4682's Internal Control IC for Channels 0 and 1. In most applications, SV_{IN_01} connects to V_{IN01}. SV_{IN_01} can be operated from an auxiliary supply separate from V_{IN01} for powering the V_{IN01} from a lower supply like 6V. The SVIN_01 pin requires 1Ω and 1µF decoupling capacitor to measure the actual control chip current. The 1Ω resistor is used to measure the actual control chip current. See MFR_READ_ICHIP and MFR_ADC_CONTROL COMMAND section. When operating from 4.5V to 5.75V with no auxiliary bias supply, then the main input supply should connect to SV_{IN_01} and $INTV_{CC\_01}$. See Test Circuit 2 for an example. In this configuration, the ICHIP current will not be relevant since $INTV_{CC\_01}$ is connected to SV_{IN_01}.

$INTV_{CC\_01}$ (J9): Internal Regulator, 5.5V Output. When operating the LTM4682 from $5.75V \le SV_{IN\_01} \le 16V$, an internal LDO generates $INTV_{CC\_01}$ from SV_{IN_01} to bias internal control circuits and the MOSFET drivers of the LTM4682's Channels 0 and 1. An external 4.7µF ceramic decoupling capacitor is required. The $INTV_{CC\_01}$ is on regulated regardless of the RUN*n* pin state. When operating the LTM4682 with $4.5V \le SV_{IN\_01} < 5.75V$, $INTV_{CC\_01}$ must be electrically shorted to SV_{IN_01}, and the RUNP pin must be pulled to GND. The V_{BIAS} takes over after startup when the input voltage is greater than 7V.

$I_{IN\_01}^-$ (J10): Negative Current Sense Amplifier Input. If the input current sense amplifier is not used, this pin must be shorted to the $I_{IN\_01}^+$ and SV_{IN_01} pin. See the Applications Information section for more details about the input current sensing.

V_{OSNS0}^+ (J11): Channel 0 Positive Differential Voltage Sense Input. Together, V_{OSNS0}^+ and V_{OSNS0}^- serve to Kelvin-sense the V_{OUT0} output voltage at V_{OUT0}'s point of load (POL) and provide the differential feedback signal directly to Channel 0's feedback loop. Command V_{OUT0}'s target regulation voltage by serial bus. Its initial command value at SV_{IN_01} power-up is dictated by NVM contents (factory default: 0.75V)—or, optionally, may be set by configuration resistors; see VOUT0_CFG, VTRIM0_CFG and the Applications Information section.

V_{IN23} (N5-N6, P5-P6, R5-R6, T5-T6, U5-U6, V5-V6, W5-W6, Y5-Y6, AA5-AA6, AB5-AB6): Positive Power Input to Channels 2 and 3 Switching Stages. Provide sufficient decoupling capacitance in the form of MLCCs and low ESR electrolytic (or equivalent) to handle reflected input current ripple from the step-down switching stage. The MLCCs should be placed as close to the LTM4682 as physically possible. See the Layout Checklist/Example section in the Applications Information section.

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V_{IN_VBIAS} (N9): Input pin to the internal step down regulator that produces 5.5V (V_{BIAS} pin) to power both internal controllers to reduce power dissipation after power up. Each internal controller has an $INTV_{CC\_01}$ or $INTV_{CC\_23}$ regulator that is powered from SV_{IN_01} or SV_{IN_23}. To eliminate this power loss through these linear regulators, the V_{BIAS} powers both at very high efficiency.

V_{BIAS} (N10): A 5.5V step down output that powers both internal controllers to reduce power loss. It provides a 22µF ceramic bypass capacitor on this pin to GND. SV_{IN_01} and SV_{IN_23} must be higher than 7V for this V_{BIAS} to supply the controllers. When the input voltage is between 4.5V to 5.75V, pull the RUNP pin to GND, and connect SV_{IN_01} and SV_{IN_23} to $INTV_{CC\_01}$ and $INTV_{CC\_23}$, respectively. Powering up the V_{BIAS} regulator with the SV_{IN_01} and SV_{IN_23} greater than 7V will power the $INTV_{CC\_01}$, $INTV_{CC\_02}$, the V_{DD33_01}, V_{DD33_23}, V_{DD25_01}, and V_{DD25_23} from V_{BIAS}. Otherwise, these sources will get their power from SV_{IN_01} and SV_{IN_23}. This will allow the programming each internal controller's EEPROM with the power regulator channels in the off position.

RUNP (N11): This pin enables the Internal 5.5V V_{BIAS} step down regulator. Pulling this pin above 0.85V will enable the Internal regulator. The pin is rated to V_{IN}, so connect to V_{IN} to enable, and connect to GND to disable. When the input voltage is between 4.5V to 5.75V, pull the RUNP pin to GND, and connect SV_{IN_01} and SV_{IN_23} to $INTV_{CC\_01}$ and $INTV_{CC\_23}$, respectively.

V_{OUT2} (N13-N15, P13-P15, R13-R15, T13-T15, U13-U15): Channel 2 Output Voltage. Place the recommended output capacitors from this shape to GND. See the Layout Checklist/Example section.

SW2 (P1-P2, R1-R2, T1-T2): Switching Node of Channel 2 Step-Down Converter Stage. Used for test purposes or EMI-snubbing. It may be routed a short distance to a local test point to monitor switching action of Channel 2, if desired, but do not route near any sensitive signals. Otherwise, leave it open.

V_{OSNS2}^{+} (P8): Channel 2 Positive Differential Voltage Sense Input. Together, V_{OSNS2}^{+} and V_{OSNS2}^{-} serve to Kelvin-sense the V_{OUT2} output voltage at V_{OUT2}'s POL and provide the differential feedback signal directly to Channel 2's feedback loop. Command V_{OUT2}'s target regulation voltage by serial bus. Its initial command value at SV_{IN_23} power-up is dictated by NVM contents (factory default: 0.75V)—or, optionally, may be set by configuration resistors; see VOUT2_CFG, VTRIM2_CFG and the Applications Information section.

$I_{IN\_23}^{-}$ (P9): Negative Current Sense Amplifier Input. If the input current sense amplifier is not used, this pin must be shorted to the $I_{IN\_23}^{+}$ and SV_{IN_23} pin. See the Applications Information section for more details about the input current sensing.

$INTV_{CC\_23}$ (P10): Internal Regulator, 5.5V Output. When operating the LTM4682 from $5.75V \le SV_{IN\_23} \le 16V$, an internal LDO generates $INTV_{CC\_23}$ from SV_{IN_23} to bias internal control circuits and the MOSFET drivers of the LTM4682's Channels 2 and 3. An external 4.7µF ceramic decoupling i capacitor s required. $INTV_{CC\_23}$ is on regulated regardless of the RUN*n* pin state. When operating the LTM4682 with $4.5V \le SV_{IN\_23} < 5.75V$, $INTV_{CC\_23}$ must be electrically shorted to SV_{IN_23}, and the RUNP pin must be pulled to GND. V_{BIAS} takes over after startup when the input voltage is greater than 7V.

SV_{IN_23} (P11): Input Supply for LTM4682's Internal Control IC for Channels 2 and 3. In most applications, SV_{IN_23} connects to V_{IN_23}. SV_{IN_23} can be operated from an auxiliary supply separate from V_{IN23} for powering the V_{IN23} from a lower supply like 6V. The SVIN_23 pin requires 1Ω and 1µF decoupling capacitor to measure the actual control chip current. The 1Ω resistor is used to measure the actual control chip current. See MFR_READ_ICHIP and MFR_ADC_CONTROL COMMAND section. When operating from 4.5V to 5.75V with no auxiliary bias supply, then the main input supply should connect to SV_{IN_23} and $INTV_{CC\_23}$. See Test Circuit 2 for an example. In this configuration, the I_{CHIP} current will not be relevant since $INTV_{CC\_23}$ is connected to SV_{IN_23}.

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V_{OSNS2}^- (R8): Channel 2 Negative Differential Voltage Sense Input. See V_{OSNS2}^+.

$I_{IN\_23}^+$ (R9): Positive Current Sense Amplifier Input. If the input current sense amplifier is not used, this pin must be shorted to the $I_{IN\_23}^-$ and SV_{IN_23} pin. See the Applications Information section for more details about the input current sensing.

V_{OSNS3}^+ (R11): Channel 3 Positive Differential Voltage Sense Input. Together, V_{OSNS3}^+ and V_{OSNS3}^- serve to Kelvin-sense the V_{OUT3} output voltage at V_{OUT3}'s POL and provide the differential feedback signal directly to Channel 3's feedback loop. Command V_{OUT3}'s target regulation voltage by serial bus. Its initial command value at SV_{IN_23} power-up is dictated by NVM contents (factory default: 0.75V)—or, optionally, may be set by configuration resistors; see VOUT3_CFG, VTRIM3_CFG and the Applications Information section.

V_{OSNS3}^- (T11): Channel 3 Negative Differential Voltage Sense Input. See V_{OSNS3}^+.

SW3 (V1-V2, W1-W2, Y1-Y2): Switching Node of Channel 3 Step-Down Converter Stage. Used for test purposes or EMI-snubbing. It may be routed a short distance to a local test point to monitor switching action of Channel 3, if desired, but do not route near any sensitive signals. Otherwise, leave it open.

V_{OUT3} (V13-V15, W13-W15, Y13-Y15, AA13-AA15, AB13-AB15): Channel 3 Output Voltage. Place the recommended output capacitors from this shape to GND See the Layout Checklist/Example section.

RUN2, RUN3 (Y9, Y8): Enable Run Input for Channels 2 and 3, respectively. Open-drain input and output. The logic high on these pins enables the respective outputs of the LTM4682. These open-drain output pins hold the pin low until the LTM4682 is out of reset and SV_{IN_23} is detected to exceed V_{IN_ON}. A pull-up resistor to 3.3V is required in the application. The LTM4682 pulls RUN2 and/or RUN3 low, as appropriate, when a global fault and/or channel-specific fault occurs whose fault response is configured to latch off and cease regulation; issuing a CLEAR_FAULTS command through I^2C or power-cycling SV_{IN_23} is necessary to restart the module, in such cases. Do not pull RUN logic high with a low impedance source. $INTV_{CC}$ is active when SVIN_23 is above UVLO. This provides power to the V_{DD33} and V_{DD25} to allow programming the EEPROM.

V_{DD33_23} (Y10): Internally Generated 3.3V Power Supply Output Pin for Channels 2 and 3 Circuits. This pin should only be used to provide external current for the pull-up resistors required for FAULT_*nn*, SHARE_CLK_*nn*, and SYNC_*nn*, and may be used to provide external current for pull-up resistors on RUN*n*, SDA_*nn*, SCL_*nn*, ALERT_*nn* and PGOOD*n*. Where *nn* is either 0,1 or 2,3 channels, and *n* is the actual channel. No external decoupling is required. V_{DD33_23} can be powered from V_{BIAS}, such that this controller 2 can be programmed with RUN*n* low.

SIMPLIFIED BLOCK DIAGRAM

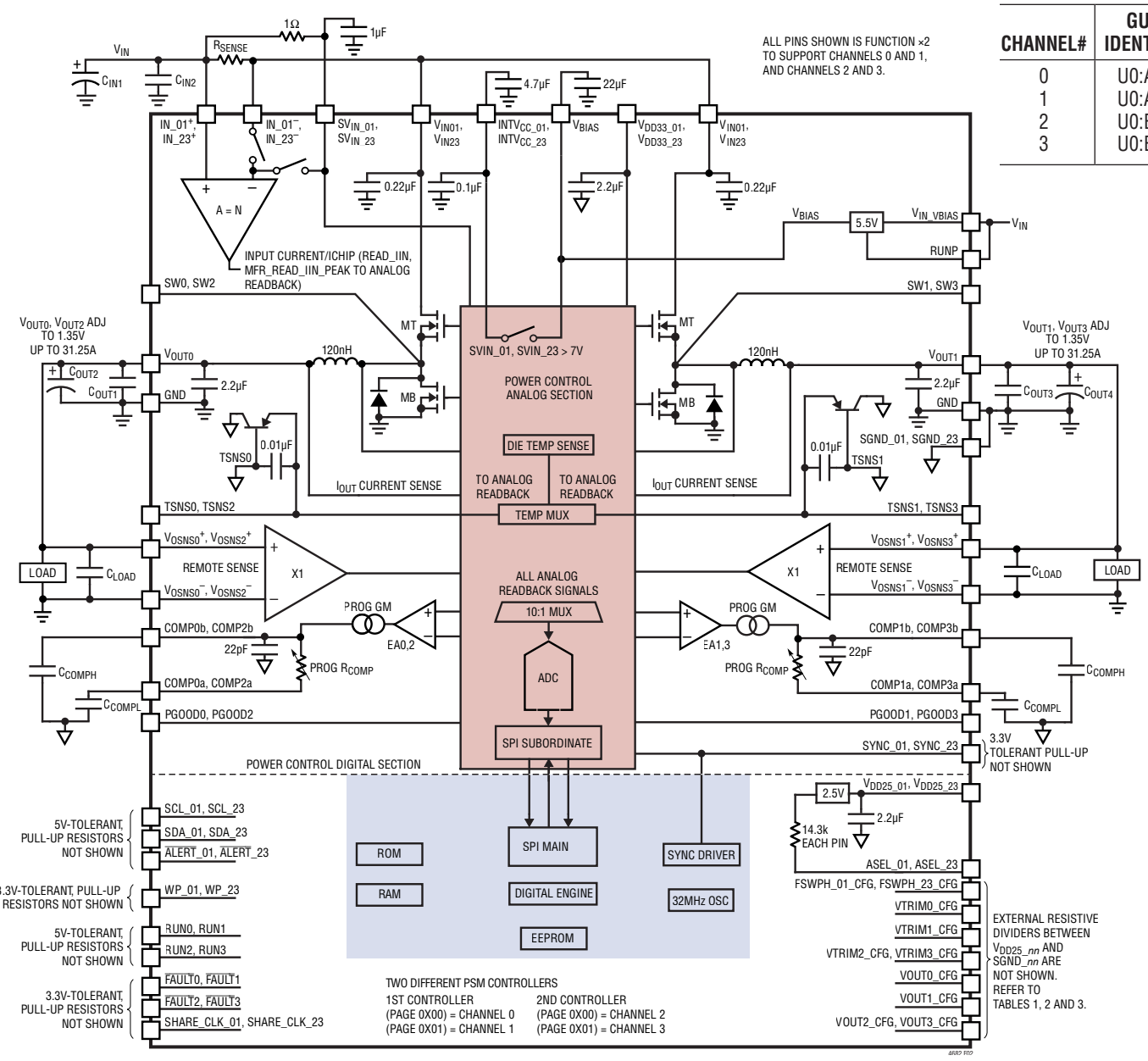


Figure 2. Simplified LTM4682 Block Diagram of the 1/2 Function

DECOUPLING REQUIREMENTS

T_A = 25°C. Using Figure 2 configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{INH}	External High Frequency Input Capacitor Requirement (5.75V ≤ V_{IN} ≤ 16V, V_{OUTn} Commanded to 0.75V).	I_{OUT0} = 31.25A I_{OUT1} = 31.25A		100 100		µF µF
C_{OUTn}	External High Frequency Output Capacitor Requirement (5.75V ≤ V_{IN} ≤ 16V, V_{OUTn} Commanded to 0.75V).	I_{OUT0} = 31.25A I_{OUT1} = 31.25A		800 800		µF µF

FUNCTIONAL DIAGRAM

CHANNEL#	GUI IDENTITY
0	U0:A0
1	U0:A1
2	U0:B0
3	U0:B1

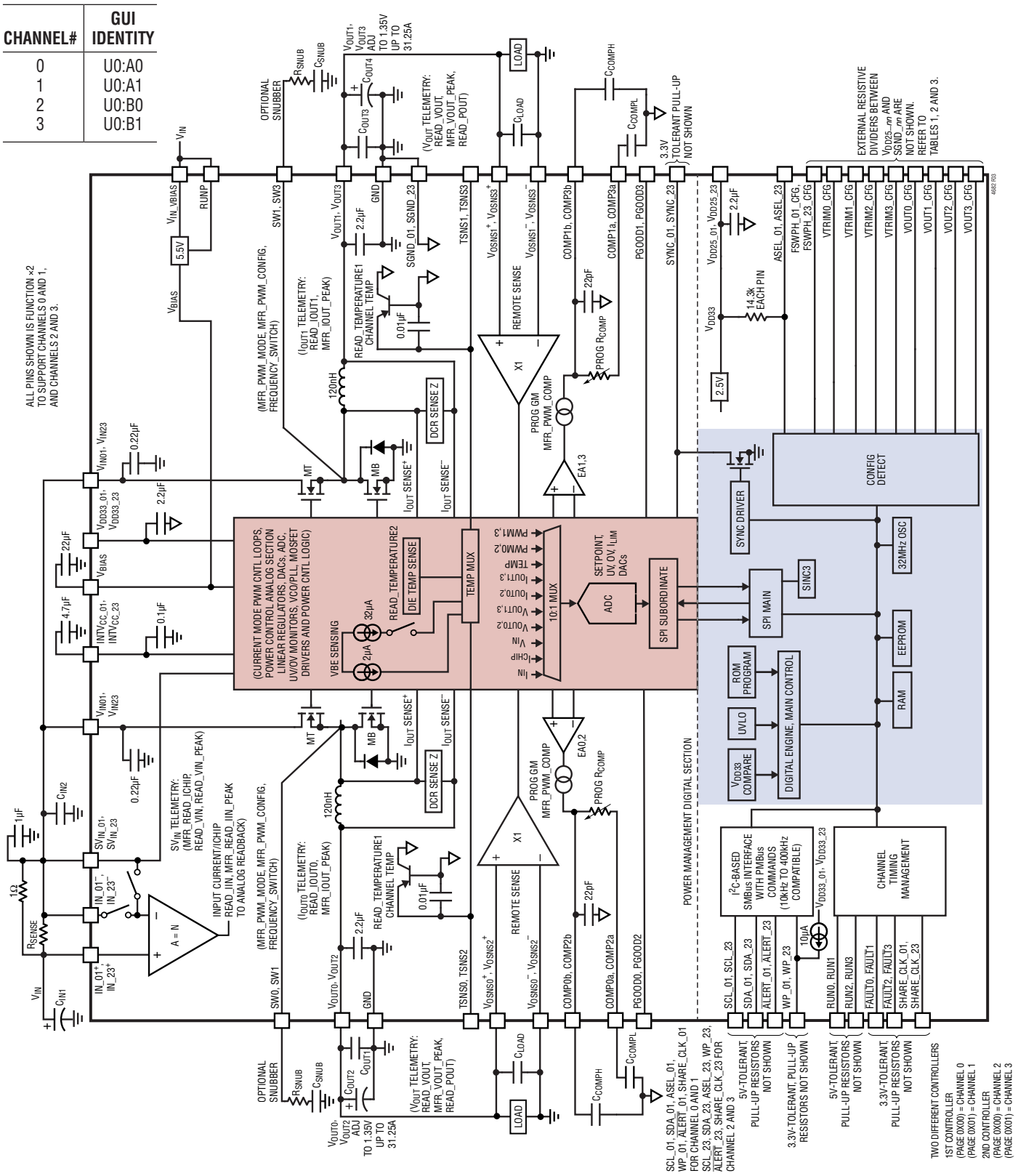
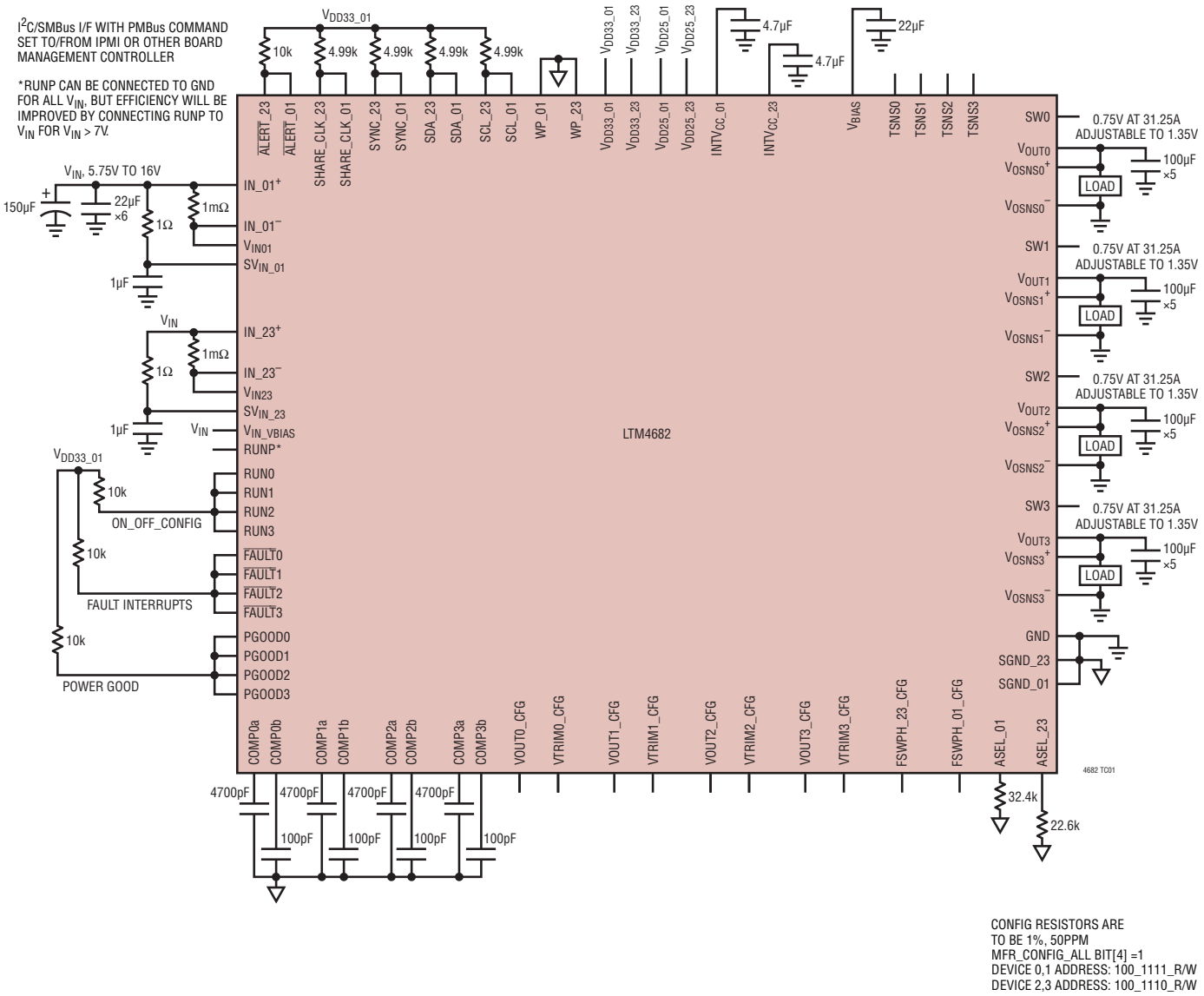


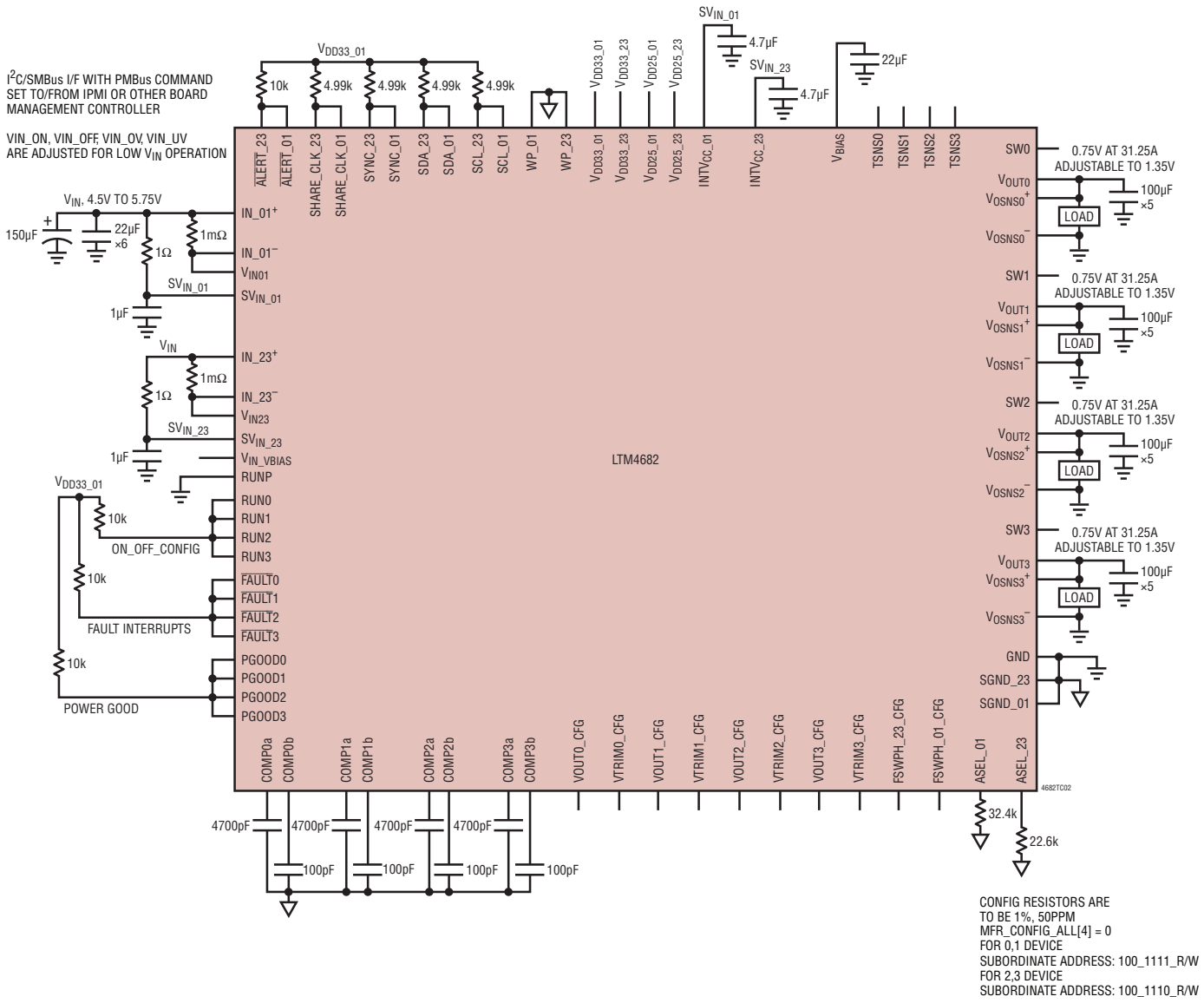
Figure 3. Functional LTM4682 Block Diagram

TEST CIRCUITS



Test Circuit 1.

TEST CIRCUITS



Test Circuit 2.

OPERATION

POWER MODULE INTRODUCTION

The LTM4682 is a highly configurable quad 31.25A output standalone nonisolated switching mode step-down DC/DC power supply with built-in EEPROM NVM with error correction coding (ECC) and I²C-based PMBus/SMBus 2-wire serial communication interface capable of 400kHz SCL bus speed. Four output voltages can be regulated (V_{OUT0}, V_{OUT1}, V_{OUT2}, and V_{OUT3}) with a few external input and output capacitors and pull-up resistors. Readback telemetry data of input and output voltages and input and output currents, and module temperatures are continually digitized cyclically by an integrated 16-bit analog-to-digital converter (ADC). Many fault thresholds and responses are customizable. Data can be autonomously saved to EEPROM when a fault occurs, and the resulting fault log can be retrieved over I²C later, for analysis. See Figure 2 and Figure 3 for the Block Diagrams. One controller for Channels 0 and 1, and second controller for Channels 2 and 3.

POWER MODULE OVERVIEW, MAJOR FEATURES

Major Features Include:

- Dedicated Power Good Indicators
- Direct Input and Chip Current Sensing
- Programmable Loop Compensation Parameters
- T_{INIT} Start-Up Time: 30ms
- PWM Synchronization Circuit, (See the Switching Frequency and Phase Section for More Details)
- MFR_ADC_CONTROL for Fast ADC Sampling of One Parameter (as Fast as 8ms) (See the PMBus Command Details Section)
- Fully Differential Output Sensing for All Four Channels; V_{OUT0}, V_{OUT1}, V_{OUT2}, and V_{OUT3}. All Programmable Up to 1.2V
- Power-Up and Program EEPROM with V_{BIAS}
- Input Voltage Up to 16V
- ΔV_{BE} Temperature Sensing
- SYNC Contention Circuit (See the Switching Frequency and Phase Section for More Details)
- Fault Logging
- Programmable Output Voltage
- Programmable Input Voltage On and Off Threshold Voltage
- Programmable Current Limit
- Programmable Switching Frequency
- Programmable OV and UV Threshold Voltage
- Programmable ON and Off Delay Times
- Programmable Output Rise/Fall Times
- Phase-Locked Loop for Synchronous PolyPhase® Operation (2, 3, 4 or 6 Phases)
- Nonvolatile Memory Configuration with ECC
- Optional External Configuration Resistors for Key Operating Parameters
- Optional Time Base Interconnect for Synchronization Between Multiple Controllers
- WP Pin to Protect Internal Configuration
- Stand Along Operation After User Factory Configuration
- PMBus, Version 1.2, 400kHz-Compliant Interface

The PMBus interface provides access to important power management data during system operation including:

- Internal Controller Temperature
- Internal Power Channel Temperature
- Average Output Current
- Average Output Voltage
- Average Input Voltage
- Average Input Current
- Average Chip Input Current from V_{IN}
- Configurable, Latched and Unlatched Individual Fault and Warning Status

Individual channels are accessed through the PMBus using the PAGE command, i.e., PAGE 0 or 1.

Fault reporting and shutdown behavior are fully configurable. Four individual $\overline{FAULT0}$, $\overline{FAULT1}$, $\overline{FAULT2}$,

OPERATION

and $\overline{\text{FAULT}}$3, outputs are provided. Each $\overline{\text{FAULT}}n$ can be masked independently.

Six dedicated pins for $\overline{\text{ALERT}}$_01, $\overline{\text{ALERT}}$_23, PGOOD0, PGOOD1, PGOOD2, and PGOOD3 functions are provided. The shutdown operation also allows all faults to be individually masked and can be operated in either unlatched (hiccup) or latched modes.

Individual status commands enable fault reporting over the serial bus to identify the specific fault event. Fault or warning detection includes the following:

- Output Undervoltage/Overvoltage
- Input Undervoltage/Overvoltage
- Input and Output Overcurrent
- Internal Overtemperature
- Communication, Memory or Logic (CML) Fault

EEPROM WITH ECC

The LTM4682 contains internal EEPROM with ECC to store user configuration settings and fault log information for Channels 0 and 1, and Channels 2 and 3. The EEPROM endurance retention and mass write operation time are specified in the Electrical Characteristics and Absolute Maximum Ratings sections. Write operations above T_J = 85°C are possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded. Read operations performed at temperatures between –40°C and 125°C will not degrade the EEPROM. Writing to the EEPROM above 85°C will result in degrading retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 85°C, the slight degradation in the data retention characteristics of the fault log will not take away from the usefulness of the function.

It is recommended that the EEPROM not be written when the die temperature is greater than 85°C. If the die temperature exceeds 130°C, the LTM4682 will disable all EEPROM write operations. All EEPROM write operations will be re-enabled when the die temperature drops below 125°C. The controller will also disable all the switching when the die temperature exceeds the internal overtemperature fault limit 160°C with a 10°C hysteresis.

The degradation in EEPROM retention for temperatures >125°C can be approximated by calculating the dimensionless acceleration factor using the following equation:

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor

E_a = activation energy = 1.4eV

$k = 8.617 \bullet 10^{-5}$ eV/K

T_{USE} = 125°C specified junction temperature

T_{STRESS} = actual junction temperature in °C

Example: Calculate the effect on retention when operating at a junction temperature of 130°C for 10 hours.

T_{STRESS} = 130°C

T_{USE} = 125°C,

$AF = e^{([(1.4/8.617 \bullet 10^{-5}) \bullet (1/398 - 1/403)])} = 1.66$

The equivalent operating time at 125°C = 16.6 hours.

Thus the overall retention of the EEPROM was degraded by 6.6 hours as a result of operating at a junction temperature of 130°C for 10 hours. The effect of the overstress is negligible when compared to the overall EEPROM retention rating of 87,600 hours at a maximum junction temperature of 125°C.

The integrity of the entire onboard EEPROM is checked with a CRC calculation each time its data is to be read, such as after a power-on reset or execution of a RESTORE_USER_ALL command. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the EEPROM CRC Error bit in the STATUS_MFR_SPECIFIC command is set, and the $\overline{\text{ALERT}}$ and RUN pins pulled low (PWM channels off). At that point the device will only respond at a special address 0x7C, which is activated only after an invalid CRC has been detected. The chip will also respond at the global addresses 0x5A and 0x5B, but using these addresses when attempting to recover

OPERATION

from a CRC issue is not recommended. All power supply rails associated with either PWM channel of a device reporting an invalid CRC should remain disabled until the issue is resolved. See the Applications Information section or contact the factory for more details on efficient in-system EEPROM programming, including bulk EEPROM Programming, which the LTM4682 also supports.

The LTM4682 contains two dual internal constant frequency current mode control buck regulators (Channel 0 and Channel 1, and Channel 2 and Channel 3) and whose power MOSFETs are capable of fast switching speed. Reference to the signal pins will be Name_*nn*, where *n* is either 01 or 23, or with name*n* when referring to signal pins that are related to the actual channel. The factory NVM-default switching frequency clocks SYNC_*nn* at 575kHz, to which the regulators synchronize their switching frequency. The default phase-interleaving angle between the channels is 180°. A pin-strapping resistor on FSWPH_*nn*_CFG configures the frequency of the SYNC_*nn* clock (switching frequency) and the channel phase relationship of the channels to each other and for the falling edge of the SYNC_*nn* signal. (Most possible combinations of the switching frequency and the phase-angle assignments are settleable by the resistor pin programming; see Table 3. Configure the LTM4682's NVM to implement settings unavailable by resistor-pin strapping.) When a FSWPH_*nn*_CFG pin-strap resistor sets the channel phase relationship of the LTM4682's channels, the SYNC_*nn* clock is not driven by the module. Instead, SYNC_*nn* becomes strictly a high impedance input, and the channel switching frequency is then synchronized to SYNC_*nn* provided by an externally-generated clock or sibling LTM4682 with a pull-up resistor to V_{DD33_nn}. Switching frequency and phase relationship can be altered through the I^2C interface, but only when the switching action is off, i.e., when the module is not regulating the outputs. See the Applications Information section for more details.

Programmable analog feedback loop compensation for Channel 0 to Channel 3 is accomplished with a capacitor connection from COMP*n*a to SGND, and a capacitor from COMP*n*b to SGND.) The COMP*n*b pin is for the high frequency gain roll-off and is the g_m amplifier output that has a programmable range, and the COMP*n*a pin has the programmable resistor range, along with a capacitor to SGND that sets the frequency compensation. See the Programmable Loop Compensation section. The LTM4682 module has sufficient stability margins and good transient performance with a wide range of output capacitors—even all-ceramic MLCCs. Table 13 provides guidance on input and output capacitors recommended for many common operating conditions, along with the programmable compensation settings. The Analog Devices LTpowerCAD® tool is available for transient and stability analysis, and experienced users who prefer to adjust the module's feedback loop compensation parameters can use this tool.

POWER-UP AND INITIALIZATION

The LTM4682 is designed to provide standalone supply sequencing and controlled turn-on and turn-off operation. It operates from a single input supply (4.5V to 16V) while three on-chip linear regulators generate internal 2.5V, 3.3V, and 5.5V per controller. If the V_{IN}*nn* does not exceed 5.75V, and the V_{BIAS} pin is turned off, the $INTV_{CC}$, V_{IN}*nn* and SV_{IN_nn} pins must be connected together. The controller configuration is initialized by an internal threshold-based UVLO where V_{IN}*nn* must be approximately 4V, and the 5.5V, 3.3V, and 2.5V linear regulators must be within approximately 20% of the regulated values. In addition to the power supply, a PMBus RESTORE_USER_ALL or MFR_RESET command can initialize the part, too.

The V_{BIAS} pin is the output of an internal 5.5V buck regulator to improve the efficiency of the circuit and minimize power loss on the LTM4682. The V_{BIAS} pin must exceed approximately 4.8V, and V_{IN} must exceed 7V before the $INTV_{CC}$ LDO operates from the V_{BIAS} pin. The V_{BIAS} regulator is powered from V_{IN_VBIAS} and enabled with RUNP.

During initialization, the external configuration resistors are identified and/or contents of the NVM are read into the controller's commands, and the power train is held off. The RUN*n*, $\overline{\text{FAULT}}$*n*, and PGOOD*n* are held low. The LTM4682 will use the contents of Table 1 through Table 5 to determine the resistor-defined parameters. See the R_{CONFIG} (Resistor Configuration) Pins section for more details. The resistor configuration pins only control some of the preset values of the controller. The remaining values are programmed in NVM either at the factory or by the user.

OPERATION

If the configuration resistors are not inserted or if the ignore RCONFIG bit is asserted (bit 6 of the MFR_CONFIG_ALL configuration command), the LTM4682 will use only the contents of NVM to determine the DC/DC characteristics. The ASEL_*nn* value read at power-up or reset is always respected unless the pin is open. The ASEL_*nn* will set the bottom 4LSBs, and the MSBs are set by NVM. See the Applications Information section for more details.

After the part has initialized, an additional comparator monitors V_{IN} through the SV_{IN_nn} pins. The VIN_ON threshold must be exceeded before the output power sequencing can begin. After V_{IN} is initially applied, the part will typically require 30ms to initialize and begin the TON_DELAY timer. The readback of voltages and currents may require an additional 0ms to 90ms.

SOFT-START

The method of start-up sequencing described in this section is time-based. The part must enter the run state before soft-start. The RUN pins are released by the LTM4682 after the part is initialized and SV_{IN_nn} exceeds the VIN_ON threshold. If multiple LTM4682s are used in an application, they all hold their respective RUN pins low until all devices are initialized, and SV_{IN_nn} exceeds the VIN_ON threshold for every device. The SHARE_CLK_*nn* pin assures all the devices connected to the signal use the same time base. The SHARE_CLK_*nn* pin is held low until the part has been initialized after V_{IN} is applied. The LTM4682 can be set to turn-off (or remain off) if SHARE_CLK_*nn* is low (set bit 2 of MFR_CHAN_CONFIG to 1). This allows the user to ensure synchronization across numerous Analog Devices ICs even if the RUN*n* pins cannot be connected together due to board constraints. In general, if the user cares about synchronization between chips, it is best not only to connect all the respective RUN*n* pins together but also to connect all the respective SHARE_CLK_*nn* pins together and pulled up to V_{DD33_nn} with a 10k resistor. This assures all chips begin sequencing simultaneously and use the same time base.

After the RUN*n* pins release and before entering a constant output voltage regulation state, the LTM4682 performs a monotonic initial ramp or soft-start. Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set-point. Once the LTM4682 is commanded to turn on (after power up and initialization), the controller waits for the user specified turn-on delay (TON_DELAY) before initiating this output voltage ramp. The rise time of the voltage ramp can be programmed using the TON_RISE command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting the value of TON_RISE to any value less than 0.25ms. The LTM4682 PWM always uses discontinuous mode during the TON_RISE operation. In discontinuous mode, the bottom MOSFET is turned off as soon as reverse current is detected in the inductor. This will allow the regulator to start up into a pre-biased load. When the TON_MAX_FAULT_LIMIT is reached, the part transitions to continuous mode, if so programmed. If TON_MAX_FAULT_LIMIT is set to zero, there is no time limit, and the part transitions to the desired conduction mode after TON_RISE completes and $V_{OUT}n$ has exceeded the VOUT_UV_FAULT_LIMIT and IOUT_OC is not present. However, setting TON_MAX_FAULT_LIMIT to a value of 0 is not recommended.

TIME-BASED SEQUENCING

The default mode for sequencing the outputs on and off is time-based. Each output is enabled after waiting a TON_DELAY amount of time following either a RUN pin going high, a PMBus command to turn on or the V_{IN} rising above a preprogrammed voltage. Off-sequencing is handled similarly. To ensure proper sequencing, make sure all ICs connect the SHARE_CLK_*nn* pin together and RUN*n* pins together. If the RUN*n* pins cannot be connected together for some reasons, set bit 2 of MFR_CHAN_CONFIG to 1. This bit requires the SHARE_CLK_*nn* pin to be clocking before the power supply output can start. When the RUN*n* pin is pulled low, the LTM4682 will hold the pin low for the MFR_RESTART_DELAY. The minimum MFR_RESTART_DELAY is TOFF_DELAY + TOFF_FALL + 136ms. This delay assures proper sequencing of all rails. The LTM4682 calculates this delay internally and will not process a shorter delay. However, a longer commanded MFR_RESTART_DELAY can be used by the part. The maximum allowed value is 65.52 seconds.

OPERATION

VOLTAGE-BASED SEQUENCING

The sequence can also be voltage-based. As shown in Figure 4, The PGOOD*n* pin is asserted when the UV threshold is exceeded for each output. It is possible to feed the PGOOD*n* pin from one LTM4682 channel into the RUN*n* pin of the next LTM4682 channel in the sequence, especially across multiple LTM4682s. The PGOOD*n* has a 100µs filter. If the V_{OUTn} voltage bounces around the UV threshold for a long period of time, it is possible for the PGOOD*n* output to toggle more than once. To minimize this problem, set the TON_RISE time under 100ms.

If a fault in the string of rails is detected, only the faulted rail and downstream rails will fault off. The rails in the string of devices in front of the faulted rail will remain on unless commanded off.

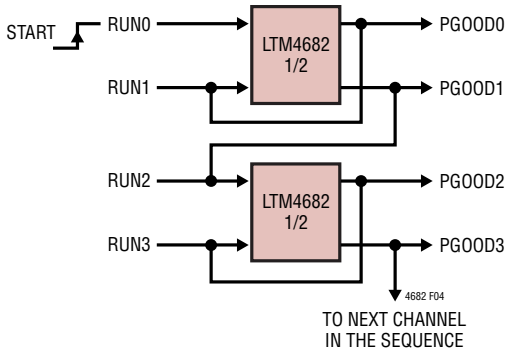


Figure 4. Event (Voltage) Based Sequencing

SHUTDOWN

The LTM4682 supports two shutdown modes. The first mode is a closed-loop shutdown response, with a user-defined turn-off delay (TOFF_DELAY) and ramp down rate (TOFF_FALL). The controller will maintain the mode of operation for TOFF_FALL. The second mode is the discontinuous conduction mode, the controller will not draw current from the load and the fall time will be set by the output capacitance, and load current, instead of TOFF_FALL.

The shutdown occurs in response to a fault condition or loss of SHARE_CLK_*nn* (if bit 2 of MFR_CHAN_CONFIG is set to a 1), or V_{INnn} falling below the VIN_OFF threshold, or $\overline{FAULT}$ pulled low externally (if the MFR_FAULT_RESPONSE is set to inhibit). Under these conditions, the power stage is disabled in order to stop the transfer of energy to the load as quickly as possible. The shutdown state can be entered from the soft-start or active regulation states or through user intervention.

There are two ways to respond to faults; retry mode and latched-off mode. In retry mode, the controller responds to a fault by shutting down and entering the inactive state for a programmable delay time (MFR_RETRY_DELAY). This delay minimizes the duty cycle associated with autonomous retries if the fault that causes the shutdown disappears once the output is disabled. The retry delay time is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. If multiple outputs are controlled by the same $\overline{FAULT}n$ pin, the decay time of the faulted output determines the retry delay. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG. Alternatively, latched-off mode means the controller remains latched-off following a fault, and clearing requires user intervention, such as toggling RUN*n* or commanding the part OFF and then ON.

LIGHT-LOAD CURRENT OPERATION

The LTM4682 has two modes of operation: high efficiency discontinuous conduction mode or forced continuous conduction mode. Mode selection is done using the MFR_PWM_MODE command (discontinuous conduction is always the start-up mode, and forced continuous is the default running mode).

If a controller is enabled for discontinuous operation, the inductor current is not allowed to reverse. The reverse current comparator's output turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined solely by the voltage on the COMP*n* pins. In this mode, the efficiency at light loads is lower than in discontinuous mode operation. However, continuous mode exhibits

OPERATION

lower output ripple and less interference with audio circuitry, but may result in a reverse inductor current, which can cause the input supply to boost. The VIN_OV_FAULT_LIMIT can detect this and turn off the offending channel. However, this fault is based on an ADC read and can take up to $t_{CONVERT}$ to detect. If there is a concern about the input supply boosting, keep the part in discontinuous conduction mode.

If the part is set to discontinuous mode operation, as the inductor average current increases, the controller will automatically modify the operation from discontinuous mode to continuous mode.

SWITCHING FREQUENCY AND PHASE

The switching frequency of the PWM can be established with an internal oscillator or an external time base. The internal phase-locked loop (PLL) synchronizes the PWM control to this timing reference with proper phase relation, whether the clock is provided internally or externally. The device can also be configured to provide the main device clock to other devices through the PMBus command, NVM setting, or external configuration resistors, as outlined in Table 3.

As a main clock, the LTM4682 will drive its open-drain SYNC_*nn* pin at the selected rate with a pulse width of 500ns. An external pull-up resistor between SYNC_*nn* and V_{DD33_nn} is required in this case. Only one device connected to SYNC_*nn* should be designated to drive the pin. The LTM4682 will automatically revert to an external SYNC_*nn* input, disabling its SYNC_*nn*, as long as the external SYNC_*nn* frequency is greater than 80% of the programmed SYNC_*nn* frequency. The external SYNC input shall have a duty cycle between 20% and 80%.

Whether configured to drive SYNC_*nn* or not, the LTM4682 can continue PWM operation using its internal oscillator if an external clock signal is subsequently lost.

The device can also be programmed to always require an external oscillator for PWM operation by setting bit 4 of MFR_CONFIG_ALL. The status of the SYNC driver circuit is indicated by bit 10 of MFR_PADS.

The MFR_PWM_CONFIG command can be used to configure the phase of each channel. The desired phase can also be set from EEPROM or external configuration resistors, as outlined in Table 3. The designated phase is the relationship between the falling edge of SYNC and the internal clock edge that sets the PWM latch to turn on the top power switch. Additional small propagation delays to the PWM control pins will also apply. Both channels must be off before the FREQUENCY_SWITCH and MFR_PWM_CONFIG commands can be written to the LTM4682.

The phase relationships and frequency options provide for numerous application options. Multiple LTM4682 modules can be synchronized to realize a PolyPhase array. In this case, the phases should be separated by 360/*n* degrees, where *n* is the number of phases driving the output voltage rail.

PWM LOOP COMPENSATION

The internal PWM loop compensation resistors R_{COMPna} of the LTM4682 can be adjusted using bit[4:0] of the MFR_PWM_COMP command for each controller.

The transconductance (g_m) of the LTM4682 PWM error amplifier can be adjusted using bit[7:5] of the MFR_PWM_COMP command. These two loop compensation parameters can be programmed when the device is in operation. See the Programmable Loop Compensation subsection in the Applications Information section for further details.

OUTPUT VOLTAGE SENSING

All four channels in LTM4682 have differential amplifiers, which allow the remote sensing of the load voltage between V^+ and V^- pins. The telemetry ADC is also fully differential and makes measurements between V_{OSNSn}^+ and V_{OSNSn}^- voltages for both channels at the V^+ and V^- pins, respectively. The maximum allowed is 1.5V, but the LTM4682 design is limited to 1.35V.

$INTV_{CC}/V_{BIAS}$ POWER

Power for the internal top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the RUNP pin is shorted to GND and the V_{BIAS} is off, an internal 5.5V linear regulator supplies $INTV_{CC}$

OPERATION

power from SV_{IN_nn}. When enabling V_{BIAS} at 5.5V output and SV_{IN} exceeds 7.0V, an internal switch turned on to source power from V_{BIAS} instead of $INTV_{CC}$ regulator. Using the V_{BIAS} allows the $INTV_{CC}$ power to be derived from a high efficiency internal source. V_{BIAS} can provide power to the internal 3.3V linear regulators when V_{IN} is present, which allows the LTM4682 controllers to be initialized and programmed even with channels off.

The $INTV_{CC\_nn}$ regulator is powered from the SV_{IN_nn} pin; the power through the IC is equal to $SV_{IN\_nn} \bullet I_{INTVCCnn}$. The gate charge current is dependent on the operating frequency. The typical $INTV_{CC\_nn}$ current for the LTM4682 is ~50mA. A 12V input voltage would equate to a difference of 7V per controller drop across the internal controller, when multiplied by 50mA equals a 350mW power loss. This loss can be eliminated by utilizing the V_{BIAS} regulator.

Do not connect $INTV_{CC\_nn}$ on the LTM4682 to an external supply because $INTV_{CC\_nn}$ will attempt to pull the external supply high and hit the current limit, significantly increasing the die temperature.

For applications where V_{IN} is 5V, connect the SV_{IN_nn} and $INTV_{CC\_nn}$ pins together to the 5V input through a 1Ω resistor, as shown in Test Circuit 2.

OUTPUT CURRENT SENSING AND SUB MILLIOHM DCR CURRENT SENSING

The LTM4682 uses a unique sub-milliohm inductor current sensing technique that provides a high level signal-to-noise ratio while sensing very low signals in current mode operation. This enables higher conversion efficiencies using the internal sub-milliohm inductors in heavy load applications. The current limit threshold can be accurately set with the MFR_PWM_MODE[7] for the high and low range (see IOUT_OC_FAULT_LIMIT).

The internal DCR sensing network, thus, the current limit is calculated based on the DCR of the inductor at room temperature. The DCR of the inductor has a large temperature coefficient, approximately 3900ppm/°C. The temperature coefficient of the inductor is written to the MFR_IOUT_CAL_GAIN_TC register. The external temperature is sensed near the inductor and used to modify the internal current limit circuit to maintain an essentially constant current limit with temperature. The current sensed is then digitized by the LTM4682's telemetry ADC with an input range of ±128mV, a noise floor of $7\mu V_{RMS}$, and a peak-peak noise of approximately 46.5µV. The LTM4682 computes the inductor current using the DCR value stored in the IOUT_CAL_GAIN command and the temperature coefficient stored in the MFR_IOUT_CAL_GAIN_TC command. The resulting current value is returned by the READ_IOUT command.

INPUT CURRENT SENSING

To sense the total input current consumed by the LTM4682's power stages, a sense resistor is placed between the supply voltage and the drain of the top N-channel MOSFET. The $I_{IN\_nn}^+$ and $I_{IN\_nn}^-$ pins are connected to the sense resistor. The filtered voltage is amplified by the internal high-side current sense amplifier and digitized by the LTM4682's telemetry ADC. The input current sense amplifier has three gain settings of 2×, 4×, and 8× set by the bit[6:5] of the MFR_PWM_CONFIG command. The maximum input sense voltage for the three gain settings is 50mV, 25mV, and 10mV, respectively. The LTM4682 computes the input current using the internal R_{SENSE} value stored in the IIN_CAL_GAIN command. The resulting measured power stage current is returned by the READ_IIN command. $I_{IN\_01}^+$, $I_{IN\_01}^-$ for controller 1 (Channels 0 and 1), and $I_{IN\_23}^+$, $I_{IN\_23}^-$ for controller 2 (Channels 2 and 3).

The LTM4682 uses a 1Ω resistor to measure the SV_{IN_nn} pin supply current being consumed by each LTM4682 internal controller. This value is returned by the MFR_READ_ICHIP command. The chip current is calculated by using the 1Ω value stored in the MFR_ICHIP_CAL_GAIN command. See the subsection titled Input Current Sense Amplifier in the Applications Information section for further details.

PolyPhase LOAD SHARING

Multiple LTM4682s can be arrayed to provide a balanced load-share solution by bussing the necessary pins. Figure 50 illustrates an 8-phase design sharing connections required for load sharing.

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If an external oscillator is not provided, the SYNC_*nn* pins should only be enabled on one of the LTM4682s controllers. The other(s) should be programmed to disable SYNC_*nn* controllers using bit 4 of MFR_CONFIG_ALL. If an external oscillator is present, the chip with the SYNC_*nn* pin enabled will detect the presence of the external clock and disable its output.

Multiple channels need to connect all the V_{OSNSn}^+ pins together, and all the V_{OSNSn}^- pins together, C_{OMPna} and C_{OMPnb} pins together as well. Do not assert bit[4] of MFR_CONFIG_ALL except in a PolyPhase application.

The user must share the SYNC_*nn*, SHARE_CLK_*nn*, $\overline{FAULT}n$, and $\overline{ALERT}n$ pins of these parts. Use the pull-up resistors on SYNC_*nn*, $\overline{FAULT}n$, SHARE_CLK_*nn* and $\overline{ALERT}n$. See the Typical Application section.

INTERNAL TEMPERATURE SENSE

Temperature is measured using the internal diode-connected PNP transistors, and the outputs are connected to TSNS0 to TSNS3 pins corresponding to Channels 0 to 3. These outputs are used for testing. Two different currents are applied to the diode (nominally 2µA and 32µA), and the temperature is calculated from a ΔV_{BE} measurement made with the internal 16-bit monitor ADC (see Figure 2 Block Diagram).

The LTM4682 will only implement ΔV_{BE} temperature sensing. Therefore the MFR_PWM_MODE bit[5] is reserved.

R_{CONFIG} (RESISTOR CONFIGURATION) PINS

There are twelve input pins utilizing 1% resistors between these pins to select key operating parameters. The pins are ASEL_01, ASEL_23, FSWPH_01_CFG, FSWPH_23_CFG, VOUT0_CFG, VOUT1_CFG, VOUT2_CFG, VOUT3_CFG, VTRIM0_CFG, VTRIM1_CFG, VTRIM2_CFG, and VTRIM3_CFG. If pins are floated, the value stored in the corresponding NVM command is used. If bit 6 of the MFR_CONFIG_ALL configuration command is asserted in NVM, the resistor input is ignored upon power-up except for ASEL, which is always respected. The resistor configuration pins are only measured during a power-up reset or after a MFR_RESET, or after an RESTORE_USER_ALL command is executed.

The VOUT*n*_CFG pin settings are described in Table 1. These pins set the LTM4682 V_{OUT0} to V_{OUT3} output voltage coarse settings. If the pin is open, the VOUT_COMMAND command is loaded from NVM to determine the output voltage. The default setting is to have the switcher off unless the voltage configuration pins are installed. The VTRIM*n*_CFG pins in Table 2 are used to set the output voltage fine adjustment setting. Both combine to offer several distinct output voltages.

The following parameters are set as a percentage of the output voltage if the R_{CONFIG} pins are used to determine the output voltage:

- VOUT_OV_FAULT_LIMIT.....+10%
- VOUT_OV_WARN_LIMIT.....+7.5%
- VOUT_MAX.....+7.5%
- VOUT_MARGIN_HIGH.....+5%
- VOUT_MARGIN_LOW.....–5%
- VOUT_UV_FAULT_LIMIT.....–7%

The FSWPH_CFG_*nn* pin settings are described in Table 3. This pin selects the switching frequency and phase of each channel. The phase relationships between the two channels and the SYNC_*nn* pin are determined in Table 3. To synchronize to an external clock, the part should be put into external clock mode (SYNC_*nn* output disabled but frequency set to the nominal value). If no external clock is supplied, the part will clock at the programmed frequency. If the application is multiphase and the SYNC_*nn* signal between chips is lost, the parts will not operate at the designed phase, even if they are programmed and trimmed to the same frequency.

This may increase the ripple voltage on the output, possibly producing undesirable operation. If the external SYNC_*nn* signal is being generated internally and external SYNC_*nn* is not selected, bit 10 of MFR_PADS will be asserted. If no frequency is selected and the external SYNC_*nn* frequency is not present, a PLL_FAULT will occur. If the user does not wish to see the $\overline{ALERT}$ from a PLL_FAULT, even if there is not a valid synchronization signal at power-up, the $\overline{ALERT}$ mask for PLL_FAULT must be written. See the description on SMBALERT_MASK for more details. If the SYNC_*nn* pin is connected between multiple ICs, only one of the ICs should have the SYNC_*nn* pin enabled using the

OPERATION

MFR_CONFIG_ALL[4] = 1, and all other ICs should be configured to have the SYNC pin disabled with MFR_CONFIG_ALL[4] = 0.

The ASEL_*nn* pin settings are described in Table 4. ASEL_*nn* selects the subordinate address for the LTM4682 internal controller. See Table 5.

Note: Per the PMBus specification, pin-programmed parameters can be overridden by commands from the digital interface, with the exception of ASEL_*nn*, which is always honored. Do not set any part address to 0x5A or 0x5B because these are global addresses, and all parts will respond to them.

Table 1. VOUT*n*_CFG Pin Strapping Look-Up Table for the LTM4682's Output Voltage, Coarse Setting (Not Applicable if MFR_CONFIG_ALL[6] = 1b) Top Resistor = 14.3k

R_{VOUTn_CFG}* (kΩ)	V_{OUTn} (V) SETTING COARSE	MFR_PWM_MODE*n*[1] BIT
Open	NVM	NVM
32.4	NVM	NVM
3.24	1.3	1
2.43	1.1	1
1.65	0.9	1
0.787	0.7	1
0	0.5	1

*R_{VOUTn_CFG} value indicated is nominal. Select R_{VOUTn_CFG} from a resistor vendor such that its value is always within 3% of the value indicated in the table. Consider resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity), and other effects (depending on one's specific application) could also affect R_{VOUTn_CFG}'s value over time. All such effects must be considered for resistor pin strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET or RESTORE_USER_ALL, over the lifetime of one's product. R_{TOP} = 14.3k is external to the part.

Example:

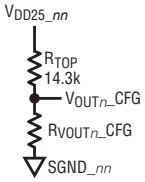
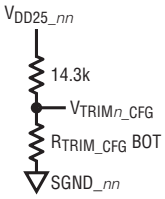


Table 2. VTRIMn_CFG Pin Strapping Look-Up Table for the LTM4682's Output Voltage, Fine Adjustment Setting (Not Applicable if MFR_CONFIG_ALL[6] = 1b) Top Resistor = 14.3k

R_{VTRIMn_CFG}* (kΩ)	V_{TRIM} (mV) FINE ADJUSTMENT TO V_{OUTn} SETTING WHEN RESPECTIVE
Open	0
32.4	99
22.6	86.625
18.0	74.25
15.4	61.875
12.7	49.5
10.7	37.125
9.09	24.75
7.68	12.375
6.34	–12.375
5.23	–24.75
4.22	–37.125
3.24	–49.5
2.43	–61.875
1.65	–74.25
0.787	–86.625
0	–99

*R_{VTRIMn_CFG} value indicated is nominal. Select R_{VTRIMn_CFG} from a resistor vendor such that its value is always within 3% of the value indicated in the table. Consider resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect R_{VTRIMn_CFG}'s value over time. All such effects must be considered for resistor pin strapping to yield the expected result at every SV_{IN_nn} power-up and/or every execution of MFR_RESET, or RESTORE_USER_ALL over the lifetime of one's product. R_{TOP} = 14.3k is external to the part.

Example:



OPERATION

Table 3. FSWPH_*nn*_CFG Pin Strapping Look-Up Table to Set the LTM4682's Switching Frequency and Channel Phase-Interleaving Angle (Not Applicable if MFR_CONFIG_ALL[6] = 1b), *nn* = 01 or 23 Channels, Set Top Resistor to 14.3k

R_{FSWPH_CFG}* (kΩ)	SWITCHING FREQUENCY (kHz)	θSYNC TO θ0,2	θSYNC TO θ1,3	BITS [2:0] of MFR_PWM_CONFIG	BIT [4] of MFR_CONFIG_ALL
Open	NVM; LTM4682 Default = 575	NVM; LTM4682 Default = 0°	NVM; LTM4682 Default = 180°	NVM; LTM4682 Default = 000b	NVM; LTM4682 Default = 0b
32.4	250	0°	180°	000b	0b
22.6	350	0°	180°	000b	0b
18.0	425	0°	180°	000b	0b
15.4	575	0°	180°	000b	0b
12.7	650	0°	180°	000b	0b
10.7	750	0°	180°	000b	0b
7.68	500	120°	240°	100b	0b
6.34	500	90°	270°	001b	0b
5.23	External**	0°	240°	010b	1b
4.22	External**	0°	120°	011b	1b
3.24	External**	60°	240°	101b	1b
2.43	External**	120°	300°	110b	1b
1.65	External**	90°	270°	001b	1b
0.787	External**	0°	180°	000b	1b
0	External**	120°	240°	100b	1b

*$R_{FSWPH\_nn\_CFG}$ value indicated is nominal. Select $R_{FSWPH\_nn\_CFG}$ from a resistor vendor such that its value is always within 3% of the value indicated in the table. Consider resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity), and other effects (depending on one's specific application) could also affect $R_{FSWPH\_nn\_CFG}$'s value over time. All such effects must be considered for resistor pin-strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET or RESTORE_USER_ALL, over the lifetime of one's product.

**External setting corresponds to FREQUENCY_SWITCH (Register 0x33) value set to 0x0000; the device synchronizes its switching frequency to that of the clock provided on the SYNC_*nn* pin, provided MFR_CONFIG_ALL[4] = 1b. R_{TOP} = 14.3k is external to the part.

Example:

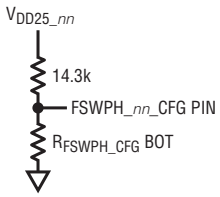


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Table 4. ASEL_*nn* Pin Strapping Look-Up Table to Set the LTM4682's Subordinate Address (Applicable Regardless of MFR_CONFIG_ALL[6] Setting)

R_{ASEL}* (kΩ)	SUBORDINATE ADDRESS
Open	100_1111_R/W
32.4	100_1111_R/W
22.6	100_1110_R/W
18.0	100_1101_R/W
15.4	100_1100_R/W
12.7	100_1011_R/W
10.7	100_1010_R/W
9.09	100_1001_R/W
7.68	100_1000_R/W
6.34	100_0111_R/W
5.23	100_0110_R/W
4.22	100_0101_R/W
3.24	100_0100_R/W
2.43	100_0011_R/W
1.65	100_0010_R/W
0.787	100_0001_R/W
0	100_0000_R/W

Where:

R/W = Read/Write bit in the control byte

All PMBus device addresses listed in the specification are 7 bits wide unless otherwise noted.

Note: The LTM4682 will always respond to subordinate addresses 0x5A and 0x5B regardless of the NVM or ASEL resistor configuration values.

*R_{CFG} value indicated is nominal. Select R_{CFG} from a resistor vendor such that its value is always within 3% of the value indicated in the table. Consider resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock cycling, moisture (humidity), and other effects (depending on one's specific application) could also affect R_{CFG}'s value over time. All such effects must be considered for resistor pin-strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET or RESTORE_USER_ALL, over the lifetime of one's product.

Example:

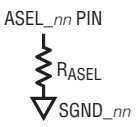

Table 5. LTM4682 MFR_ADDRESS Command Examples Expressed in 7- and 8-Bit Addressing

	HEX DEVICE ADDRESS		BIT								
DESCRIPTION	7-BIT	8-BIT	7	6	5	4	3	2	1	0	R/W
Rail[4]	0x5A	0xB4	0	1	0	1	1	0	1	0	0
Global[4]	0x5B	0xB6	0	1	0	1	1	0	1	1	0
Default	0x4F	0x9E	0	1	0	0	1	1	1	1	0
Example 1	0x40	0x80	0	1	0	0	0	0	0	0	0
Example 2	0x41	0x82	0	1	0	0	0	0	0	1	0
Disabled[2,3]			1	0	0	0	0	0	0	0	0

[1]This table can be applied to the MFR_RAIL_ADDRESS*n* commands, but not the MFR_ADDRESS command.

[2]A disabled value in one command does not disable the device, nor does it disable the global address.

[3]A disabled value in one command does not inhibit the device from responding to device addresses specified in other commands.

[4]It is not recommended to write the value 0x00, 0x0C (7-bit), 0x5A (7-bit), 0x5B (7-bit) or 0x7C(7-bit) to the MFR_CHANNEL_ADDRESS*n* or the MFR_RAIL_ADDRESSn commands.

FAULT DETECTION AND HANDLING

A variety of fault and warning reporting and handling mechanisms are available. Fault and warning detection capabilities include:

- Input OV $\overline{\text{FAULT}}$ Protection and UV Warning
- Average Input OC Warn
- Output OV/UV Fault and Warn Protection
- Output OC Fault and Warn Protection
- Internal control Die and Internal Module Overtemperature Fault and Warn Protection
- Internal Undertemperature Fault and Warn Protection
- CML Fault (Communication, Memory or Logic)
- External Fault Detection through the Bidirectional $\overline{\text{FAULT}}$*n* Pins

In addition, the LTM4682 can map any combination of fault indicators to their respective $\overline{\text{FAULT}}$*n* pin using the propagate $\overline{\text{FAULT}}$*n* response commands, MFR_FAULT_PROPAGATE. Typical usage of a $\overline{\text{FAULT}}$*n* pin is as a driver for an external crowbar device, overtemperature alert,

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overvoltage alert or as an interrupt to cause a microcontroller to poll the fault commands. Alternatively, the $\overline{FAULT}n$ pins can be used as inputs to detect external faults downstream of the controller that requires an immediate response.

Any fault or warning event will always cause the $\overline{ALERT}\_nn$ pin to assert low unless the fault or warning is masked by the SMBALERT_MASK. The pin will remain asserted low until the CLEAR_FAULTS command is issued, the fault bit is written to a 1 or, bias power is cycled, or an MFR_RESET command is issued, or the RUN*n* pins are toggled OFF/ON, or the part is commanded OFF/ON through PMBus, or an alert response address (ARA) command operation is performed. The MFR_FAULT_PROPAGATE command determines if the $\overline{FAULT}n$ pins are pulled low when a fault is detected.

Output and input fault event handling is controlled by the corresponding fault response byte as specified in Table 17 through Table 21. Shutdown recovery from these types of faults can either be autonomous or latched. For autonomous recovery, the faults are not latched, so if the fault conditions not present after the retry interval has elapsed, a new soft-start is attempted.

If the fault persists, the controller will continue to retry. The retry interval is specified by the MFR_RETRY_DELAY command and prevents damage to the regulator components by repetitive power cycling, assuming the fault condition itself is not immediately destructive. The MFR_RETRY_DELAY must be greater than 120ms. It can not exceed 83.88 seconds.

Status Registers and $\overline{ALERT}$ Masking

Figure 5 summarizes the internal LTM4682 status registers accessible by the PMBus command. These contain indications of various faults, warnings and other important operating conditions. As shown, the STATUS_BYTE and STATUS_WORD commands also summarize the contents of other status registers. See the PMBus Command Details section for specific information.

NONE OF THE ABOVE in the STATUS_BYTE indicates that one or more of the bits in the most-significant nibble of STATUS_WORD are also set.

In general, any asserted bit in a STATUS_x register also pulls the $\overline{ALERT}\_nn$ pin low. Once set, $\overline{ALERT}\_nn$ pin will remain low until one of the following occurs.

- A CLEAR_FAULTS or MFR_RESET Command Is Issued
- The Related Status Bit Is Written to a One
- The Faulted Channel Is Properly Commanded Off and Back On
- The LTM4682 Successfully Transmits Its Address During a PMBus ARA
- Bias Power Is Cycled

With some exceptions, the SMBALERT_MASK command can be used to prevent the LTM4682 from asserting $\overline{ALERT}\_nn$ for bits in these registers on a bit-by-bit basis. These mask settings are promoted to STATUS_WORD and STATUS_BYTE in the same fashion as the status bits themselves. For example, if $\overline{ALERT}\_nn$ is masked for all bits in channel *n* STATUS_VOUT, then $\overline{ALERT}\_nn$ is effectively masked for the V_{OUT} bit in STATUS_WORD for PAGE*n*. The BUSY bit in STATUS_BYTE also asserts $\overline{ALERT}\_nn$ low and cannot be masked. This bit can be set as a result of various internal interactions with PMBus communication. This fault occurs when a command is received that cannot be safely executed with one or both channels enabled. As discussed in the Application Information, BUSY faults can be avoided by polling MFR_COMMON before executing some commands.

If masked faults occur immediately after power up, $\overline{ALERT}\_nn$ may still be pulled low because there has not been time to retrieve all of the programmed masking information from EEPROM.

Status information contained in MFR_COMMON and MFR_PADS can be used to further debug or clarify the contents of STATUS_BYTE or STATUS_WORD as shown, but the contents of these registers do not affect the state of the $\overline{ALERT}\_nn$ pin and may not directly influence bits in STATUS_BYTE or STATUS_WORD.

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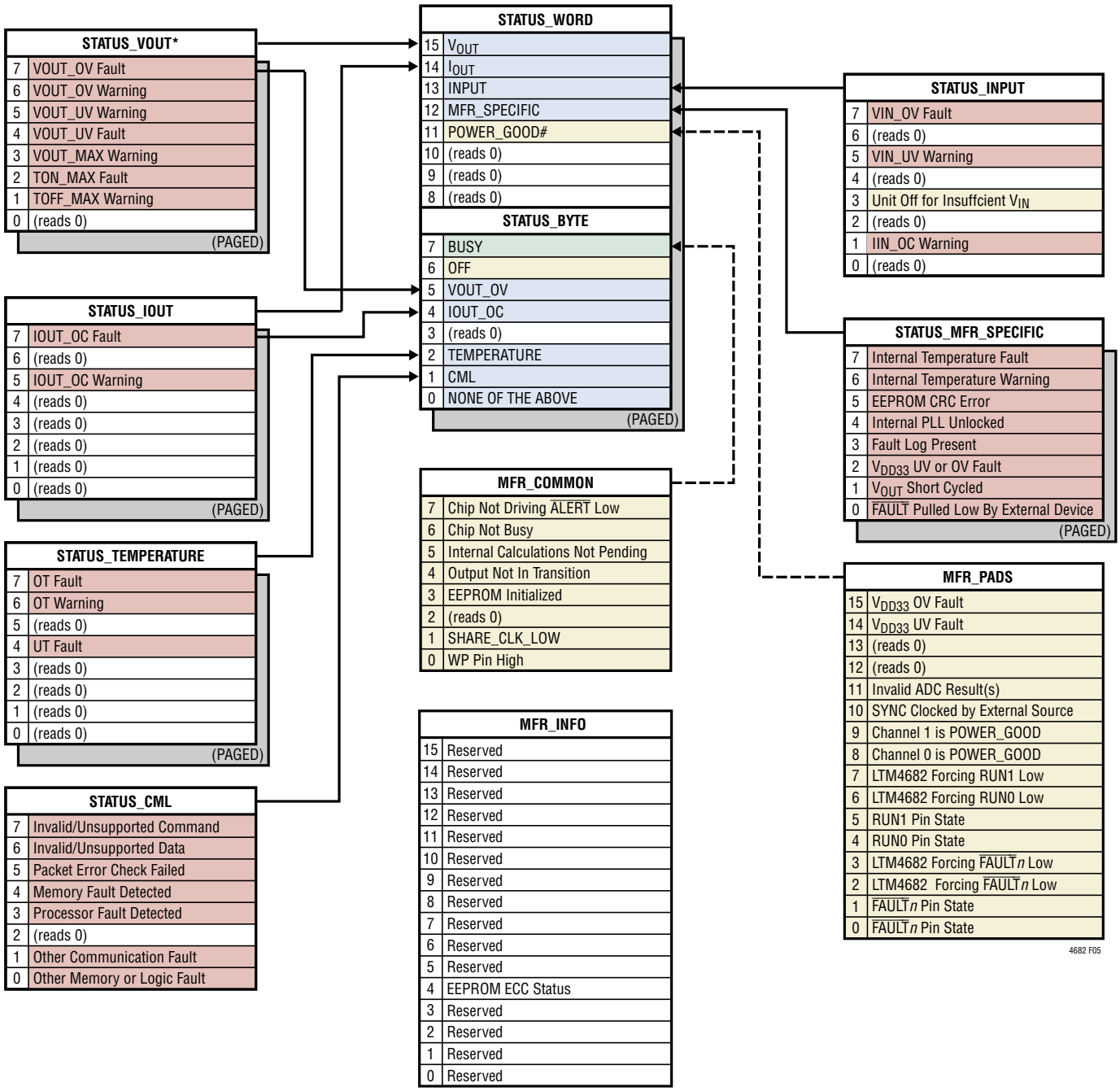

DESCRIPTION	MASKABLE	GENERATES ALERT	BIT CLEARABLE
General Fault or Warning Event	Yes	Yes	Yes
General Non-Maskable Event	No	Yes	Yes
Dynamic	No	No	No
Status Derived from Other Bits	No	Not Directly	No

Figure 5. LTM4682 Status Register Summary per Controller

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Mapping Faults to $\overline{\text{FAULT}}n$ Pins

Channel-to-channel fault (including channels from multiple LTM4682s) dependencies can be created by connecting $\overline{\text{FAULT}}n$ pins together. In the event of an internal fault, one or more of the channels is configured to pull the bussed $\overline{\text{FAULT}}n$ pins low. The other channels are then configured to shut down when the $\overline{\text{FAULT}}n$ pins are pulled low. For autonomous group retry, the faulted channel is configured to let go of the $\overline{\text{FAULT}}n$ pin(s) after a retry interval, assuming the original fault has cleared. All the channels in the group then begin a soft-start sequence. If the fault response is LATCH_OFF, the $\overline{\text{FAULT}}n$ pin remains asserted low until either the RUN*n* pin is toggled OFF/ON or the part is commanded OFF/ON. The toggling of the RUN*n* either by the pin or OFF/ON command will clear faults associated with the channel. If it is desired to have all faults cleared when either the RUN*n*, pin is toggled or, set bit 0 of MFR_CONFIG_ALL to a 1.

The status of all faults and warnings is summarized in the STATUS_WORD and STATUS_BYTE commands.

Additional fault detection and handling capabilities including power good pins and CRC protection.

Power Good Pins

The PGOOD*n* pins of the LTM4682 are connected to the open drains of internal MOSFETs. The MOSFETs turn on and pull the PGOOD*n* pins low when the channel output voltage is not within the channel's UV and OV voltage thresholds. During TON_DELAY and TON_RISE sequencing, the PGOOD*n* pin is held low. The PGOOD*n* pin is also pulled low when the respective RUN*n* pin is low. The PGOOD*n* pin response is deglitched by an internal 100µs digital filter. The PGOOD*n* pin and PGOOD status may be different at times due to communication latency of up to 10µs.

CRC Protection

The integrity of the NVM memory is checked after a power on reset. A CRC error will prevent the controller from leaving the inactive state. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the $\overline{\text{ALERT}}$_*nn* pin will be pulled low. NVM repair can be attempted by writing the desired configuration to the controller and executing a STORE_USER_ALL command followed by a CLEAR_FAULTS command.

The LTM4682 manufacturing section of the NVM is mirrored. If both copies are corrupted, the NVM CRC Fault in the STATUS_MFR_SPECIFIC command is set. If this bit remains set after being cleared by issuing a CLEAR_FAULTS or writing a 1 to this bit, an irrecoverable internal fault has occurred. The user is cautioned to disable both output power supply rails associated with this specific part. There are no provisions for field repair of NVM faults in the manufacturing section.

SERIAL INTERFACE

The LTM4682 serial interface is a PMBus-compliant subordinate device and can operate at any frequency between 10kHz and 400kHz. The address is configurable using either the NVM or an external resistor. In addition, the LTM4682 always responds to the global broadcast address of 0x5A (7-bit) or 0x5B (7-bit).

The serial interface supports the following protocols defined in the PMBus specifications: 1) send command, 2) write byte, 3) write word, 4) group, 5) read byte, 6) read word, 7) read block and 8) write block. All read operations will return a valid PEC if the PMBus main device requests it. If the PEC_REQUIRED bit is set in the MFR_CONFIG_ALL command, the PMBus write operations will not be acted upon until a valid PEC has been received by the LTM4682.

Communication Protection

PEC write errors (if PEC_REQUIRED is active), attempts to access unsupported commands, or writing invalid data to supported commands will result in a CML fault. The CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_CML command, and the $\overline{\text{ALERT}}$ pin is pulled low.

DEVICE ADDRESSING

The LTM4682 offers four different types of addressing over the PMBus interface, specifically: 1) global, 2) device, 3) rail addressing and 4) alert response address (ARA).

OPERATION

Global addressing provides a means for the PMBus main device to address all LTM4682 devices on the bus. The LTM4682 global address is fixed 0x5A (7-bit) or 0xB4 (8-bit) and cannot be disabled. Commands sent to the global address act the same as if PAGE is set to a value of 0xFF. Commands sent are written to both channels simultaneously. Global command 0x5B (7-bit) or 0xB6 (8-bit) is paged and allows channel-specific command of all LTM4682 devices on the bus. Other Analog Devices IC types may respond at one or both of these global addresses. Reading from global addresses is strongly discouraged.

Device addressing provides the standard means of the PMBus main device communicating with a single instance of an LTM4682. The value of the device address is set by a combination of the ASEL_*nn* configuration pin and the MFR_ADDRESS command. When this addressing means is used, the PAGE command determines the channel being acted upon. Device addressing can be disabled by writing a value of 0x80 to the MFR_ADDRESS.

Rail addressing provides a means for the bus main device to communicate simultaneously with all channels connected together to produce a single output voltage (PolyPhase). While similar to global addressing, the rail address can be dynamically assigned with the paged MFR_RAIL_ADDRESS command, allowing for any logical grouping of channels that might be required for reliable system control. Reading from rail addresses is also strongly discouraged.

All four means of PMBus addressing require the user to employ disciplined planning to avoid addressing conflicts. Communication to LTM4682 devices at global and rail addresses should be limited to command write operations.

RESPONSES TO V_{OUT} AND I_{IN}/I_{OUT} FAULTS

V_{OUT} OV and UV conditions are monitored by comparators. The OV and UV limits are set in the following three ways.

- As a Percentage of the V_{OUT} if Using the Resistor Configuration Pins
- In NVM, if Either Programmed at the Factory or Through the GUI
- By PMBus Command

The I_{IN} and I_{OUT} overcurrent monitors are performed by ADC readings and calculations. Thus, these values are based on average currents and can have a time latency of up to $t_{CONVERT}$. The I_{OUT} calculation accounts for the DCR and their temperature coefficient. The input current equals to the voltage measured across the $R_{SENSE}n$ resistor divided by the resistor value as set with the MFR_IIN_CAL_GAIN command. If this calculated input current exceeds the IN_OC_WARN_LIMIT, the $\overline{\text{ALERT}}$_*nn* pin is pulled low, and the IIN_OC_WARN bit is asserted in the STATUS_INPUT command.

The digital processor within the LTM4682 provides the ability to ignore the fault, shut down and latch off or shut down and retry indefinitely (hiccup). The retry interval is set in MFR_RETRY_DELAY and can be from 120ms to 83.88 seconds in 10µs increments. The shutdown for OV/UV and OC can be done immediately or after a user-selectable deglitch time.

Output Overvoltage Fault Response

A programmable overvoltage comparator (OV) guards against transient overshoots and long-term overvoltages at the output. In such cases, the top MOSFET is turned off, and the bottom MOSFET is turned on. However, the reverse output current is monitored while the device is in OV fault. When it reaches the limit, both top and bottom MOSFETs are turned off. The top and bottom MOSFETs will keep their state until the overvoltage condition is cleared, regardless of the PMBus VOUT_OV_FAULT_RESPONSE command byte value. This hardware-level fault response delay is typically 2µs from the overvoltage condition to BG asserted high. Using the VOUT_OV_FAULT_RESPONSE command, the user can select any of the following behaviors.

- OV Pull-Down Only (OV Cannot Be Ignored)
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

Either the Latch Off or Retry fault responses can be deglitched in increments of (0-7) • 10µs. See Table 17.

OPERATION

Output Undervoltage Response

The response to an undervoltage comparator output can be the following:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

The UV responses can be deglitched. See Table 18.

Peak Output Overcurrent Fault Response

Due to the current mode control algorithm, peak output current across the inductor is always limited on a cycle-by-cycle basis. The value of the peak current limit is specified in the Electrical Characteristics table. The current limit circuit operates by limiting the COMP*n* maximum voltage. Since internal DCR sensing is used, the COMP*n* maximum voltage has a temperature dependency directly proportional to the TC of the DCR of the inductor. The LTM4682 automatically monitors the external temperature sensors and modifies the maximum allowed COMP*n* to compensate for this term. The IOUT_OC_FAULT_LIMIT section provides data points for I_{OUT} Limiting, see IOUT_OC_FAULT_LIMIT.

The overcurrent fault processing circuitry can execute the following behaviors.

- Current Limit Indefinitely
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

The overcurrent responses can be deglitched in increments of (0-7) • 16ms. See Table 19.

RESPONSES TO TIMING FAULTS

TON_MAX_FAULT_LIMIT is the time allowed for V_{OUT} to rise and settle at start-up. The TON_MAX_FAULT_LIMIT condition is predicated upon detecting the VOUT_UV_FAULT_LIMIT as the output is undergoing a SOFT_START sequence. The TON_MAX_FAULT_LIMIT time is started after TON_DELAY has been reached and a SOFT_START sequence is started. The resolution of the TON_MAX_FAULT_LIMIT is 10µs. If the VOUT_UV_FAULT_LIMIT is not reached within the TON_MAX_FAULT_LIMIT time, the response of this fault is determined by the value of the TON_MAX_FAULT_RESPONSE command value. This response may be one of the following.

- Ignore
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

This fault response is not deglitched. A value of 0 in TON_MAX_FAULT_LIMIT means the fault is ignored. The TON_MAX_FAULT_LIMIT should be set longer than the TON_RISE time. It is recommended that TON_MAX_FAULT_LIMIT always be set to a non-zero value, otherwise the output may never come up, and no flag will be set to the user. See Table 21.

RESPONSES TO V_{IN} OV FAULTS

V_{IN} overvoltage is measured with the ADC. The response is naturally deglitched by the 100ms typical response time of the ADC. The fault responses include the following.

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY. See Table 21.

RESPONSES TO OT/UT FAULTS

Internal Overtemperature Fault Response

An internal temperature sensor protects against NVM damage. Above 85°C, no writes to NVM are recommended. Above 130°C, the internal overtemperature warns threshold is exceeded and the part disables the NVM, and does not re-enable until the temperature has dropped to 125°C. When the die temperature exceeds 160°C, the internal temperature fault response is enabled, and the PWM is disabled until the die temperature drops below 150°C. Temperature is measured by the ADC. Internal temperature faults cannot be ignored. Internal temperature limits cannot be adjusted by the user. See Table 20.

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Overtemperature and Undertemperature Fault Response

Four internal temperature sensors are used to sense the temperature of critical circuit elements like inductors and power MOSFETs on each channel. The OT_FAULT_RESPONSE and UT_FAULT_RESPONSE commands are used to determine the appropriate response to an overtemperature and under temperature conditions, respectively. If no external sense elements are used (not recommended), set the UT_FAULT_RESPONSE to ignore—and set the UT_FAULT_LIMIT to 275°C. The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time

Interval Specified in MFR_RETRY_DELAY. See Table 21.

RESPONSES TO INPUT OVERCURRENT AND OUTPUT UNDERCURRENT FAULTS

Input overcurrent and output undercurrent are measured with the ADC. The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

RESPONSES TO EXTERNAL FAULTS

When either $\overline{\text{FAULT}}n$ pin is pulled low, the OTHER bit is set in the STATUS_WORD command, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the $\overline{\text{ALERT}}$_*nn* pin is pulled low. Responses are not deglitched. Each channel can be configured to ignore or shut down then retry in response to its $\overline{\text{FAULT}}n$ pin going low by modifying the MFR_FAULT_RESPONSE command. To avoid the $\overline{\text{ALERT}}$_*nn* pin asserting low when $\overline{\text{FAULT}}n$ is pulled low, assert bit 1 of MFR_CHAN_CONFIG, or mask the ALERT using the SMBALERT_MASK command.

FAULT LOGGING

The LTM4682 has the fault logging capability. Data is logged into memory in the order shown in Table 23. The data is stored in a continuously updated buffer in RAM. When a fault event occurs, the fault log buffer is copied from the RAM buffer into the NVM. Fault logging is allowed at temperatures above 85°C; however, retention of 10 years is not guaranteed. When the die temperature exceeds 130°C, the fault logging is delayed until the die temperature drops below 125°C. The fault log data remains in NVM until a MFR_FAULT_LOG_CLEAR command is issued. Issuing this command re-enables the fault log feature. Before re-enabling the fault log, be sure no faults are present, and a CLEAR_FAULTS command has been issued.

When the LTM4682 powers-up or exits its reset state, it checks the NVM for a valid fault log. If a valid fault log exists in NVM, the Valid Fault Log bit in the STATUS_MFR_SPECIFIC command will be set, and an $\overline{\text{ALERT}}$ event will be generated. Also, fault logging will be blocked until the LTM4682 has received a MFR_FAULT_LOG_CLEAR command before fault logging will be re-enabled.

The information is stored in EEPROM in the event of any fault that disables the controller on either channel. A $\overline{\text{FAULT}}n$ being externally pulled low will not trigger a fault logging event.

BUS TIMEOUT PROTECTION

The LTM4682 implements a timeout feature to avoid persistent faults on the serial interface. The data packet timer begins at the first START event before the device address write byte. Data packet information must be completed within 30ms, or the LTM4682 will three-state the bus and ignore the given data packet. If more time is required, assert bit 3 of MFR_CONFIG_ALL to allow typical bus timeouts of 255ms. Data packet information includes the device address byte write, command byte, repeat start event (if a read operation), device address byte read (if a read operation), all data bytes and the PEC byte if applicable.

The LTM4682 allows longer PMBus timeouts for block-read data packets. This timeout is proportional to the length of the block read. The additional block read timeout

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applies primarily to the MFR_FAULT_LOG command. The timeout period defaults to 32ms.

The user is encouraged to use as high a clock rate as possible to maintain efficient data packet transfer between all devices sharing the serial bus interface. The LTM4682 supports the full PMBus frequency range from 10kHz to 400kHz.

SIMILARITY BETWEEN PMBus, SMBus AND I²C 2-WIRE INTERFACE

The PMBus 2-wire interface is an incremental extension of the SMBus. The SMBus is built upon I²C with some minor differences in timing, DC parameters, and protocol. The PMBus/SMBus protocols are more robust than simple I²C byte commands because PMBus/SMBus provide timeouts to prevent persistent bus errors and optional packet error checking (PEC) to ensure data integrity. In general, a main device that can be configured for I²C communication can be used for PMBus communication with little or no change to hardware or firmware. Repeat start (restart) is not supported by all I²C controllers but is required for SMBus/PMBus reads. If a general-purpose I²C controller is used, check that repeat start is supported.

The LTM4682 supports the maximum SMBus clock speed of 100kHz and is compatible with the higher speed PMBus specification (between 100kHz and 400kHz) if MFR_COMMON polling or clock stretching is enabled. For robust communication and operation see the Note section in the PMBus Command Summary section. Clock stretching is enabled by asserting bit 1 of MFR_CONFIG_ALL.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.2: Paragraph 5: Transport. To describe the differences between SMBus and I²C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B—Differences Between SMBus and I²C.

PMBus SERIAL DIGITAL INTERFACE

The LTM4682 communicates with a host (main device) using the standard PMBus serial bus interface. The PMBus Timing Diagram, Figure 6, shows the timing relationship of the signals on the bus. The two-bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines. The LTM4682 is a subordinate device. The main device can communicate with the LTM4682 using the following formats.

- Main Transmitter, Subordinate Receiver
- Main Receiver, Subordinate Transmitter

The following PMBus protocols are supported.

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read, Block Write
- Alert Response Address

Figure 7 to Figure 24 illustrate the aforementioned PMBus protocols. All transactions support PEC and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the PMBus timeout may be extended when reading the fault log.

Figure 7 is the key to the protocol diagrams in this section. PEC is optional. A value shown below a field in Figure 7 to Figure 24 is a mandatory value for that field.

The data formats implemented by PMBus are:

- Main transmitter transmits to an subordinate receiver. The transfer direction, in this case, has not been changed.
- Main device reads the subordinate immediately after the first byte. At the moment of the first acknowledgement (provided by the subordinate receiver), the main transmitter becomes a main receiver, and the subordinate receiver becomes the subordinate transmitter.
- Combined format. During a change of direction within a transfer, the main device repeats both a start condition and the subordinate address but with the R/W bit reversed. In this case, the main receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

See Figure 7 for a legend.

Handshaking features are included to ensure robust system communication. See the PMBus Communication and Command Processing subsection of the Applications Information section for further details.

OPERATION

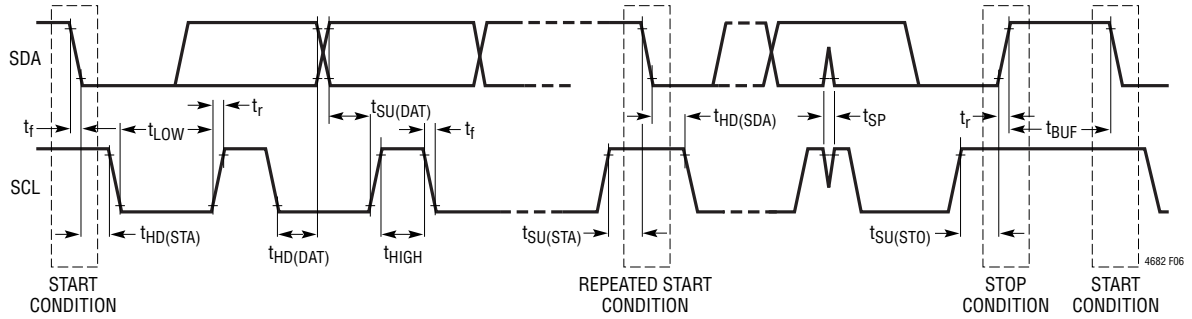

Figure 6. PMBus Timing Diagram

Table 6. Abbreviations of Supported Data Formats

	PMBus		ADI		
	TERMINOLOGY	**SPECIFICATION REFERENCE**	**TERMINOLOGY**	**DEFINITION**	**EXAMPLE**
L11	Linear	Part II ¶7.1	Linear_5s_11s	Floating point 16-bit data: value = Y • 2^N, where N = b[15:11] and Y = b[10:0], both two's compliment binary integers.	b[15:0] = 0x9807 = 10011_000_0000_0111 value = 7 • 2^{-13} = 854E^{-6}
L16	Linear VOUT_MODE	Part II ¶8.2	Linear_16u	Floating point 16-bit data: value = Y • 2^{-12}, where Y = b[15:0], an unsigned integer.	b[15:0] = 0x4C00 = 0100_1100_0000_0000 value = 19456 • 2^{-12} = 4.75
CF	DIRECT	Part II ¶7.2	Varies	16-bit data with a custom format defined in the PMBus Command Details section.	Often an unsigned or two's compliment integer.
Reg	Register Bits	Part II ¶10.3	Reg	Per-bit meaning defined in the PMBus Command Details section.	PMBus STATUS_BYTE command.
ASC	Text Characters	Part II ¶22.2.1	ASCII	ISO/IEC 8859-1 [A05]	LTC (0x4C5443)

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FIGURE 7 TO FIGURE 24 PMBus PROTOCOLS

S START CONDITION
Sr REPEATED START CONDITION
Rd READ (BIT VALUE OF 1)
Wr WRITE (BIT VALUE OF 0)
A ACKNOWLEDGE (THIS BIT POSITION MAY BE 0 FOR AN ACK OR 1 FOR A NACK)
P STOP CONDITION
PEC PACKET ERROR CODE
MAIN TO SUBORDINATE
SUBORDINATE TO MAIN
... CONTINUATION OF PROTOCOL

4682 F07

Figure 7. PMBus Packet Protocol Diagram Element Key

Figure 8. Quick Command Protocol

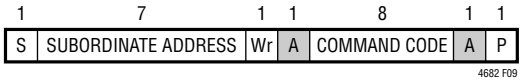

Figure 9. Send Byte Protocol

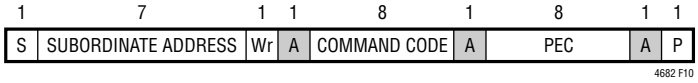

Figure 10. Send Byte Protocol with PEC

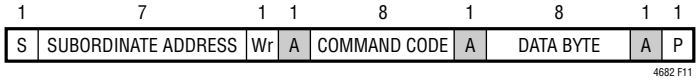

Figure 11. Write Byte Protocol

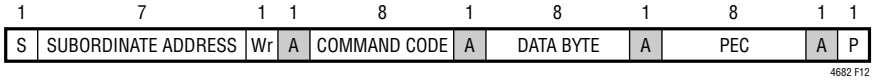

Figure 12. Write Byte Protocol with PEC

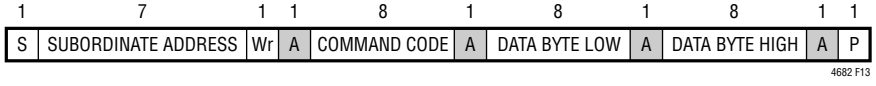

Figure 13. Write Word Protocol

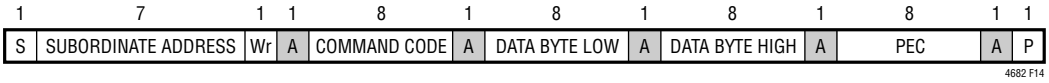

Figure 14. Write Word Protocol with PEC

OPERATION

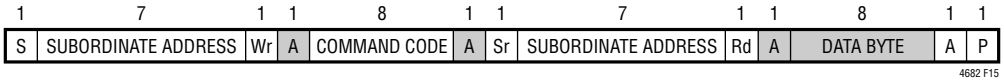

Figure 15. Read Byte Protocol

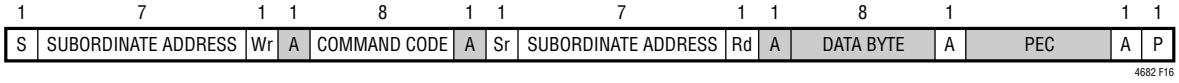

Figure 16. Read Byte Protocol with PEC

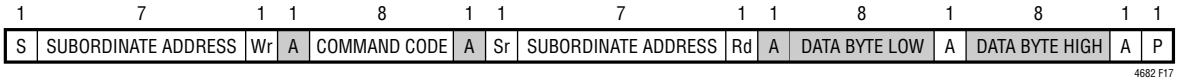

Figure 17. Read Word Protocol

Figure 18. Read Word Protocol with PEC

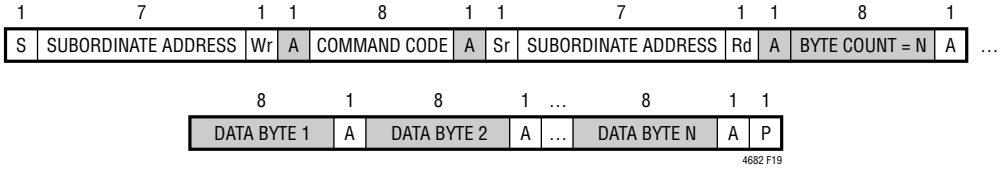

Figure 19. Block Read Protocol

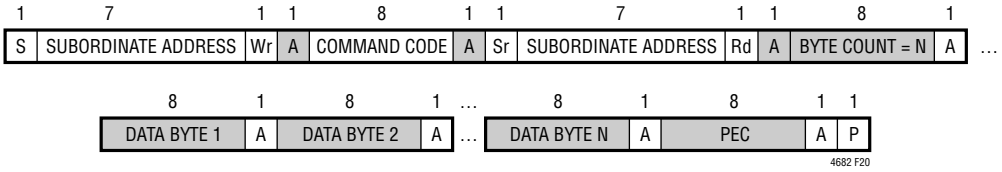

Figure 20. Block Read Protocol with PEC

OPERATION

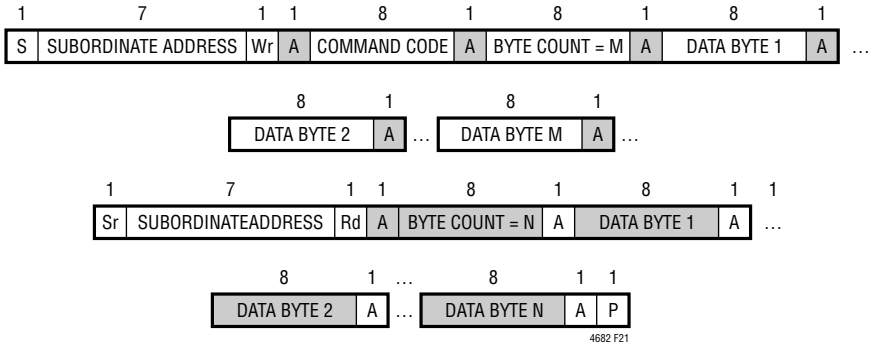

Figure 21. Block Write – Block Read Process Call

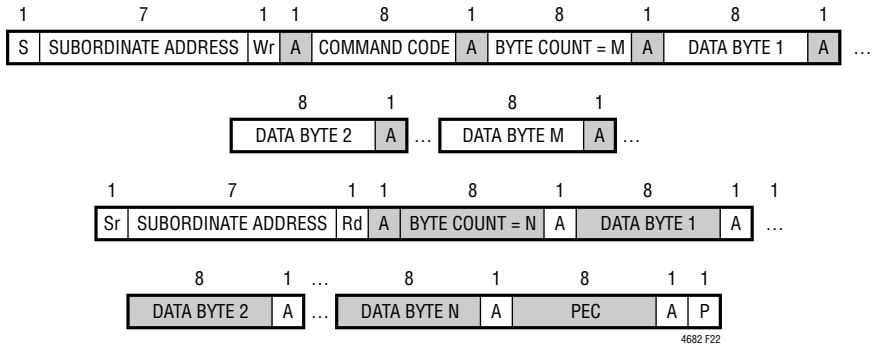

Figure 22. Block Write – Block Read Process Call with PEC

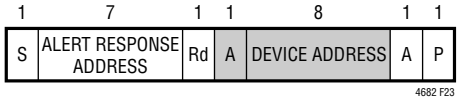

Figure 23. Alert Response Address Protocol

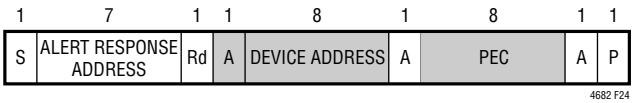

Figure 24. Alert Response Address Protocol with PEC

PMBus COMMAND SUMMARY

PMBus COMMANDS

Table 7 lists supported PMBus commands and manufacturer-specific commands. A complete description of these commands can be found in the PMBus Power System Management Protocol Specification – Part II – Revision 1.2. Users are encouraged to reference this specification. Exceptions or manufacturer-specific implementations are listed in Table 7. Floating point values listed in the DEFAULT VALUE column are either Linear 16-bit Signed (PMBus Section 8.3.1) or Linear_5s_11s (PMBus Section 7.1) format, whichever is appropriate for the command. All commands from 0xD0 through 0xFF not listed in Table 7 are implicitly reserved by the manufacturer. Users should avoid blind writes within this range of commands to avoid the undesired operation of the part. All commands from 0x00 through 0xCF not listed in Table 7 are implicitly not supported by the manufacturer. Attempting to access non-supported or reserved commands may result in a CML command fault event. All output voltage settings and measurements are based on the VOUT_MODE setting of 0x14. This translates to an exponent of 2^{-12}.

If PMBus commands are received faster than they are being processed, the part may become too busy to handle new commands. In these circumstances, the part follows the protocols defined in the PMBus Specification v1.2, Part II, Section 10.8.7, to communicate that it is busy. The part includes handshaking features to eliminate busy errors and simplify error-handling software while ensuring robust communication and system behavior. See the subsection titled PMBus Communication and Command Processing in the Applications Information section for further details.

Table 7. PMBus Commands Summary (Note: The Data Format Abbreviations Are Detailed in Table 8)

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
PAGE	0x00	Provides integration with multi-page PMBus devices.	R/W Byte	N	Reg			0x00	81
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x80	85
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E	85
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				NA	110
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	W Block	N					81
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Block R/W	N					81
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	82
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				NA	120
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				NA	120
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	109
SMBALERT_MASK	0x1B	Mask $\overline{\text{ALERT}}$ activity.	Block R/W	Y	Reg		Y	See CMD	110
VOUT_MODE	0x20	Output voltage format and exponent (2^{-12}).	R Byte	Y	Reg			2^{-12} 0x14	91
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	L16	V	Y	0.75 0x0C00	92
VOUT_MAX	0x24	The upper limit on the commanded output voltage, including VOUT_MARGIN_HI.	R/W Word	Y	L16	V	Y	1.5 0x1800	91

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point. It must be greater than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.80 0x0CCD	92
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point. It must be less than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.70 0x0B33	92
VOUT_TRANSITION_RATE	0x27	Rate the output changes when V_{OUT} is commanded to a new value.	R/W Word	Y	L11	V/ms	Y	0.25 0xD010	98
FREQUENCY_SWITCH	0x33	Switching frequency of the controller.	R/W Word	N	L11	kHz	Y	575kHz 0x023F	89
VIN_ON (SVIN_XX)	0x35	Input voltage at which the unit should start power conversion.	R/W Word	N	L11	V	Y	4.75 0xD130	90
VIN_OFF (SVIN_XX)	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	N	L11	V	Y	4.5 0xD120	90
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	0.85 0x0D9A	91
VOUT_OV_FAULT_RESPONSE	0x41	Action is to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8	100
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	0.825 0xD33	91
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.675 0x0ACD	92
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	L16	V	Y	0.65 0x0A66	92
VOUT_UV_FAULT_RESPONSE	0x45	Action is to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8	101
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	42.00 0xE2A0	94
IOUT_OC_FAULT_RESPONSE	0x47	Action is to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	103
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	35.0 0xE918	95
OT_FAULT_LIMIT	0x4F	External overtemperature fault limit.	R/W Word	Y	L11	C	Y	128.0 0xF200	96
OT_FAULT_RESPONSE	0x50	Action is to be taken by the device when an external overtemperature fault is detected.	R/W Byte	Y	Reg		Y	0xB8	105
OT_WARN_LIMIT	0x51	External overtemperature warning limit.	R/W Word	Y	L11	C	Y	125.0 0xEBE8	96
UT_FAULT_LIMIT	0x53	External undertemperature fault limit.	R/W Word	Y	L11	C	Y	–45.0 0xE530	97
UT_FAULT_RESPONSE	0x54	Action is to be taken by the device when an external undertemperature fault is detected.	R/W Byte	Y	Reg		Y	0xB8	105
VIN_OV_FAULT_LIMIT	0x55	Input supply overvoltage fault limit.	R/W Word	N	L11	V	Y	16.8 0xDA1A	89
VIN_OV_FAULT_RESPONSE	0x56	Action is to be taken by the device when an input overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	100
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	N	L11	V	Y	4.65 0xD12A	90
IIN_OC_WARN_LIMIT	0x5D	Input supply overcurrent warning limit.	R/W Word	N	L11	A	Y	10.0 0xD280	95

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	L11	ms	Y	0.0 0x8000	97
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the V_{OUT} commanded value.	R/W Word	Y	L11	ms	Y	3.0 0xC300	97
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for V_{OUT} to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	L11	ms	Y	5.0 0xCA80	98
TON_MAX_FAULT_ RESPONSE	0x63	Action is to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	103
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	L11	ms	Y	0.0 0x8000	98
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	L11	ms	Y	3.0 0xC300	98
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL is completed, for the unit to decay below 12.5%.	R/W Word	Y	L11	ms	Y	0 0x8000	99
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			NA	111
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			NA	112
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			NA	112
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			NA	113
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg			NA	113
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMERATURE_1.	R/W Byte	Y	Reg			NA	114
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			NA	114
STATUS_MFR_SPECIFIC	0x80	Manufacturer-specific fault and state information.	R/W Byte	Y	Reg			NA	115
READ_VIN	0x88	Measured input supply voltage.	R Word	N	L11	V		NA	117
READ_IIN	0x89	Measured input supply current.	R Word	N	L11	A		NA	117
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	L16	V		NA	117
READ_IOUT	0x8C	Measured output current.	R Word	Y	L11	A		NA	117
READ_TEMPERATURE_1	0x8D	External temperature sensor temperature. This is the value used for all temperature-related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	C		NA	117
READ_TEMPERATURE_2	0x8E	Internal die junction temperature. Does not affect any other commands.	R Word	N	L11	C		NA	117
READ_FREQUENCY	0x95	Measured PWM switching frequency.	R Word	Y	L11	Hz		NA	117
READ_POUT	0x96	Measured output power	R Word	Y	L11	W		N/A	117
READ_PIN	0x97	Calculated input power	R Word	Y	L11	W		N/A	118
PMBus_REVISION	0x98	PMBus revision is supported by this device. The current revision is 1.2.	R Byte	N	Reg			0x22	109
MFR_ID	0x99	The manufacturer ID of the LTM4682 in ASCII.	R String	N	ASC			LTC	109
MFR_MODEL	0x9A	Manufacturer part number is in ASCII.	R String	N	ASC				109

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
MFR_VOUT_MAX	0xA5	Maximum allowed output voltage including VOUT_OV_FAULT_LIMIT.	R Word	Y	L16	V		1.5 0x1800	93
MFR_PIN_ACCURACY	0xAC	Returns the accuracy of the READ_PIN command.	R Byte	N	%			5.0%	118
USER_DATA_00	0xB0	OEM RESERVED. Typically used for part serialization.	R/W Word	N	Reg		Y	NA	109
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	109
USER_DATA_02	0xB2	OEM RESERVED. Typically used for part serialization	R/W Word	N	Reg		Y	NA	109
USER_DATA_03	0xB3	An NVM word is available for the user.	R/W Word	Y	Reg		Y	0x0000	109
USER_DATA_04	0xB4	An NVM word is available for the user.	R/W Word	N	Reg		Y	0x0000	109
MFR_EE_UNLOCK	0xBD	Contact factory.							125
MFR_EE_ERASE	0xBE	Contact factory.							125
MFR_EE_DATA	0xBF	Contact factory.							125
MFR_CHAN_CONFIG	0xD0	Configuration bits that are channel-specific.	R/W Byte	Y	Reg		Y	0x1D	83
MFR_CONFIG_ALL	0xD1	General configuration bits.	R/W Byte	N	Reg		Y	0x21	84
MFR_FAULT_PROPAGATE	0xD2	Configuration that determines which faults are propagated to the $\overline{\text{FAULT}}$ pin.	R/W Word	Y	Reg		Y	0x6993	106
MFR_PWM_COMP	0xD3	PWM loop compensation configuration	R/W Byte	Y	Reg		Y	0x76	87
MFR_PWM_MODE	0xD4	Configuration for the PWM engine.	R/W Byte	Y	Reg		Y	0xC7	86
MFR_FAULT_RESPONSE	0xD5	Action is to be taken by the device when the $\overline{\text{FAULT}}$ pin is externally asserted low.	R/W Byte	Y	Reg		Y	0xC0	108
MFR_OT_FAULT_RESPONSE	0xD6	Action is to be taken by the device when an internal overtemperature fault is detected.	R Byte	N	Reg			0xC0	104
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since the last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		NA	118
MFR_ADC_CONTROL	0xD8	ADC telemetry parameter selected for repeated fast ADC read back.	R/W Byte	N	Reg			0x00	119
MFR_RETRY_DELAY	0xDB	Retry interval during $\overline{\text{FAULT}}$ retry mode.	R/W Word	Y	L11	ms	Y	250.0 0xF3E8	99
MFR_RESTART_DELAY	0xDC	The minimum time the RUN pin is held low by the LTM4682.	R/W Word	Y	L11	ms	Y	150.0 0xF258	99
MFR_VOUT_PEAK	0xDD	The maximum measured value of READ_VOUT since the last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		NA	118
MFR_VIN_PEAK	0xDE	The maximum measured value of READ_VIN since the last MFR_CLEAR_PEAKS.	R Word	N	L11	V		NA	118
MFR_TEMPERATURE_1_PEAK	0xDF	The maximum measured value of external Temperature (READ_TEMPERATURE_1) since the last MFR_CLEAR_PEAKS.	R Word	Y	L11	C		NA	118
MFR_READ_IIN_PEAK	0xE1	The maximum measured value of READ_IIN command since the last MFR_CLEAR_PEAKS.	R Word	N	L11	A		NA	118
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	N				NA	111
MFR_READ_ICHIP	0xE4	Measured supply current of the SV_{IN} pin.	R Word	N	L11	A		NA	119
MFR_PADS	0xE5	Digital status of the I/O pads.	R Word	N	Reg			NA	115

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte, Ch 0 and 1.	R/W Byte	N	Reg		Y	0x4F	83
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte, Ch 2 and 3.	R/W Byte	N	Reg		Y	0x4E	83
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTM4682 and revision.	R Word	N	Reg			0x418X	109
MFR_IIN_CAL_GAIN	0xE8	The resistance value of the input current sense element in mΩ.	R/W Word	N	L11	mΩ	Y	2.0 0xC200	95
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	121
MFR_INFO	0x	Contact factory.							125
MFR_IOUT_CAL_GAIN	0xDA	SET AT FACTORY. Typical 0.36mΩ.	R Word	Y	L11	mΩ		0.360 Typical 0xD017	93
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging.	Send Byte	N				NA	125
MFR_FAULT_LOG	0xEE	Fault log data bytes.	R Block	N	Reg		Y	NA	121
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA	116
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with NVM.	Send Byte	N				NA	120
MFR_TEMPERATURE_2_PEAK	0xF4	Peak internal die temperature since the last MFR_CLEAR_PEAKS.	R Word	N	L11	C		NA	119
MFR_PWM_CONFIG	0xF5	Set numerous parameters for the DC/DC controller, including phasing.	R/W Byte	N	Reg		Y	0x10	88
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient of the current sensing element.	R/W Word	Y	CF	ppm/°C	Y	3900 0x0F3C	93
MFR_RVIN_CAL_GAIN	0xF7	The resistance value of the V_{IN} pin filter element in mΩ.	R/W Word	N	L11	mΩ	Y	1000 0x03E8	90
MFR_TEMP_1_GAIN	0xF8	Sets the slope of the external temperature sensor.	R/W Word	Y	CF		Y	0.995 0x3FAE	96
MFR_TEMP_1_OFFSET	0xF9	Sets the offset of the external temperature sensor with respect to –273.1°C	R/W Word	Y	L11	C	Y	0.0 0x8000	96
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80	83
MFR_REAL_TIME	0xFB	48-bit share-clock counter value.	R Block	N	CF			NA	122
MFR_RESET	0xFD	Commanded reset without requiring a power down.	Send Byte	N				NA	85

Note 1: Commands indicated with Y in the NVM column indicate that these commands are stored and restored using the STORE_USER_ALL and RESTORE_USER_ALL commands, respectively.

Note 2: Commands with a default value of NA indicate not applicable. Commands with a default value of FS indicate factory set on a per part basis.

Note 3: The LTM4682 contains additional commands not listed in Table 7. Reading these commands is harmless to the operation of the IC; however, the contents and meaning of these commands can change without notice.

Note 4: Some of the unpublished commands are read-only and will generate a CML bit 6 fault if written.

Note 5: Writing to commands not published in Table 7 is not permitted.

Note 6: The user should not assume compatibility of commands between different parts based upon command names. Always refer to the manufacturer's data sheet for each part for a complete definition of a command's function. Analog Devices strives to keep command functionality compatible between all Analog Devices devices. Differences may occur to address specific product requirements.

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Table 8. Data Format Abbreviations

L11	Linear_5s_11s	PMBus data field b[15:0] Value = $Y \cdot 2^N$ where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer. Example: For b[15:0] = 0x9807 = 'b10011_000_0000_0111 Value = $7 \cdot 2^{-13} = 854 \cdot 10^{-6}$ From PMBus Spec Part II: Paragraph 7.1
L16	Linear_16u	PMBus data field b[15:0] Value = $Y \cdot 2^N$ where Y = b[15:0] is an unsigned integer and N = VOUT_MODE_PARAMETER is a 5-bit two's complement exponent that is hardwired to –12 decimal Example: For b[15:0] = 0x4C00 = 'b0100_1100_0000_0000 Value = $19456 \cdot 2^{-12} = 4.75$ From PMBus Spec Part II: Paragraph 8.2
Reg	Register	PMBus data field b[15:0] or b[7:0]. Bit field meaning is defined in the PMBus Command Details section.
L16	Integer Word	PMBus data field b[15:0] Value = Y where Y = b[15:0] is a 16-bit unsigned integer Example: For b[15:0] = 0x9807 = 'b1001_1000_0000_0111 Value = 38919 (decimal)
CF	Custom Format	Value is defined in the PMBus Command Details section. This is often an unsigned or two's complement integer scaled by an MFR specific constant.
ASC	ASCII Format	A variable length string of text characters conforming to ISO/IEC 8859-1 standard.

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V_{IN} TO V_{OUT} STEP-DOWN RATIOS

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage. Each output of the LTM4682 is capable of the 95% duty cycle at 500kHz, but the V_{IN} to V_{OUT} minimum dropout is still a function of its load current and will limit output current capability related to the high duty cycle on the topside switch.

Minimum on-time $t_{ON(MIN)}$ is another consideration in operating at a specified duty cycle while operating at a certain frequency due to the fact that $t_{ON(MIN)} < D/f_{SW}$, where D is the duty cycle and f_{SW} is the switching frequency. $t_{ON(MIN)}$ is specified in the electrical parameters as 85ns. See Note 6 in the Electrical Characteristics section for output current guidelines.

INPUT CAPACITORS

The LTM4682 module should be connected to a low AC impedance DC source. For the regulator input, four 22µF input ceramic capacitors are used to handle the RMS ripple current. A 47µF to 150µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated as:

$$D_n = \frac{V_{OUTn}}{V_{INn}}$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CINn(RMS)} = \frac{I_{OUTn(MAX)}}{\eta\%} \bullet \sqrt{D_n \bullet (1-D_n)}$$

In the above equation, $\eta\%$ is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor, or a polymer capacitor. Application Note 77 can be utilized to help calculate ripple current cancellation for multiphase applications.

OUTPUT CAPACITORS

The LTM4682 is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. The C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer or a ceramic capacitor. The typical output capacitance range for each output is from 400µF to 1000µF. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spikes is required. Table 13 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 10A to 20A step, with 10A/µs transient on each channel. Table 13 optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 13 matrix, and the LTpowerCAD design tool will be provided for stability analysis. Multiphase operation reduces effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The LTpowerCAD design tool can calculate the output ripple reduction as the number of implemented phases increases by N times. A small value 10Ω resistor can be placed in series from V_{OUTn} to the V_{OSNS0}^+ pin to allow for a bode plot analyzer to inject a signal into the control loop and validate the regulator stability. The LTM4682's stability compensation can be adjusted using two external capacitors (COMP*n*a, COMP*n*b), and the MFR_PWM_COMP commands.

LIGHT LOAD CURRENT OPERATION

The LTM4682 has two modes of operation including high efficiency, discontinuous conduction mode or forced continuous conduction mode. The mode of operation is configured by bit 0 of the MFR_PWM_MODE*n* command (discontinuous conduction is always the start-up mode, forced continuous is the default running mode).

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If a channel is enabled for discontinuous mode operation, the inductor current is not allowed to reverse. The reverse current comparator, I_{REV}, turns off the bottom MOSFET (MB*n*) just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller can operate in discontinuous (pulse-skipping) operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined solely by the voltage on the COMP*n* pin. In this mode, the efficiency at light loads is lower than in discontinuous mode operation. However, continuous mode exhibits lower output ripple and less interference with audio circuitry. Forced continuous conduction mode may result in reverse inductor current, which can cause the input supply to boost. The VIN_OV_FAULT_LIMIT can detect this (if SV_{IN_nn} is connected to V_{IN01} and/or V_{IN23}) and turn off the offending channel. However, this fault is based on an ADC read and can nominally take up to 100ms to detect. If there is a concern about the input supply boosting, keep the part in discontinuous conduction operation.

SWITCHING FREQUENCY AND PHASE

The switching frequency of the LTM4682's channels is established by its analog phase-locked-loop (PLL) locking on to the clock present at the module's SYNC_*nn* pin. The clock waveform on the SYNC_*nn* pin can be generated by the LTM4682's internal circuitry when an external pull-up resistor to 3.3V (e.g., V_{DD33}) is provided, in combination with the LTM4682 control IC's FREQUENCY_SWITCH command being set to one of the following supported values: 250kHz, 350kHz, 425kHz, 500kHz, 575kHz, 650kHz, and 750kHz. In this configuration, the module is called a sync main device: (using the factory-default setting of MFR_CONFIG_ALL[4] = 0b), SYNC_*nn* becomes a bidirectional open-drain pin, and the LTM4682 pulls SYNC logic low for nominally 500ns at a time, at the prescribed clock rate. The SYNC signal can be bused to other LTM4682 modules (configured as sync subordinates), for purposes of synchronizing switching frequencies of multiple modules within a system—but only one LTM4682 internal controllers should be configured as a sync main device the other LTM4682(s) should be configured as sync subordinates.

The most straightforward way is to set its FREQUENCY_SWITCH command to 0x0000 and MFR_CONFIG_ALL[4] = 1b. This can be easily implemented with resistor pin-strap settings on the FSWPH_*nn*_CFG pin (see Table 3). Using the MFR_CONFIG_ALL[4] = 1b, the LTM4682s SYNC pin becomes a high impedance input only—i.e., it does not drive SYNC low. The module synchronizes its frequency to the clock applied to its SYNC pin. The only shortcoming of this approach is without an externally applied clock, the switching frequency of the module will default to the low end of its frequency-synchronization capture range (~225kHz).

If fault-tolerance to the loss of an externally applied SYNC clock is desired, the FREQUENCY_SWITCH command of a sync subordinate can be left at the nominal target switching frequency of the application and not 0x0000 However, it is still necessary to configure MFR_CONFIG_ALL[4] = 1b. With this combination of configurations, the LTM4682's SYNC_*nn* pins becomes a high impedance input and the module synchronizes its frequency to that of the externally applied clock, provided that the frequency of the externally applied clock exceeds ~½. of the target frequency (FREQUENCY_SWITCH). If the SYNC clock is absent, the module responds by operating at its target frequency, indefinitely. If and when the SYNC clock is restored, the module automatically phase-locks to the SYNC clock as normal. The only shortcoming of this approach is that the EEPROM must be configured per above guidance; resistor pin-strapping options on the FSWPH_*nn*_CFG pin alone cannot provide fault-tolerance to the absence of the SYNC clock.

The FREQUENCY_SWITCH register can be altered through I^2C commands, but only when the switching action is disengaged, i.e., the module's outputs are turned off. The FREQUENCY_SWITCH command takes on the value stored in NVM at SV_{IN} power-up, but is overridden according to a resistor pin-strap applied between the FSWPH_*nn*_CFG pin and SGND only if the module is configured to respect resistor pin-strap settings (MFR_CONFIG_ALL[6] = 0b).

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Table 3 highlights the available resistor pin-strap and corresponding FREQUENCY_SWITCH settings.

The relative phasing of all active channels in a PolyPhase rail should be optimally phased. The relative phasing of each rail is 360°/*n*, where *n* is the number of phases in the rail. MFR_PWM_CONFIG[2:0] configures channel relative phasing to the SYNC_*nn* pin. Phase relationship values are indicated with 0° corresponding to the falling edge of SYNC being coincident with the turn-on of the top MOSFETs.

The MFR_PWM_CONFIG command can be altered through I^2C commands, but only when the switching action is disengaged, i.e., the module's outputs are turned off. The MFR_PWM_CONFIG command takes on the value stored in NVM at SV_{IN_nn} power-up, but is overridden according to a resistor pin-strap applied between the FSWPH_*nn*_CFG pin and SGND only if the module is configured to respect resistor pin-strap settings (MFR_CONFIG_ALL[6] = 0b). Table 3 highlights the available resistor pin-strap and corresponding MFR_PWM_CONFIG[2:0] settings.

Some combinations of FREQUENCY_SWITCH and MFR_PWM_CONFIG[2:0] are unavailable by resistor pin-strapping the FSWPH_*nn*_CFG pin. All combinations of supported values for FREQUENCY_SWITCH and MFR_PWM_CONFIG[2:0] can be configured by NVM programming—or, I^2C transactions, provided switching action is disengaged, i.e., the module's outputs are turned off.

Care must be taken to minimize capacitance on SYNC to ensure that the pull-up resistor versus the capacitor load has a low enough time constant for the application to form a clean clock. See Open-Drain Pins, later in this section.

When an LTM4682 is configured as a sync subordinate, it is permissible for external circuitry to drive the SYNC_*nn* pin from a current-limited source (less than 10mA), rather than using a pull-up resistor. Any external circuitry must not drive high with arbitrarily low impedance at SV_{IN_nn} power-up, because the SYNC_*nn* output can be low impedance until NVM contents have been downloaded to RAM.

The recommended LTM4682 switching frequencies for operation of many common V_{IN}-to-V_{OUT} applications are indicated Table 9. When the two channels of an LTM4682 are stepping input voltage(s) down to output voltages whose recommended switching frequencies in Table 9 are significantly different, operation at the higher of the two recommended switching frequencies is preferable, but minimum on-time must be considered. See the Minimum On-Time Considerations section.

Table 9. Recommended Switching Frequency for Various V_{IN}-to-V_{OUT} Step-Down Scenarios

	$5V_{IN}$	$8V_{IN}$	$12V_{IN}$
$0.7V_{OUT}$	575kHz	575kHz	575kHz
$0.8V_{OUT}$	650kHz	650kHz	650kHz
$0.9V_{OUT}$	650kHz	650kHz	650kHz
$1.0V_{OUT}$	650kHz	650kHz	650kHz
$1.2V_{OUT}$	650kHz	650kHz	650kHz
$1.35V_{OUT}$	750kHz	750kHz	750kHz

OUTPUT CURRENT LIMIT PROGRAMMING

The cycle-by-cycle current limit (= V_{ISENSE}/DCR) is proportional to COMP*n*b, which can be programmed from 1.45V to 2.2V using the PMBus command IOUT_OC_FAULT_LIMIT. The LTM4682 uses only the sub-milliohm sensing to detect current levels. See IOUT_OC_FAULT_LIMIT. The LTM4682 has two ranges of current limit programming. The value of MFR_PWM_MODE[2] is reserved, and the MFR_PWM_MODE[7], and IOUT_OC_FAULT_LIMIT are used to set the current limit level, see the section of the PMBus commands, the device can regulate output voltage with the peak current under the value of IOUT_OC_FAULT_LIMIT in normal operation. In case output current exceeds the current limit, a OC fault will be issued. Each of the IOUT_OC_FAULT_LIMIT ranges will affect the loop gain, and subsequently affect the loop stability, so setting the range of current limiting is a part of loop design.

The LTpowerCAD design tool can be used to look at the loop stability changes if the current limit range is adjusted. The LTM4682 will automatically update the current limit as the inductor temperature changes. Keep in mind this operation is on a cycle-by-cycle basis and is only a function of the peak inductor current. The average inductor current is monitored by the ADC converter, and can provide a warning if too much average output current is detected. The overcurrent fault is detected when the

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COMP*nb* voltage hits the maximum value. The digital processor within the LTM4682 provides the ability to either ignore the fault, shut down and latch off or shut down and retry indefinitely (hiccup). See the Peak Output Overcurrent Fault Response in the Operation section for more details. The Read_POUT can be used to readback calculated output power.

MINIMUM ON-TIME CONSIDERATIONS

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTM4682 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit, and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUTn}}{V_{INn} \bullet f_{OSC}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTM4682 is 85ns.

VARIABLE DELAY TIME, SOFT-START AND OUTPUT VOLTAGE RAMPING

The LTM4682 must enter its run state before soft-start. The RUN*n* pins are released after the part initializes and SV_{IN_nn} exceeds the VIN_ON threshold. If multiple LTM4682s are used in an application, they should be configured to share the same RUN*n* pins. They all hold their respective RUN*n* pins low until all devices initialize and SV_{IN} exceeds the VIN_ON threshold for all devices. The SHARE_CLK_*nn* pin assures all the devices connected to the signal use the same time base.

After the RUN*n* pin is released, the controller waits for the user-specified turn-on delay (TON_DELAY*n*) before initiating an output voltage ramp. Multiple LTM4682s and other Analog Devices parts can be configured to start with variable delay times. To work correctly, all devices use the same timing clock (SHARE_CLK), and all devices must share the RUN*n* pin.

This allows the relative delay of all parts to be synchronized. The actual variation in the delay will be dependent on the highest clock rate of the devices connected to the SHARE_CLK pin (all Analog Devices ICs are configured to allow the fastest SHARE_CLK signal to control the timing of all devices). The SHARE_CLK signal can be ±10% in frequency, thus the actual time delays will have some variance.

Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set point. The rise time of the voltage ramp can be programmed using the TON_RISE*n* command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting TON_RISE*n* to any value less than 0.250ms. The LTM4682 performs the necessary math internally to ensure the voltage ramp are controlled to the desired slope. However, the voltage slope can not be any faster than the V_{OUTn} fundamental limits of the power stage. The number of $t_{ON(MIN)}$ steps in the ramp is equal to TON_RISE/0.1ms.Therefore, the shorter the TON_RISE*n* time setting, the more discrete steps in the soft-start ramp appear.

The LTM4682 PWM always operates in discontinuous mode during the TON_RISE*n* operation. In discontinuous mode, the bottom MOSFET (MB*n*) is turned off as soon as reverse current is detected in the inductor. This allows the regulator to start up into a pre-biased load.

There is no analog tracking feature in the LTM4682; however, two outputs can be given the same TON_RISE*n* and TON_DELAY*n* times to achieve ratiometric rail tracking. Because the RUN*n* pins are released simultaneously and both units use the same time base (SHARE_CLK), the outputs track very closely. If the circuit is in a PolyPhase configuration, all timing parameters must be the same.

DIGITAL SERVO MODE

For maximum accuracy in the regulated output voltage, enable the digital servo loop by asserting bit 6 of the MFR_PWM_MODE command. In digital servo mode, the LTM4682 will adjust the regulated output voltage based

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on the ADC voltage reading. Every 90ms, the digital servo loop will step the LSB of the DAC (nominally 1.375mV or 0.6875mV depending on the voltage range bit) until the output is at the correct ADC reading. At power-up, this mode engages after TON_MAX_FAULT_LIMIT unless the limit is set to 0 (infinite). If the TON_MAX_FAULT_LIMIT is set to 0 (infinite), the servo begins after TON_RISE is complete and V_{OUT} has exceeded the VOUT_UV_FAULT_LIMIT. This same point in time is when the output changes from discontinuous to the programmed mode, as indicated in MFR_PWM_MODE bit 0. See Figure 25 for more details on the V_{OUT} waveform under time-based sequencing. If the TON_MAX_FAULT_LIMIT is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE is set to ignore 0x00, the servo begins:

1. After the TON_RISE sequence is complete
2. After the TON_MAX_FAULT_LIMIT time is reached; and
3. After the VOUT_UV_FAULT_LIMIT has been exceeded or the IOUT_OC_FAULT_LIMIT is no longer active.

If the TON_MAX_FAULT_LIMIT is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE is not set to ignore 0x00, the servo begins:

1. After the TON_RISE sequence is complete
2. After the TON_MAX_FAULT_LIMIT time has expired and both VOUT_UV_FAULT and IOUT_OC_FAULT are not present.

The maximum rise time is limited to 1.3 seconds.

In a PolyPhase configuration it is recommended that only one of the control loops have the digital servo mode enabled. This will insure the various loops do not work against each other due to slight differences in the reference circuits.

SOFT OFF (SEQUENCED OFF)

In addition to a controlled start-up, the LTM4682 also supports controlled turn-off. The TOFF_DELAY and TOFF_FALL functions are shown in Figure 26. TOFF_FALL is processed when the RUN*n* pin goes low, or when the part is commanded off. If the part faults off or $\overline{\text{FAULT}}n$ is pulled low externally and the part is programmed to respond to this, the output will be three-state rather than exhibiting a controlled ramp. The output will decay as a function of the load. The output voltage will operate as shown in Figure 26 as long as the part is in forced continuous mode and the TOFF_FALL time is sufficiently slow that the power stage can achieve the desired slope. The TOFF_FALL time can only be met if the power stage and controller can sink sufficient current to ensure the output is at zero volts by the end of the fall time interval. If the TOFF_FALL time is set shorter than the time required to discharge the load capacitance, the output will not reach the desired zero-volt state. At the end of TOFF_FALL, the controller will cease to sink current, and V_{OUT} will decay at the natural rate determined by the load impedance. If the controller is in discontinuous mode, the controller will

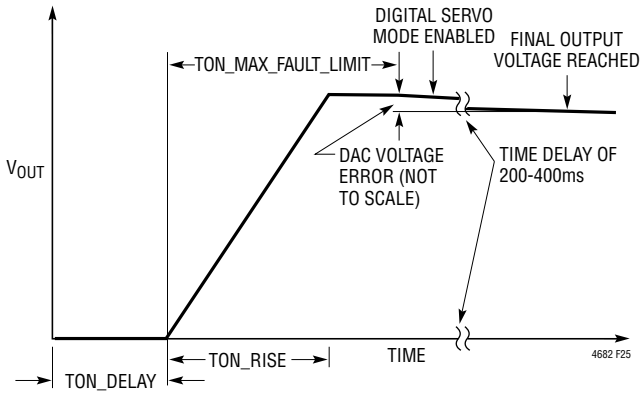

Figure 25. Timing Controlled V_{OUT} Rise

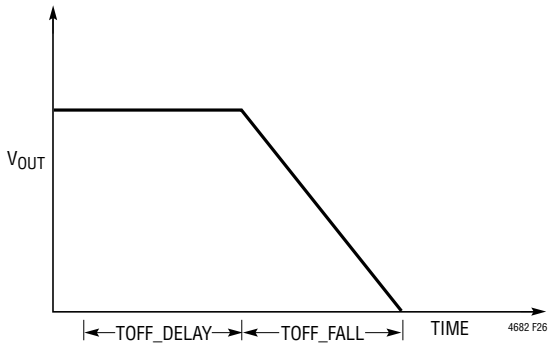

Figure 26. TOFF_DELAY and TOFF_FALL

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not pull a negative current, and the output will be pulled low by the load, not the power stage. The maximum fall time is limited to 1.3 seconds. The shorter the TOFF_FALL time is set, the larger the discrete steps in the TOFF_FALL ramp will appear. The number of steps in the ramp is equal to TOFF_FALL/0.1ms.

UNDERVOLTAGE LOCKOUT

The LTM4682 is initialized by an internal threshold-based UVLO where V_{IN} must be approximately 4V and $INTV_{CC\_nn}$, V_{DD33_nn}, and V_{DD25_nn} must be within approximately 20% of their regulated values. In addition, V_{DD33_nn} must be within approximately 7% of the targeted value before the RUN*n* pin is released. After the part has initialized, an additional comparator monitors V_{IN}. The VIN_ON threshold must be exceeded before the power sequencing can begin. When the V_{IN} drops below the VIN_OFF threshold, the SHARE_CLK_*nn* pin will be pulled low, and the V_{IN} must increase above the VIN_ON threshold before the controller will restart. The normal start-up sequence will be allowed after the VIN_ON threshold is crossed. If $\overline{FAULT}n$ is held low when V_{IN} is applied, $\overline{ALERT}nn$ will be asserted low even if the part is programmed not to assert $\overline{ALERT}nn$ when $\overline{FAULT}n$ is held low. If I^2C communication occurs before the LTM4682 is out of reset and only a portion of the command is seen by the part, this can be interpreted as a CML fault. If a CML fault is detected, $\overline{ALERT}nn$ is asserted low.

It is possible to program the contents of the NVM in the application if the V_{DD33_nn} supply is externally driven directly to V_{DD33_nn} or through V_{BIAS}. This will activate the digital portion of the LTM4682 without engaging the high-voltage sections. PMBus communications are valid in this supply configuration. If the V_{IN} has not been applied to the LTM4682, bit 3 (NVM Not Initialized) in MFR_COMMON will be asserted low. If this condition is detected, the part will only respond to addresses 5A and 5B. To initialize the part, the following set of commands are used: global address 0x5B command 0xBD data 0x2B followed by global address 5B command 0xBD and data 0xC4. The part will now respond to the correct address. Configure the part as desired, then issue a STORE_USER_ALL. When V_{IN} is applied, an MFR_RESET command must be issued to allow the PWM to be enabled and valid ADC conversions to be read.

FAULT DETECTION AND HANDLING

The LTM4682 $\overline{FAULT}n$ pins are configurable to indicate a variety of faults including, OV, UV, OC, OT, timing faults, and peak overcurrent faults. In addition, the $\overline{FAULT}n$ pins can be pulled low by external sources, indicating a fault in some other portion of the system. The fault response is configurable and allows the following options:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

See the PMBus PMBus Command Details, and the PMBus Command Summary sections of this data sheet and the PMBus specification for more details.

The OV response is automatic. If an OV condition is detected, TG*n* goes low, and BG*n* is asserted.

Fault logging is available on the LTM4682. The fault logging is configurable to automatically store data when a fault occurs that causes the unit to fault off. The header portion of the fault logging table contains peak values. It is possible to read these values at any time. This data will be useful while troubleshooting the fault.

If the LTM4682 internal temperature is in excess of 85°C, writes into the NVM (other than fault logging) is not recommended. The data will still be held in RAM, unless the 3.3V supply UVLO threshold is reached. If the die temperature exceeds 130°C, all NVM communication is disabled until the die temperature drops below 120°C.

OPEN-DRAIN PINS

The LTM4682 has the following open-drain pins:

3.3V Pins

1. $\overline{FAULT}n$
2. SYNC_*nn*

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3. SHARE_CLK_*nn*
4. PGOODn

5V Pins (5V pins operate correctly when pulled to 3.3V.)

1. RUN*n*
2. $\overline{\text{ALERT}}$_*nn*
3. SCL_*nn*
4. SDA_*nn*

All the open-drain pins have on-chip pull-down transistors that can sink 3mA at 0.4V. The low threshold on the pins is 0.8V; thus, there is plenty of margin on the digital signals with 3mA of current. For 3.3V pins, 3mA of current is a 1.1k resistor. Unless transient speed issues are associated with the RC time constant of the resistor pull-up and parasitic capacitance to the ground, a 10k resistor or larger is generally recommended.

For high-speed signals such as the SDA, SCL, and SYNC, a lower-value resistor may be required. The RC time constant should be set to 1/3 to 1/5 of the required rise time to avoid timing issues. For a 100pF load and a 400kHz PMBus communication rate, the rise time must be less than 300ns. The resistor pull-up on the SDA_*nn* and SCL_*nn* pins with the time constant set to 1/3 of the rise time is:

$$R_{PULLUP} = \frac{t_{RISE}}{3 \bullet 100pF} = 1k$$

The closest 1% resistor value is 1k. Be careful to minimize parasitic capacitance on the SDA and SCL pins to avoid communication problems. To estimate the loading capacitance, monitor the signal in question and measure how long it takes for the desired signal to reach approximately 63% of the output value. This is a one-time constant. The SYNC_*nn* pin has an on-chip pull-down transistor with the output held low for nominally 500ns. If the internal oscillator is set for 500kHz and, the load is 100pF, and a 3x time constant is required, the resistor calculation is as follows:

$$R_{PULLUP} = \frac{2\mu s - 500ns}{3 \bullet 100pF} = 5k$$

The closest 1% resistor is 4.99k.

If timing errors occur or the SYNC frequency is not as fast as desired, monitor the waveform and determine if the RC time constant is too long for the application. If possible, reduce the parasitic capacitance. If not, reduce the pull-up resistor sufficiently to ensure proper timing. The SHARE_CLK_*nn* pull-up resistor has a similar equation with a period of 10µs and a pull-down time of 1µs. The RC time constant should be approximately 3µs or faster.

PHASE-LOCKED LOOP AND FREQUENCY SYNCHRONIZATION

The LTM4682 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. The PLL is locked to the falling edge of the SYNC_*nn* pin. The phase relationship between the PWM controller and the falling edge of SYNC is controlled by the lower 3 bits of the MFR_PWM_CONFIG command. For PolyPhase applications, it is recommended that all the phases be spaced evenly. Thus, for a 2-phase system, the signals should be 180° out of phase, and a 4-phase system should be spaced 90°.

The phase detector is an edge-sensitive digital type that provides a known phase shift between the external and internal oscillators. This type of phase detector does not exhibit a false lock to the harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. The PLL lock range is guaranteed between 250kHz and 1MHz. Nominal parts will have a range beyond this; however, the operation to a wider frequency range is not guaranteed.

The PLL has a lock detection circuit. If the PLL should lose lock during operation, bit 4 of the STATUS_MFR_SPECIFIC command is asserted, and the $\overline{\text{ALERT}}$_*nn* pin is pulled low. The fault can be cleared by writing a 1 to the bit. If the user does not wish to see the $\overline{\text{ALERT}}$_*nn* pin assert if a PLL_FAULT occurs, the SMBALERT_MASK command can be used to prevent the alert.

If the SYNC signal is not clocking in the application, the nominal programmed frequency will control the PWM circuitry. However, if multiple parts share the SYNC_*nn*

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pins and the signal is not clocking, the parts will not be synchronized, and excess voltage ripple on the output may be present. Bit 10 of MFR_PADS will be asserted low if this condition exists.

If the PWM signal appears to be running at too high a frequency, monitor the SYNC_*nn* pin. Extra transitions on the falling edge will result in the PLL trying to lock on to noise versus the intended signal. Review the routing of digital control signals and minimize crosstalk to the SYNC signal to avoid this problem. Multiple LTM4682s are required to share one SYNC_*nn* pin in PolyPhase configurations. For other configurations, connecting the SYNC_*nn* pins to form a single SYNC signal is optional. If the SYNC_*nn* pin is shared between LTM4682s, only one LTM4682 controller can be programmed with frequency output. All the other LTM4682s should be programmed to disable the SYNC_*nn* output. However, their frequency should be programmed to the nominal desired value.

INPUT CURRENT SENSE AMPLIFIER

The LTM4682 input current sense amplifier can sense the supply current into the V_{IN01} and V_{IN23} power stage pins using an external sense resistor, as shown in Figure 2 Block Diagram. The $R_{SENSE}n$ value can be programmed using the MFR_IIN_CAL_GAIN command. Kelvin sensing is recommended across the R_{SENSE} resistor to eliminate errors. The MFR_PWM_CONFIG [6:5] sets the input current sense amplifier gain. See the MFR_PWM_CONFIG section. The IIN_OC_WARN_LIMIT command sets the value of the input current measured by the ADC, in amperes, which causes a warning indicating the input current is high. The READ_IIN value will determine if this limit has been exceeded. The READ_IIN command returns the input current, in Amperes, as measured across the input current sense resistor.

There is an IR voltage drop from the supply to the SV_{IN_nn} pin due to the current flowing into the SV_{IN_nn} pin. To compensate for this voltage drop, the MFR_RVIN will be automatically set to the 1Ω internal sense resistor in the Figure 2 Block Diagram. The LTM4682 will multiply the MFR_READ_ICHIP measurement value by this 1Ω resistor and add this voltage to the measured voltage at the SV_{IN_nn} pin. Therefore, READ_VIN = VSVIN_PIN + (MFR_READ_ICHIP • 1Ω). The MFR_READ_ICHIP command is used to measure the internal controller current. Using the READ_PIN command allows for reading calculated input power.

PROGRAMMABLE LOOP COMPENSATION

The LTM4682 offers programmable loop compensation to optimize the transient response without hardware change. The error amplifier gain g_m varies from 1.0mS to 5.76mS, and the compensation resistor $R_{COMP}n$ varies from 0kΩ to 62kΩ inside the controller. Two compensation capacitors, COMP*n*a and COMP*n*b, are required in the design, and the typical ratio between COMP*n*a and COMP*n*b is 10. Also, see Figure 2 Block Diagram and Figure 27.

By adjusting the g_m and $R_{COMP}n$ only, the LTM4682 can provide a flexible Type II compensation network to optimize the loop over a wide range of output capacitors. Adjusting the g_m will change the compensation's gain over the whole frequency range without moving the pole and zero location, as shown in Figure 28.

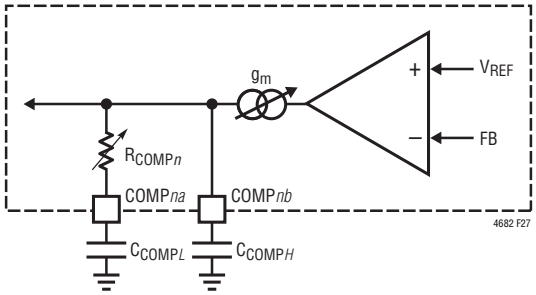

Figure 27. Programmable Loop Compensation

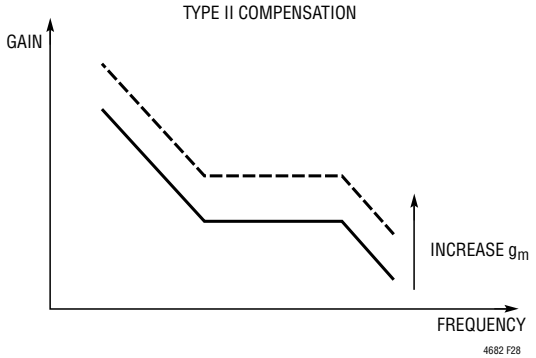

Figure 28. Error Amp g_m Adjust

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Adjusting the R_{COMP} will change the pole and zero location, as shown in Figure 29. It is recommended that the user determines the appropriate value for the g_m and R_{COMPn} using the LTpowerCAD tool.

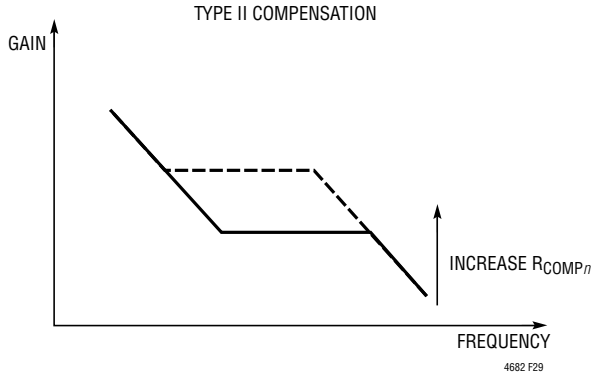

Figure 29. R_{COMP} Adjust

CHECKING TRANSIENT RESPONSE

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for excessive overshoot or ringing, indicating a stability problem. The availability of the COMP pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time, and settling at this test point truly reflect the closed-loop response. Assuming a predominantly second-order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The COMP*n*a external capacitor shown in the Typical Application circuit section will provide an adequate starting point for most applications. The programmable parameters that affect loop gain are the voltage range, bit[1] of the MFR_PWM_MODE command, the current range bit[7] of the MFR_PWM_MODE command, the g_m of the PWM channel amplifier bits [7:5] of MFR_PWM_COMP, and the internal R_{COMP} compensation resistor, bits[4:0] of MFR_PWM_COMP. Be sure to establish these settings before compensation calculation.

The COMP*n*a series internal R_{COMPn} and external C_{COMPna} filter sets the dominant pole-zero loop compensation. The internal R_{COMPn} value can be modified (from 0Ω to 62k) using bits[4:0] of the MFR_PWM_COMP command. Adjust the value of R_{COMPn} to optimize transient response once the final PCB layout is done and the particular C_{COMPbn} filter capacitor and output capacitor type and value have been determined. The output capacitors must be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and COMP pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET with a resistor to the ground directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a load step. The MOSFET + R_{SERIES} will produce output currents approximately equal to V_{OUT}/R_{SERIES}. R_{SERIES} values from 0.1Ω to 2Ω are valid depending on the current limit settings and the programmed output voltage. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine the phase margin. This is why it is better to look at the COMP pin signal, which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_{COMP}, and the bandwidth of the loop will be increased by decreasing C_{COMPna}. If R_{COMP} is increased by the same factor that C_{COMP} is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The gain of the loop will be proportional to the transconductance of the error amplifier, g_m, which is set using bits[7:5] of the MFR_PWM_COMP command. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. A second, more severe transient is caused by switching in loads with large (>1µF)

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supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus, a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PolyPhase Configuration

When configuring a PolyPhase rail with multiple LTM4682s, the user must share the SYNC, COMP, SHARE_CLK, $\overline{\text{FAULT}}$, and $\overline{\text{ALERT}}$ pins of these parts. Be sure to use pull-up resistors on $\overline{\text{FAULT}}$, SHARE_CLK, and $\overline{\text{ALERT}}$. One of the part's SYNC pins must be set to the desired switching frequency, and all other FREQUENCY_SWITCH commands must be set to External Clock. If an external oscillator is provided, set the FREQUENCY_SWITCH command to an external clock for all parts. The relative phasing of all the channels should be spaced equally. The MFR_RAIL_ADDRESS of all the devices should be set to the same value.

Multiple channels need to connect all the V_{SENSEn}^+ pins together, and all the V_{SENSEn}^- pins together, COMP*n*a and COMP*n*b pins together as well. Do not assert bit[4] of MFR_CONFIG_ALL except in a PolyPhase application. See the typical application example, Figure 50.

CONNECTING THE USB TO I²C/SMBUS/PMBUS CONTROLLER TO THE LTM4682 IN SYSTEM

The Analog Devices USB-to-I²C/SMBus/PMBus adapter (DC1613A or equivalent) can be interfaced to the LTM4682 on the user's board for programming, telemetry, and system debug. The adapter, when used in conjunction with LTpowerPlay, provides a powerful way to debug an entire power system. Faults are quickly diagnosed using the telemetry, fault status commands, and the fault log. The final configuration can be quickly developed and stored in the LTM4682 EEPROM. Figure 30 illustrates the application schematic for powering, programming, and communication with one or more LTM4682s through the Analog Devices I²C/SMBus/PMBus adapter, regardless of whether or not system power is present. If system power is not present, the dongle will power the LTM4682 through the V_{DD33_nn} supply pin. To initialize the part when V_{INnn} is

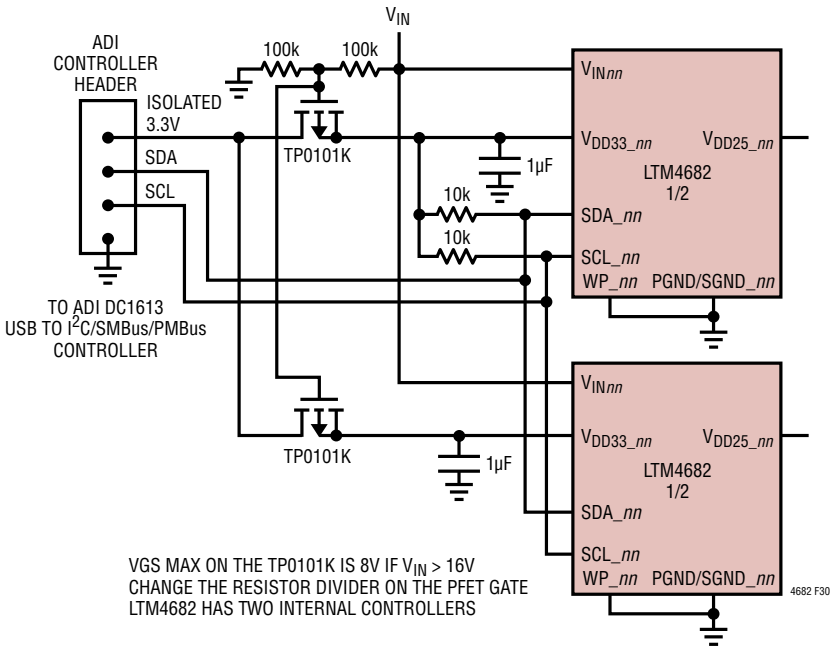

Figure 30. Controller Connection

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not applied, and the V_{DD33_nn} pin is powered, use global address 0x5B command 0xBD data 0x2B followed by address 0x5B command 0xBD data 0xC4. The LTM4682 can now communicate with the internal EEPROM and read the project file. To write the updated project file to the NVM, issue a STORE_USER_ALL command. When V_{IN} is applied, an MFR_RESET must be issued to allow the PWM POWER to be enabled and valid ADCs to be read.

Because of the adapter's limited current sourcing capability, only the LTM4682s, their associated pull-up resistors, and the I^2C pull-up resistors should be powered from the V_{DD33} 3.3V supply. In addition, any device sharing the I^2C bus connections with the LTM4682 should not have body diodes between the SDA/SCL pins and their respective V_{DD} node because this will interfere with bus communication without system power. If the V_{IN} is applied, the DC1613A will not supply the power to the LTM4682s on the board. It is recommended that the RUN*n* pins be held low, or no voltage configuration resistors be inserted to avoid providing power to the load until the part is fully configured.

The LTM4682 is fully isolated from the host PC's ground by the DC1613A. The 3.3V from the adapter and the LTM4682 V_{DD33_nn} pin must be driven to each LTM4682 internal controller with a separate PFET. If both V_{IN} and V_{BIAS} are not on, the V_{DD33_nn} pins can be in parallel because the on-chip LDO is off. The controller's 3.3V current limit is 100mA, but typical V_{DD33_nn} currents are under 15mA. The V_{DD33_nn} does backdrive the $INTV_{CC}$/V_{BIAS} pin. Normally, this is not an issue if the V_{IN} is open.

LTpowerPlay: AN INTERACTIVE GUI FOR DIGITAL POWER

The LTpowerPlay (see Figure 31) is a powerful Windows-based development environment supporting Analog Devices, digital power system management ICs, and the LTM4682. The software supports a variety of different tasks. The LTpowerPlay can evaluate Analog Devices ICs by connecting to a demo board or the user application. The LTpowerPlay can also be used in an offline mode (with no hardware present) to build multiple IC configuration files that can be saved and reloaded later. The LTpowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program or tweak the power system or to diagnose power issues when bringing up rails. LTpowerPlay utilizes Analog Devices's USB-to-I^2C/SMBus/PMBus adapter to communicate with one of the many potential targets, including the DC2924A, DC3082A demo boards, or a customer target system. The software also provides an automatic update feature to keep the revisions current with the latest set of device drivers and documentation.

A great deal of context-sensitive help is available with LTpowerPlay, along with several tutorial demos.

PMBus COMMUNICATION AND COMMAND PROCESSING

The LTM4682 internal controllers have a one-deep buffer to hold the last data written for each supported command before processing, as shown in Figure 32, Write Command Data Processing. When the part receives a new command from the bus, it copies the data into the Write Command Data Buffer, indicates to the internal processor that this command data needs to be fetched, and converts the command to its internal format to be executed. Two distinct parallel blocks manage command buffering and command processing (fetch, convert, and execute) to ensure the last data written to any command is never lost. Command data buffering handles incoming PMBus writes by storing the command data to the Write Command Data Buffer and marking these commands for future processing. The internal processor runs in parallel and handles the sometimes slower task of fetching, converting and executing commands marked for processing. Some computationally intensive commands (e.g., timing parameters, temperatures, voltages, and currents) have internal processor execution times that may be long relative to PMBus timing. If the part is busy processing a command, and new command(s) arrive, execution may be delayed or processed in a different order than received. The part indicates when internal calculations are in the process through bit 5 of MFR_COMMON (calculations not pending). When the part is busy calculating, bit 5 is cleared. When this bit is set, the part is ready for another

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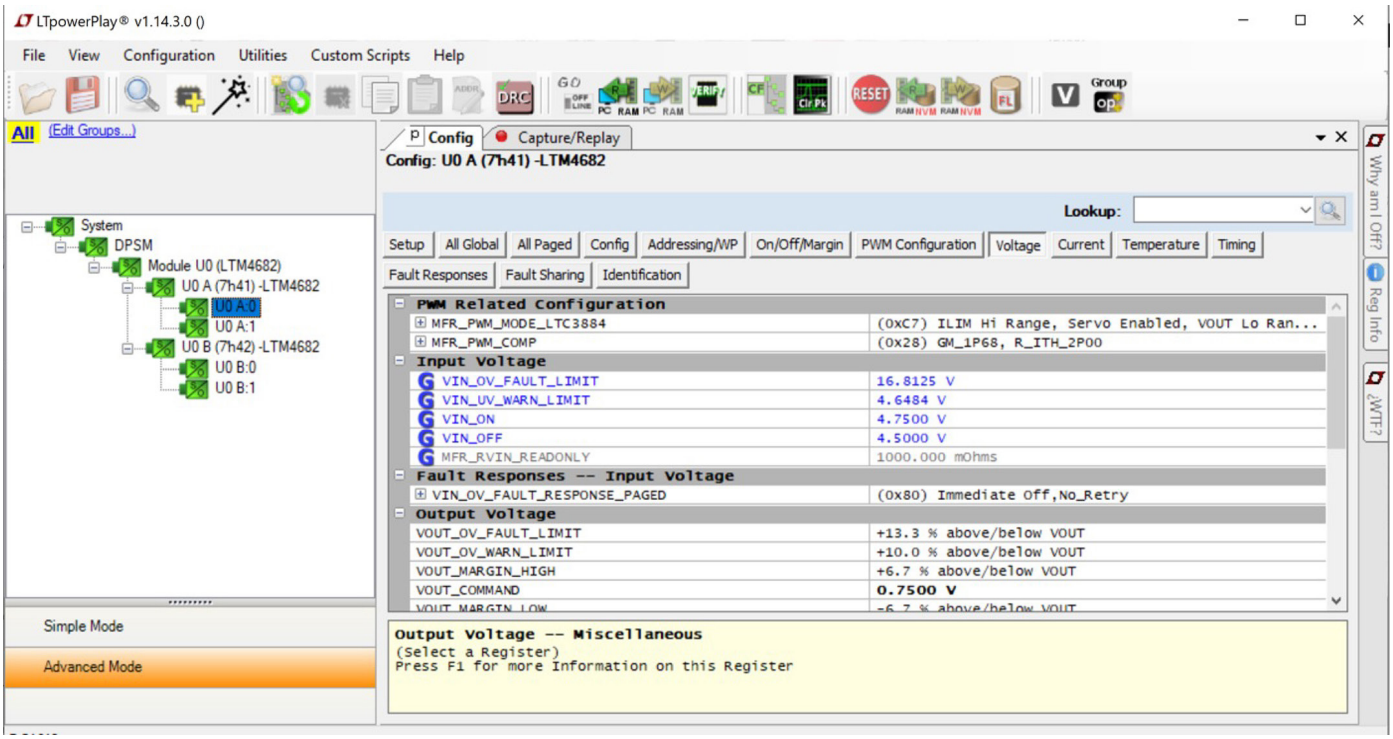
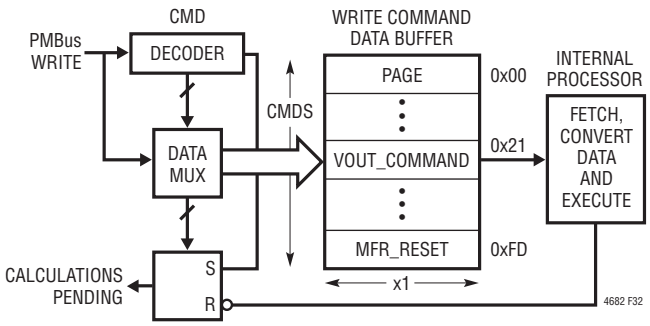


Figure 31. LTpowerPlay Screen Shot



Channel #	GUI Identity
0	U0:A0
1	U0:A1
2	U0:B0
3	U0:B1

Figure 32. Write Command Data Processing

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command. An example polling loop is shown in Figure 33, which ensures that commands are processed in order while simplifying error-handling routines.

When the part receives a new command while it is busy, it will communicate this condition using standard PMBus protocol. Depending on the part configuration it may either NACK the command or return all ones (0xFF) for reads. It may also generate a BUSY fault and $\overline{\text{ALERT}}$ notification, or stretch the SCL clock low. For more information, refer to PMBus Specification v1.1, Part II, Section 10.8.7, and SMBus v2.0, section 4.3.3. Clock stretching can be enabled by asserting bit 1 of MFR_CONFIG_ALL. Clock stretching will only occur if enabled, and the bus communication speed exceeds 100kHz.

```
// wait until chip is not busy
do
{
mfrCommonValue = PMBUS_READ_BYTE(0xEF);
partReady = (mfrCommonValue & 0x68) == 0x68;
}while(!partReady)
// now the part is ready to receive the next
command
PMBUS_WRITE_WORD(0x21, 0x2000); //write VOUT_
COMMAND to 2V
```

Figure 33. Example of a Command Write of VOUT_COMMAND

The PMBus busy protocols are well-accepted standards, but can make writing system-level software somewhat complex. The part provides three hand-shaking status bits, which reduce complexity while enabling robust system-level communication.

The three hand-shaking status bits are in the MFR_COMMON register. When the part is busy executing an internal operation, it will clear bit 6 of MFR_COMMON (chip not busy). When the part is busy specifically because it is in a transitional V_{OUT} state (margining hi/lo, power off/on, moving to a new output voltage set point, etc.), it will clear bit 4 of MFR_COMMON (output not in transition). When internal calculations are in process, the part will clear bit 5 of MFR_COMMON (calculations not pending). These three status bits can be polled with a PMBus read byte of the MFR_COMMON register until all three bits are set. A command immediately following the status bits being set will be accepted without NACKing or generating a BUSY fault/ALERT notification. The part can NACK commands for other reasons, however, as required by the PMBus spec (for instance, an invalid command or data). An example of a robust command write algorithm for the VOUT_COMMAND register is provided in Figure 33.

It is recommended that all command writes (write byte, write word, etc.) be preceded with a polling loop to avoid the extra complexity of dealing with busy behavior and unwanted $\overline{\text{ALERT}}$ notifications. A simple way to achieve this is to create a SAFE_WRITE_BYTE() and SAFE_WRITE_WORD() subroutine. The above polling mechanism allows your software to remain clean and simple while robustly communicating with the part. For a detailed discussion of these topics and other special cases, refer to the Application Note search section feature at Analog.com.

When communicating using bus speeds at or below 100kHz, the polling mechanism shown here provides a simple solution that ensures robust communication without clock stretching. At bus speeds in excess of 100kHz, it is strongly recommended that the part be configured to enable clock stretching. This requires a PMBus main device that supports clock stretching. System software that detects and properly recovers from the standard PMBus NACK/BUSY faults as described in the PMBus Specification v1.1, Par II, Section 10.8.7 is required to communicate. The LTM4682 is not recommended in applications with bus speeds in excess of 400kHz.

THERMAL CONSIDERATIONS AND OUTPUT CURRENT DERATING

The thermal resistances reported in the Pin Configuration section of this data sheet are consistent with those parameters defined by JESD51-12. They are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board defined by JESD51-9 (Test Boards for Area Array Surface Mount Package Thermal Measurements). The motivation for providing these thermal coefficients is found in JESD51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

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Many designers may use laboratory equipment and a test vehicle, such as the demo board, to predict the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance on thermal performance; instead, the derating curves provided later in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in one cubic foot sealed enclosure. This environment is sometimes referred to as still air, although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$, the thermal resistance from the junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don't generally match the user's application.
3. θ_{JCtop}, the thermal resistance from the junction to the top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages, but the test conditions don't generally match the user's application.
4. θ_{JB}, the thermal resistance from the junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured at a specified distance from the package, using a two-sided, two-layer board. This board is described in JESD51-9.

A graphical representation of the aforementioned thermal resistances is shown in Figure 34; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance

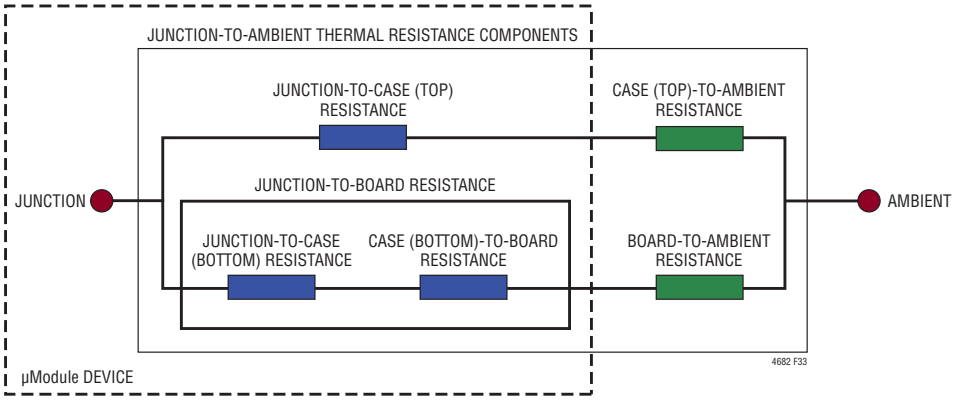

Figure 34. Graphical Representation of JESD51-12 Thermal Coefficients

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parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through the bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4682, be aware that there are multiple power devices and components dissipating power, with the consequence that the thermal resistances relative to different junctions of components or die are not exactly linear to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4682 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 and JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4682 with heat sink, and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves provided in later sections of this data sheet, along with well-correlated JESD51-12-defined θ values provided in the Pin Configuration section of this data sheet.

The 5V, 8V, and 12V power loss curves in Figure 35, Figure 36, and Figure 37, respectively, can be used in coordination with the load current derating curves in Figure 41 to Figure 46 for calculating an approximate θ_{JA} thermal resistance for the LTM4682 with various airflow conditions and without heat sinks. These thermal resistances represent the demonstrated performance of the LTM4682 on hardware, an 8-layer FR4 PCB measuring 215mm × 160mm × 1.6mm using 2oz copper on all layers. The power loss curves are taken at room temperature, and are increased with multiplicative factors of 1.35 when the junction temperature reaches 125°C. The derating curves are plotted with the LTM4682's paralleled outputs initially sourcing up to 120A and the ambient temperature at 25°C. The output voltages are 0.75V, 1V and 1.35V. These are chosen to include the lower and higher output voltage ranges to correlate the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber, along with thermal modeling analysis. The junction temperatures are monitored while the ambient temperature is increased with and without airflow.

The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 125°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current decreases the internal module loss as the ambient temperature is increased. The monitored junction temperature of 125°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 43, the load current is derated to ~80A at ~67°C ambient with no air or heat sink, and the room temperature (25°C) power loss for this $12V_{IN}$ to $1V_{OUT}$ at $80A_{OUT}$ condition is ~9.7W. A 13.1W loss is calculated by multiplying the ~9.7W room temperature loss from the $12V_{IN}$ to $1V_{OUT}$ power loss curve at 80A (Figure 37), with the 1.35 multiplying factor. If the 67°C ambient temperature is subtracted from the 125°C junction temperature, then the difference of 58°C divided by 13.1W yields a thermal resistance, θ_{JA}, of 4.4°C/W—in good agreement with the value derived from thermal simulation shown

APPLICATIONS INFORMATION-DERATING CURVES

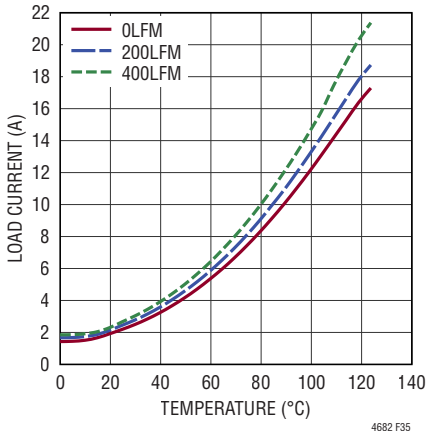

Figure 35. $5V_{IN}$ Power Loss Curve

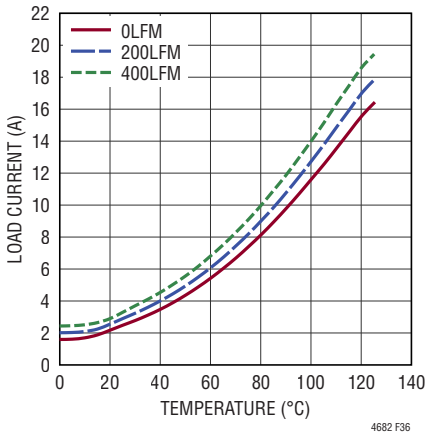

Figure 36. $8V_{IN}$ Power Loss Curve

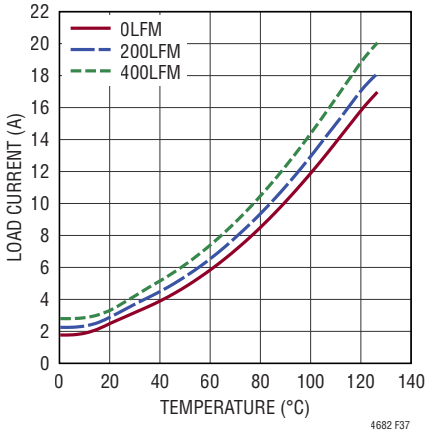

Figure 37. $12V_{IN}$ Power Loss Curve

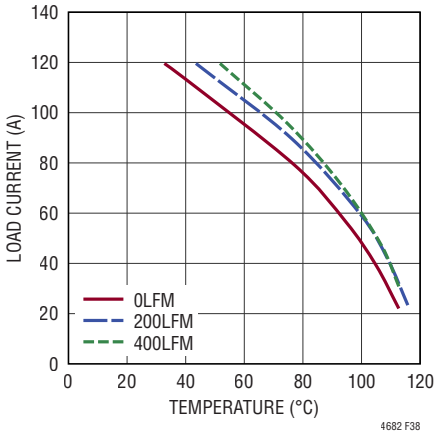

Figure 38. $5V_{IN}$ to $0.75V_{OUT}$ Derating Curve, No Heatsink

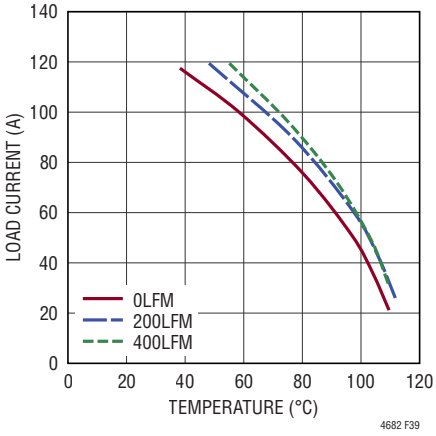

Figure 39. $8V_{IN}$ to $0.75V_{OUT}$ Derating Curve, No Heatsink

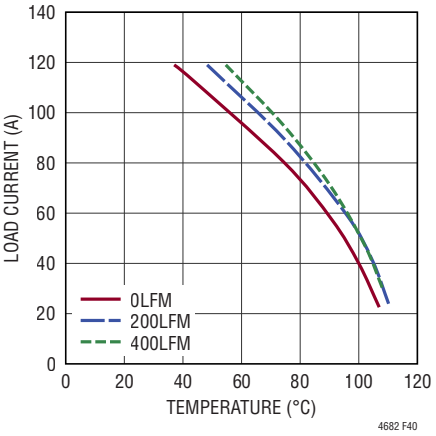

Figure 40. $12V_{IN}$ to $0.75V_{OUT}$ Derating Curve, No Heatsink

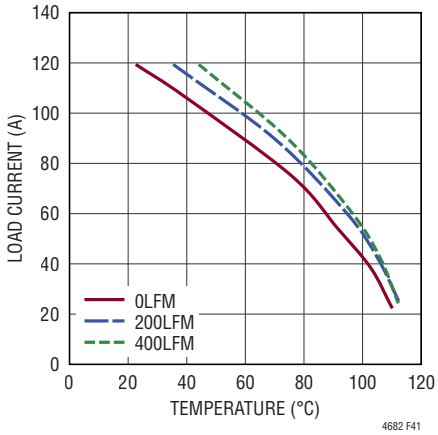

Figure 41. $5V_{IN}$ to $1V_{OUT}$ Derating Curve, No Heat Sink

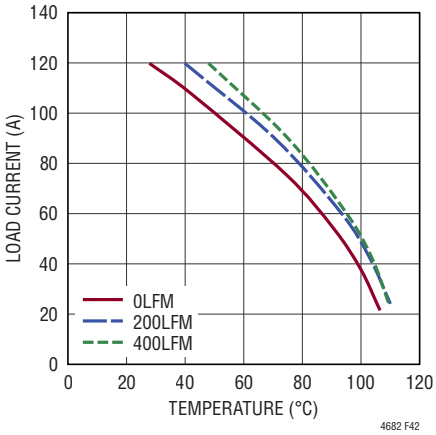

Figure 42. $8V_{IN}$ to $1V_{OUT}$ Derating Curve, No Heat Sink

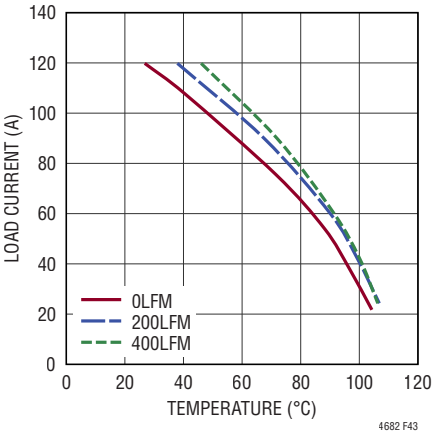

Figure 43. $12V_{IN}$ to $1V_{OUT}$ Derating Curve, No Heat Sink

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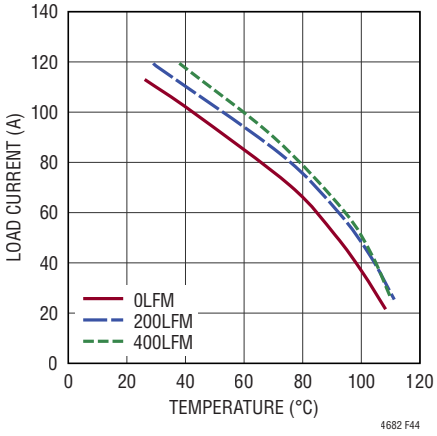


Figure 44. $5V_{IN}$ to $1.35V_{OUT}$ Derating Curve, No Heat Sink

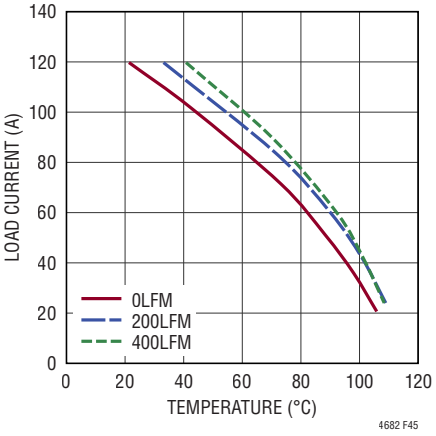


Figure 45. $8V_{IN}$ to $1.35V_{OUT}$ Derating Curve, No Heat Sink

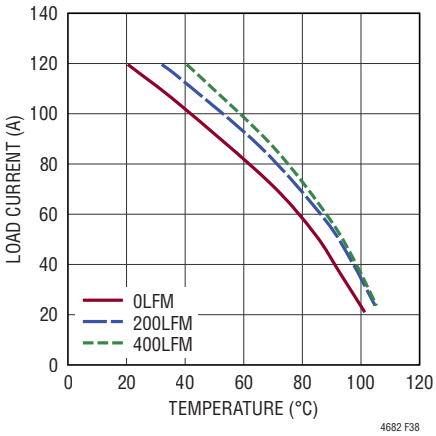


Figure 46. $12V_{IN}$ to $1.35V_{OUT}$ Derating Curve, No Heat Sink

in the Pin Configuration section. Table 10, Table 11, and Table 12 provide equivalent thermal resistances for 0.75V, 1V, and 1.35V outputs with and without airflow. The derived thermal resistances in Table 10 through Table 12 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors.

Table 10 through Table 12: Output Current Derating

Table 10. 0.75V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 38 to Figure 40	5, 8, 12	Figure 35 to Figure 37	0	None	4.4
Figure 38 to Figure 40	5, 8, 12	Figure 35 to Figure 37	200	None	4
Figure 38 to Figure 40	5, 8, 12	Figure 35 to Figure 37	400	None	3

Table 11. 1V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 41 to Figure 43	5, 8, 12	Figure 35 to Figure 37	0	None	4.4
Figure 41 to Figure 43	5, 8, 12	Figure 35 to Figure 37	200	None	4
Figure 41 to Figure 43	5, 8, 12	Figure 35 to Figure 37	400	None	3

Table 12. 1.35V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 44 to Figure 46	5, 8, 12	Figure 35 to Figure 37	0	None	4.4
Figure 44 to Figure 46	5, 8, 12	Figure 35 to Figure 37	200	None	4
Figure 44 to Figure 46	5, 8, 12	Figure 35 to Figure 37	400	None	3

Table 13. Single Channel Output Voltage vs Capacitor Selection, 10A to 20A Load Step with 10A/µs Slew Rate

V_{IN} (V)	V_{OUT} (V)	I_{LIM} RANGE	V_{OUT} RANGE	C_{OUT} (CER CAP)	C_{OUT} (BULK CAP)	C_{COMPb} (pF)	C_{COMPa} (nF)	R_{COMP} (kΩ)	EA– g_m (mS)	f_{SW} (kHz)	LOAD STEP (A)	V_{OUT} DROOP (mV)	PK–PK DEVIATION (mV)	RECOVERY TIME (µs)	PHASE MARGIN CROSS OVER FREQ (kHz)	PHASE MARGIN (DEG)	GAIN MARGIN (dB)	GAIN MARGIN CROSS OVER FREQ (kHz)
5	0.7	High	Low	*100µF ×4	**470µF ×3	150	2.2	15	3.02	575	10 to 20	30	60	33	29	65	–14	128
12	0.7	High	Low	*100µF ×4	**470µF ×3	150	2.2	15	3.02	575	10 to 20	29	58	33	29	66	–13	136
5	0.9	High	Low	*100µF ×4	**470µF ×3	150	2.2	15	3.02	575	10 to 20	30	59	29	30	65	–14	132
12	0.9	High	Low	*100µF ×4	**470µF ×3	150	2.2	15	3.02	575	10 to 20	31	61	28	29	64	–13	121
5	1.0	High	Low	*100µF ×4	**470µF ×3	150	2.2	15	3.02	650	10 to 20	29	57	27	30	66	–14	141
12	1.0	High	Low	*100µF ×4	**470µF ×3	150	2.2	15	3.02	650	10 to 20	29	58	26	30	64	–14	129
5	1.2	High	Low	*100µF ×4	**470µF ×3	150	2.2	15	3.02	650	10 to 20	28	56	24	31	66	–14	144
12	1.2	High	Low	*100µF ×4	**470µF ×3	150	2.2	15	3.02	650	10 to 20	30	60	23	30	64	–14	130
5	1.35	High	Low	*100µF ×4	**470µF ×3	150	2.2	15	3.02	750	10 to 20	28	56	21	31	67	–14	154
12	1.35	High	Low	*100µF ×4	**470µF ×3	150	2.2	15	3.02	750	10 to 20	30	59	21	31	65	–14	137

*TDK C3225X5R0J107M, 100µF, 6.3V, X5R.

**Panasonic ETPF470M5H, 470µF, 2.5V, 5mΩ

These Values Should Be Check with a BODE Analyzer.

Table 14. Single Channel Output Voltage vs Capacitor Selection, All Ceramic Configuration, 10A to 20A Load Step with 10A/µs Slew Rate

V_{IN} (V)	V_{OUT} (V)	I_{LIM} RANGE	V_{OUT} RANGE	C_{OUT} (CER CAP)	C_{OUT} (BULK CAP)	C_{COMPb} (pF)	C_{COMPa} (nF)	R_{COMP} (kΩ)	EA– g_m (mS)	f_{SW} (kHz)	LOAD STEP (A)	V_{OUT} DROOP (mV)	PK–PK DEVIATION (mV)	RECOVERY TIME (µs)	PHASE MARGIN CROSS OVER FREQ (kHz)	PHASE MARGIN (DEG)	GAIN MARGIN (dB)	GAIN MARGIN CROSS OVER FREQ (kHz)
5	0.7	High	Low	*220µF ×10	none	150	2.2	15	3.02	575	10 to 20	39	77	28	30	38	–13	73
12	0.7	High	Low	*220µF ×10	none	150	2.2	15	3.02	575	10 to 20	39	77	24	28	40	–14	75
5	0.9	High	Low	*220µF ×10	none	150	2.2	15	3.02	575	10 to 20	38	75	23	30	38	–13	76
12	0.9	High	Low	*220µF ×10	none	150	2.2	15	3.02	575	10 to 20	38	76	22	29	37	–12	69
5	1.0	High	Low	*220µF ×10	none	150	2.2	15	3.02	650	10 to 20	38	75	22	31	38	–14	80
12	1.0	High	Low	*220µF ×10	none	150	2.2	15	3.02	650	10 to 20	39	77	22	29	38	–13	73
5	1.2	High	Low	*220µF ×10	none	150	2.2	15	3.02	650	10 to 20	38	76	21	31	39	–14	82
12	1.2	High	Low	*220µF ×10	none	150	2.2	15	3.02	650	10 to 20	39	78	20	30	38	–12	73
5	1.35	High	Low	*220µF ×10	none	150	2.2	15	3.02	750	10 to 20	37	74	19	32	39	–15	87
12	1.35	High	Low	*220µF ×10	none	150	2.2	15	3.02	750	10 to 20	38	76	21	30	38	–13	76

*Murata GRM32EC80E227ME05L, 220µF, 2.5V, X6S.

These values should be check with a BODE Analyzer.

Table 15. Dual Connected Channels Output Voltage vs Capacitor Selection, Bulk and Ceramic Cap Configuration, 10A to 30A Load Step with 20A/µs Slew Rate

V_{IN} (V)	V_{OUT} (V)	I_{LIM} RANGE	V_{OUT} RANGE	C_{OUT} (CER CAP)	C_{OUT} (BULK CAP)	C_{COMPb} (pF)	C_{COMPa} (nF)	R_{COMP} (kΩ)	EA–g_m (mS)	f_{SW} (kHz)	LOAD STEP (A)	V_{OUT} DROOP (mV)	PK–PK DEVIATION (mV)	RECOVERY TIME (µs)	PHASE MARGIN CROSS OVER FREQ (kHz)	PHASE MARGIN (DEG)	GAIN MARGIN (dB)	GAIN MARGIN CROSS OVER FREQ (kHz)
12	0.7	High	Low	*100µF ×8	**560µF ×4	150	3.3	15	3.02	575	10 to 30	37	74	48	33	55	–14	166
12	0.9	High	Low	*100µF ×8	**560µF ×4	150	3.3	15	3.02	575	10 to 30	37	75	42	33	53	–14	150
12	1.0	High	Low	*100µF ×8	**560µF ×4	150	3.3	15	3.02	650	10 to 30	37	74	39	33	54	–14	159
12	1.2	High	Low	*100µF ×8	**560µF ×4	150	3.3	15	3.02	650	10 to 30	37	73	32	34	53	–14	159
12	1.35	High	Low	*100µF ×8	**560µF ×4	150	3.3	15	3.02	750	10 to 30	37	73	30	34	54	–14	166

*TDK C3225X5R0J107M, 100µF, 6.3V, X5R.

**Panasonic EEFGX0D561R, 560µF, 2.0V, 3mΩ.

These Values Should Be Check with a BODE Analyzer.

Table 16. Quad Connected Channels Output Voltage vs Capacitor Selection, Bulk and Ceramic Cap Configuration, 10A to 40A Load Step with 15A/µs Slew Rate

V_{IN} (V)	V_{OUT} (V)	I_{LIM} RANGE	V_{OUT} RANGE	C_{OUT} (CER CAP)	C_{OUT} (BULK CAP)	C_{COMPb} (pF)	C_{COMPa} (nF)	R_{COMP} (kΩ)	EA–g_m (mS)	f_{SW} (kHz)	LOAD STEP (A)	V_{OUT} DROOP (mV)	PK–PK DEVIATION (mV)	RECOVERY TIME (µs)	PHASE MARGIN CROSS OVER FREQ (kHz)	PHASE MARGIN (DEG)	GAIN MARGIN (dB)	GAIN MARGIN CROSS OVER FREQ (kHz)
12	0.7	High	Low	*100µF ×12	**560µF ×4	150	6.8	15	3.02	575	10 to 40	31	62	24	62	43	–7	145
12	0.9	High	Low	*100µF ×12	**560µF ×4	150	6.8	15	3.02	575	10 to 40	32	63	20	63	40	–7	137
12	1.0	High	Low	*100µF ×12	**560µF ×4	150	6.8	15	3.02	650	10 to 40	30	60	20	63	42	–7	144
12	1.20	High	Low	*100µF ×12	**560µF ×4	150	6.8	15	3.02	650	10 to 40	32	63	17	64	42	–7	146
12	1.35	High	Low	*100µF ×12	**560µF ×4	150	6.8	15	3.02	750	10 to 40	32	64	13	62	45	–8	153

*TDK C3225X5R0J107M, 100µF, 6.3V, X5R.

**Panasonic EEFGX0D561R, 560µF, 2.0V, 3mΩ.

These Values Should Be Check with a BODE Analyzer.

APPLICATIONS INFORMATION

EMI PERFORMANCE

The SW*n* pin provides access to the midpoint of the power MOSFETs in LTM4682's power stages.

Connecting an optional series RC network from SW*n* to GND can dampen high-frequency (~30MHz+) switch node ringing caused by parasitic inductances and capacitances in the switched-current paths. The RC network is called a snubber circuit because it dampens (or snubs) the resonance of the parasitics, at the expense of higher power loss. To use a snubber, choose first how much power to allocate to the task and how much PCB real estate is available to implement the snubber. For example, if PCB space allows a low inductance 0.5W resistor to be used, then the capacitor in the snubber network (CSW) is computed by:

$$C_{SW} = \frac{P_{SNUB}}{V_{INn(MAX)}^2 \bullet f_{SW}}$$

where $V_{INn(MAX)}$ is the maximum input voltage that the input to the power stage (V_{INn}) will see in the application, and f_{SW} is the DC/DC converter's switching frequency of operation. C_{SW} should be NPO, C0G, or X7R-type (or better) material.

The snubber resistor (R_{SW}) value is then given by:

$$R_{SW} = \sqrt{\frac{5nH}{C_{SW}}}$$

The snubber resistor should be low ESL and capable of withstanding the pulsed currents present in snubber circuits. A value between 0.7Ω and 4.2Ω is normal.

A 2.2nF snubber capacitor is a good value to start with in series with the snubber resistor to the ground. The no-load input quiescent current can be monitored while selecting different RC series snubber components to get an increased power loss versus switch node ringing attenuation.

SAFETY CONSIDERATIONS

The LTM4682 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current must be provided to protect each unit from catastrophic failure.

The fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage. Thus, the internal bottom MOSFET will turn on indefinitely, trying to protect the load. Under this fault condition, the input voltage will source very large currents to the ground through the failed internal top MOSFET and enabled internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation. The device supports overcurrent and overtemperature protection.

APPLICATIONS INFORMATION

LAYOUT CHECKLIST/EXAMPLE

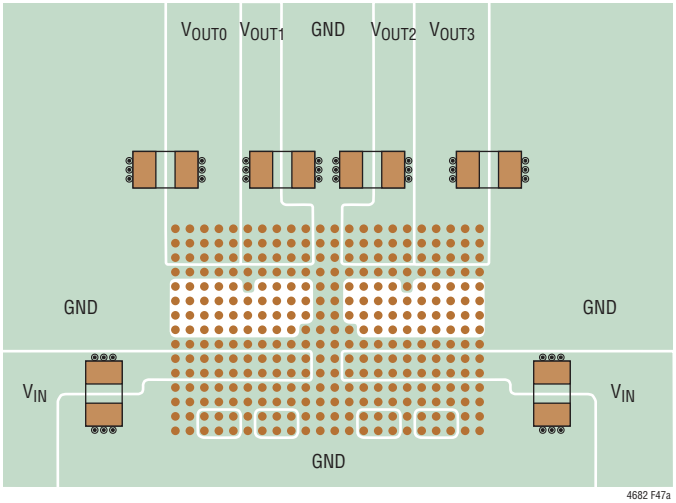
The high integration of LTM4682 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including $V_{IN}n$, GND, and $V_{OUT}n$. It helps to minimize the PCB conduction loss and thermal stress.
- Place high-frequency ceramic input and output capacitors next to the $V_{IN}n$, GND, and $V_{OUT}n$ pins to minimize high-frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between the top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4682.
- Use Kelvin sense connections across the input R_{SENSE} resistor if input current monitoring is used.

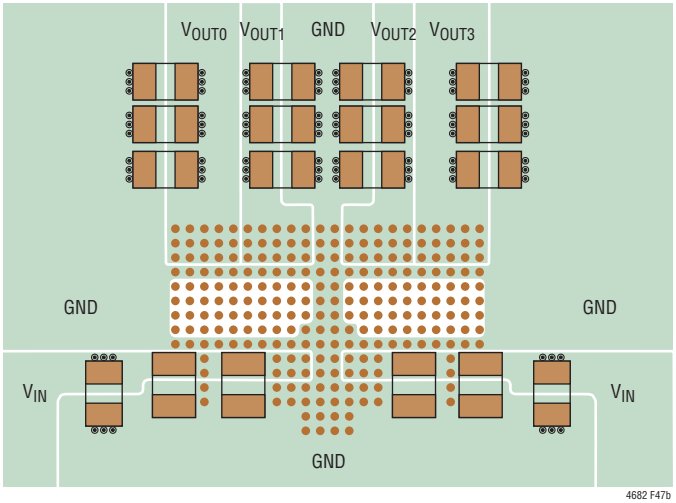
For parallel modules, connect the $V_{OUT}n$, $V_{OSNS}n^+/V_{OSNS}n^-$ voltage-sense differential pair lines, RUN*n*, COMP*n*a, and COMP*n*b pins together.

- The user must share the SYNC_*nn*, SHARE_CLK_*nn*, $\overline{\text{FAULT}}n$, and $\overline{\text{ALERT}}$_*nn* pins of these parts. Be sure to use pull-up resistors on $\overline{\text{FAULT}}n$, SHARE_CLK_*nn*, and $\overline{\text{ALERT}}$_*nn*.
- Bring out test points on the signal pins for monitoring.

Figure 47 gives a good example of the recommended layout.



(a) LTM4682 Top Layer



(b) LTM4682 Bottom Layer

Figure 47. Recommended PCB Layout Package Top View

TYPICAL APPLICATION

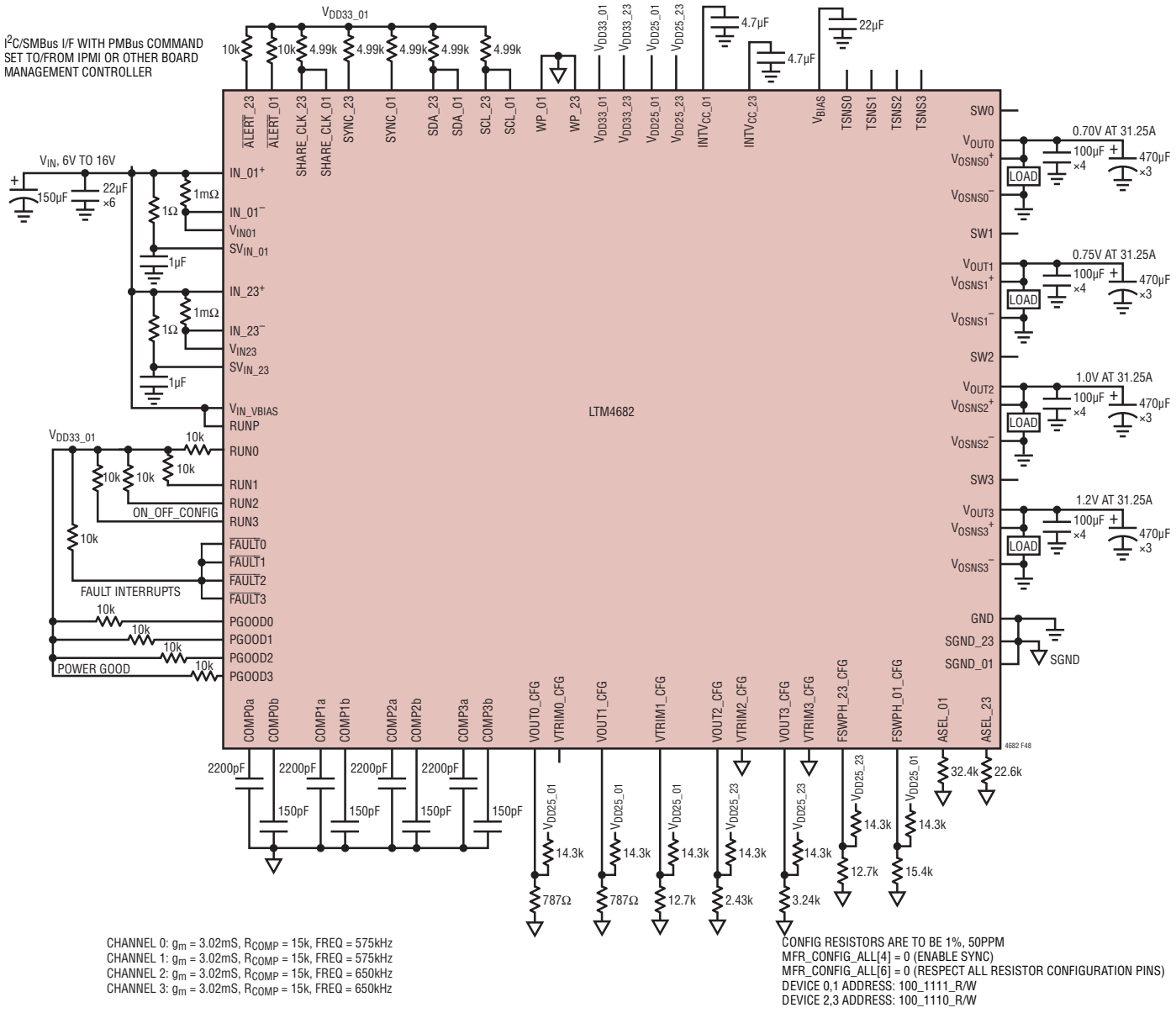


Figure 48. Quad 31.25A DC/DC µModule Regulator with I²C/SMBus/PMBus Serial Interface

TYPICAL APPLICATION

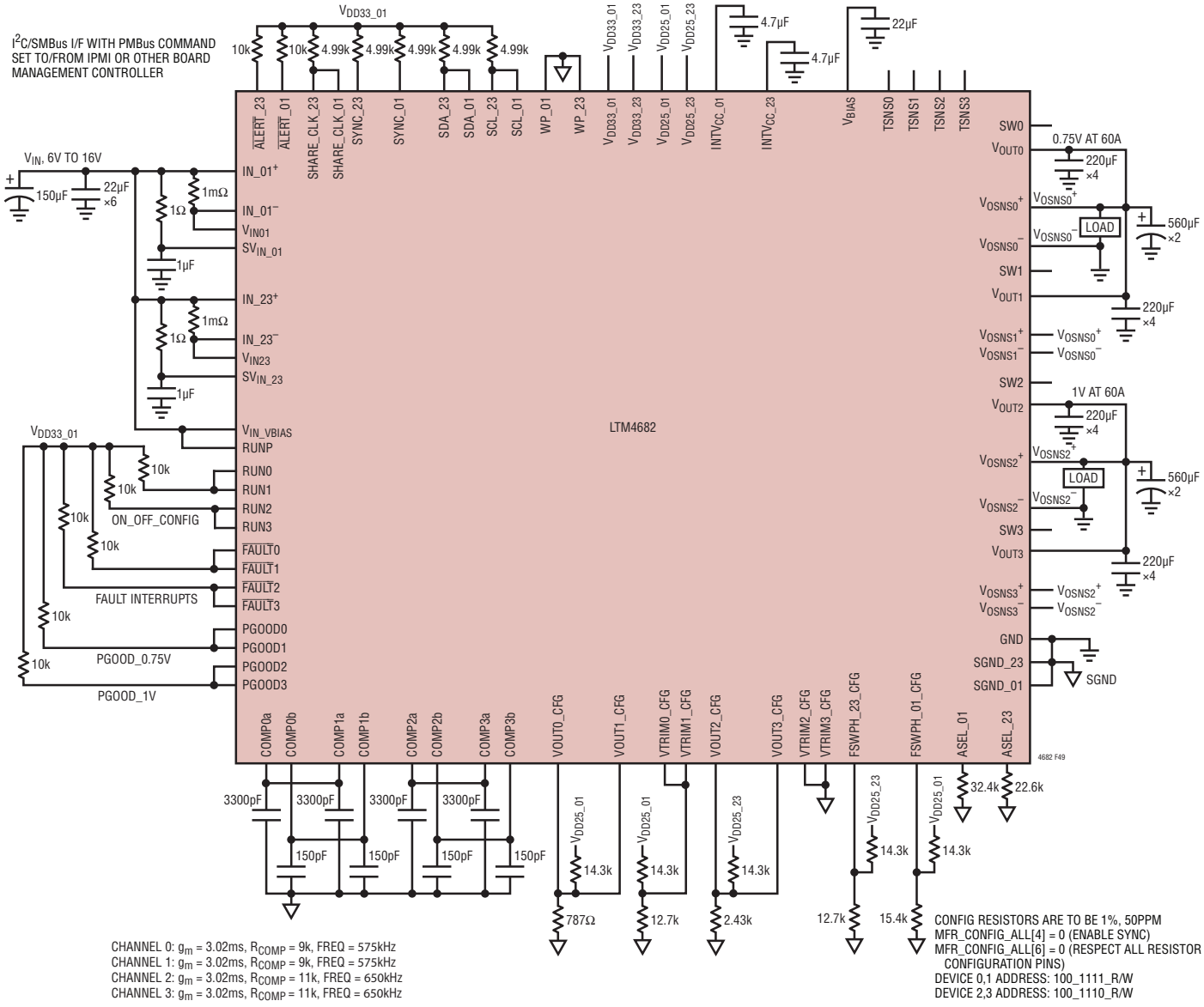


Figure 49. 0.75V and 1V Outputs at 60A with Providing I²C/SMBus/PMBus Serial Interface

TYPICAL APPLICATION

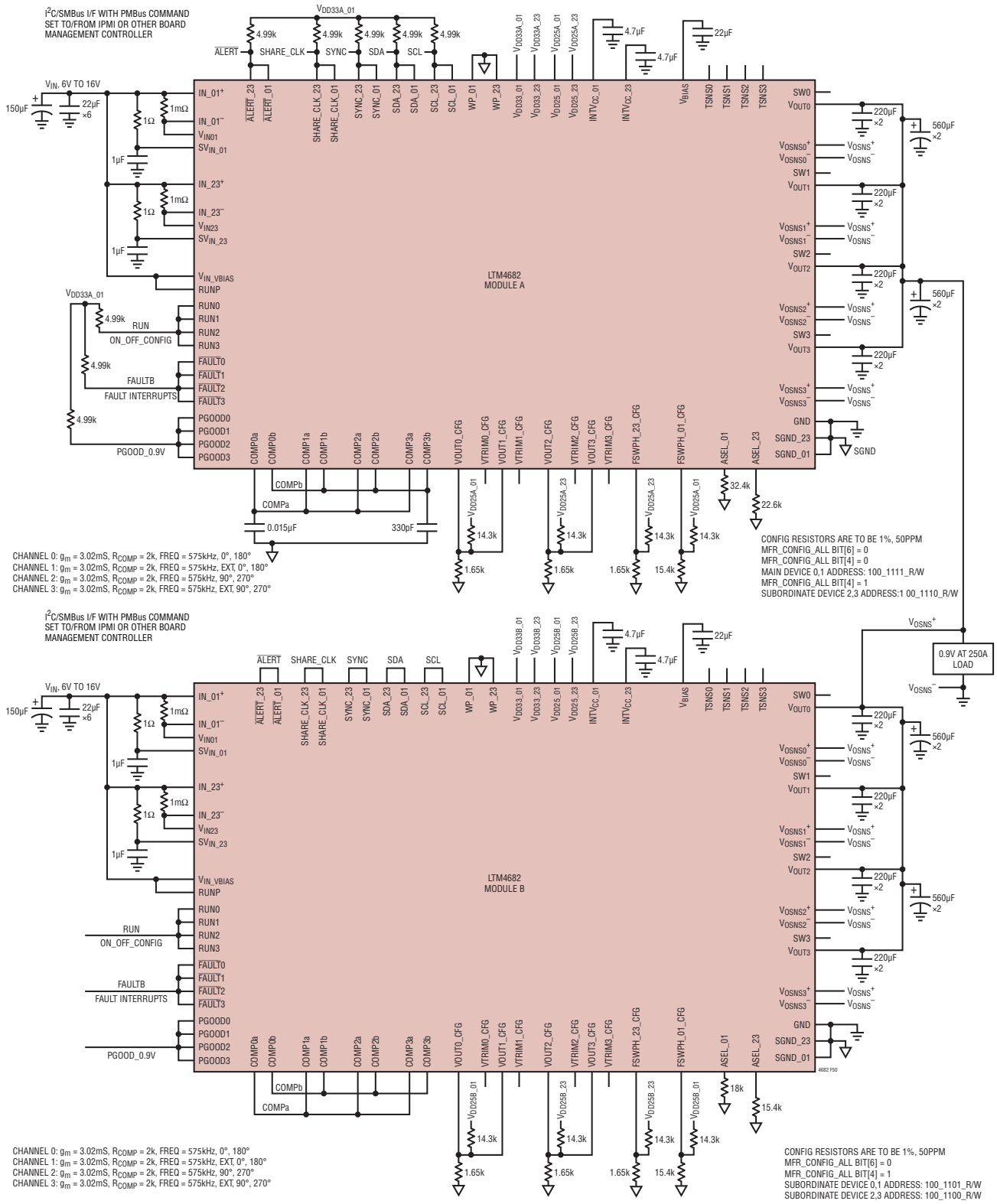


Figure 50. Two Paralleled LTM4682 Producing 0.9V_{OUT} at 250A, Integrated Power System Management Features Accessible Over 2-Wire I²C/SMBus/PMBus Serial Interface

TYPICAL APPLICATION

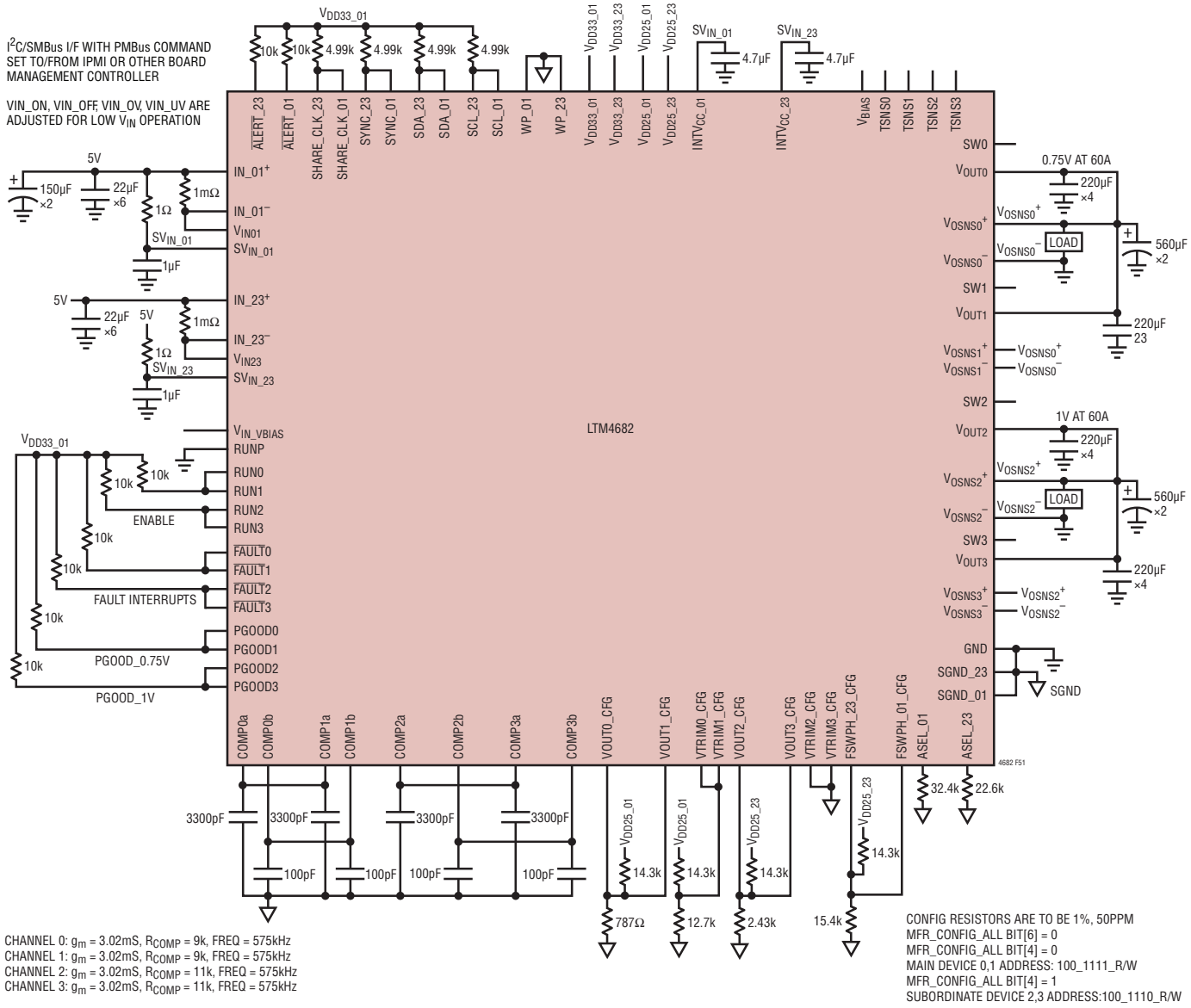


Figure 51. 0.75V/60A and 1V/60A Outputs Generated from 5V Power Input and Providing I²C/SMBus/PMBus Serial Interface

TYPICAL APPLICATION

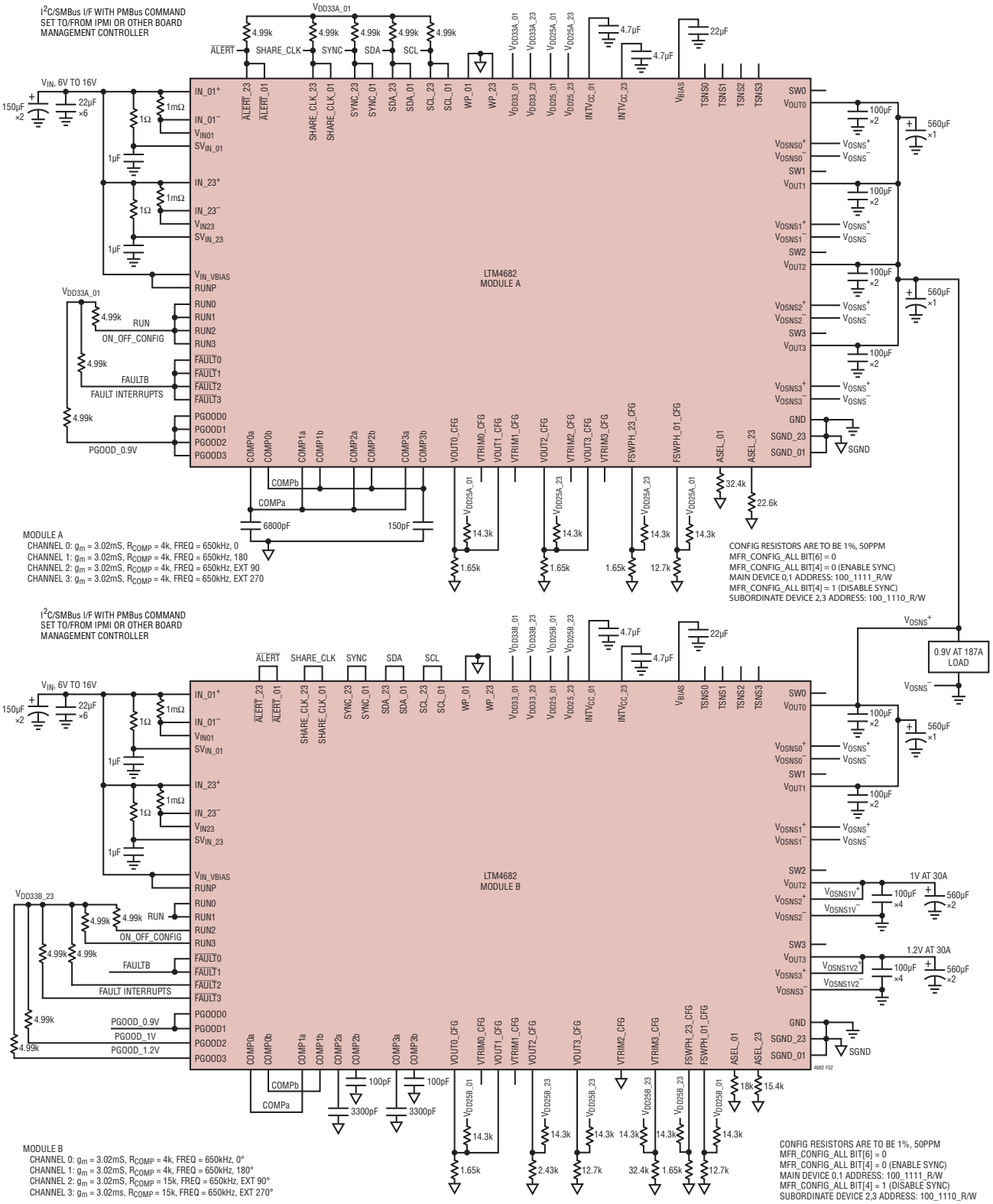


Figure 52. Six-Phase Operation Producing 0.9V at 187A, One-Phase for 1V at 30A, and 1.2V at 30A, Power System Management Features Accessible Through LTM4682 Over 2-Wire I²C/SMBus/PMBus Serial Interface

Rev. 0

PMBus COMMAND DETAILS

ADDRESSING AND WRITE PROTECT

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
PAGE	0x00	Provides integration with multi-page PMBus devices.	R/W Byte	N	Reg			0x00
PAGE_PLUS_WRITE	0x05	Write a supported command directly to a PWM channel.	W Block	N				
PAGE_PLUS_READ	0x06	Read a supported command directly from a PWM channel.	Block R/W	N				
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W Byte	N	Reg		Y	0x4F
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80

PAGE

The PAGE command provides the ability to configure, control and monitor both PWM channels through only one physical address, either the MFR_ADDRESS or GLOBAL device address. Each PAGE contains the operating commands for one PWM channel.

Pages 0x00 and 0x01 correspond to Channel 0 and Channel 1, respectively, in this device.

ASEL_01 sets the address for Channels 0 and 1, and ASEL_23 sets the address for Channels 2 and 3. Each of the ASEL pins will have a different programmed address.

Setting PAGE to 0xFF applies any following paged commands to both outputs. With PAGE set to 0xFF, the LTM4682 will respond to read commands as if PAGE were set to 0x00 (Channel 0 results).

This command has one data byte.

PAGE_PLUS_WRITE

The PAGE_PLUS_WRITE command provides a way to set the page within a device, send a command, and then send the data for the command, all in one communication packet. Commands allowed by the present write protection level may be sent with PAGE_PLUS_WRITE.

The value stored in the PAGE command is not affected by PAGE_PLUS_WRITE. If PAGE_PLUS_WRITE is used to send a non-paged command, the Page Number byte is ignored.

This command uses the Write Block protocol. An example of the PAGE_PLUS_WRITE command with PEC sending a command that has two data bytes is shown in Figure 53.

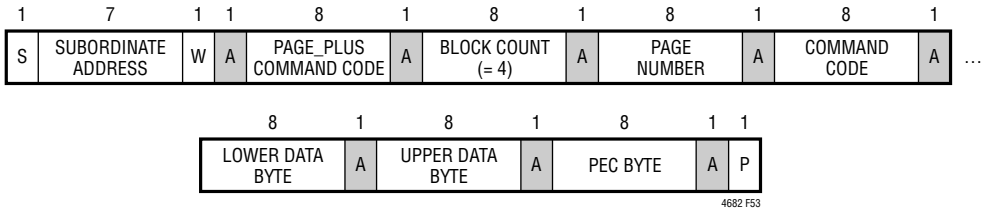


Figure 53. Example of PAGE_PLUS_WRITE

PAGE_PLUS_READ

The PAGE_PLUS_READ command provides the ability to set the page within a device, send a command, and then read the data returned by the command, all in one communication packet.

PMBus COMMAND DETAILS

The value stored in the PAGE command is not affected by PAGE_PLUS_READ. If PAGE_PLUS_READ is used to access data from a non-paged command, the Page Number byte is ignored.

This command uses the Process Call protocol. An example of the PAGE_PLUS_READ command with PEC is shown in Figure 54.

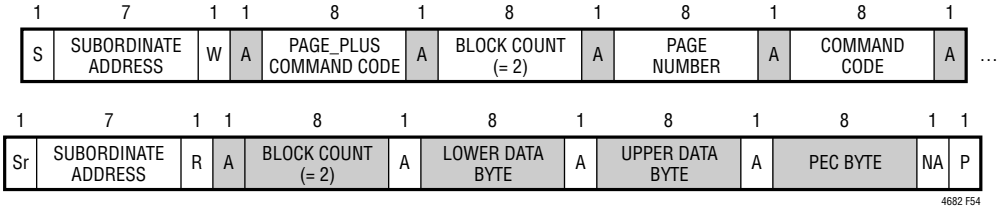


Figure 54. Example of PAGE_PLUS_READ

Note: PAGE_PLUS commands cannot be nested. A PAGE_PLUS command cannot be used to read or write another PAGE_PLUS command. If this is attempted, the LTM4682 will NACK the entire PAGE_PLUS packet and issue a CML fault for Invalid/Unsupported Data.

WRITE_PROTECT

The WRITE_PROTECT command is used to control writing to the LTM4682 device. This command does not indicate the status of the WP pin, which is defined in the MFR_COMMON command. The WP pin takes precedence over the value of this command.

BYTE	MEANING
0x80	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, and STORE_USER_ALL commands.
0x40	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, STORE_USER_ALL, OPERATION, and CLEAR_FAULTS command. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.
0x20	Disable all writes except to the WRITE_PROTECT, OPERATION, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, CLEAR_FAULTS, PAGE, ON_OFF_CONFIG, VOUT_COMMAND and STORE_USER_ALL. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.
0x10	Reserved, must be 0.
0x08	Reserved, must be 0.
0x04	Reserved, must be 0.
0x02	Reserved, must be 0.
0x01	Reserved, must be 0.

Enable writes to all commands when WRITE_PROTECT is set to 0x00.

If the WP pin is high, PAGE, OPERATION, MFR_CLEAR_PEAKS, MFR_EE_UNLOCK, WRITE_PROTECT, and CLEAR_FAULTS commands are supported. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.

PMBus COMMAND DETAILS

MFR_ADDRESS

The MFR_ADDRESS command byte sets the 7 bits of the PMBus subordinate address for this device.

Setting this command to a value of 0x80 disables device addressing. The GLOBAL device address, 0x5A and 0x5B, cannot be deactivated. If RCONFIG is set to ignore, the ASEL_*nn* pins are still used to determine the LSB of the channel address. If the ASEL_01 and ASEL_23 pins are both open, the LTM4682 will use the address value stored in NVM. If the ASEL_*nn* pins are open, the LTM4682 will use the lower 4 bits of the MFR_ADDRESS value stored in NVM to construct the effective address of the part.

This command has one data byte.

MFR_RAIL_ADDRESS

The MFR_RAIL_ADDRESS command enables direct device address access to the PAGE-activated channel. The value of this command should be common to all devices attached to a single power supply rail.

The user should only perform command writes to this address. If a read is performed from this address and the rail devices do not respond with EXACTLY the same value, the LTM4682 will detect bus contention and may set a CML communications fault.

Setting this command to a value of 0x80 disables rail device addressing for the channel.

This command has one data byte.

GENERAL CONFIGURATION COMMANDS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_CHAN_CONFIG	0xD0	Configuration bits that are channel specific.	R/W Byte	Y	Reg		Y	0x1D
MFR_CONFIG_ALL	0xD1	General configuration bits.	R/W Byte	N	Reg		Y	0x21

MFR_CHAN_CONFIG

General purpose configuration command common to multiple Analog Devices' products.

BIT	MEANING
7	Reserved
6	Reserved
5	Reserved
4	Disable RUN Low. When asserted, the RUN pin is not pulsed low if commanded OFF.
3	Enable Short Cycle recognition if this bit is set to a 1.
2	SHARE_CLOCK control. If SHARE_CLOCK is held low, the output is disabled.
1	No $\overline{\text{FAULT}}$ $\overline{\text{ALERT}}$, $\overline{\text{ALERT}}$ is not pulled low if $\overline{\text{FAULT}}$ is pulled low externally. Assert this bit if either POWER_GOOD or VOUT_UVUF are propagated on $\overline{\text{FAULT}}$.
0	Disables the V_{OUT} decay value requirement for MFR_RETRY_TIME and $t_{OFF(MIN)}$ processing. When this bit is set to a 0, the output must decay to less than 12.5% of the programmed value for any action that turns off the rail, including a fault, an OFF/ON command, or a toggle of RUN from high to low to high.

This command has one data byte.

PMBus COMMAND DETAILS

A ShortCycle event occurs whenever the PWM channel is commanded back ON, or reactivated, after the part has been commanded OFF and is processing either the TOFF_DELAY or the TOFF_FALL states. The PWM channel can be turned ON and OFF through either the RUN pin, and or the PMBus OPERATION command.

If the PWM channel is reactivated during the TOFF_DELAY, the part will perform the following:

1. Immediately tri-state the PWM channel output;
2. Start the retry delay timer as specified by the $t_{OFF(MIN)}$.
3. After the $t_{OFF(MIN)}$ value has expired, the PWM channel will proceed to the TON_DELAY state and the STATUS_MFR_SPECIFIC bit #1 will assert.

If the PWM channel is reactivated during the TOFF_FALL, the part will perform the following:

1. Stop ramping down the PWM channel output;
2. Immediately tri-state the PWM channel output;
3. Start the retry delay timer as specified by the $t_{OFF(MIN)}$.
4. After the $t_{OFF(MIN)}$ value has expired, the PWM channel will proceed to the TON_DELAY state, and the STATUS_MFR_SPEFIFIC bit #1 will assert.

If the ShortCycle event occurs and the ShortCycle MFR_CHAN_CONFIG bit is not set, the PWM channel state machine will complete its TOFF_DELAY and TOFF_FALL operations as previously commanded by the user.

MFR_CONFIG_ALL

General purpose configuration command common to multiple Analog Devices' products.

BIT	MEANING
7	Enable fault logging.
6	Ignore resistor configuration pins.
5	Mask PMBus, Part II, Section 10.9.1 Violations.
4	Disable SYNC output.
3	Enable 255ms PMBus timeout.
2	A valid PEC is required for PMBus writes to be accepted. If this bit is not set, the part will accept commands with invalid PEC.
1	Enable the use of PMBus clock stretching.
0	Execute CLEAR_FAULTS on the rising edge of either RUN pin.

This command has one data byte.

ON/OFF/MARGIN

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E
OPERATION	0x01	Operating mode control. On/off, margin high, and margin low.	R/W Byte	Y	Reg		Y	0x80
MFR_RESET	0xFD	Commanded reset without requiring a power-down.	Send Byte	N				NA

PMBus COMMAND DETAILS

ON_OFF_CONFIG

The ON_OFF_CONFIG command specifies the combination of the RUN*n* pin input state and PMBus commands needed to turn the PWM channel on and off.

Supported Values:

VALUE	MEANING
0x1F	The OPERATION value and RUN*n* pin must both command the device to start/run. The device executes immediate off when commanded off.
0x1E	The OPERATION value and RUN*n* pin must both command the device to start/run. The device uses TOFF_ command values when commanded off.
0x17	RUN*n* pin control with immediate off when commanded off. OPERATION on/off control ignored.
0x16	RUN*n* pin control using TOFF_ command values when commanded off. OPERATION on/off control ignored.

Programming an unsupported ON_OFF_CONFIG value will generate a CML fault, and the command will be ignored.

This command has one data byte.

OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the input from the RUN*n* pins. It is also used to cause the unit to set the output voltage to the upper or lower MARGIN VOLTAGEs. The unit stays in the commanded operating mode until a subsequent OPERATION command or change in the state of the RUN*n* pin instructs the device to change to another mode. If the part is stored in the MARGIN_LOW/HIGH state, the next RESET or POWER_ON cycle will ramp to that state. If the OPERATION command is modified, for example, ON is changed to MARGIN_LOW, the output will move at a fixed slope set by the VOUT_TRANSITION_RATE. The default operation command is Sequence Off. If the V_{IN} is applied to a part with factory default programming and the VOUT_CONFIG resistor configuration pins are not installed, the outputs will be commanded off.
The part defaults to the Sequence Off state.
This command has one data byte.

Supported Values:

VALUE	MEANING
0xA8	Margin high.
0x98	Margin low.
0x80	On (V_{OUT} back to nominal even if bit 3 of ON_OFF_CONFIG is not set).
0x40*	Soft off (with sequencing).
0x00*	Immediate off (no sequencing).

*Device does not respond to these commands if bit 3 of ON_OFF_CONFIG is not set.

Programming an unsupported OPERATION value will generate a CML fault, and the command will be ignored.

This command has one data byte.

MFR_RESET

This command provides a means to reset the LTM4682 from the serial bus. This forces the LTM4682 to turn off both PWM channels, load the operating memory from internal EEPROM, clear all faults and then perform a soft-start of both PWM channels if enabled.

This write-only command has no data bytes.

PMBus COMMAND DETAILS

PWM CONFIGURATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_PWM_COMP	0xD3	PWM loop compensation configuration.	R/W Byte	Y	Reg		Y	0x76
MFR_PWM_MODE	0xD4	Configuration for the PWM engine.	R/W Byte	Y	Reg		Y	0xC7
MFR_PWM_CONFIG	0xF5	Set numerous parameters for the DC/DC controller, including phasing.	R/W Byte	N	Reg		Y	0x10
FREQUENCY_SWITCH	0x33	Switching frequency of the controller.	R/W Word	N	L11	kHz	Y	575 0x023F

MFR_PWM_MODE

The MFR_PWM_MODE command sets important PWM controls for each channel.

The MFR_PWM_MODE command allows the user to program the PWM controller to use discontinuous (pulse-skipping mode), or forced continuous conduction mode.

BIT	MEANING
7	Use a high range of I_{LIMIT}.
0b	Low current range.
1b	High current range.
6	Enable servo mode
5	External temperature sense:
	0: ΔV_{BE} measurement.
	Now reserved, ΔV_{BE} only supported.
4	Page 0 Only: Use of TSNS1a-Sensed Temperature Telemetry.
	0 – Temperature sensed through TSNS1a is used to temperature-correct the current-sense information digitized by Channel 1's current-sense input, ISNS1a+/ISNS1a–.
	1 – Temperature sensed through TSNS0a is used to temperature-correct the current-sense information digitized by Channel 1's current-sense input, ISNS1a+/ISNS1a–. Telemetry obtained from the thermal sensor connected to TSNS1a can be external to the module, if desired.
3	Reserved
2	Reserved
1	V_{OUT} range.
1b	The maximum output voltage is 2.75V.
0b	The maximum output voltage is 3.6V, which is not needed.
Bit[0]	Mode.
0b	Discontinuous.
1b	Forced continuous.

Bit [7] of this command determines if the part is in a high range or low range of the IOUT_OC_FAULT_LIMIT command. Changing this bit value changes the PWM loop gain and compensation. This bit value should not be changed when the channel output is active. Writing this bit when the channel is active will generate a CML fault.

Bit [6] The LTM4682 will not servo while the part is OFF, ramping on or ramping off. When set to one, the output servo is enabled. The output set point DAC will be slowly adjusted to minimize the difference between the READ_VOUT_ADC and the VOUT_COMMAND (or the appropriate margined value).

The LTM4682 computes temperature in °C from ΔV_{BE} measured by the ADC at the TSNS*n* pin as

$$T = (G \bullet \Delta V_{BE} \bullet q/(K \bullet \ln(16))) - 273.15 + O$$

PMBus COMMAND DETAILS

For both equations,

G = MFR_TEMP_1_GAIN • 2^{-14}, and

O = MFR_TEMP_1_OFFSET

Bit[1] of this command determines if the part is in a high range or low voltage range. Changing this bit value changes the PWM loop gain and compensation. This bit value should not be changed when the channel output is active. Writing this bit when the channel is active will generate a CML fault.

Bit[0] determines if the PWM mode of operation is discontinuous (pulse-skipping mode), or forced continuous conduction mode. Whenever the channel is ramping on, the PWM mode will be discontinuous, regardless of the value of this bit. This command has one data byte.

MFR_PWM_COMP

The MFR_PWM_COMP command sets the g_m of the PWM channel error amplifiers and the value of the internal R_{ITHn} compensation resistors. This command affects the loop gain of the PWM output, which may require modifications to the external compensation network.

BIT	MEANING
BIT [7:5]	**Error Amplifier GM Adjust (mS)**
000b	1.00
001b	1.68
010b	2.35
011b	3.02
100b	3.69
101b	4.36
110b	5.04
111b	5.76
BIT [4:0]	**R_{COMP} (kΩ)**
00000b	0
00001b	0.25
00010b	0.5
00011b	0.75
00100b	1
00101b	1.25
00110b	1.5
00111b	1.75
01000b	2
01001b	2.5
01010b	3
01011b	3.5
01100b	4
01101b	4.5
01110b	5
01111b	5.5
10000b	6

PMBus COMMAND DETAILS

BIT	MEANING
10001b	7
10010b	8
10011b	9
10100b	11
10101b	13
10110b	15
10111b	17
11000b	20
11001b	24
11010b	28
11011b	32
11100b	38
11101b	46
11110b	54
11111b	62

This command has one data byte.

MFR_PWM_CONFIG

The MFR_PWM_CONFIG command sets the switching frequency phase offset to the falling edge of the SYNC signal. The part must be in the OFF state to process this command. Either the RUN pins must be low, or the channels must be commanded off. If either channel is in the RUN state and this command is written, the command will be NACK'd, and a BUSY fault will be asserted.

BIT	MEANING	
7	Reserved	
[6:5]	Input current sense gain.	
00b	2x gain. 0mV to 50mV range.	
01b	4x gain. 0mV to 25mV range.	
10b	8x gain. 0mV to 10mV range.	
11b	Reserved	
4	Share Clock Enable: If this bit is 1, the SHARE_CLK pin will not be released until V_{IN} > VIN_ON. The SHARE_CLK pin will be pulled low when V_{IN} < VIN_OFF. If this bit is 0, the SHARE_CLK pin will not be pulled low when VIN < VIN_OFF except for the initial application of VIN.	
3	Reserved	
BIT [2:0]	**CHANNEL 0 (DEGREES)**	**CHANNEL 1 (DEGREES)**
000b	0	180
001b	90	270
010b	0	240
011b	0	120
100b	120	240
101b	60	240
110b	120	300

PMBus COMMAND DETAILS

FREQUENCY_SWITCH

The FREQUENCY_SWITCH command sets the switching frequency, in kHz, of the LTM4682.

Supported Frequencies:

VALUE [15:0]	RESULTING FREQUENCY (TYP)
0x0000	External oscillator
0xF3E8	250kHz
0xFABC	350kHz
0xFB52	425kHz
0xFBE8	500kHz
0x023F	575kHz
0x028A	650kHz
0x02EE	750kHz
0x03E8	1000kHz

The part must be in the OFF state to process this command. The RUN pin must be low, or both channels must be commanded off. If the part is in a RUN state and this command is written, the command will be NACK'd, and a BUSY fault will be asserted. When the part is commanded off, and the frequency is changed, a PLL_UNLOCK status may be detected as the PLL locks onto the new frequency.

This command has two data bytes and is formatted in Linear_5s_11s format.

VOLTAGE

Input Voltage and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VIN_OV_FAULT_LIMIT	0x55	Input supply overvoltage fault limit.	R/W Word	N	L11	V	Y	16.8 0xDA1A
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	N	L11	V	Y	4.65 0xD12A
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	N	L11	V	Y	4.75 0xD130
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	N	L11	V	Y	4.5 0xD120
MFR_ICHIP_CAL_GAIN	0xF7	The resistance value of the V_{IN} pin filter element in mΩ.	R/W Word	N	L11	mΩ	Y	1000 0x03E8

VIN_OV_FAULT_LIMIT

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured by the ADC, in volts, that causes an input overvoltage fault.

This command has two data bytes in Linear_5s_11s format.

PMBus COMMAND DETAILS

VIN_UV_WARN_LIMIT

The VIN_UV_WARN_LIMIT command sets the value of input voltage measured by the ADC that causes an input undervoltage warning. This warning is disabled until the input exceeds the input startup threshold value set by the VIN_ON command and the unit has been enabled. If the V_{IN} Voltage drops below the VIN_UV_WARN_LIMIT, the device:

- Sets the INPUT bit in the STATUS_WORD
- Sets the V_{IN} undervoltage warning bit in the STATUS_INPUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$, unless masked

VIN_ON

The VIN_ON command sets the input voltage, in Volts, at which the unit starts power conversion.

This command has two data bytes and is formatted in Linear_5s_11s format.

VIN_OFF

The VIN_OFF command sets the input voltage, in Volts, at which the unit stops power conversion.

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_ICHIP_CAL_GAIN

The MFR_ICHIP_CAL_GAIN command is used to set the resistance value of the V_{IN} pin filter element in milliohms. (See also READ_VIN). Set MFR_RVIN equal to 0 if no filter element is used.

This command has two data bytes and is formatted in Linear_5s_11s format.

Output Voltage and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VOUT_MODE	0x20	The output voltage format and exponent (2^{-12}).	R Byte	Y	Reg			2^{-12} 0x14
VOUT_MAX	0x24	The upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	1.5V 0x1800
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	0.85 0x0D9A
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	0.825 0x0D33
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point. It must be greater than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.80 0x0CCD
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	L16	V	Y	0.75 0x0C00
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point. It must be less than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.70 0x0B33
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.675 0x0ACD
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	L16	V	Y	0.65 0x0A66
MFR_VOUT_MAX	0xA5	Maximum allowed output voltage.	R Word	Y	L16	V		1.5 0x1800

PMBus COMMAND DETAILS

VOUT_MODE

The data byte for the VOUT_MODE command, used for commanding and reading output voltage, consists of a 3-bit mode (only linear format is supported) and a 5-bit parameter representing the exponent used in output voltage Read/Write commands.

This read-only command has one data byte.

VOUT_MAX

The VOUT_MAX command sets an upper limit on any voltage, including VOUT_MARGIN_HIGH. The unit can command regardless of any other commands or combinations. The maximum allowed value of this command is 1.5V. The maximum output voltage the LTM4682 can produce is 1.35V, including VOUT_MARGIN_HIGH. However, the VOUT_OV_FAULT_LIMIT can be commanded as high as 1.5V.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_OV_FAULT_LIMIT

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage measured by the OV supervisor comparator at the sense pins, in volts, which causes an output overvoltage fault.

If the VOUT_OV_FAULT_LIMIT is modified and the part is in the RUN state, allow 10ms after the command is modified to ensure the new value is being honored. The part indicates if it is busy making a calculation. Monitor bits 5 and 6 of MFR_COMMON. Either bit is low if the part is busy. If this wait time is not honored and the VOUT_COMMAND is modified above the old overvoltage limit, an OV condition might temporarily be detected, resulting in undesirable behavior and possible damage to the switcher.

If the VOUT_OV_FAULT_RESPONSE is set to OV_PULLDOWN or 0x00, the $\overline{\text{FAULT}}$ pin will not assert if the VOUT_OV_FAULT is propagated. The LTM4682 will pull the TG low and assert the BG bit when the overvoltage condition is detected.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_OV_WARN_LIMIT

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage measured by the ADC at the sense pins, in volts, which causes an output voltage high warning. The MFR_VOUT_PEAK value can be used to determine if this limit has been exceeded.

In response to the VOUT_OV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the V_{OUT} bit in the STATUS_WORD
- Sets the V_{OUT} overvoltage warning bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This condition is detected by the ADC, so that the response time may be up to $t_{CONVERT}$.

PMBus COMMAND DETAILS

This command has two data bytes and is formatted in Linear_16u format.

VOUT_MARGIN_HIGH

The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed, in Volts, when the OPERATION command is set to Margin High. The value should be greater than VOUT_COMMAND. The maximum guaranteed value on VOUT_MARGIN_HIGH is 1.5V.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_COMMAND

The VOUT_COMMAND consists of two bytes and is used to set the output voltage, in volts. The maximum guaranteed value on VOUT is 1.5V.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_MARGIN_LOW

The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed, in volts, when the OPERATION command is set to Margin Low. The value must be less than VOUT_COMMAND.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_UV_WARN_LIMIT

The VOUT_UV_WARN_LIMIT command reads the value of the output voltage measured by the ADC at the sense pins, in volts, which causes an output voltage low warning.

In response to the VOUT_UV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the V_{OUT} bit in the STATUS_WORD
- Sets the V_{OUT} undervoltage warning bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has two data bytes and is formatted in Linear_16u format.

VOUT_UV_FAULT_LIMIT

The VOUT_UV_FAULT_LIMIT command reads the value of the output voltage measured by the UV supervisor comparator at the sense pins, in volts, which causes an output undervoltage fault.

This command has two data bytes and is formatted in Linear_16u format.

PMBus COMMAND DETAILS

MFR_VOUT_MAX

The MFR_VOUT_MAX command is the maximum output voltage in volts for each channel, including VOUT_OV_FAULT_LIMIT. If the output voltages are set to a high range (Bit 1 of MFR_PWM_MODE set to 0) MFR_VOUT_MAX is 3.6V. The (Bit 6 of MFR_PWM_CONFIG set to a 0), MFR_VOUT_MAX is 3.6V is not used since the outputs are limited to 1.5V. If the output voltage is set to a low range (Bit 1 of MFR_PWM_MODE set to a 1), the MFR_VOUT_MAX is 2.75V. Entering a VOUT_COMMAND value greater than this will result in a CML fault, and the output voltage setting will be clamped to the maximum level. This will also result in Bit 3 VOUT_MAX_Warning in the STATUS_VOUT command being set.

This read only command has 2 data bytes and is formatted in Linear_16u format.

OUTPUT CURRENT AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_IOUT_CAL_GAIN	0xDA	The ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the resistance value in mΩ.	R Word	Y	L11	mΩ	Factory Only NVM	0.360 0xD017
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient of the current sensing element.	R/W Word	Y	CF		Y	3900 0x0F3C
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	42.0 0xE940
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	35.0 0xE918

MFR_IOUT_CAL_GAIN

The MFR_IOUT_CAL_GAIN command sets the resistance value of the current sense resistor in milliohms. (see also MFR_IOUT_CAL_GAIN_TC).

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_IOUT_CAL_GAIN_TC

The MFR_IOUT_CAL_GAIN_TC command is used to program the temperature coefficient of the IOUT_CAL_GAIN sense resistor or inductor DCR in ppm/°C in manufacturing.

This command has two data bytes and is formatted in 16-bit 2's complement integer ppm. N = –32768 to 32767 • 10^{-6}. The nominal temperature is 27°C. The IOUT_CAL_GAIN is multiplied by:

[1.0 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERATURE_1-27)].

DCR sensing will have a typical value of 3900.

The IOUT_CAL_GAIN and MFR_IOUT_CAL_GAIN_TC impact all current parameters, including: READ_IOUT, MFR_IOUT_PEAK, IOUT_OC_FAULT_LIMIT, and IOUT_OC_WARN_LIMIT.

PMBus COMMAND DETAILS

IOUT_OC_FAULT_LIMIT

The IOUT_OC_FAULT_LIMIT command sets the value of the peak output current limit, in Amperes. When the controller is in the current limit, the overcurrent detector will indicate an overcurrent fault condition. The following table lists the programmable peak output current limit value in mV between I_{SENSE}^+ and I_{SENSE}^-. The actual value of the current limit is ($I_{SENSE}^+ – I_{SENSE}^-$)/IOUT_CAL_GAIN in Amperes.

BASED ON PEAK-TO-PEAK INDUCTOR CURRENT = 50% OF 30A FOR WORSE CASE, THESE ARE APPROXIMATES, SO USE GUARDBAND AND CHECK

MFR_PWM_MODE[7] = 1 HIGH CURRENT RANGE (mV)	~I_L PEAK (A)	~I_{OUT} (A)	MFR_PWM_MODE[7] = 0 LOW CURRENT RANGE (mV)	~ I_L PEAK (A)	~ I_{OUT} (A)
17.73	49.25	41.75	9.85	27.36	19.86
18.86	52.38	44.88	10.48	29.11	21.61
20.42	NA	NA	11.34	31.5	24
21.14	NA	NA	11.74	32.61	25.11
22.27	NA	NA	12.37	34.36	26.86
23.41	NA	NA	13.01	36.13	28.63
24.55	NA	NA	13.64	37.88	30.38

Note: This is the peak of the current waveform. The READ_IOUT command returns the average current. The peak output current limits are adjusted with temperature based on the MFR_IOUT_CAL_GAIN_TC using the equation:

Peak Current Limit = IOUT_CAL_GAIN • (1 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERTURE_1-27.0)).

The LTM4682 automatically converts currents to the appropriate internal bit value.

The I_{OUT} range is set with bit 7 of the MFR_PWM_MODE command.

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

If the IOUT_OC_FAULT_LIMIT is exceeded, the device:

- Sets the I_{OUT} bit in the STATUS word
- Sets the I_{OUT} Overcurrent fault bit in the STATUS_IOUT
- Notifies the host by asserting $\overline{\text{ALERT}}$, unless masked

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

IOUT_OC_WARN_LIMIT

This command sets the value of the output current measured by the ADC that causes an output overcurrent warning in Amperes. The READ_IOUT value will be used to determine if this limit has been exceeded.

In response to the IOUT_OC_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the I_{OUT} bit in the STATUS_WORD
- Sets the I_{OUT} Overcurrent Warning bit in the STATUS_IOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

This command has two data bytes and is formatted in Linear_5s_11s format.

Input Current and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_IIN_CAL_GAIN	0xE8	The resistance value of the input current sense element in mΩ.	R/W Word	L11	mΩ	Y	1.000 0x03E8

MFR_IIN_CAL_GAIN

The MFR_IIN_CAL_GAIN command sets the resistance value of the input current sense resistor in milliohms. (see also READ_IIN).

This command has two data bytes and is formatted in Linear_5s_11s format.

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IIN_OC_WARN_LIMIT	0x5D	Input overcurrent warning limit.	R/W Word	N	L11	A	Y	10.0 0xD280

IIN_OC_WARN_LIMIT

The IIN_OC_WARN_LIMIT command sets the value of the input current measured by the ADC, in amperes, which causes a warning indicating the input current is high. The READ_IIN value will be used to determine if this limit has been exceeded.

In response to the IIN_OC_WARN_LIMIT being exceeded, the device:

- Sets the OTHER bit in the STATUS_BYTE
- Sets the INPUT bit in the upper byte of the STATUS_WORD
- Sets the I_{IN} Overcurrent Warning bit[1] in the STATUS_INPUT command
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

TEMPERATURE

Power Stage DCR Temperature Calibration

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_TEMP_1_GAIN	0xF8	Sets the slope of the external temperature sensor.	R/W Word	Y	CF		Y	0.995 0x3FAE
MFR_TEMP_1_OFFSET	0xF9	Sets the offset of the external temperature sensor.	R/W Word	Y	L11	C	Y	0.0 0x8000

MFR_TEMP_1_GAIN

The MFR_TEMP_1_GAIN command will modify the slope of the power stage sensor to account for non-idealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in 16-bit 2's complement integer. The effective gain adjustment is $N \bullet 2^{-14}$. The nominal value is 1. N = 8192 to 32767

MFR_TEMP_1_OFFSET

The MFR_TEMP_1_OFFSET command will modify the offset of the power stage temperature sensor to account for non-idealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in Linear_5s_11s format. The part starts the calibration with a –273.15, so the default adjustment is zero.

Power Stage Temperature Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
OT_FAULT_LIMIT	0x4F	Power stage overtemperature fault limit.	R/W Word	Y	L11	C	Y	128.0 0xF200
OT_WARN_LIMIT	0x51	Power stage overtemperature warning limit.	R/W Word	Y	L11	C	Y	125.0 0xEBE8
UT_FAULT_LIMIT	0x53	Power stage undertemperature fault limit.	R/W Word	Y	L11	C	Y	–45.0 0xE530

OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the value of the power stage temperature measured by the ADC, in degrees Celsius, which causes an overtemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

This command has two data bytes and is formatted in Linear_5s_11s format.

OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the value of the power stage temperature measured by the ADC, in degrees Celsius, which causes an overtemperature warning. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

PMBus COMMAND DETAILS

In response to the OT_WARN_LIMIT being exceeded, the device:

• Sets the TEMPERATURE bit in the STATUS_BYTE

• Sets the Overtemperature Warning bit in the STATUS_TEMPERATURE command, and

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has two data bytes and is formatted in Linear_5s_11s format.

UT_FAULT_LIMIT

The UT_FAULT_LIMIT command sets the value of the power stage temperature measured by the ADC, in degrees Celsius, which causes an undertemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

Note: If the temperature sensors are not installed, the UT_FAULT_LIMIT can be set to –275°C and the UT_FAULT_LIMIT response set to ignore to avoid $\overline{\text{ALERT}}$ being asserted.

This command has two data bytes and is formatted in Linear_5s_11s format.

TIMING

Timing—On Sequence/Ramp

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	L11	ms	Y	0.0 0x8000
TON_RISE	0x61	Time from when the output rises until the output voltage reaches the V_{OUT} commanded value.	R/W Word	Y	L11	ms	Y	3.0 0xC300
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for VOUT to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	L11	ms	Y	5.0 0xCA80
VOUT_TRANSITION_RATE	0x27	Rate the output changes when V_{OUT} is commanded to a new value.	R/W Word	Y	L11	V/ms	Y	0.25 0xD010

TON_DELAY

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received until the output voltage rises. Values from 0ms to 83 seconds are valid. The resulting turn-on delay will have a typical delay of 270µs for TON_DELAY = 0 and an uncertainty of ±50µs for all values of TON_DELAY.

This command has two data bytes and is formatted in Linear_5s_11s format.

TON_RISE

The TON_RISE command sets the time, in milliseconds, from the time the output starts to rise to the time the output enters the regulation band. Values from 0 to 1.3 seconds are valid. The part will be in discontinuous mode during TON_RISE events. If TON_RISE is less than 0.25ms, the LTM4682 digital slope will be bypassed, and the output voltage transition will only be controlled by the analog performance of the PWM switcher. The number of steps in TON_RISE is equal to TON_RISE (in ms)/0.1ms with an uncertainty of ±0.1ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

TON_MAX_FAULT_LIMIT

The TON_MAX_FAULT_LIMIT command sets the value, in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit.

A data value of 0ms means there is no limit, and the unit can attempt to bring up the output voltage indefinitely. The maximum limit is 83 seconds.

This command has two data bytes and is formatted in Linear_5s_11s format.

VOUT_TRANSITION_RATE

When a PMBus device receives either a VOUT_COMMAND or OPERATION (Margin High, Margin Low) that causes the output voltage to change, this command sets the rate in V/ms at which the output voltage changes. The commanded rate of change does not apply when the unit is commanded on or off. The maximum allowed slope is 4V/ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

Timing—Off Sequence/Ramp

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	L11	ms	Y	0.0 0x8000
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	L11	ms	Y	3.0 0xC300
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL is completed, for the unit to decay below 12.5%.	R/W Word	Y	L11	ms	Y	0 0x8000

TOFF_DELAY

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received until the output voltage starts to fall. Values from 0 to 83 seconds are valid. The resulting turn-off delay will have a typical delay of 270µs for TOFF_DELAY = 0 and an uncertainty of ±50µs for all values of TOFF_DELAY. TOFF_DELAY is not applied when a fault event occurs

This command has two data bytes and is formatted in Linear_5s_11s format.

TOFF_FALL

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-off delay time until the output voltage is commanded to zero. It is the ramp time of the V_{OUT} DAC. When the V_{OUT} DAC is zero, the PWM output will be set to a high impedance state.

The part will maintain the mode of operation programmed. For defined TOFF_FALL times, the user should set the part to continuous conduction mode. Loading the max value indicates that the part will ramp down at the slowest possible rate. The minimum supported fall time is 0.25ms. A value less than 0.25ms will result in a 0.25ms ramp. The maximum fall time is 1.3 seconds. The number of steps in TOFF_FALL is equal to TOFF_FALL (in ms)/0.1ms with an uncertainty of ±0.1ms.

In discontinuous conduction mode, the controller will not draw current from the load, and the fall time will be set by the output capacitance and load current.

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

TOFF_MAX_WARN_LIMIT

The TOFF_MAX_WARN_LIMIT command sets the value, in milliseconds, on how long the output voltage exceeds 12.5% of the programmed voltage before a warning is asserted. The output is considered off when the V_{OUT} voltage is less than 12.5% of the programmed VOUT_COMMAND value. The calculation begins after TOFF_FALL is complete.

A data value of 0ms means there is no limit, and the output voltage exceeds 12.5% of the programmed voltage indefinitely. Other than 0, values from 120ms to 524 seconds are valid.

This command has two data bytes and is formatted in Linear_5s_11s format.

Precondition for Restart

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_RESTART_DELAY	0xDC	Minimum time the RUN pin is held low by the LTM4682.	R/W Word	Y	L11	ms	Y	150 0xF258

MFR_RESTART_DELAY

This command specifies the minimum RUN off time in milliseconds. This device will pull the RUN pin low for this length of time once a falling edge of RUN has been detected. The minimum recommended value is 136ms.

Note: The restart delay is different from the retry delay. The restart delay pulls RUN low for the specified time, after which a standard start-up sequence is initiated. The minimum restart delay should be equal to TOFF_DELAY + TOFF_FALL + 136ms. Valid values are from 136ms to 65.52 seconds in 16ms increments. To ensure a minimum off time, set the MFR_RESTART_DELAY 16ms longer than the desired time. The output rail can be off longer than the MFR_RESTART_DELAY after the RUN pin is pulled high if the output decay bit 0 is enabled in MFR_CHAN_CONFIG and the output takes a long time to decay below 12.5% of the programmed value.

This command has two data bytes and is formatted in Linear_5s_11s format.

FAULT RESPONSE

Fault Responses All Faults

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	Y	L11	ms	Y	250 0xF3E8

MFR_RETRY_DELAY

This command sets the time in milliseconds between retries if the fault response is to retry the controller at specified intervals. This command value is used for all fault responses that require retry. The retry time starts once the fault has been detected by the offending channel. Valid values are from 120ms to 83.88 seconds in 10µs increments.

Note: The retry delay time is determined by the length of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG.

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

Fault Responses Input Voltage

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VIN_OV_FAULT_RESPONSE	0x56	Action is to be taken by the device when an input supply overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80

VIN_OV_FAULT_RESPONSE

The VIN_OV_FAULT_RESPONSE command instructs the device on what action is to be taken in response to an input overvoltage fault. The data byte is in the format given in Table 21.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD
- Sets the V_{IN} overvoltage fault bit in the STATUS_INPUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

Fault Responses Output Voltage

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VOUT_OV_FAULT_RESPONSE	0x41	Action is to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
VOUT_UV_FAULT_RESPONSE	0x45	Action is to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
TON_MAX_FAULT_RESPONSE	0x63	Action is to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8

VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action is to be taken in response to an output overvoltage fault. The data byte is in the format as shown in Table 17.

The device also:

- Sets the VOUT_OV bit in the STATUS_BYTE
- Sets the V_{OUT} bit in the STATUS_WORD
- Sets the V_{OUT} overvoltage fault bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

The only values recognized for this command are:

0x00 Part performs OV pull down only, or OV_PULLDOWN.

0x80 The device shuts down (disables the output), and the unit does not attempt to retry. (PMBus, Part II, Section 10.7).

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0xB8 The device shuts down (disables the output), and the device attempts to retry continuously, without limitation, until it is commanded OFF (by the RUN pin, or OPERATION command, or both), bias power is removed, or another fault condition causes the unit to shut down.

0x4*n* The device shuts down, and the unit does not attempt to retry. The output remains disabled until the part is commanded OFF, then ON, or the RUN pin is asserted low, then high or RESET through the command or removal of VIN. The OV fault must remain active for a period of n • 10µs, where n is a value from 0 to 7.

0x78*n* The device shuts down, and the unit attempts to retry continuously until either the fault condition is cleared or the part is commanded OFF, then ON, or the RUN pin is asserted low, then high or RESET through the command or removal of VIN. The OV fault must remain active for a period of n • 10µs, where n is a value from 0 to 7.

Any other value will result in a CML fault, and the write will be ignored.

This command has one data byte.

Table 17. VOUT_OV_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4682: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTM4682.	00	Part performs OV pull down only or OV_PULLDOWN (i.e., turns off the top MOSFET and turns on lower MOSFET while V_{OUT} is > VOUT_OV_FAULT).
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000-111	The delay time is in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. It is only valid for the deglitched off state.

VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action is to be taken in response to an output undervoltage fault. The data byte is in the format as shown in Table 18.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the V_{OUT} bit in the STATUS_WORD
- Sets the V_{OUT} undervoltage fault bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

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The UV fault and warn are masked until the following criteria are achieved:

1) The TON_MAX_FAULT_LIMIT has been reached
2) The TON_DELAY sequence has been completed
3) The TON_RISE sequence has been completed
4) The VOUT_UV_FAULT_LIMIT threshold has been reached
5) The IOUT_OC_FAULT_LIMIT is not present

The UV fault and warn are masked whenever the channel is not active.

The UV fault and warn are masked during TON_RISE and TOFF_FALL sequencing.

This command has one data byte.

Table 18. VOUT_UV_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4682: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • The device receives a RESTORE_USER_ALL command. • The device receives a MFR_RESET command. • The device supply power is cycled.	00	The PMBus device continues operation without interruption. (Ignores the fault functionally).
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
		10	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000-111	The delay time is in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. It is only valid for the deglitched off state.

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TON_MAX_FAULT_RESPONSE

The TON_MAX_FAULT_RESPONSE command instructs the device on what action is to be taken in response to a TON_MAX fault. The data byte is in the format as shown in Table 21.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the V_{OUT} bit in the STATUS_WORD
- Sets the TON_MAX_FAULT bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

A value of 0 disables the TON_MAX_FAULT_RESPONSE. It is not recommended to use 0.

Note: The PWM channel remains in discontinues mode until the TON_MAX_FAULT_LIMIT has been exceeded.

This command has one data byte.

Fault Responses Output Current

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IOUT_OC_FAULT_RESPONSE	0x47	Action is to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00

IOUT_OC_FAULT_RESPONSE

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action is to be taken in response to an output overcurrent fault. The data byte is in the format given in Table 19.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the IOUT_OC bit in the STATUS_BYTE
- Sets the I_{OUT} bit in the STATUS_WORD
- Sets the I_{OUT} Overcurrent Fault bit in the STATUS_IOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

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Table 19. IOUT_OC_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4682: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • The device receives a RESTORE_USER_ALL command. • The device receives a MFR_RESET command. • The device supply power is cycled.	00	The LTM4682 continues to operate indefinitely while maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage (known as constant-current or brick-wall limiting).
		01	Not supported.
		10	The LTM4682 continues to operate, maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage, for the delay time set by bits [2:0]. If the device is still operating in the current limit at the end of the delay time, the device responds as programmed by the Retry Setting in bits [5:3].
		11	The LTM4682 shuts down immediately and responds as programmed by the Retry Setting in bits [5:3].
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared by cycling the RUN pin or removing bias power.
		111	The device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000-111	The number of delay time units in 16ms increments. This delay time is used to determine the amount of time a unit is to continue operating after a fault is detected before shutting down. It is only valid for the deglitched off response.

Fault Responses IC Temperature

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_OT_FAULT_RESPONSE	0xD6	Action is to be taken by the device when an internal overtemperature fault is detected.	R Byte	N	Reg			0xC0

MFR_OT_FAULT_RESPONSE

The MFR_OT_FAULT_RESPONSE command byte instructs the device on what action should be taken in response to an internal overtemperature fault. The data byte is in the format given in Table 20.

The LTM4682 also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the MFR bit in the STATUS_WORD
- Sets the overtemperature fault bit in the STATUS_MFR_SPECIFIC command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

PMBus COMMAND DETAILS

This command has one data byte.

Table 20. Data Byte Contents MFR_OT_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTM4682: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTM4682.	00	Not supported. Writing this value will generate a CML fault.
		01	Not supported. Writing this value will generate a CML fault.
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	The device's output is disabled while the fault is present. Operation resumes, and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared.
		001-111	Not supported. Writing this value will generate a CML fault.
2:0	Delay Time	XXX	Not supported. Value ignored.

Fault Responses External Temperature

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
OT_FAULT_RESPONSE	0x50	Action is to be taken by the device when an external overtemperature fault is detected,	R/W Byte	Y	Reg		Y	0xB8
UT_FAULT_RESPONSE	0x54	Action is to be taken by the device when an external undertemperature fault is detected.	R/W Byte	Y	Reg		Y	0xB8

OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE command instructs the device on what action is to be taken in response to an external overtemperature fault on the external temperature sensors. The data byte is in the format given in Table 21.

The device also:

• Sets the TEMPERATURE bit in the STATUS_BYTE

• Sets the overtemperature fault bit in the STATUS_TEMPERATURE command

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

UT_FAULT_RESPONSE

The UT_FAULT_RESPONSE command instructs the device on what action is to be taken in response to an external undertemperature fault on the external temp sensors. The data byte is in the format given in Table 15.

The device also:

• Sets the TEMPERATURE bit in the STATUS_BYTE

• Sets the undertemperature fault bit in the STATUS_TEMPERATURE command

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• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This condition is detected by the ADC so that the response time may be up to $t_{CONVERT}$.

This command has one data byte.

Table 21. Data Byte Contents: TON_MAX_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE, OT_FAULT_RESPONSE, UT_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response	00	The PMBus device continues operation without interruption.
	For all values of bits [7:6], the LTM4682: • Sets the corresponding fault bit in the status commands, and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked.	01	Not supported. Writing this value will generate a CML fault.
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
	The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • The device receives a RESTORE_USER_ALL command. • The device receives a MFR_RESET command. • The device supply power is cycled.	11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin, or OPERATION command, or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	XXX	Not supported. Values ignored.

FAULT SHARING

Fault Sharing Propagation

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_FAULT_PROPAGATE	0xD2	Configuration that determines which faults are propagated to the FAULT pins.	R/W Word	Y	Reg		Y	0x6993

MFR_FAULT_PROPAGATE

The MFR_FAULT_PROPAGATE command enables the faults that can cause the $\overline{\text{FAULT}}$*n* pin to assert low. The command is formatted as shown in Table 22. Faults can only be propagated to the $\overline{\text{FAULT}}$*n* pin if they are programmed to respond to faults.

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This command has two data bytes.

Table 22. $\overline{\text{FAULT}}n$ Propagate Fault Configuration

The $\overline{\text{FAULT0}}$ and $\overline{\text{FAULT1}}$ pins are designed to provide electrical notification of selected events to the user. Some of these events are common to both output channels. Others are specific to an output channel. They can also be used to share faults between channels.

BIT(S)	SYMBOL	OPERATION
B[15]	VOUT disabled while not decayed.	This is used in a PolyPhase configuration when bit 0 of the MFR_CHAN_CONFIG_LTM4682 is zero. If the channel is turned off, by toggling the RUN pin, or commanding the part OFF, and then the RUN is reasserted, or the part is commanded back on before the output has decayed, VOUT will not restart until the 12.5% decay is honored. The $\overline{\text{FAULT}}$ pin is asserted during this condition if bit 15 is asserted.
B[14]	Mfr_fault_propagate_short_CMD_cycle	0: No action. 1: Asserts low if commanded off then on before the output has sequenced off. Re-asserts high $t_{OFF(MIN)}$ after sequence off.
b[13]	Mfr_fault_propagate_ton_max_fault	0: No action if a TON_MAX_FAULT fault is asserted. 1: Associated output will be asserted low if a TON_MAX_FAULT fault is asserted. $\overline{\text{FAULT0}}$ is associated with page 0 TON_MAX_FAULT faults. $\overline{\text{FAULT1}}$ is associated with page 1 TON_MAX_FAULT faults.
b[12]	Reserved	
b[11]	Mfr_fault0_propagate_int_ot, Mfr_fault1_propagate_int_ot	0: No action if the MFR_OT_FAULT_LIMIT fault is asserted. 1: Associated output will be asserted low if the MFR_OT_FAULT_LIMIT fault is asserted.
b[10]	Reserved	
b[9]	Reserved	
b[8]	Mfr_fault0_propagate_ut, Mfr_fault1_propagate_ut	0: No action if the UT_FAULT_LIMIT fault is asserted. 1: Associated output will be asserted low if the UT_FAULT_LIMIT fault is asserted. $\overline{\text{FAULT0}}$ is associated with page 0 UT faults. $\overline{\text{FAULT1}}$ is associated with page 1 UT faults.
b[7]	Mfr_fault0_propagate_ot, Mfr_fault1_propagate_ot	0: No action if the OT_FAULT_LIMIT fault is asserted. 1: Associated output will be asserted low if the OT_FAULT_LIMIT fault is asserted. $\overline{\text{FAULT0}}$ is associated with page 0 OT faults. $\overline{\text{FAULT1}}$ is associated with page 1 OT faults.
b[6]	Reserved	
b[5]	Reserved	
b[4]	Mfr_fault0_propagate_input_ov, Mfr_fault1_propagate_input_ov	0: No action if the VIN_OV_FAULT_LIMIT fault is asserted. 1: Associated output will be asserted low if the VIN_OV_FAULT_LIMIT fault is asserted.
b[3]	Reserved	
b[2]	Mfr_fault0_propagate_iout_oc, Mfr_fault1_propagate_iout_oc	0: No action if the IOUT_OC_FAULT_LIMIT fault is asserted. 1: Associated output will be asserted low if the IOUT_OC_FAULT_LIMIT fault is asserted. $\overline{\text{FAULT0}}$ is associated with page 0 OC faults. $\overline{\text{FAULT1}}$ is associated with page 1 OC faults.
b[1]	Mfr_fault0_propagate_vout_uv, Mfr_fault1_propagate_vout_uv	0: No action if the VOUT_UV_FAULT_LIMIT fault is asserted. 1: Associated output will be asserted low if the VOUT_UV_FAULT_LIMIT fault is asserted. $\overline{\text{FAULT0}}$ is associated with page 0 UV faults. $\overline{\text{FAULT1}}$ is associated with page 1 UV faults.
b[0]	Mfr_fault0_propagate_vout_ov, Mfr_fault1_propagate_vout_ov	0: No action if the VOUT_OV_FAULT_LIMIT fault is asserted. 1: Associated output will be asserted low if the VOUT_OV_FAULT_LIMIT fault is asserted. $\overline{\text{FAULT0}}$ is associated with page 0 OV faults. $\overline{\text{FAULT1}}$ is associated with page 1 OV faults.

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Fault Sharing Response

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_FAULT_RESPONSE	0xD5	Action is to be taken by the device when the FAULT pin is asserted low.	R/W Byte	Y	Reg		Y	0xC0

MFR_FAULT_RESPONSE

The MFR_FAULT_RESPONSE command instructs the device on what action is to be taken in response to the $\overline{\text{FAULT}}n$ pin being pulled low by an external source.

Supported Values:

VALUE	MEANING
0xC0	FAULT_INHIBIT. The LTM4682 will three-state the output in response to the $\overline{\text{FAULT}}$ pin pulled low.
0x00	FAULT_IGNORE. The LTM4682 continues operation without interruption.

The device also:

- Sets the MFR bit in the STATUS_WORD
- Sets bit 0 in the STATUS_MFR_SPECIFIC command to indicate $\overline{\text{FAULT}}n$ is being pulled low
- Notifies the host by asserting $\overline{\text{ALERT}}$, unless masked

This command has one data byte.

SCRATCHPAD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
USER_DATA_00	0xB0	OEM reserved. Typically used for part serialization.	R/W Word	N	Reg		Y	NA
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA
USER_DATA_02	0xB2	OEM reserved. Typically used for part serialization.	R/W Word	N	Reg		Y	NA
USER_DATA_03	0xB3	A NVM word available for the user.	R/W Word	Y	Reg		Y	0x0000
USER_DATA_04	0xB4	A NVM word available for the user.	R/W Word	N	Reg		Y	0x0000

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USER_DATA_00 through USER_DATA_04

These commands are nonvolatile memory locations for customer storage. The customer has the option to write any value to the USER_DATA_nn at any time. However, the LTpowerPlay software and contract manufacturers use some of these commands for inventory control. Modifying the reserved USER_DATA_nn commands may lead to undesirable inventory control and incompatibility with these products.

These commands have 2 data bytes and are in a register format.

IDENTIFICATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
PMBus_REVISION	0x98	PMBus revision, supported by this device. The current revision is 1.2.	R Byte	N	Reg		FS	0x22
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0
MFR_ID	0x99	The manufacturer ID of the LTM4682 is in ASCII.	R String	N	ASC			LTC
MFR_MODEL	0x9A	Manufacturer part number in ASCII.	R String	N	ASC			LTM4682
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTM4682.	R Word	N	Reg			0x418X

PMBus_REVISION

The PMBUS_REVISION command indicates the revision of the PMBus to which the device is compliant. The LTM4682 is PMBus Version 1.2 compliant in both Part I and Part II.

This read-only command has one data byte.

CAPABILITY

This command provides a way for a host system to determine some key capabilities of a PMBus device.

The LTM4682 supports packet error checking, 400kHz bus speeds, and an $\overline{\text{ALERT}}$ pin.

This read-only command has one data byte.

MFR_ID

The MFR_ID command indicates the manufacturer ID of the LTM4682 using ASCII characters.

This read-only command is in block format.

MFR_MODEL

The MFR_MODEL command indicates the manufacturer's part number of the LTM4682 using ASCII characters.

This read-only command is in block format.

MFR_SPECIAL_ID

The 16-bit word represents the part name and revision. 0x418X denotes that the part is an LTM4682, and X is adjustable by the manufacturer.

This read-only command has two data bytes.

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FAULT WARNING AND STATUS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				NA
SMBALERT_MASK	0x1B	Mask activity.	Block R/W	Y	Reg		Y	See CMD Details
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	Y				NA
STATUS_BYTE	0x78	One-byte summary of the unit's fault condition.	R/W Byte	Y	Reg			NA
STATUS_WORD	0x79	Two-byte summary of the unit's fault condition.	R/W Word	Y	Reg			NA
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			NA
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			NA
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg			NA
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMERATURE_1.	R/W Byte	Y	Reg			NA
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			NA
STATUS_MFR_SPECIFIC	0x80	Manufacturer-specific fault and state information.	R/W Byte	Y	Reg			NA
MFR_PADS	0xE5	Digital status of the I/O pads.	R Word	N	Reg			NA
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status commands simultaneously. At the same time, the device negates (clears, releases) its $\overline{\text{ALERT}}$ pin signal output if the device is asserting the $\overline{\text{ALERT}}$ pin signal. If the fault is still present when the bit is cleared, the fault bit will remain set, and the host will be notified by asserting the $\overline{\text{ALERT}}$ pin low. CLEAR_FAULTS can take up to 10µs to process. If a fault occurs within that time frame, it may be cleared before the status register is set.

This write-only command has no data bytes.

The CLEAR_FAULTS does not cause a unit that has latched off for a fault condition to restart. Units that have shut down for a fault condition are restarted when:

- The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or
- MFR_RESET command is issued.
- Bias power is removed and reapplied to the integrated circuit

SMBALERT_MASK

The SMBALERT_MASK command can be used to prevent a particular status bit or bits from asserting $\overline{\text{ALERT}}$ as they are asserted.

Figure 55 shows an example of the Write Word format used to set an $\overline{\text{ALERT}}$ mask, in this case, without PEC. The bits in the mask byte align with bits in the specified status register. For example, if the STATUS_TEMPERATURE command code is sent in the first data byte, and the mask byte contains 0x40, then a subsequent External Overtemperature Warning

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would still set bit 6 of STATUS_TEMPERATURE but not assert $\overline{\text{ALERT}}$. All other supported STATUS_TEMPERATURE bits would continue to assert $\overline{\text{ALERT}}$ if set.

Figure 55 and Figure 56 show an example of the Block Write – Block Read Process Call protocol used to read back the present state of any supported status register, again without PEC.

SMBALERT_MASK cannot be applied to STATUS_BYTE, STATUS_WORD, MFR_COMMON, or MFR_PADS_LTM4682. Factory default masking for applicable status registers is shown below. Providing an unsupported command code to SMBALERT_MASK will generate a CML for Invalid/Unsupported Data.

SMBALERT_MASK Default Setting: (See Figure 2)

STATUS RESISTER	ALERT MASK VALUE	MASKED BITS
STATUS_VOUT	0x00	None
STATUS_IOUT	0x00	None
STATUS_TEMPERATURE	0x00	None
STATUS_CML	0x00	None
STATUS_INPUT	0x00	None
STATUS_MFR_SPECIFIC	0x11	Bit 4 (internal PLL unlocked), bit 0 ($\overline{\text{FAULT}}$ pulled low by external device).

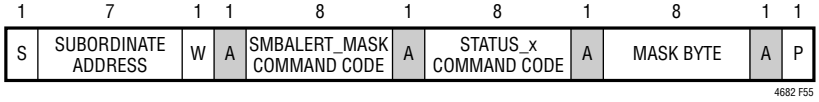

Figure 55. Example of Writing SMBALERT_MASK

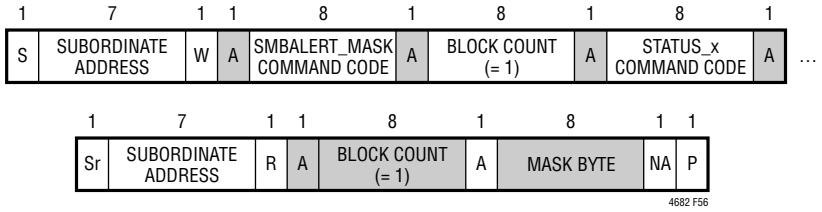

Figure 56. Example of Reading SMBALERT_MASK

MFR_CLEAR_PEAKS

The MFR_CLEAR_PEAKS command clears the MFR_*_PEAK data values. A MFR_RESET command will also clear the MFR_*_PEAK data values.

This write-only command has no data bytes.

STATUS_BYTE

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults. This is the lower byte of the status word.

PMBus COMMAND DETAILS

STATUS_BYTE Message Contents:

BIT	STATUS BIT NAME	MEANING
7*	BUSY	A fault was declared because the LTM4682 was unable to respond.
6	OFF	This bit is set if the channel is not providing power to its output, regardless of the reason, including not being enabled.
5	VOUT_OV	An output overvoltage fault has occurred.
4	IOUT_OC	An output overcurrent fault has occurred.
3	VIN_UV	Not supported (LTM4682 returns 0).
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0*	NONE OF THE ABOVE	A fault Not listed in bits[7:1] has occurred.

*$\overline{\text{ALERT}}$ can be asserted if either of these bits is set. They may be cleared by writing a 1 to their bit position in the STATUS_BYTE instead of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_WORD

The STATUS_WORD command returns a two-byte summary of the channel's fault condition. The low byte of the STATUS_WORD is the same as the STATUS_BYTE command.

STATUS_WORD High Byte Message Contents:

BIT	STATUS BIT NAME	MEANING
15	V_{OUT}	An output voltage fault or warning has occurred.
14	I_{OUT}	An output current fault or warning has occurred.
13	INPUT	An input voltage fault or warning has occurred.
12	MFR_SPECIFIC	A fault or warning specific to the LTM4682 has occurred.
11	POWER_GOOD#	The POWER_GOOD state is false if this bit is set.
10	FANS	Not supported (LTM4682 returns 0).
9	OTHER	Not supported (LTM4682 returns 0).
8	UNKNOWN	Not supported (LTM4682 returns 0).

If any of the bits in the upper byte are set, NONE_OF_THE_ABOVE is asserted.

This command has two data bytes.

STATUS_VOUT

The STATUS_VOUT command returns one byte of V_{OUT} status information.

STATUS_VOUT Message Contents:

BIT	MEANING
7	V_{OUT} overvoltage fault.
6	V_{OUT} overvoltage warning.
5	V_{OUT} undervoltage warning.
4	V_{OUT} undervoltage fault.
3	V_{OUT} max warning.
2	TON max fault.
1	TOFF max fault.
0	Not supported (LTM4682 returns 0).

PMBus COMMAND DETAILS

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

STATUS_IOUT

The STATUS_IOUT command returns one byte of I_{OUT} status information.

STATUS_IOUT Message Contents:

BIT	MEANING
7	I_{OUT} overcurrent fault.
6	Not supported (LTM4682 returns 0).
5	I_{OUT} overcurrent warning.
4:0	Not supported (LTM4682 returns 0).

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event. This command has one data byte.

STATUS_INPUT

The STATUS_INPUT command returns one byte of V_{IN} (V_{INSNS}) status information.

STATUS_INPUT Message Contents:

BIT	MEANING
7	V_{IN} overvoltage fault.
6	Not supported (LTM4682 returns 0).
5	V_{IN} undervoltage warning.
4	Not supported (LTM4682 returns 0).
3	Unit off for insufficient V_{IN}.
2	Not supported (LTM4682 returns 0).
1	I_{IN} overcurrent warning.
0	Not supported (LTM4682 returns 0).

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event. Bit 3 of this command is not latched and will not generate an $\overline{\text{ALERT}}$ even if it is set. This command has one data byte.

PMBus COMMAND DETAILS

STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns one byte with status information on temperature. This is a paged command and is related to the respective READ_TEMPERATURE_1 value.

STATUS_TEMPERATURE Message Contents:

BIT	MEANING
7	External overtemperature fault
6	External overtemperature warning
5	Not supported (LTM4682 returns 0)
4	External undertemperature fault
3:0	Not supported (LTM4682 returns 0)

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

This command has one data byte.

STATUS_CML

The STATUS_CML command returns one byte of status information on received commands, internal memory, and logic.

STATUS_CML Message Contents:

BIT	MEANING
7	Invalid or unsupported command received.
6	Invalid or unsupported data received.
5	The packet error check failed.
4	Memory fault detected.
3	Processor fault detected.
2	Reserved (LTM4682 returns 0).
1	Other communication faults.
0	Other memory or logic faults.

If either bit 3 or bit 4 of this command is set, a serious and significant internal error has been detected. Continued operation of the part is not recommended if these bits are continuously set.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

PMBus COMMAND DETAILS

STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC commands return one byte with the manufacturer-specific status information.

The format for this byte is:

BIT	MEANING
7	Internal temperature fault limit exceeded.
6	Internal temperature warn limit exceeded.
5	Factory trim area NVM CRC fault.
4	PLL is unlocked.
3	Fault log present.
2	V_{DD33} UV or OV fault.
1	ShortCycle event detected.
0	$\overline{\text{FAULT}}$ pin asserted low by external device.

If any of these bits are set, the MFR bit in the STATUS_WORD will be set, and $\overline{\text{ALERT}}$ may be asserted.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command. However, the fault log present bit can only be cleared by issuing the MFR_FAULT_LOG_CLEAR command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

MFR_PADS

This command provides the user with a means of directly reading the digital status of the I/O pins of the device. The bit assignments of this command are as follows:

BIT	ASSIGNED DIGITAL PIN
15	V_{DD33} OV fault.
14	V_{DD33} UV fault.
13	Reserved.
12	Reserved.
11	ADC values invalid, occurs during start-up. may occur briefly on current measurement channels during normal operation.
10	SYNC clocked by an external device (when LTM4682 configured to drive SYNC pin).
9	Channel 1 power good.
8	Channel 0 power good.
7	LTM4682 driving RUN1 low.
6	LTM4682 driving RUN0 low.
5	RUN1 pin state.
4	RUN0 pin state.
3	LTM4682 driving $\overline{\text{FAULT}}$1 low.
2	LTM4682 driving $\overline{\text{FAULT}}$0 low.
1	$\overline{\text{FAULT}}$1 pin state.
0	$\overline{\text{FAULT}}$0 pin state.

A 1 indicates the condition is true.

This read-only command has two data bytes.

PMBus COMMAND DETAILS

MFR_COMMON

The MFR_COMMON command contains bits that are common to all Analog Devices digital power and telemetry products.

BIT	MEANING
7	Module not driving $\overline{\text{ALERT}}$ low.
6	LTM4682 not busy.
5	Calculations not pending.
4	LTM4682 outputs not in transition.
3	NVM Initialized.
2	Reserved.
1	SHARE_CLK timeout.
0	WP pin status.

This read-only command has one data byte.

TELEMETRY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
READ_VIN	0x88	Measured input supply voltage.	R Word	N	L11	V		NA
READ_IIN	0x89	Measured input supply current.	R Word	N	L11	A		NA
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	L16	V		NA
READ_IOUT	0x8C	Measured output current.	R Word	Y	L11	A		NA
READ_TEMPERATURE_1	0x8D	Power stage temperature sensor. This is the value used for all temperature-related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	C		NA
READ_TEMPERATURE_2	0x8E	Internal junction temperature. Does not affect any other controller commands.	R Word	N	L11	C		NA
READ_FREQUENCY	0x95	Measured PWM switching frequency.	R Word	Y	L11	Hz		NA
READ_POUT	0x96	Calculated output power.	R Word	Y	L11	W		NA
READ_PIN	0x97	Calculated input power.	R Word	N	L11	W		NA
MFR_PIN_ACCURACY	0xAC	Returns the accuracy of the READ_PIN command	R Byte	N		%		5.0%
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since the last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		NA
MFR_VOUT_PEAK	0xDD	The maximum measured value of READ_VOUT since the last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		NA
MFR_VIN_PEAK	0xDE	The maximum measured value of READ_VIN since the last MFR_CLEAR_PEAKS.	R Word	N	L11	V		NA
MFR_TEMPERATURE_1_PEAK	0xDF	The maximum measured value of external Temperature (READ_TEMPERATURE_1) since the last MFR_CLEAR_PEAKS.	R Word	Y	L11	C		NA
MFR_READ_IIN_PEAK	0xE1	The maximum measured value of the READ_IIN command since the last MFR_CLEAR_PEAKS.	R Word	N	L11	A		NA
MFR_READ_ICHIP	0xE4	Measured current used by the LTM4682.	R Word	N	L11	A		NA
MFR_TEMPERATURE_2_PEAK	0xF4	Peak internal die temperature since the last MFR_CLEAR_PEAKS.	R Word	N	L11	C		NA
MFR_ADC_CONTROL	0xD8	The ADC telemetry parameter selected for repeated fast ADC read back.	R/W Byte	N	N	Reg		NA

PMBus COMMAND DETAILS

READ_VIN

The READ_VIN command returns the measured V_{IN} pin voltage, in volts added to READ_ICHIP • MFR_RVIN. This compensates for the IR voltage drop across the V_{IN} filter element due to the supply current of the LTM4682.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_VOUT

The READ_VOUT command returns the measured output voltage by the VOUT_MODE command.

This read-only command has two data bytes and is formatted in Linear_16u format.

READ_IIN

The READ_IIN command returns the input current, in Amperes, as measured across the input current sense resistor (see also MFR_IIN_CAL_GAIN).

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_IOUT

The READ_IOUT command returns the average output current in amperes. The I_{OUT} value is a function of:

a) the differential voltage measured across the I_{SENSE} pins

b) the IOUT_CAL_GAIN value

c) the MFR_IOUT_CAL_GAIN_TC value, and

d) READ_TEMPERATURE_1 value

e) The MFR_TEMP_1_GAIN and the MFR_TEMP_1_OFFSET

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the temperature, in degrees Celsius, of the power stage sense element.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_TEMPERATURE_2

The READ_TEMPERATURE_2 command returns the LTM4682's die temperature, in degrees Celsius, of the internal sense element.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_FREQUENCY

The READ_FREQUENCY command is a reading of the PWM switching frequency in kHz.

This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

READ_POUT

The READ_POUT command is a reading of the DC/DC converter output power in Watts. POUT is calculated based on the most recent correlated output voltage and current reading.

This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

READ_PIN

The READ_PIN command is a reading of the DC/DC converter input power in Watts. The PIN is calculated based on the most recent input voltage and current reading.

This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

MFR_PIN_ACCURACY

The MFR_PIN_ACCURACY command returns the accuracy, in percent, of the value returned by the READ_PIN command.

There is one data byte. The value is 0.1% per bit, which gives a range of ±0.0% to ±25.5%.

This read-only command has one data byte and is formatted as an unsigned integer.

MFR_IOUT_PEAK

The MFR_IOUT_PEAK command reports the highest current, in amperes, reported by the READ_IOUT measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_VOUT_PEAK

The MFR_VOUT_PEAK command reports the highest voltage, in volts, reported by the READ_VOUT measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_16u format.

MFR_VIN_PEAK

The MFR_VIN_PEAK command reports the highest voltage, in volts, reported by the READ_VIN measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_TEMPERATURE_1_PEAK

The MFR_TEMPERATURE_1_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_1 measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_READ_IIN_PEAK

The MFR_READ_IIN_PEAK command reports the highest current, in Amperes, reported by the READ_IIN measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

MFR_READ_ICHIP

The MFR_READ_ICHIP command returns the measured input current, in Amperes, used by the LTM4682.

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_TEMPERATURE_2_PEAK

The MFR_TEMPERATURE_2_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_2 measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_ADC_CONTROL

The MFR_ADC_CONTROL command determines the ADC read back selection. A default value of 0 in the command runs the standard telemetry loop with all parameters updated in a round-robin fashion with a typical latency of $t_{CONVERT}$. The user can command a non-zero value to monitor a single parameter with an approximate update rate of 8ms. This command has a latency of up to 2 ADC conversions or approximately 16ms (external temperature conversions may have a latency of up to 3 ADC conversions or approximately 24ms). It is recommended that the part remain in standard telemetry mode except for special cases where fast ADC updates of a single parameter is required. The part should be commanded to monitor the desired parameter for a limited period of time (less than 1 second), then set the command back to standard round-robin mode. If this command is set to any value except standard round-robin telemetry (0), all warnings and faults associated with telemetry other than the selected parameter are effectively disabled, and voltage servoing is disabled. When a round-robin is reasserted, all warnings and faults and servo mode are re-enabled.

COMMANDED VALUE	TELEMETRY COMMAND NAME	DESCRIPTION
0x0F		Reserved
0x0E		Reserved
0x0D		Reserved
0x0C	READ_TEMPERATURE_1	Channel 1 external temperature.
0x0B		Reserved
0x0A	READ_IOUT	Channel 1 measured output current.
0x09	READ_VOUT	Channel 1 measured output voltage.
0x08	READ_TEMPERATURE_1	Channel 0 external temperature.
0x07		Reserved
0x06	READ_IOUT	Channel 0 measured output current.
0x05	READ_VOUT	Channel 0 measured output voltage.
0x04	READ_TEMPERATURE_2	Internal junction temperature.
0x03	READ_IIN	Measured input supply current.
0x02	MFR_READ_ICHIP	Measured supply current of the LTM4682.
0x01	READ_VIN	Measured input supply voltage.
0x00		Standard ADC round-robin telemetry.

If a reserved command value is entered, the telemetry will default to Internal IC temperature and issue a CML fault. The CML faults will continue to be issued by the LTM4682 until a valid command value is entered. The accuracy of the measured input supply voltage is only guaranteed if the MFR_ADC_CONTROL command is set to standard round-robin telemetry.

This write-only command has 1 data byte and is formatted in a register format.

PMBus COMMAND DETAILS

NVM MEMORY COMMANDS

Store/Restore

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				NA
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				NA
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with NVM.	Send Byte	N				NA

STORE_USER_ALL

The STORE_USER_ALL command instructs the PMBus device to copy the nonvolatile user contents of the operating memory to the matching locations in the nonvolatile User NVM memory.

Executing this command if the die temperature exceeds 85°C or is below 0°C is not recommended, and the data retention of 10 years cannot be guaranteed. If the die temperature exceeds 130°C, the STORE_USER_ALL command is disabled. The command is re-enabled when the IC temperature drops below 125°C.

Communication with the LTM4682 and programming of the NVM can be initiated when $EXTV_{CC}$ or V_{DD33} is available, and V_{IN} is not applied. To enable the part in this state, using global address 0x5B, write MFR_EE_UNLOCK to 0x2B followed by 0xC4. The LTM4682 will now communicate normally, and the project file can be updated. To write the updated project file to the NVM issue, a STORE_USER_ALL command. When V_{IN} is applied, an MFR_RESET must be issued to allow the PWM to be enabled and valid ADCs to be read.

This write-only command has no data bytes.

RESTORE_USER_ALL

The RESTORE_USER_ALL command instructs the LTM4682 to copy the contents of the nonvolatile user memory to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the user commands. The LTM4682 ensures both channels are off, loads the operating memory from the internal EEPROM, clears all faults, reads the resistor configuration pins, and then performs a soft-start of both PWM channels if applicable.

STORE_USER_ALL, MFR_COMPARE_USER_ALL and RESTORE_USER_ALL commands are disabled if the die exceeds 130°C and are not re-enabled until the die temperature drops below 125°C.

This write-only command has no data bytes.

MFR_COMPARE_USER_ALL

The MFR_COMPARE_USER_ALL command instructs the PMBus device to compare current command contents with what is stored in nonvolatile memory. If the compare operation detects differences, a CML bit 0 fault will be generated.

This write-only command has no data bytes.

PMBus COMMAND DETAILS

Fault Logging

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_FAULT_LOG	0xEE	Fault log data bytes.	R Block	N	CF		Y	NA
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging.	Send Byte	N				NA

MFR_FAULT_LOG

The MFR_FAULT_LOG command allows the user to read the contents of the FAULT_LOG after the first fault occurrence since the last MFR_FAULT_LOG_CLEAR command was written. The contents of this command are stored in nonvolatile memory, and are cleared by the MFR_FAULT_LOG_CLEAR command. The length and content of this command are listed in Table 15. If the user accesses the MFR_FAULT_LOG command and a no-fault log is present, the command will return a data length of 0. If a fault log is present, the MFR_FAULT_LOG will return a block of data 147 bytes long. If a fault occurs within the first second of applying power, some of the earlier pages in the fault log may not contain valid data.

NOTE: The approximate transfer time for this command is 3.4ms using a 400kHz clock.

This read-only command is in block format.

MFR_FAULT_LOG_STORE

The MFR_FAULT_LOG_STORE command forces the fault log operation to be written to NVM just as if a fault event occurred. This command will set bit 3 of the STATUS_MFR_SPECIFIC fault if bit 7, Enable Fault Logging, is set in the MFR_CONFIG_ALL command.

If the die temperature exceeds 130°C, the MFR_FAULT_LOG_STORE command is disabled until the IC temperature drops below 125°C.

This write-only command has no data bytes.

PMBus COMMAND DETAILS

Table 23. Fault Logging

This table outlines the format of the block data from a read block data of the MFR_FAULT_LOG command.

Data Format Definitions				LIN 11 = PMBus = Rev 1.2, Part 2, section 7.1
				LIN 16 = PMBus Rev 1.2, Part 2, section 8. Mantissa portion only.
				BYTE = 8 bits interpreted per definition of this command.
DATA	**BITS**	**DATA FORMAT**	**BYTE NUM**	**BLOCK READ COMMAND**
Block Length		Byte	147	The MFR_FAULT_LOG command is a fixed length of 147 bytes. The block length will be zero if a data log event has not been captured.
HEADER INFORMATION				
Fault Log Preface	[7:0]	ASC	0	Returns LTxx beginning at byte 0 if a partial or complete fault log exists. Word xx is a factory identifier that may vary from part to part.
	[7:0]		1	
	[15:8]	Reg	2	
	[7:0]		3	
Fault Source	[7:0]	Reg	4	See Table 19.
MFR_REAL_TIME	[7:0]	Reg	5	48-bit share-clock counter value when the fault occurred (200µs resolution).
	[15:8]		6	
	[23:16]		7	
	[31:24]		8	
	[39:32]		9	
	[47:40]		10	
MFR_VOUT_PEAK (PAGE 0)	[15:8]	L16	11	Peak READ_VOUT on Channel 0 since the last power-on or CLEAR_ PEAKS command.
	[7:0]		12	
MFR_VOUT_PEAK (PAGE 1)	[15:8]	L16	13	Peak READ_VOUT on Channel 1 since the last power-on or CLEAR_ PEAKS command.
	[7:0]		14	
MFR_IOUT_PEAK (PAGE 0)	[15:8]	L11	15	Peak READ_IOUT on Channel 0 since the last power-on or CLEAR_ PEAKS command.
	[7:0]		16	
MFR_IOUT_PEAK (PAGE 1)	[15:8]	L11	17	Peak READ_IOUT on Channel 1 since the last power-on or CLEAR_ PEAKS command.
	[7:0]		18	
MFR_VIN_PEAK	[15:8]	L11	19	Peak READ_VIN since the last power-on or CLEAR_PEAKS command.
	[7:0]		20	
READ_TEMPERATURE1 (PAGE 0)	[15:8]	L11	21	Power stage temperature sensor 0 during the last event.
	[7:0]		22	
READ_TEMPERATURE1 (PAGE 1)	[15:8]	L11	23	Power stage temperature sensor 1 during the last event.
	[7:0]		24	
READ_TEMPERATURE2	[15:8]	L11	25	LTM4682 die temperature sensor during the last event.
	[7:0]		26	

PMBus COMMAND DETAILS

CYCLICAL DATA				
EVENT n **(Data at Which Fault Occurred; Most Recent Data)**				Event n represents one complete cycle of ADC reads through the MUX at the time of fault. Example: If the fault occurs when the ADC is processing step 15, it will continue to take readings through step 25 and then store the header and all six event pages to EEPROM.
READ_VOUT (PAGE 0)	[15:8]	LIN 16	27	
	[7:0]	LIN 16	28	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	29	
	[7:0]	LIN 16	30	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	31	
	[7:0]	LIN 11	32	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	33	
	[7:0]	LIN 11	34	
READ_VIN	[15:8]	LIN 11	35	
	[7:0]	LIN 11	36	
READ_IIN	[15:8]	LIN 11	37	
	[7:0]	LIN 11	38	
STATUS_VOUT (PAGE 0)		Byte	39	
STATUS_VOUT (PAGE 1)		Byte	40	
STATUS_WORD (PAGE 0)	[15:8]	Word	41	
	[7:0]	Word	42	
STATUS_WORD (PAGE 1)	[15:8]	Word	43	
	[7:0]	Word	44	
STATUS_MFR_SPECIFIC (PAGE 0)		Byte	45	
STATUS_MFR_SPECIFIC (PAGE 1)		Byte	46	
EVENT n-1 **(data measured before fault was detected)**				
READ_VOUT (PAGE 0)	[15:8]	LIN 16	47	
	[7:0]	LIN 16	48	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	49	
	[7:0]	LIN 16	50	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	51	
	[7:0]	LIN 11	52	

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READ_IOUT (PAGE 1)	[15:8]	LIN 11	53	
	[7:0]	LIN 11	54	
READ_VIN	[15:8]	LIN 11	55	
	[7:0]	LIN 11	56	
READ_IIN	[15:8]	LIN 11	57	
	[7:0]	LIN 11	58	
STATUS_VOUT (PAGE 0)		BYTE	59	
STATUS_VOUT (PAGE 1)		BYTE	60	
STATUS_WORD (PAGE 0)	[15:8]	WORD	61	
	[7:0]	WORD	62	
STATUS_WORD (PAGE 1)	[15:8]	WORD	63	
	[7:0]	WORD	64	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	65	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	66	
EVENT n-5 (Oldest Recorded Data)				
READ_VOUT (PAGE 0)	[15:8]	LIN 16	127	
	[7:0]	LIN 16	128	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	129	
	[7:0]	LIN 16	130	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	131	
	[7:0]	LIN 11	132	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	133	
	[7:0]	LIN 11	134	
READ_VIN	[15:8]	LIN 11	135	
	[7:0]	LIN 11	136	
READ_IIN	[15:8]	LIN 11	137	
	[7:0]	LIN 11	138	
STATUS_VOUT (PAGE 0)		BYTE	139	
STATUS_VOUT (PAGE 1)		BYTE	140	
STATUS_WORD (PAGE 0)	[15:8]	WORD	141	
	[7:0]	WORD	142	
STATUS_WORD (PAGE 1)	[15:8]	WORD	143	
	[7:0]	WORD	144	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	145	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	146	

PMBus COMMAND DETAILS

Table 24. Explanation of Position_Fault Values

POSITION_FAULT VALUE	SOURCE OF FAULT LOG
0xFF	MFR_FAULT_LOG_STORE
0x00	TON_MAX_FAULT
0x01	VOUT_OV_FAULT
0x02	VOUT_UV_FAULT
0x03	IOUT_OC_FAULT
0x05	TEMP_OT_FAULT
0x06	TEMP_UT_FAULT
0x07	VIN_OV_FAULT
0x0A	MFR_TEMP_2_OT_FAULT

MFR_INFO

Contact the factory for more details.

MFR_IOUT_CAL_GAIN

Contact the factory for more details.

MFR_FAULT_LOG_CLEAR

The MFR_FAULT_LOG_CLEAR command will erase the fault log file stored values. It will also clear bit 3 in the STATUS_MFR_SPECIFIC command. After a clear is issued, the status can take up to 8ms to clear.

This write-only command is to send bytes.

Block Memory Write/Read

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA

All the NVM commands are disabled if the die temperature exceeds 130°C. The NVM commands are re-enabled when the die temperature drops below 125°C.

MFR_EE_xxxx

The MFR_EE_xxxx commands facilitate bulk programming of the LTM4682 internal EEPROM. Contact the factory for more details.

PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Table 25. LTM4682 BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND	B1	GND	C1	SW0	D1	SW0	E1	SW0	F1	GND
A2	GND	B2	GND	C2	SW0	D2	SW0	E2	SW0	F2	GND
A3	GND	B3	GND	C3	GND	D3	GND	E3	GND	F3	GND
A4	GND	B4	GND	C4	GND	D4	GND	E4	GND	F4	GND
A5	V_{IN01}	B5	V_{IN01}	C5	V_{IN01}	D5	V_{IN01}	E5	V_{IN01}	F5	V_{IN01}
A6	V_{IN01}	B6	V_{IN01}	C6	V_{IN01}	D6	V_{IN01}	E6	V_{IN01}	F6	V_{IN01}
A7	GND	B7	GND	C7	GND	D7	GND	E7	GND	F7	GND
A8	VOUT0_CFG	B8	VOUT1_CFG	C8	V_{DD25_01}	D8	SHARE_CLK_01	E8	V_{DD33_01}	F8	V_{OSNS1}^-
A9	FSWPH_01_CFG	B9	ASEL_01	C9	VTRIM1_CFG	D9	VTRIM0_CFG	E9	WP_01	F9	COMP1b
A10	$\overline{\text{FAULT1}}$	B10	RUN0	C10	SDA_01	D10	SCL_01	E10	TSNS1	F10	SGND_01
A11	$\overline{\text{FAULT0}}$	B11	RUN1	C11	$\overline{\text{ALERT}}$_01	D11	SYNC_01	E11	TSNS0	F11	SGND_01
A12	GND	B12	GND	C12	GND	D12	GND	E12	GND	F12	GND
A13	V_{OUT0}	B13	V_{OUT0}	C13	V_{OUT0}	D13	V_{OUT0}	E13	V_{OUT0}	F13	V_{OUT1}
A14	V_{OUT0}	B14	V_{OUT0}	C14	V_{OUT0}	D14	V_{OUT0}	E14	V_{OUT0}	F14	V_{OUT1}
A15	V_{OUT0}	B15	V_{OUT0}	C15	V_{OUT0}	D15	V_{OUT0}	E15	V_{OUT0}	F15	V_{OUT1}

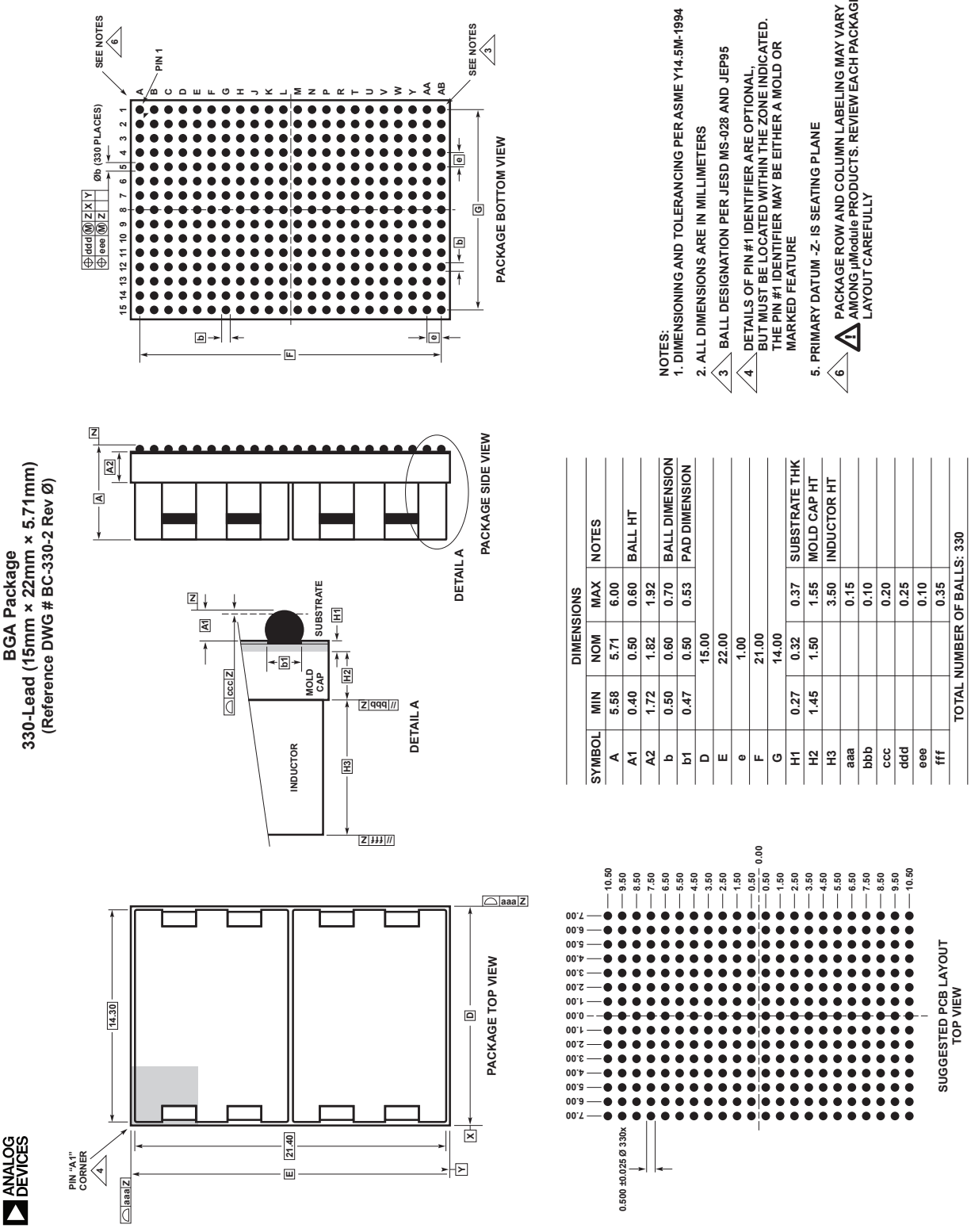
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	SW1	H1	SW1	J1	SW1	K1	GND	L1	GND	M1	GND
G2	SW1	H2	SW1	J2	SW1	K2	GND	L2	GND	M2	GND
G3	GND	H3	GND	J3	GND	K3	GND	L3	GND	M3	GND
G4	GND	H4	GND	J4	GND	K4	GND	L4	GND	M4	GND
G5	V_{IN01}	H5	V_{IN01}	J5	V_{IN01}	K5	V_{IN01}	L5	GND	M5	GND
G6	V_{IN01}	H6	V_{IN01}	J6	V_{IN01}	K6	V_{IN01}	L6	GND	M6	GND
G7	GND	H7	GND	J7	GND	K7	GND	L7	GND	M7	GND
G8	V_{OSNS1}^+	H8	PGOOD1	J8	SV_{IN_01}	K8	GND	L8	GND	M8	GND
G9	COMP1a	H9	PGOOD0	J9	$INTV_{CC\_01}$	K9	GND	L9	GND	M9	GND
G10	COMP0b	H10	$I_{IN\_01}^+$	J10	I_{IN_01}–	K10	GND	L10	GND	M10	GND
G11	COMP0a	H11	V_{OSNS0}^-	J11	V_{OSNS0}^+	K11	GND	L11	GND	M11	GND
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND
G13	V_{OUT1}	H13	V_{OUT1}	J13	V_{OUT1}	K13	V_{OUT1}	L13	GND	M13	GND
G14	V_{OUT1}	H14	V_{OUT1}	J14	V_{OUT1}	K14	V_{OUT1}	L14	GND	M14	GND
G15	V_{OUT1}	H15	V_{OUT1}	J15	V_{OUT1}	K15	V_{OUT1}	L15	GND	M15	GND

PACKAGE DESCRIPTION

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
N1	GND	P1	SW2	R1	SW2	T1	SW2	U1	GND	V1	SW3
N2	GND	P2	SW2	R2	SW2	T2	SW2	U2	GND	V2	SW3
N3	GND	P3	GND	R3	GND	T3	GND	U3	GND	V3	GND
N4	GND	P4	GND	R4	GND	T4	GND	U4	GND	V4	GND
N5	V_{IN23}	P5	V_{IN23}	R5	V_{IN23}	T5	V_{IN23}	U5	V_{IN23}	V5	V_{IN23}
N6	V_{IN23}	P6	V_{IN23}	R6	V_{IN23}	T6	V_{IN23}	U6	V_{IN23}	V6	V_{IN23}
N7	GND	P7	GND	R7	GND	T7	GND	U7	GND	V7	GND
N8	GND	P8	V_{OSNS2}^{+}	R8	V_{OSNS2}^{-}	T8	COMP2a	U8	TSNS2	V8	SDA_23
N9	V_{IN_VBIAS}	P9	$I_{IN\_23}^{-}$	R9	$I_{IN\_23}^{+}$	T9	COMP2b	U9	TSNS3	V9	SYNC_23
N10	V_{BIAS}	P10	$INTV_{CC\_23}$	R10	PGOOD2	T10	PGOOD3	U10	SGND_23	V10	$\overline{FAULT}$2
N11	RUNP	P11	SV_{IN_23}	R11	V_{OSNS3}^{+}	T11	V_{OSNS3}^{-}	U11	SGND_23	V11	COMP3a
N12	GND	P12	GND	R12	GND	T12	GND	U12	GND	V12	GND
N13	V_{OUT2}	P13	V_{OUT2}	R13	V_{OUT2}	T13	V_{OUT2}	U13	V_{OUT2}	V13	V_{OUT3}
N14	V_{OUT2}	P14	V_{OUT2}	R14	V_{OUT2}	T14	V_{OUT2}	U14	V_{OUT2}	V14	V_{OUT3}
N15	V_{OUT2}	P15	V_{OUT2}	R15	V_{OUT2}	T15	V_{OUT2}	U15	V_{OUT2}	V15	V_{OUT3}

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
W1	SW3	Y1	SW3	AA1	GND	AB1	GND
W2	SW3	Y2	SW3	AA2	GND	AB2	GND
W3	GND	Y3	GND	AA3	GND	AB3	GND
W4	GND	Y4	GND	AA4	GND	AB4	GND
W5	V_{IN23}	Y5	V_{IN23}	AA5	V_{IN23}	AB5	V_{IN23}
W6	V_{IN23}	Y6	V_{IN23}	AA6	V_{IN23}	AB6	V_{IN23}
W7	GND	Y7	GND	AA7	GND	AB7	GND
W8	$\overline{ALERT}$_23	Y8	RUN3	AA8	VOUT2_CFG	AB8	VOUT3_CFG
W9	SCL_23	Y9	RUN2	AA9	FSWPH_23_CFG	AB9	VTRIM3_CFG
W10	$\overline{FAULT}$3	Y10	V_{DD33_23}	AA10	ASEL_23	AB10	VTRIM2_CFG
W11	COMP3b	Y11	WP_23	AA11	SHARE_CLK_23	AB11	V_{DD25_23}
W12	GND	Y12	GND	AA12	GND	AB12	GND
W13	V_{OUT3}	Y13	V_{OUT3}	AA13	V_{OUT3}	AB13	V_{OUT3}
W14	V_{OUT3}	Y14	V_{OUT3}	AA14	V_{OUT3}	AB14	V_{OUT3}
W15	V_{OUT3}	Y15	V_{OUT3}	AA15	V_{OUT3}	AB15	V_{OUT3}

PACKAGE DESCRIPTION



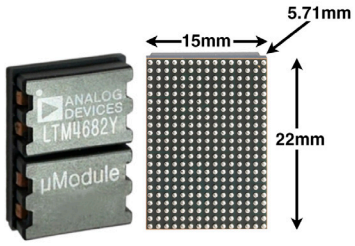
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	5.58	5.71	6.00	
A1	0.40	0.50	0.60	BALL HT
A2	1.72	1.82	1.92	
b	0.50	0.60	0.70	BALL DIMENSION
b1	0.47	0.50	0.53	PAD DIMENSION
D		15.00		
E		22.00		
e		1.00		
F		21.00		
G		14.00		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	1.45	1.50	1.55	MOLD CAP HT
H3			3.50	INDUCTOR HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.25	
eee			0.10	
fff			0.35	
TOTAL NUMBER OF BALLS: 330				

REVISION HISTORY

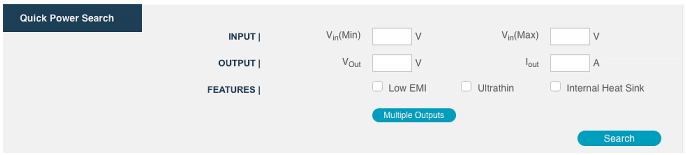
REV	DATE	DESCRIPTION	PAGE NUMBER
0	07/24	Initial Release.	—

PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTP8800-2	135A DC/DC µModule Regulator with PMBus Interface	45V ≤ V_{IN} ≤ 65V, 0.5V ≤ V_{OUT} ≤ 1.0V, 22mm × 24mm × 6.7mm Surface Mount Package
LTP8800-1A	150A DC/DC µModule Regulator with PMBus Interface	45V ≤ V_{IN} ≤ 65V, 0.5V ≤ V_{OUT} ≤ 1.1V, 22mm × 24mm × 6.7mm Surface Mount Package
LTP8803-1A	160A DC/DC µModule Regulator with PMBus Interface	45V ≤ V_{IN} ≤ 65V, 0.5V ≤ V_{OUT} ≤ 1.5V, 22mm × 24mm × 22mm Surface Mount Package
LTP8800-4A	200A DC/DC µModule Regulator with PMBus Interface	45V ≤ V_{IN} ≤ 65V, 0.5V ≤ V_{OUT} ≤ 1.1V, 22mm × 24mm × 22mm Surface Mount Package
LTM4683	Low V_{OUT}, Quad 31.25A or Single 125A µModule Regulator with Digital Power System Management (PSM)	4.5V ≤ V_{IN} ≤ 14V, 0.3V ≤ V_{OUT} ≤ 0.7V, 15mm × 22mm × 5.71mm BGA
LTM4675	Dual 9A or Single 18A Step-Down µModule Regulator, Digital PSM	4.5V ≤ V_{IN} ≤ 17V, 0.5V ≤ V_{OUT} ≤ 5.5V, 11.9mm × 16mm × 3.51mm BGA
LTM4673	Dual 12A and Dual 5A, Quad µModule Regulator, Digital PSM	4.5V ≤ V_{IN} ≤ 16V, 0.6V ≤ V_{OUT} ≤ 3.3V or 5.5V, 16mm × 16mm × 4.72mm BGA
LTM4686/ LTM4686-1	Ultrathin Dual 10A or Single 20A µModule Regulator, Digital PSM	4.5V ≤ V_{IN} ≤ 17V, 0.5V ≤ V_{OUT} ≤ 3.6V (LTM4686), 2.375V ≤ V_{IN} ≤ 17V (LTM4686-1) 11.9mm × 16mm × 1.82mm LGA
LTM4686B	Ultrathin Dual 14A or Single 28A µModule Regulator, Digital PSM, Low V_{OUT}, Higher I_{OUT} Version of LTM4686/LTM4686-1	4.5V ≤ V_{IN} ≤ 5.75, 0.5V ≤ V_{OUT} ≤ 3.6V, 11.9mm × 16mm × 1.82mm LGA
LTM4676A	Dual 13A or Single 26A Step-Down µModule Regulator, Digital PSM	4.5V ≤ V_{IN} ≤ 26.5V, 0.5V ≤ V_{OUT} ≤ 5.5V, 16mm × 16mm × 5.01mm BGA
LTM4677	Dual 18A or Single 36A Step-Down µModule Regulator, Digital PSM	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 1.8V, 16mm × 16mm × 5.01mm BGA
LTM4678	Dual 25A or Single 50A µModule Regulator with Digital PSM	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.4V, 16mm × 16mm × 5.86mm BGA
LTM4664	54V_{IN}, Dual 25A or Single 50A µModule Regulator with Digital PSM	30V ≤ V_{IN} ≤ 58V, 0.5V ≤ V_{OUT} ≤ 1.5V, 16mm × 16mm × 7.72mm BGA
LTM4680	Dual 30A or Single 60A µModule Regulator with Digital PSM	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.3V, 16mm × 16mm × 7.82mm BGA
LTM4681	Quad 31.25A or Single 125A, µModule Regulator with Digital PSM, Higher V_{OUT} Version of LTM4683	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.3V, 15mm × 22mm × 8.17mm BGA
LTM4700	Dual 50A or Single 100A µModule Regulator with Digital PSM	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 1.8V, 15mm × 22mm × 7.87mm BGA