Dual 25A or Single 50A µModule Regulator with Active Voltage Positioning

FEATURES

- Dual 25A or Single 50A Output
- 4.5V to 15V Input, 0.6V to 1.8V Output Voltage Range
- ±1.5% Maximum Total DC Output Error Over Line and Load
- Differential Remote Sense Amplifier
- Current Mode Control/Fast Transient Response
- Current Sharing Up to 300A
- AVP (Active Voltage Positioning) Compatible
- 16mm × 16mm × 5.01mm BGA Package

APPLICATIONS

- FPGA, ASIC, µProcessor Core Voltage Regulation
- Information, Communication Systems

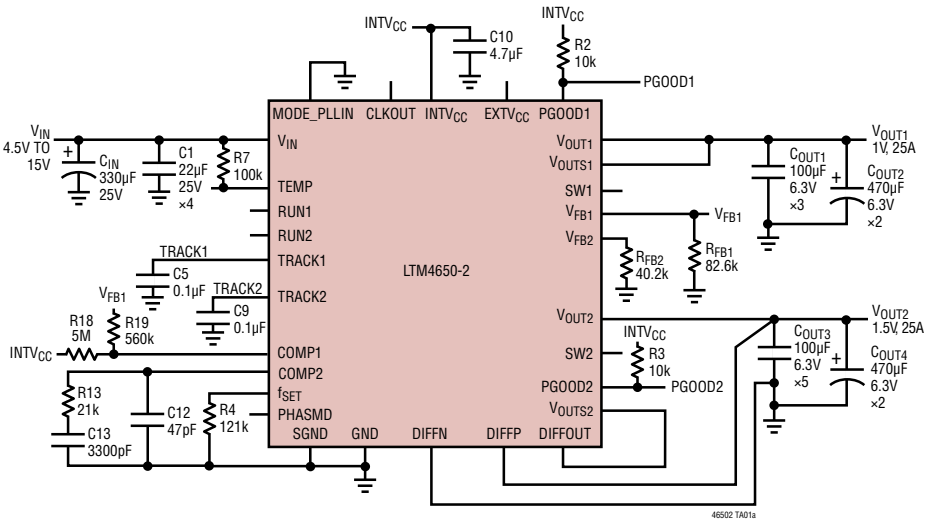
DESCRIPTION

The LTM®4650-2 is a dual 25A or single 50A output step-down µModule® (micromodule) regulator with ±1.5% total DC output error. The package includes the switching controller, power FETs, inductors, and all supporting components. External compensation allows for fast transient response to minimize output capacitance when powering FPGAs, ASICs, and processors. AVP can further improve transient response and reduce the output capacitance. With synchronized multiphase parallel current sharing, six LTM4650-2 devices can deliver up to 300A.

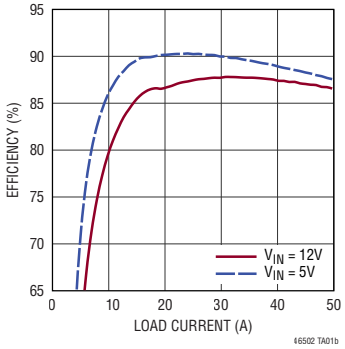
The LTM4650-2 is offered in a 16mm × 16mm × 5.01mm BGA package with SnPb or RoHS-compliant terminal finish.

TYPICAL APPLICATION

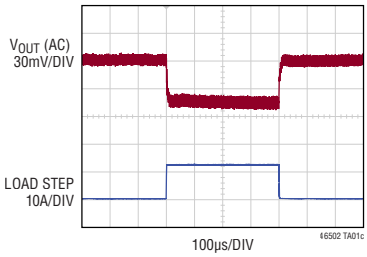
Dual 25A, 1.0V and 1.5Vouts DC/DC µModule Regulator



1.0V Output Efficiency, f_{SW} = 500kHz



50% (12.5A) Load Step Transient Response, $12V_{IN}$, $1V_{OUT}$ (with AVP)

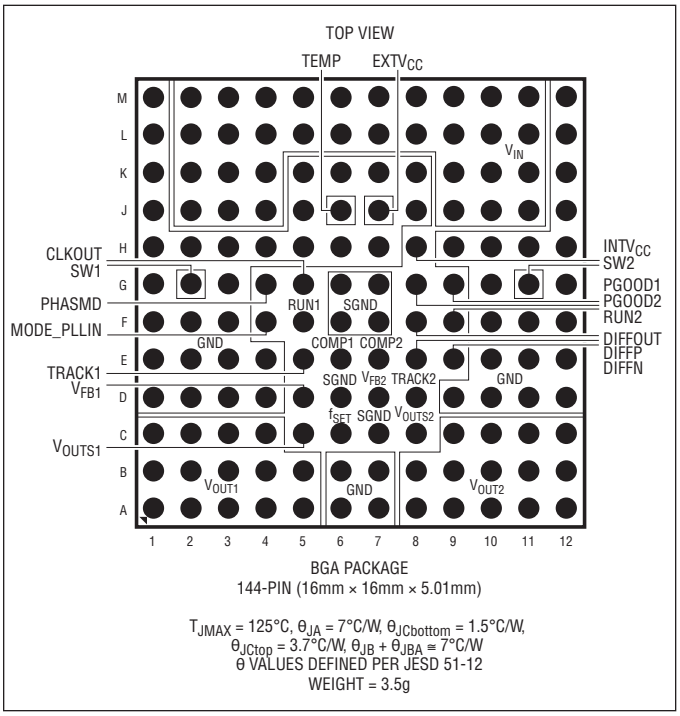


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} .....–0.3V to 16V
V_{SW1}, V_{SW2} .....–1V to 16V
PGOOD1, PGOOD2, RUN1, RUN2,
$INTV_{CC}$, $EXTV_{CC}$ ..... –0.3V to 6V
MODE_PLLIN, f_{SET}, TRACK1, TRACK2,
DIFFOUT, PHASMD .....–0.3V to $INTV_{CC}$
V_{OUT1}, V_{OUT2}, V_{OUTS1}, V_{OUTS2} (Note 6)..... –0.3V to 6V
DIFFP, DIFFN .....–0.3V to $INTV_{CC}$
$INTV_{CC}$ Peak Output Current.....100mA
Internal Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Package Body Temperature..... 245°C

PIN CONFIGURATION



BGA PACKAGE
144-PIN (16mm × 16mm × 5.01mm)

T_{JMAX} = 125°C, θ_{JA} = 7°C/W, $\theta_{JCbottom}$ = 1.5°C/W,
θ_{JCtop} = 3.7°C/W, θ_{JB} + θ_{JBA} ≅ 7°C/W
θ VALUES DEFINED PER JESD 51-12
WEIGHT = 3.5g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH*	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM4650EY-2#PBF	SAC305 (RoHS)	LTM4650Y-2	e1	BGA	4	–40°C to 125°C
LTM4650IY-2#PBF	SAC305 (RoHS)	LTM4650Y-2	e1	BGA	4	–40°C to 125°C
LTM4650IY-2	SnPb (63/37)	LTM4650Y-2	e0	BGA	4	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges.
*Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating junction temperature range. Specified as each individual output channel. T_A = 25°C (Note 2), V_{IN} = 12V and V_{RUN1}, V_{RUN2} at 5V unless otherwise noted. Per the typical application in Figure 24.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	4.5		15	V
V_{OUT}	Output DC Voltage		●	0.6		1.8	V
$V_{OUT1(DC)}$, $V_{OUT2(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF ×3, C_{OUT} = 100µF ×2 Ceramic, 470µF POSCAP, V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0A to 25A	●	1.182		1.218	V
Input Specifications							
V_{RUN1}, V_{RUN2}	RUN Pin On/Off Threshold	RUN Rising		1.1	1.25	1.40	V
$V_{RUN1HYS}$, $V_{RUN2HYS}$	RUN Pin On Hysteresis				150		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating junction temperature range. Specified as each individual output channel. T_A = 25°C (Note 2), V_{IN} = 12V and V_{RUN1}, V_{RUN2} at 5V unless otherwise noted. Per the typical application in Figure 24.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	I_{OUT} = 0A, C_{IN} = 22µF ×3, C_{SS} = 0.01µF, C_{OUT} = 100µF ×3, V_{OUT} = 1.2V			1		A
$I_{Q(VIN)}$	Input Supply Bias Current (Both Channel Running)	V_{IN} = 12V, V_{OUT} = 1.2V, Burst Mode Operation V_{IN} = 12V, V_{OUT} = 1.2V, Pulse-Skipping Mode V_{IN} = 12V, V_{OUT} = 1.2V, Switching Continuous Shutdown, RUN = 0, V_{IN} = 12V			4.5 25 240 35		mA mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 4.5V, V_{OUT} = 1.2V, I_{OUT} = 25A V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 25A			8.4 3.2		A A
Output Specifications							
$I_{OUT1(DC)}$, $I_{OUT2(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.2V (Note 6)		0		25	A
$\Delta V_{OUT1(LINE)}/V_{OUT1}$ $\Delta V_{OUT2(LINE)}/V_{OUT2}$	Line Regulation Accuracy	V_{OUT} = 1.2V, V_{IN} from 4.5V to 15V, I_{OUT} = 0A for Each Output	●		0.01	0.1	%/V
$\Delta V_{OUT1}/V_{OUT1}$ $\Delta V_{OUT2}/V_{OUT2}$	Load Regulation Accuracy	For Each Output, V_{OUT} = 1.2V, 0A to 25A, V_{IN} = 12V (Note 6)	●		0.2	0.75	%
$V_{OUT1(AC)}$, $V_{OUT2(AC)}$	Output Ripple Voltage	For Each Output, I_{OUT} = 0A, C_{OUT} = 100µF ×3 Ceramic, 470µF POSCAP, V_{IN} = 12V, V_{OUT} = 1.2V, Frequency = 500kHz			15		mV_{P-P}
f_S (Each Channel)	Output Ripple Voltage Frequency	V_{IN} = 12V, V_{OUT} = 1.2V, f_{SET} = 1.25V (Note 4)			500		kHz
f_{SYNC} (Each Channel)	SYNC Capture Range			400		750	kHz
$\Delta V_{OUTSTART}$ (Each Channel) (Note 7)	Turn-On Overshoot	C_{OUT} = 100µF Ceramic, 470µF POSCAP, V_{OUT} = 1.2V, I_{OUT} = 0A V_{IN} = 12V			10		mV
t_{START} (Each Channel)	Turn-On Time	C_{OUT} = 100µF Ceramic, 470µF POSCAP, No Load, TRACK/SS with 0.01µF to GND, V_{IN} = 12V			5		ms
$\Delta V_{OUT(LS)}$ (Each Channel) (Note 7)	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 22µF ×3 Ceramic, 470µF POSCAP, V_{IN} = 12V, V_{OUT} = 1.2V			30		mV
t_{SETTLE} (Each Channel) (Note 7)	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, V_{IN} = 12V, C_{OUT} = 100µF, 470µF POSCAP			20		µs
$I_{OUT(PK)}$ (Each Channel)	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.2V			35		A
Control Section							
V_{FB1}, V_{FB2}	Voltage at V_{FB} Pins	I_{OUT} = 0A, V_{OUT} = 1.2V	●	0.594	0.600	0.606	V
I_{FB}		(Note 5)			–5	–20	nA
V_{OVL}	Feedback Overvoltage Lockout		●	0.64	0.66	0.68	V
TRACK1 (I), TRACK2 (I)	Track Pin Soft-Start Pull-Up Current	TRACK1 (I), TRACK2 (I) Start at 0V		1	1.3	1.5	µA
UVLO	Undervoltage Lockout (Falling)				3.3		V
UVLO Hysteresis					0.6		V
$t_{ON(MIN)}$	Minimum On-Time	(Note 5)			90		ns
R_{FBHI1}, R_{FBHI2}	Resistor Between V_{OUTS1}, V_{OUTS2} and V_{FB1}, V_{FB2} Pins for Each Output			60.05	60.4	60.75	kΩ
V_{PGOOD1}, V_{PGOOD2} Low	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating junction temperature range. Specified as each individual output channel. T_A = 25°C (Note 2), V_{IN} = 12V and V_{RUN1}, V_{RUN2} at 5V unless otherwise noted. Per the typical application in Figure 24.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±5	µA
V_{PGOOD}	PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive			 –10 10		 % %
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 15V		4.8	5	5.2	V
V_{INTVCC} Load Regulation	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			0.75	2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive		4.5	4.7		V
$V_{EXTVCC(DROP)}$	$EXTV_{CC}$ Dropout	I_{CC} = 20mA, V_{EXTVCC} = 5V			50	100	mV
$V_{EXTVCC(HYST)}$	$EXTV_{CC}$ Hysteresis				220		mV
Oscillator and Phase-Locked Loop							
Frequency Nominal	Nominal Frequency	f_{SET} = 1.2V		450	500	550	kHz
Frequency Low	Lowest Frequency	f_{SET} = 0.93V			400		kHz
Frequency High	Highest Frequency	f_{SET} > 2.4V, Up to $INTV_{CC}$			750		kHz
f_{SET}	Frequency Set Current			9	10	11	µA
R_{MODE_PLLIN}	MODE_PLLIN Input Resistance				250		kΩ
CLKOUT	Phase (Relative to V_{OUT1})	PHASMD = GND PHASMD = Float PHASMD = $INTV_{CC}$			60 90 120		Deg Deg Deg
CLK High CLK Low	Clock High Output Voltage Clock Low Output Voltage			2		 0.4	V V
Differential Amplifier							
A_V Differential Amplifier	Gain				1		V/V
R_{IN}	Input Resistance	Measured at DIFFP Input			80		kΩ
V_{OS}	Input Offset Voltage	V_{DIFFP} = $V_{DIFFOUT}$ = 1.5V, $I_{DIFFOUT}$ = 100µA				3	mV
PSRR Differential Amplifier	Power Supply Rejection Ratio	5V < V_{IN} < 15V			90		dB
I_{CL}	Maximum Output Current				2		mA
$V_{OUT(MAX)}$	Maximum Output Voltage	$I_{DIFFOUT}$ = 300µA		$INTV_{CC}$ – 1.4			V
GBW (Note 8)	Gain Bandwidth Product				3		MHz
V_{TEMP}	Diode Connected PNP	I = 100µA			0.6		V
TC	Temperature Coefficient		●		–2.2		mV/°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4650-2 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4650-2E is guaranteed to meet specifications from 0°C to 125°C internal temperature. Specifications over the –40°C to 125°C internal operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4650-2I is guaranteed over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: Two outputs are tested separately, and the same testing condition is applied to each output.

Note 4: The LTM4650-2 device is designed to operate from 400kHz to 750kHz.

Note 5: These parameters are tested at wafer sort.

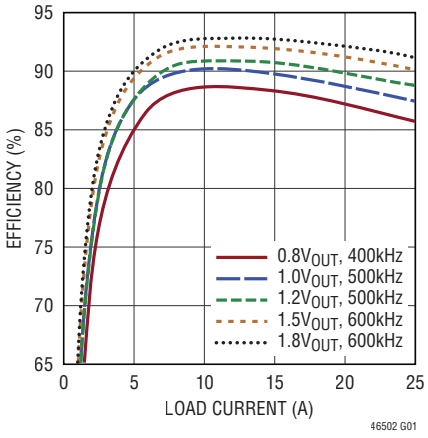
Note 6: See Thermal Considerations and Output Current Derating for different V_{IN}, V_{OUT} and T_A.

Note 7: These typical parameters are based on bench measurements.

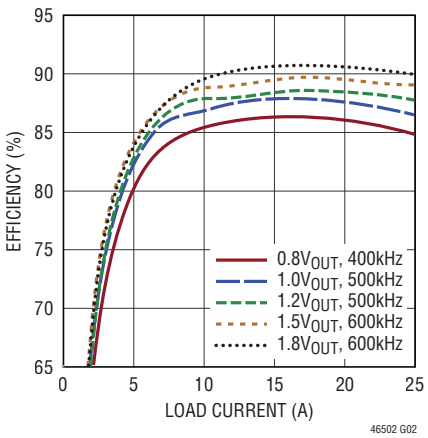
Note 8: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

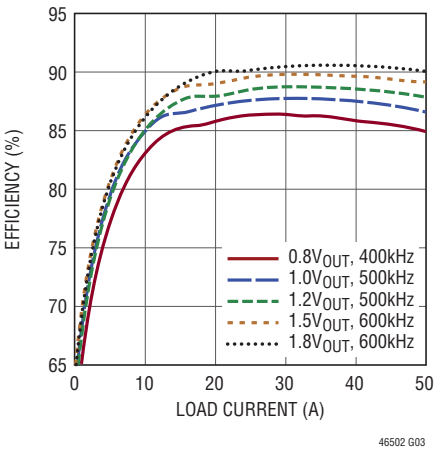
Efficiency vs Output Current, V_{IN} = 5V



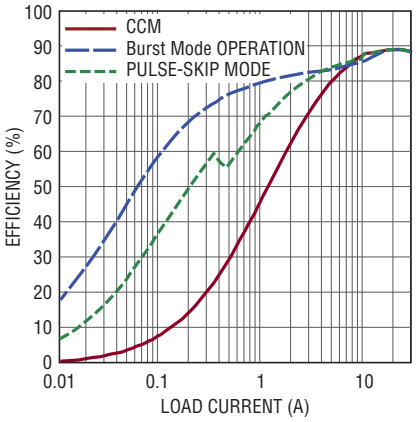
Efficiency vs Output Current, V_{IN} = 12V



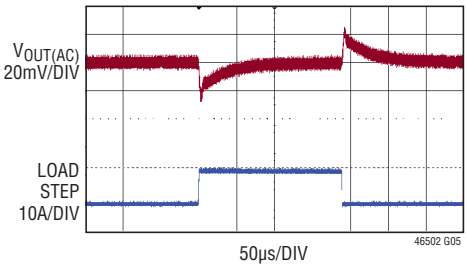
Dual-Phase Single Output Efficiency vs Output Current, V_{IN} = 12V, f_S = 500kHz



Burst Mode and Pulse-Skipping Mode Efficiency V_{IN} = 12V, V_{OUT} = 1.2V, f_S = 500kHz



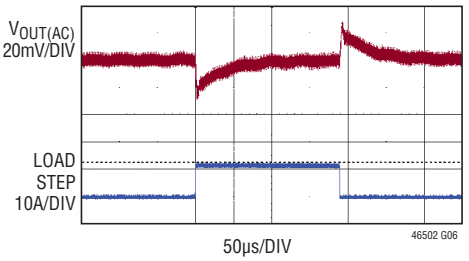
1V Dual-Phase Single Output Load Transient Response



50µs/DIV

$12V_{IN}$, $1V_{OUT}$, 500kHz, 12.5A LOAD STEP,
10A/µs STEP-UP AND STEP-DOWN
C_{OUT} = 220µF ×6 CERAMIC
C_{FF} = 68pF

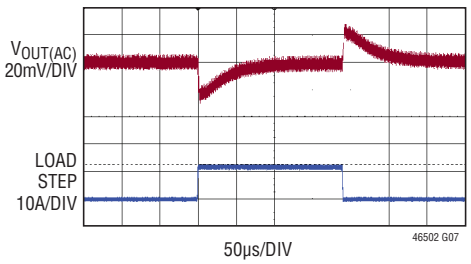
1.2V Dual-Phase Single Output Load Transient Response



50µs/DIV

$12V_{IN}$, $1.2V_{OUT}$, 500kHz, 12.5A LOAD STEP,
10A/µs STEP-UP AND STEP-DOWN
C_{OUT} = 220µF ×6 CERAMIC
C_{FF} = 68pF

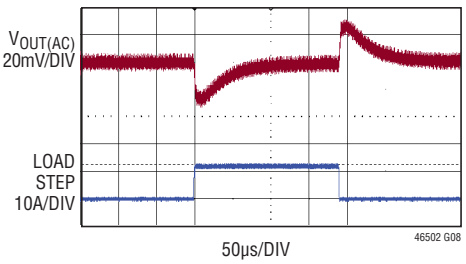
1.5V Dual-Phase Single Output Load Transient Response



50µs/DIV

$12V_{IN}$, $1.5V_{OUT}$, 600kHz, 12.5A LOAD STEP,
10A/µs STEP-UP AND STEP-DOWN
C_{OUT} = 220µF ×6 CERAMIC
C_{FF} = 68pF

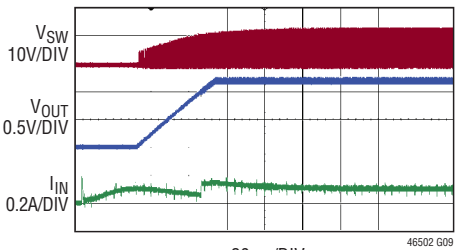
1.8V Dual-Phase Single Output Load Transient Response



50µs/DIV

$12V_{IN}$, $1.8V_{OUT}$, 600kHz, 12.5A LOAD STEP,
10A/µs STEP-UP AND STEP-DOWN
C_{OUT} = 220µF ×6 CERAMIC
C_{FF} = 68pF

Single-Phase Start-Up with No load

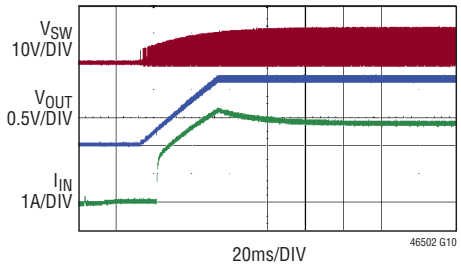


20ms/DIV

$12V_{IN}$, $1.2V_{OUT}$, 500kHz
C_{OUT} = 470µF ×1 POSCAP + 100µF ×2
CERAMIC, C_{SS} = 0.1µF

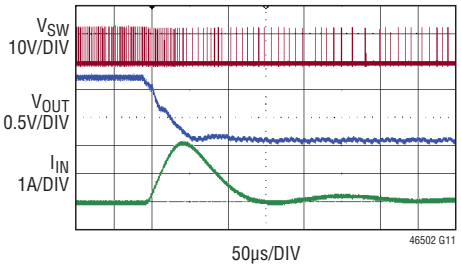
TYPICAL PERFORMANCE CHARACTERISTICS

Single-Phase Start-Up with 25A



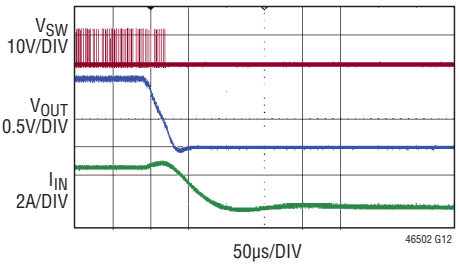
$12V_{IN}$, $1.2V_{OUT}$, 500kHz
C_{OUT} = 470µF ×1 POSCAP + 100µF ×2 CERAMIC, C_{SS} = 0.1µF

Single-Phase Short-Circuit Protection with No load



$12V_{IN}$, $1.2V_{OUT}$, 500kHz
C_{OUT} = 470µF ×1 POSCAP + 100µF ×2 CERAMIC, C_{SS} = 0.1µF

Single-Phase Short-Circuit Protection with 25A



$12V_{IN}$, $1.2V_{OUT}$, 500kHz
C_{OUT} = 470µF ×1 POSCAP + 100µF ×2 CERAMIC

PIN FUNCTIONS (Recommended to use test points to monitor signal pin connections.)

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{OUT1} (A1–A5, B1–B5, C1–C4): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See Table 4.

GND (A6–A7, B6–B7, D1–D4, D9–D12, E1–E4, E10–E12, F1–F3, F10–F12, G1, G3, G10, G12, H1–H7, H9–H12, J1, J5, J8, J12, K1, K5–K8, K12, L1, L12, M1, M12): Power Ground Pins for Both Input and Output Returns.

V_{OUT2} (A8–A12, B8–B12, C9–C12): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See Table 4.

V_{OUTS1}, V_{OUTS2} (C5, C8): This pin is connected to the top of the internal top feedback resistor for each output. The pin can be directly connected to its specific output, or connected to DIFFOUT when the remote sense amplifier is used. In paralleling modules, one of the V_{OUTS} pins is connected to the DIFFOUT pin in remote sensing or directly to V_{OUT} with no remote sensing. It is very important to connect these pins to either the DIFFOUT or V_{OUT} since this is the feedback path and cannot be left open. See the Applications Information section.

f_{SET} (C6): Frequency Set Pin. A 10µA current is sourced from this pin. A resistor from this pin to ground sets a voltage that programs the operating frequency. Alternatively, this pin can be driven with a DC voltage that can set the operating frequency. See the Applications Information section.

SGND (C7, D6, G6–G7, F6–F7): Signal Ground Pin. Return ground path for all analog and low-power circuitry. Tie a single connection to the output capacitor GND in the application. See the layout guidelines in Figure 23.

V_{FB1}, V_{FB2} (D5, D7): The Negative Input of the Error Amplifier for Each Channel. Internally, this pin is connected to V_{OUTS1} or V_{OUTS2} with a 60.4kΩ precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and GND pins. In PolyPhase® operation, tying the V_{FB} pins together allows for parallel operation. See the Applications Information section for details.

TRACK1, TRACK2 (E5, D8): Output Voltage Tracking Pin and Soft-Start Inputs. Each channel has a 1.3µA pull-up current source. When one channel is configured to be the main of the two channels, then a capacitor from this pin

PIN FUNCTIONS (Recommended to use test points to monitor signal pin connections.)

to ground will set a soft-start ramp rate. The remaining channel can be set up as the subordinate and have the main's output applied through a voltage divider to the subordinate output's track pin. This voltage divider equals the subordinate output's feedback divider for coincidental tracking. See the Applications Information section.

COMP1, COMP2 (E6, E7): Current control threshold and error amplifier compensation point for each channel. The current comparator threshold increases with this control voltage. An external RC filter circuit is required for control loop compensation. See the Applications Information section. Connect the COMP pins together for parallel operation. Do not drive this pin.

DIFFP (E8): Positive input of the remote sense amplifier. This pin is connected to the remote sense point of the output voltage. See the Applications Information section.

DIFFN (E9): Negative input of the remote sense amplifier. This pin is connected to the remote sense point of the output GND. See the Applications Information section.

MODE_PLLIN (F4): Forced Continuous Mode, Burst Mode Operation, or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to SGND to force both channels into the forced continuous mode of operation. Connect to $INTV_{CC}$ to enable the pulse-skipping mode of operation. Leaving the pin floating will enable Burst Mode operation. A clock on the pin will force both channels into continuous mode of operation and synchronized to the external clock applied to this pin.

RUN1, RUN2 (F5, F9): Run Control Pin. A voltage above 1.25V will turn on each channel in the module. A voltage below 1.25V on the RUN pin will turn off the related channel. Each RUN pin has a 1µA pull-up current; once the RUN pin reaches 1.2V, an additional 4.5µA pull-up current is added to this pin.

DIFFOUT (F8): Internal Remote Sense Amplifier Output. Connect this pin to V_{OUTS1} or V_{OUTS2} depending, on which output is using remote sense. In parallel operation, connect one of the V_{OUTS} pin to DIFFOUT for remote sensing.

SW1, SW2 (G2, G11): Switching node of each channel that is used for testing purposes. Also, an R-C snubber network can be applied to reduce or eliminate switch node ringing or otherwise leave floating. See the Applications Information section.

PHASMD (G4): Connect this pin to SGND, $INTV_{CC}$, or floating this pin to select the phase of CLKOUT to 60 degrees, 120 degrees, and 90 degrees respectively.

CLKOUT (G5): Clock output with phase control using the PHASMD pin to enable multiphase operation between devices. See the Applications Information section.

PGOOD1, PGOOD2 (G9, G8): Output Voltage Power Good Indicator. Open drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point.

$INTV_{CC}$ (H8): Internal 5V Regulator Output. The control circuits and internal gate drivers are powered from this voltage. Decouple this pin to PGND with a 4.7µF low ESR tantalum or ceramic. $INTV_{CC}$ is activated when either RUN1 or RUN2 is activated.

TEMP (J6): Temperature Monitor. An internal diode connected the NPN transistor between this pin and SGND with a 10nF filtering capacitor. See the Applications Information section.

$EXTV_{CC}$ (J7): External power input that is enabled through a switch to $INTV_{CC}$ whenever $EXTV_{CC}$ is greater than 4.7V. Do not exceed 6V on this input, and connect this pin to V_{IN} when operating V_{IN} on 5V. An efficiency increase will occur, which is a function of the (V_{IN} – $INTV_{CC}$) multiplied by the power MOSFET driver current. The typical current requirement is 30mA. V_{IN} must be applied before $EXTV_{CC}$, and $EXTV_{CC}$ must be removed before V_{IN}.

V_{IN} (M2–M11, L2–L11, J2–J4, J9–J11, K2–K4, K9–K11): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

SIMPLIFIED BLOCK DIAGRAM

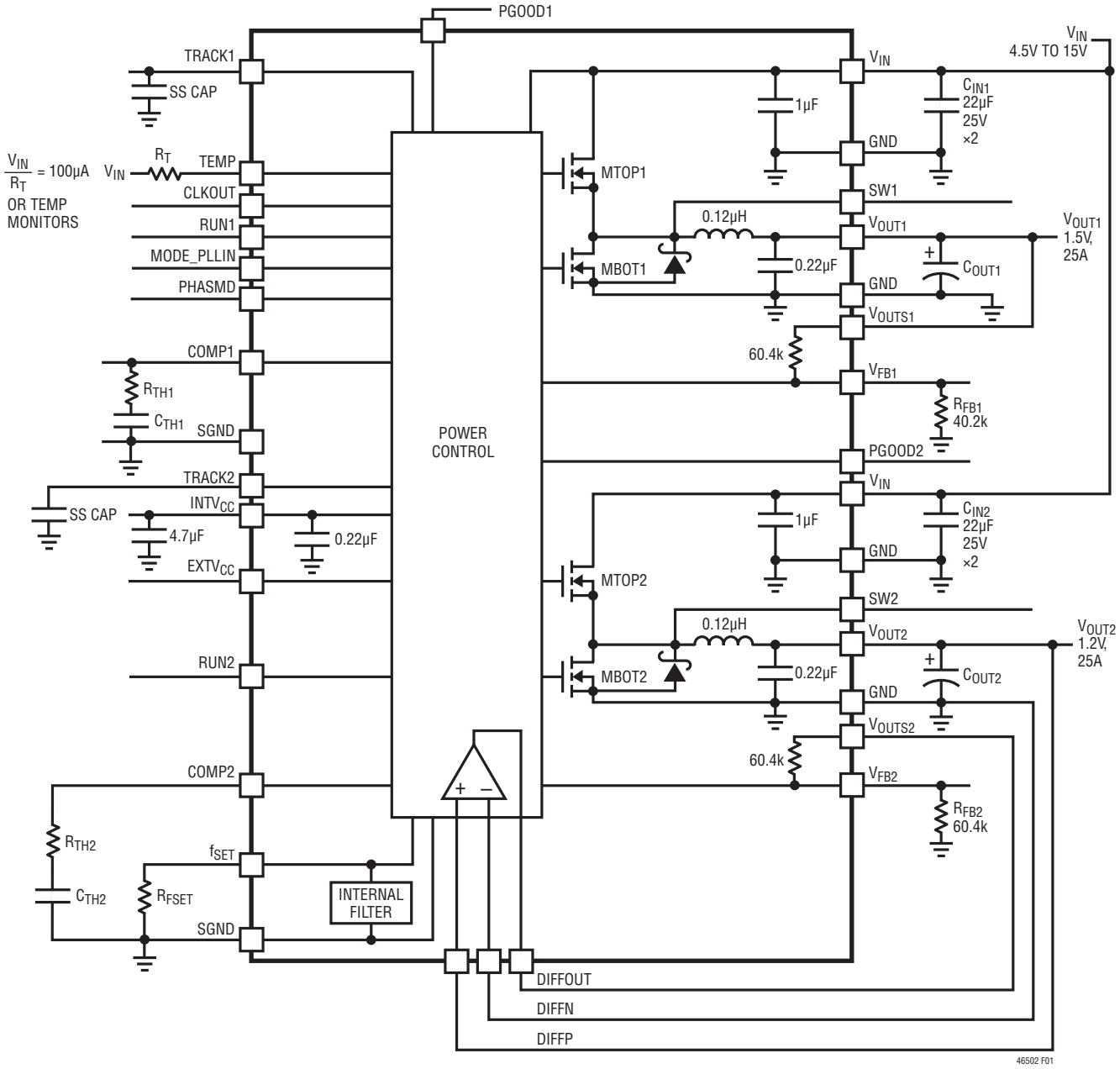


Figure 1. Simplified LTM4650-2 Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN1}, C_{IN2}	External Input Capacitor Requirement (V_{IN1} = 4.5V to 15V, V_{OUT1} = 1.5V) (V_{IN2} = 4.5V to 15V, V_{OUT2} = 1.0V)	 I_{OUT1} = 25A I_{OUT2} = 25A	 44 44	 66 66		 µF µF
C_{OUT1} C_{OUT2}	External Output Capacitor Requirement (V_{IN1} = 4.5V to 15V, V_{OUT1} = 1.5V) (V_{IN2} = 4.5V to 15V, V_{OUT2} = 1.0V)	 I_{OUT1} = 25A I_{OUT2} = 25A	 600 600	 800 800		 µF µF

OPERATION

POWER MODULE DESCRIPTION

The LTM4650-2 is a dual-output standalone nonisolated switching mode DC/DC power supply with ±1.5% total DC output error over line, load and temperature variation. It can provide two 25A outputs with few external input and output capacitors and setup components. This module provides precisely regulated output voltages programmable via external resistors from 0.6VDC to 1.8VDC over 4.5V to 15V input voltages. The typical application schematic is shown in Figure 24.

The LTM4650-2 has dual integrated constant-frequency current mode regulators and built-in power MOSFET devices with fast switching speed. The typical switching frequency is from 400kHz to 600kHz, depending on the output voltage. For switching-noise sensitive applications, it can be externally synchronized from 400kHz to 750kHz. A resistor can be used to program a free run frequency on the f_{SET} pin. See the Applications Information section.

With current mode control, the LTM4650-2 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit and foldback current limit in an overcurrent condition. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD outputs low if the output feedback voltage exits a ±10% window around the regulation point. As the output voltage exceeds 10% above regulation, the bottom MOSFET will turn on to clamp the output voltage. The top MOSFET will be turned off. This overvoltage protect is feedback voltage referred.

Pulling the RUN pins below 1.1V forces the regulators into a shutdown state by turning off both MOSFETs. The TRACK pins are used for programming the output voltage ramp and voltage tracking during start-up or for soft-starting the regulator. See the Applications Information section.

An external RC filtering circuit is required to achieve fast Type II control loop compensation. Table 4 provides a guideline for input, output capacitances and RC COMP values for several operating conditions. The Analog Devices µModule power design tool (LTpowerCAD) will be provided for transient and stability analysis. The V_{FB} pin is used to program the output voltage with a single external resistor to ground. A differential remote sense amplifier is available for sensing the output voltage accurately on one of the outputs at the load point or in parallel operation sensing the output voltage at the load point.

The multiphase operation can be easily employed with the MODE_PLLIN, PHASMD, and CLKOUT pins. Up to 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHASMD pin to different levels. See the Applications Information section.

High efficiency at light loads can be accomplished with selectable Burst Mode operation or pulse-skipping operation using the MODE_PLLIN pin. These light-load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section. See the Applications Information section for details.

A general-purpose temperature diode is included inside the module to monitor the temperature of the module. See the Applications Information section for details.

The switch pins are available for functional operation monitoring, and a resistor-capacitor snubber circuit can be carefully placed on the switch pin to ground to dampen any high-frequency ringing on the transition edges. See the Applications Information section for details.

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The typical LTM4650-2 application circuit is shown in Figure 24. External component selection is primarily determined by the maximum load current and output voltage. See Table 4 for specific external capacitor requirements for particular applications.

OUTPUT TOTAL DC ACCURACY AND AC TRANSIENT PERFORMANCE

In modern ASIC and FPGA power supply designs, a tight total voltage regulation window, ±3% for example, is required of the supply powering the core and periphery. To meet this requirement, the supply's DC voltage variance plus any AC voltage variation that may occur during any load step transient must fall within this allowed window. The DC voltage variance is determined by the accuracies of the supply's reference voltage, resistor divider, load regulation and line regulation over the operating temperature range. The AC voltage variance is determined by the supply's output voltage overshoot and undershoots in response to a load transient condition for a given output capacitor network.

Figure 2 shows a typical load step transient response waveform and DC voltage accuracy variance. For a given allowable voltage regulation window, a tighter DC voltage accuracy allows more margin for the AC variation due to a load transient response. This increased margin for AC variation allows for a reduction in the total output capacitance required to meet the regulation window requirement. This allows for a reduced total solution cost and footprint area.

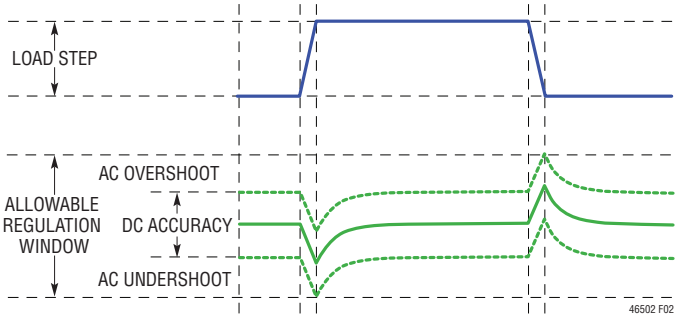

Figure 2. Typical Load Step Transient Response with DC Voltage Accuracy Variance

For example, in an FPGA core voltage application, for a 12V input, 0.9V output at 72A design, a total overall ±3% total voltage regulation window is required in responding to a 25% load step transient. Figure 3 illustrates the benefit of overall output capacitor reduction versus improved total DC accuracy by using 100µF ceramic output capacitors.

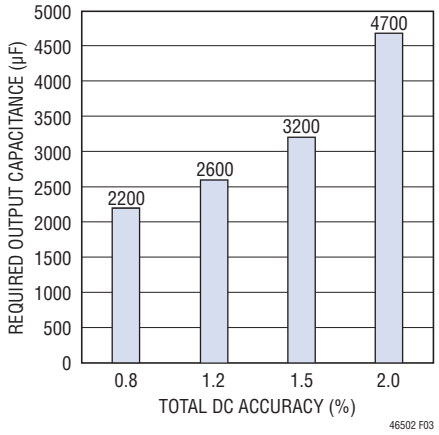

Figure 3. Overall Output Capacitor vs Total DC Accuracy

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage. Each output of the LTM4650-2 is capable of a 98% duty cycle, but the V_{IN} to V_{OUT} minimum dropout is still shown as a function of its load current and will limit output current capability related to the high duty cycle on the top side switch. Minimum on-time $t_{ON(MIN)}$ is another consideration in operating at a specified duty cycle while operating at a certain frequency because $t_{ON(MIN)} < D/f_{SW}$, where D is the duty cycle and f_{SW} is the switching frequency. $t_{ON(MIN)}$ is specified in the Electrical parameters as 90ns.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Simplified Block Diagram, a 60.4k internal feedback resistor connects between the V_{OUTS1} to V_{FB1} and V_{OUTS2} to V_{FB2}. These pins must be connected to their respective outputs for proper feedback regulation. Overvoltage can occur if these V_{OUTS1} and V_{OUTS2} pins are left floating when used as individual regulators, or at least one of them is used in paralleled regulators. The output voltage will default to 0.6V with no feedback resistor on

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either V_{FB1} or V_{FB2}. Adding a resistor R_{FB} from the V_{FB} pin to GND programs the output voltage:

$$V_{OUT} = 0.6V \bullet \frac{60.4k + R_{FB}}{R_{FB}}$$

Table 1. V_{FB} Resistor vs Various Output Voltages

V_{OUT}	0.6V	0.8V	0.9V	1.0V	1.2V	1.5V	1.8V
R_{FB}	Open	182k	121k	90.9k	60.4k	40.2k	30.2k

For parallel operation of multiple channels, the same feedback setting resistor can be used for the parallel design. This is done by connecting the V_{OUTS1} to the output, as shown in Figure 4, thus tying one of the internal 60.4k resistors to the output. All of the V_{FB} pins tie together with one programming resistor, as shown in Figure 4.

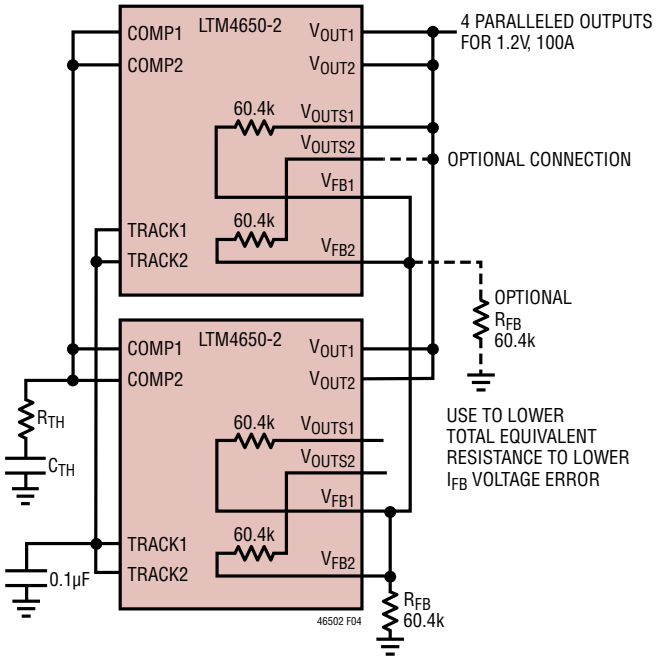

Figure 4. 4-Phase Parallel Configurations

In parallel operation, the V_{FB} pins have an I_{FB} current of 20nA maximum for each channel. To reduce output voltage error due to this current, an additional V_{OUTS} pin can be tied to V_{OUT}, and an additional R_{FB} resistor can be used to lower the total Thevenin equivalent resistance seen by this current. For example in Figure 4, the total Thevenin equivalent resistance of the V_{FB} pin is (60.4k//R_{FB}), which is 30.2k where R_{FB} is equal to 60.4k for a 1.2V output. Four phases connected in parallel equates to a worse-case feedback current of 4 • I_{FB} = 80nA maximum. The voltage error is 80nA • 30.2k = 2.4mV. If V_{OUTS2} is connected, as shown in Figure 4, to V_{OUT}, and another 60.4k resistor is connected from V_{FB2} to ground, then the voltage error is reduced to 1.2mV. If the voltage error is acceptable, then no additional connections are necessary. The onboard 60.4k resistor is 0.5% accurate, and the V_{FB} resistor can be chosen by the user to be as accurate as needed. All COMP pins are tied together for current sharing between the phases. The TRACK/SS pins can be tied together, and a single soft-start capacitor can be used to soft-start the regulator. The soft-start equation must have the soft-start current parameter increased by the number of paralleled channels. See the Output Voltage Tracking section.

Input Capacitors

The LTM4650-2 module should be connected to a low AC-impedance DC source. For the regulator input, two 22µF input ceramic capacitors are required for each channel for RMS ripple current. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low-impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, η% is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor, Polymer capacitor.

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Output Capacitors

The LTM4650-2 is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or a ceramic capacitor. The typical output capacitance range for each output is from 400µF to 600µF. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 4 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 12.5A (25%) and 25A (50%) load step transient. Table 4 optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 4 matrix, and the Analog Devices LTpowerCAD® design tool will be provided for stability analysis. In multi LTM4650-2 paralleling applications, Table 4 RC compensation value is still valid in terms of having one set of RC filters on each of the paralleling modules while connecting all the COMP, FB and V_{OUT} pins together. See Figure 29 and the Multiphase Operation section. The multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The Analog Devices LTpowerCAD design tool can calculate the output ripple reduction as the number of implemented phases increases by N times. A small value 10Ω to 50Ω resistor can be placed in series from V_{OUT} to the V_{OUTS} pin to allow for a bode plot analyzer to inject a signal into the control loop and validate the regulator stability. The same resistor could be placed in series from V_{OUT} to DIFFP, and a bode plot analyzer could inject a signal into the control loop and validate the regulator stability.

Burst Mode Operation

The LTM4650-2 is capable of Burst Mode operation on each regulator in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. Burst Mode operation is enabled with the MODE_PLLIN pin floating. During this operation, the peak current of the inductor is set to approximately one-third of the maximum peak current value in normal operation, even though the voltage at the COMP pin indicates a lower value. The voltage at the COMP pin drops when the inductor's average current is greater than the load requirement. As the COMP voltage drops below 0.5V, the BURST comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current to about 450µA for each output. The load current is now being supplied from the output capacitors. When the output voltage drops, causing COMP to rise above 0.5V, the internal sleep line goes low, and the LTM4650-2 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET, and the switching cycle repeats. Either regulator can be configured for Burst Mode operation.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4650-2 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE_PLLIN pin to $INTV_{CC}$ enables pulse-skipping operation. At light loads, the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode. This mode will maintain higher effective frequencies thus lower output ripple and lower noise than Burst Mode operation. Either regulator can be configured for pulse-skipping mode.

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Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE_PLLIN pin to GND. In this mode, the inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, the forced continuous mode is disabled, and the inductor current is prevented from reversing until the LTM4650-2's output voltage is in regulation. Either regulator can be configured for forced continuous mode.

Multiphase Operation

For output loads that demand more than 25A of current, two outputs in LTM4650-2 or even multiple LTM4650-2s can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples. The MODE_PLLIN pin allows the LTM4650-2 to synchronize to an external clock (between 400kHz and 750kHz), and the internal phase-locked-loop allows the LTM4650-2 to lock onto the incoming clock phase as well. The CLKOUT signal can be connected to the MODE_PLLIN pin of the following stage to line up both the frequency and the phase of the entire system. Tying the PHASMD pin to $INTV_{CC}$, SGND, or floating generates a phase difference (between MODE_PLLIN and CLKOUT) of 120 degrees, 60 degrees, or 90 degrees respectively. A total of 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHASMD pin of each LTM4650-2 channel to different levels. Figure 5 shows a 2-phase design, a 4-phase design and a 6-phase design example for clock phasing with the PHASMD table.

PHASMD	SGND	FLOAT	$INTV_{CC}$
CONTROLLER1	0	0	0
CONTROLLER2	180	180	240
CLKOUT	60	90	120

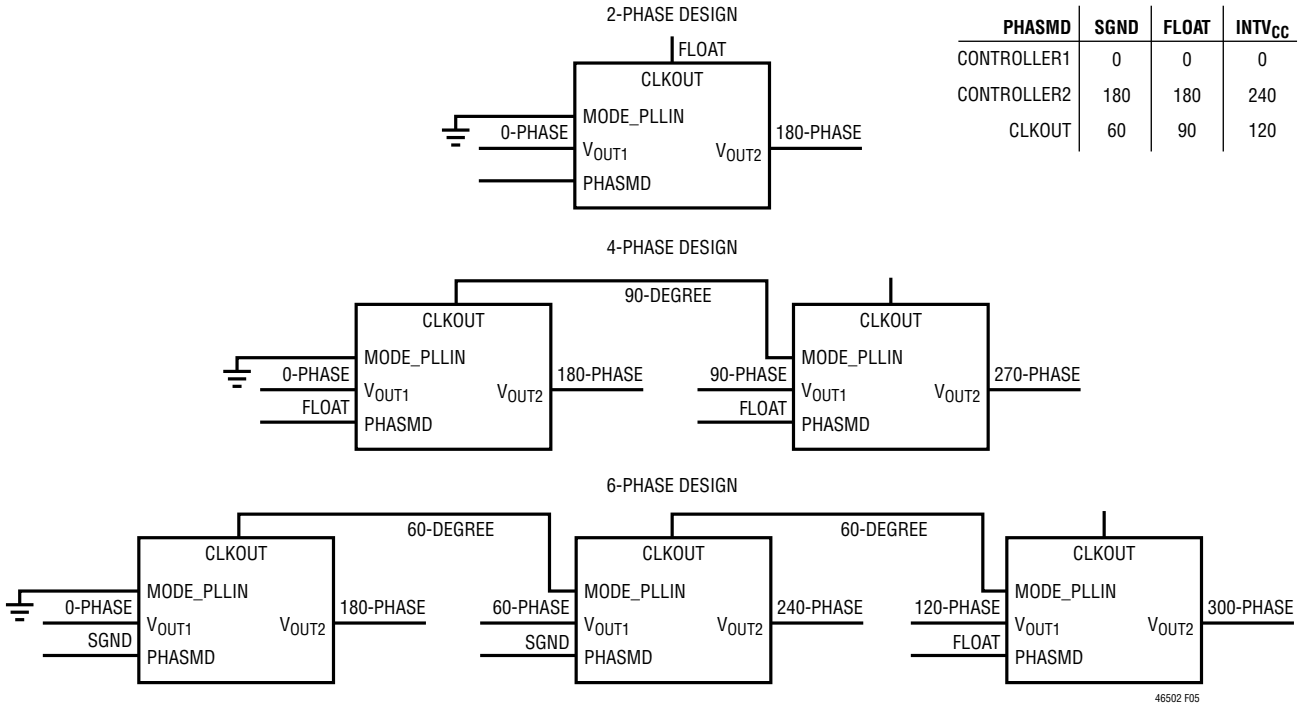

Figure 5. Examples of 2-Phase, 4-Phase, and 6-Phase Operation with PHASMD Table

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A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high-output current design.

In multi LTM4650-2s parallel applications, C_{TH} and R_{TH} values in Table 4 are still valid to achieve a ±3% transient response in a 25% load step. Connect one set of RC (R_{TH} and C_{TH}) networks to the COMP pin of each paralleling module. Then, connect the COMP pins, FB pins, TRACK/SS pin and V_{OUT} pins from different modules together. See Figure 29 for an example of parallel operation. LTpowerCAD power design tool can also be used to optimize loop compensation and transient performance if only one set of RC (R_{TH} and C_{TH}) network is to be added to the common COMP pins.

The LTM4650-2 device is an inherently current mode-controlled device so that the parallel modules will have very good current sharing. This will balance the thermals on the design. Figure 29 shows an example of parallel operation and pin connection.

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 6 shows this graph.

Frequency Selection and Phase-Lock Loop (MODE_PLLIN and f_{SET} Pins)

The LTM4650-2 device is operated over a range of frequencies to improve power conversion efficiency. It is recommended to operate the module at 400kHz for output voltage below 1.0V, 500kHz for output voltage between 1.0V to 1.5V and 600kHz for output voltage above 1.5V for the best efficiency and inductor current ripple.

The LTM4650-2 switching frequency can be set with an external resistor from the f_{SET} pin to SGND. An accurate 10µA current source into the resistor will set a voltage that programs the frequency, or a DC voltage can be applied. Figure 7 shows a graph of frequency setting versus programming voltage. An external clock can be applied to the MODE_PLLIN pin from 0V to $INTV_{CC}$ over a frequency range of 400kHz to 750kHz. The clock input high threshold is 1.6V, and the clock input low threshold is 1V. The LTM4650-2 has the PLL loop filter components on board. The frequency setting resistor should always be present to set the initial switching frequency before locking to an external clock. Both regulators will operate in continuous mode while being externally clock.

The output of the PLL phase detector has a pair of complementary current sources that charge and discharge the internal filter network. When the external clock is applied, the f_{SET} frequency resistor is disconnected with an internal switch, and the current sources control the frequency adjustment to lock to the incoming external clock. When no external clock is applied, the internal switch is on, thus connecting the external f_{SET} frequency set resistor for free-run operation.

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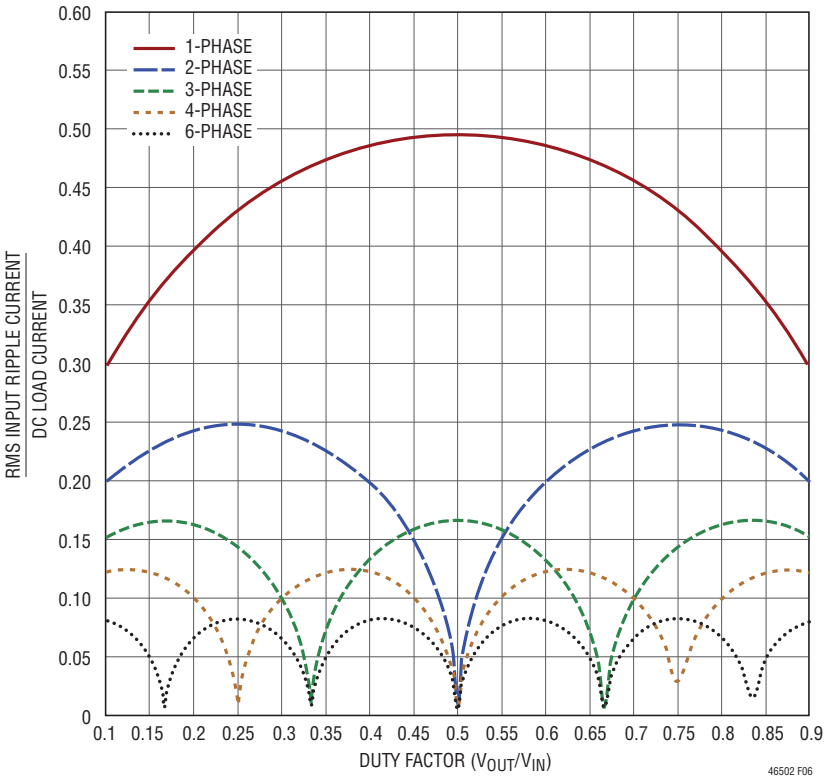

Figure 6. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

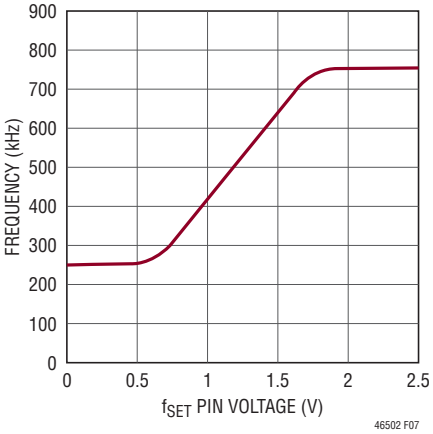

Figure 7. Operating Frequency vs f_{SET} Pin Voltage

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Minimum On-Time

Minimum on-time t_{ON} is the smallest time duration that the LTM4650-2 is capable of turning on the top MOSFET on either channel. It is determined by internal timing delays, and the gate charge required turning on the top MOSFET. Low-duty cycle applications may approach this minimum on-time limit, and care should be taken to ensure that:

$$\frac{V_{OUT}}{V_{IN} \bullet FREQ} > t_{ON(MIN)}$$

If the duty cycle falls below what can be accommodated by the minimum on time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the output ripple and current will increase. The on-time can be increased by lowering the switching frequency. A good rule of thumb is to keep on time longer than 110ns.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK pins. The output can be tracked up and down with another regulator. The main regulator's output is divided down with an external resistor divider that is the same as the subordinate regulator's feedback divider to implement coincident tracking. The LTM4650-2 uses an accurate 60.4k resistor internally for the top feedback resistor for each channel. Figure 8 shows an example of coincident tracking. The equation:

$$SUBORDINATE = \left(1 + \frac{60.4k}{R_{TA}}\right) \bullet V_{TRACK}$$

V_{TRACK} is the track ramp applied to the subordinate's track pin. V_{TRACK} has a control range of 0V to 0.6V, or the internal reference voltage. When the main's output is divided down with the same resistor values used to set the subordinate's output, then the subordinate will coincident

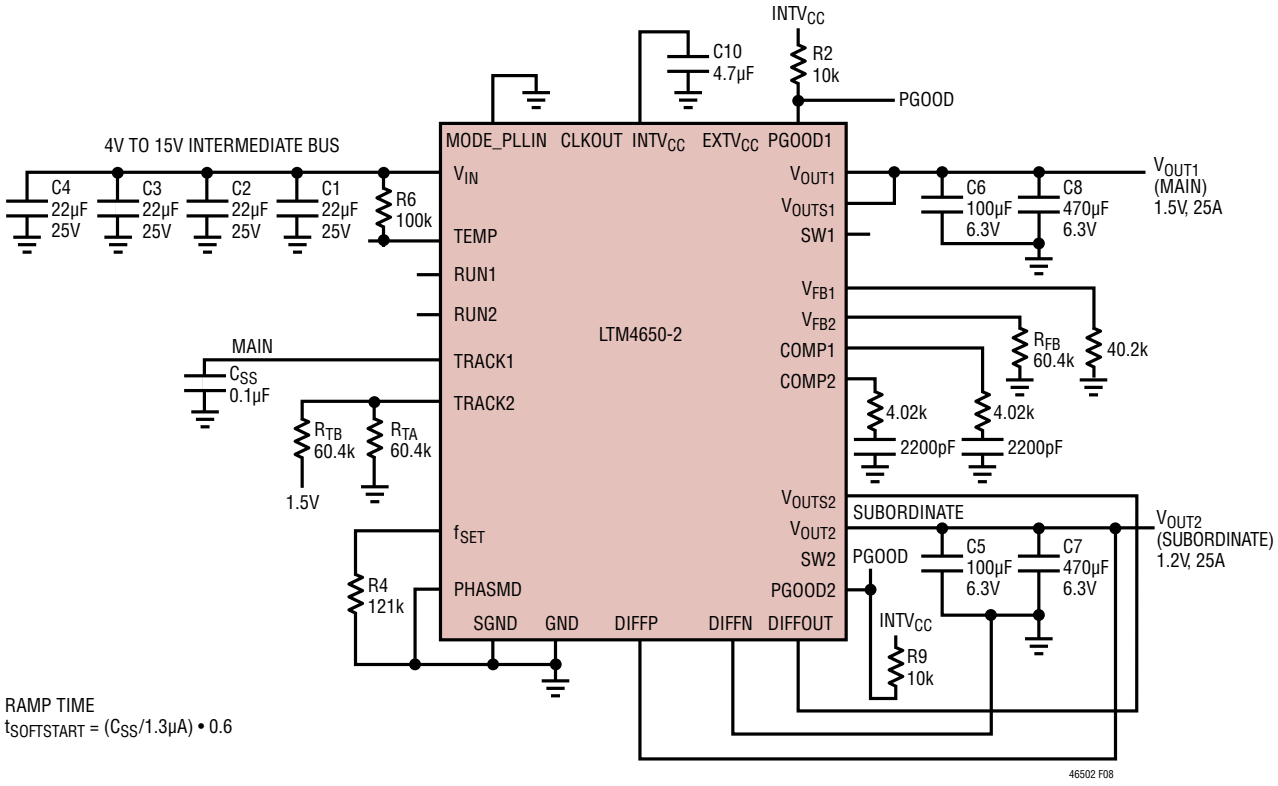

Figure 8. Example of Output Tracking Application Circuit

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track with the main until it reaches its final value. The main will continue to its final value from the subordinate's regulation point. Voltage tracking is disabled when V_{TRACK} is more than 0.6V. R_{TA} in Figure 8 will be equal to the R_{FB} for coincident tracking. Figure 9 shows the coincident tracking waveforms.

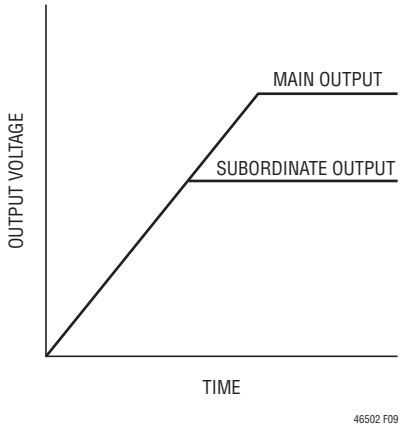

Figure 9. Output Coincident Tracking Waveform

The TRACK pin of the main can be controlled by a capacitor placed on the main regulator TRACK pin to ground. A 1.3µA current source will charge the TRACK pin up to the reference voltage and then proceed up to $INTV_{CC}$. After the 0.6V ramp, the TRACK pin will no longer be in control, and the internal voltage reference will control output regulation from the feedback divider. The foldback current limit is disabled during this sequence of turn-on during tracking or soft-starting. The TRACK pins are pulled low when the RUN pin is below 1.2V. The total soft-start time can be calculated as:

$$t_{SOFT\text{-}START} = \left(\frac{C_{SS}}{1.3\mu A}\right) \bullet 0.6$$

Regardless of the mode selected by the MODE_PLLIN pin, the regulator channels will always start in pulse-skipping mode up to TRACK = 0.5V. Between TRACK = 0.5V and 0.54V, it will operate in forced continuous mode and revert to the selected mode once TRACK > 0.54V. To track with another channel once in steady state operation, the LTM4650-2 is forced into continuous mode operation as soon as V_{FB} is below 0.54V, regardless of the setting on the MODE_PLLIN pin.

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the main's TRACK pin. As mentioned above, the TRACK pin has a control range from 0 to 0.6V. The main's TRACK pin slew rate is directly equal to the main's output slew rate in Volts/Time. The equation:

$$\frac{MR}{SR} \bullet 60.4k = R_{TB}$$

where MR is the main's output slew rate, and SR is the subordinate's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal. Thus R_{TB} is equal to the 60.4k. R_{TA} is derived from the equation:

$$R_{TA} = \frac{0.6V}{\frac{V_{FB}}{60.4k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R_{TB}}}$$

where V_{FB} is the feedback voltage reference of the regulator, and V_{TRACK} is 0.6V. Since R_{TB} is equal to the 60.4k top feedback resistor of the subordinate regulator in equal slew rate or coincident tracking, then R_{TA} is equal to R_{FB} with $V_{FB} = V_{TRACK}$. Therefore, R_{TB} = 60.4k, and R_{TA} = 60.4k in Figure 8.

In ratiometric tracking, a different slew rate may be desired for the subordinate regulator. R_{TB} can be solved when SR is slower than MR. Make sure that the subordinate supply slew rate is chosen to be fast enough so that the subordinate output voltage will reach its final value before the main output.

For example, MR = 1.5V/1ms, and SR = 1.2V/1ms. Then R_{TB} = 76.8k. Solve for R_{TA} to equal to 49.9k.

Each of the TRACK pins will have the 1.3µA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller values resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used, to reduce the TRACK pin offset to a negligible value.

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Power Good

The PGOOD pins are open drain pins that can be used to monitor valid output voltage regulation. This pin monitors a 10% window around the regulation point. A resistor can be pulled up to a particular supply voltage no greater than 6V maximum for monitoring.

Stability Compensation

An external RC filtering circuit is required to add from COMP to SGND to achieve fast Type II control loop compensation. Table 4 is provided for most application requirements. The Analog Devices µModule power design tool (LTpowerCAD) will be provided for other control loop optimization.

Run Enable

The RUN pins have an enable threshold of 1.4V maximum, typically 1.25V, with 150mV of hysteresis. They control the turn on each of the channels and $INTV_{CC}$. These pins can be pulled up to V_{IN} for 5V operation, or a 5V Zener diode can be placed on the pins, and a 10k to 100k resistor can be placed up to higher than 5V input to enable the channels. The RUN pins can also be used for output voltage sequencing. In parallel operation, the RUN pins can be tied together and controlled from a single control. See the Typical Applications circuits in Figure 24.

$INTV_{CC}$ and $EXTV_{CC}$

The LTM4650-2 module has an internal 5V low dropout regulator that is derived from the input voltage. This regulator is used to power the control circuitry and the power MOSFET drivers. This regulator can source up to 70mA, and typically uses ~30mA for powering the device at the maximum frequency. This internal 5V supply is enabled by either RUN1 or RUN2.

$EXTV_{CC}$ allows an external 5V supply to power the LTM4650-2 and reduces power dissipation from the internal low dropout 5V regulator. The power loss savings can be calculated by:

$$(V_{IN} – 5V) • 30mA = PLOSS$$

$EXTV_{CC}$ has a threshold of 4.7V for activation, and a maximum rating of 6V. When using a 5V input, connect this 5V input to $EXTV_{CC}$ also to maintain a 5V gate drive level. $EXTV_{CC}$ must sequence on after V_{IN}, and $EXTV_{CC}$ must sequence off before V_{IN}.

Differential Remote Sense Amplifier

An accurate differential remote sense amplifier is provided to sense low output voltages accurately at the remote load points. This is especially true for high current loads. The amplifier can be used on one of the two channels, or on a single parallel output. It is very important that the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to either V_{OUTS1} or V_{OUTS2}. In parallel operation, the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to one of the V_{OUTS} pins. See the parallel schematics in Figure 25 and see Figure 4.

SW Pins

The SW pins are generally for testing purposes by monitoring these pins. These pins can also be used to dampen out switch node ringing caused by LC parasitic in the switched current paths. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance, and the capacitor is chosen only to affect the high-frequency ringing across the resistor. If the stray inductance or capacitance can be measured or approximated, then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First, the SW pin can be monitored with a wide bandwidth scope with a high-frequency scope probe. The ring frequency can be measured by its value. The impedance Z can be calculated:

$$Z_L = 2\pi fL,$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by: $Z_C = 1/(2\pi fC)$. These values are a good place to start with. Modifications to these components

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should be made to attenuate the ringing with the least amount of power loss.

Temperature Monitoring

Measuring the absolute temperature of a diode is possible due to the relationship between current, voltage and temperature described by the classic diode equation:

$$I_D = I_S \bullet e^{\left(\frac{V_D}{\eta \bullet V_T}\right)}$$

or

$$V_D = \eta \bullet V_T \bullet \ln\frac{I_D}{I_S}$$

where I_D is the diode current, V_D is the diode voltage, η is the ideality factor (typically close to 1.0) and I_S (saturation current) is a process-dependent parameter. V_T can be broken out into:

$$V_T = \frac{k \bullet T}{q}$$

where T is the diode junction temperature in Kelvin, q is the electron charge, and k is Boltzmann's constant. V_T is approximately 26mV at room temperature (298K) and scales linearly with Kelvin temperature. It is this linear temperature relationship that makes diodes suitable temperature sensors. The I_S term in the previous equation is the extrapolated current through a diode junction when the diode has zero volts across the terminals. The I_S term varies from process to process, varies with temperature, and by definition must always be less than I_D. Combining all of the constants into one term:

$$K_D = \frac{\eta \bullet k}{q}$$

where $K_D = 8.62 \bullet 10^{-5}$, and knowing $\ln(I_D/I_S)$ is always positive because I_D is always greater than I_S, leaves us with the equation that:

$$V_D = T(KELVIN) \bullet K_D \bullet \ln\frac{I_D}{I_S}$$

where V_D appears to increase with temperature. It is common knowledge that a silicon diode biased with a current source has an approximate –2mV/°C temperature relationship (Figure 10), which is at odds with the equation. In fact, the I_S term increases with temperature, reducing the $\ln(I_D/I_S)$ absolute value and yielding an approximate –2mV/°C composite diode voltage slope.

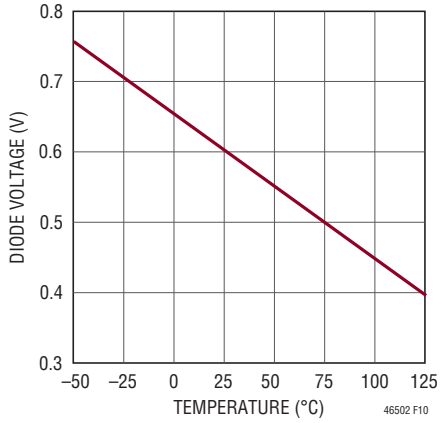

Figure 10. Diode Voltage V_D vs Temperature T (°C)

To obtain a linear voltage proportional to temperature, we cancel the I_S variable in the natural logarithm term to remove the I_S dependency from the equation. This is accomplished by measuring the diode voltage at two currents I_1, and I_2, where $I_1 = 10 \bullet I_2$) and subtracting, we get:

$$\Delta V_D = T(KELVIN) \bullet K_D \bullet IN\frac{I_1}{I_S} - T(KELVIN) \bullet K_D \bullet IN\frac{I_2}{I_S}$$

Combining like terms, then simplifying the natural log terms yields:

$$\Delta V_D = T(KELVIN) \bullet K_D \bullet IN(10)$$

and redefining constant

$$K_D' = K_D \bullet IN(10) = \frac{198\mu V}{K}$$

yields

$$\Delta V_D = K'_D \bullet T(KELVIN)$$

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Solving for temperature:

$$T(KELVIN) = \frac{\Delta V_D}{K_D'}\ (-CELSIUS) = T(KELVIN) - 273.15$$

where

300°K = 27°C

means that is we take the difference in voltage across the diode measured at two currents with a ratio of 10, the resulting voltage is 198µV per Kelvin of the junction with a zero intercept at 0 Kelvin.

The diode-connected PNP transistor at the TEMP pin can be used to monitor the internal temperature of the LTM4650-2. See Figure 25 for an example.

Improve Transient Response and Reduce Output Capacitance with AVP

Fast load transient response, limited board space and low cost are requirements of microprocessor power supplies. Active voltage positioning improves transient response and reduces the output capacitance required to power a microprocessor, where in this case, a typical load step can be from 0A to 12.5A in 1µs or 12.5A to 0A in 1µs.

Active voltage positioning is a form of deregulation. It sets the output voltage high for light loads and low for heavy loads. When the load current suddenly increases, the output voltage starts from a level higher than the nominal, so the output voltage can drop more and stay within the specified voltage range. When the load current suddenly decreases, the output voltage starts at a level lower than the nominal, so the output voltage can have more overshoot and stay within the specified voltage range. Less output capacitance is required when voltage positioning is used because more voltage variation is allowed on the output capacitors.

Figure 30 and Figure 32 show the voltage regulator without AVP and with AVP. The load transient response before and after AVP implementation are shown on Figure 31 and Figure 33. On the design with AVP, the output voltage swings from 1.05V at minimum load to 0.95V at full load. The transient performance has been improved, while using fewer output capacitors.

The Analog Devices design tool (LTpowerCAD) will be provided for AVP applications.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 (Test Boards for Area Array Surface Mount Package Thermal Measurements). The motivation for providing these thermal coefficients is found in JESD 51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance on thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased as follows:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in one cubic foot sealed enclosure. This environment is sometimes referred to as "still air", although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

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2. $\theta_{JCbottom}$, the thermal resistance from the junction to the bottom of the product case, is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don't generally match the user's application.

3. θ_{JCtop}, the thermal resistance from the junction to the top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages, but the test conditions don't generally match the user's application.

4. θ_{JB}, the thermal resistance from the junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured at a specified distance from the package using a two-sided, two-layered board. This board is described in JESD 51-9.

A graphical representation of the aforementioned thermal resistances is shown in Figure 11; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conducts exclusively through the top or exclusively through the bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware that there are multiple power devices and components dissipating power, with the consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring

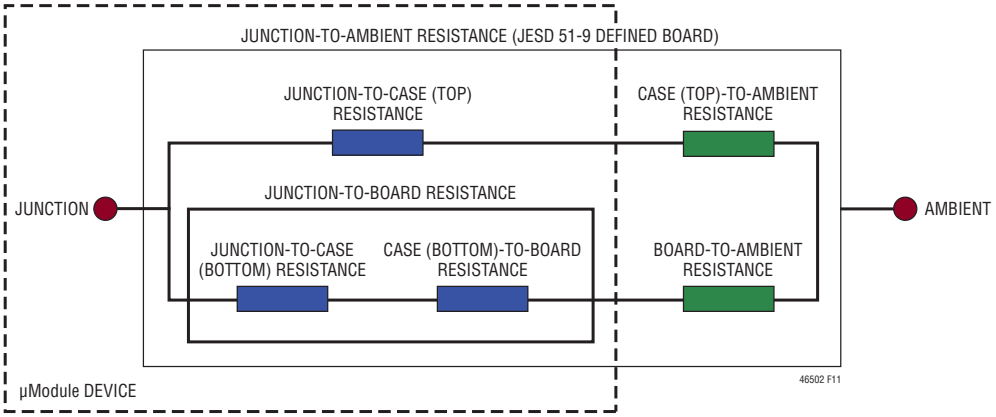

Figure 11. Graphical Representation of JESD51-12 Thermal Coefficients

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practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory tests have been performed and correlated to the µModule model, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the µModule model with no airflow or heat sinking in a properly defined chamber. This θ_{JB} + θ_{BA} value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into the ambient with no airflow or top-mounted heat sink. Each system has its own thermal characteristics, therefore thermal analysis must be performed by the user in a particular system.

The LTM4650-2 module has been designed to effectively remove heat from both the top and bottom of the package. The bottom substrate material has very low thermal resistance to the printed circuit board. An external heat sink can be applied to the top of the device for excellent heat sinking with airflow.

Figure 12 shows a temperature plot of the LTM4650-2 with 12V input, 1.0V output at 50A without a heat sink and a no airflow condition.

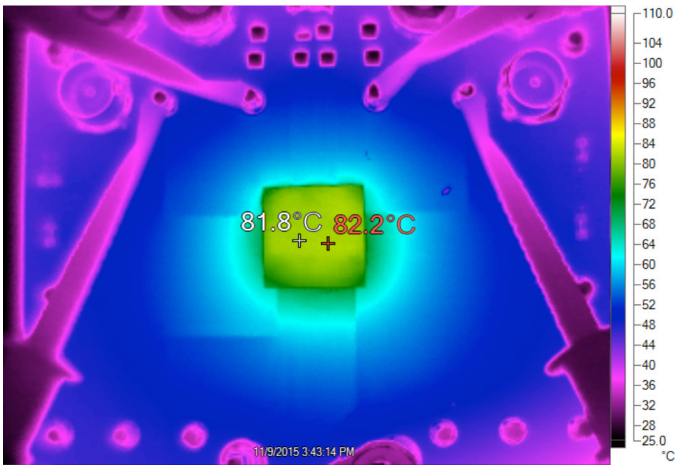

Figure 12. Thermal Image 12V to 1V, 50A with No Airflow and No Heat Sink (Based on 4-Layer 101mm × 114mm PCB Board Containing 2oz Copper on the Top, Bottom and All Internal Layers)

Safety Considerations

The LTM4650-2 modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support over current protection. A temperature diode is provided for monitoring internal temperature, and can be used to detect the need for thermal shutdown that can be done by controlling the RUN pin.

Power Derating

The 0.9V and 1.5V power loss curves in Figure 13 and Figure 14 can be used in coordination with the load current derating curves in Figure 15 to Figure 22 for calculating an approximate θ_{JA} thermal resistance for the LTM4650-2 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with a 1.2 multiplicative factor at 120°C.

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The derating curves are plotted with CH1 and CH2 in parallel single output operation starting at 50A of load with low ambient temperature. The output voltages are 0.9V and 1.5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber, along with thermal modeling analysis.

The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at ~120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased.

The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 16, the load current is derated to ~35A at ~90°C with 200LFM air, but not heat sink and the power loss for the 12V to 0.9V at 35A output is a ~5.6W loss. The 5.6W loss is calculated with the ~4.7W room temperature loss from the 12V to 0.9V power loss curve at 35A, and the 1.20 multiplying factor at 120°C junction temperature. If the 90°C ambient temperature is subtracted from

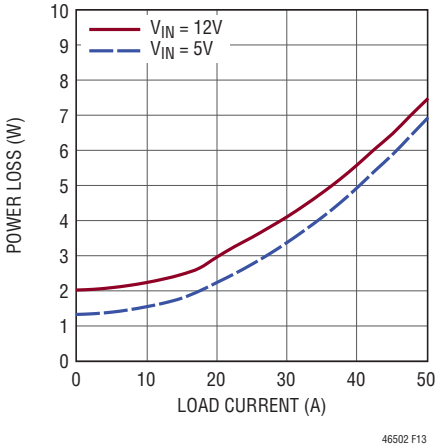

Figure 13. 0.9V Output Power Loss Curve

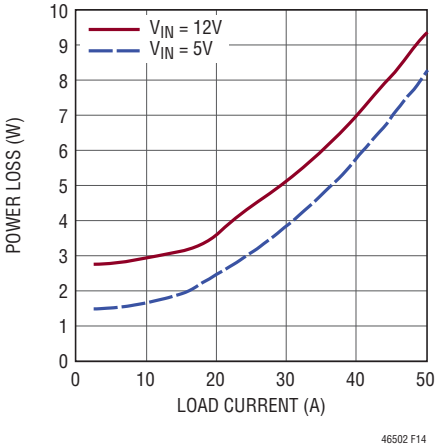

Figure 14. 1.5V Output Power Loss Curve

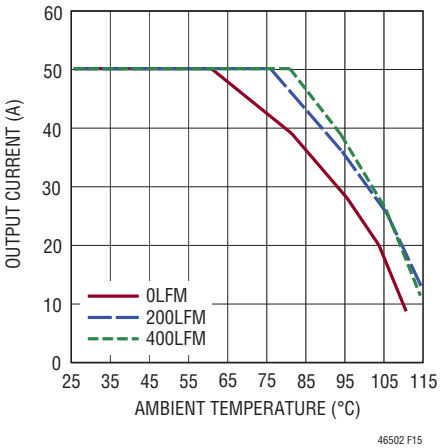

Figure 15. 5V to 0.9V Derating Curve, No Heat Sink

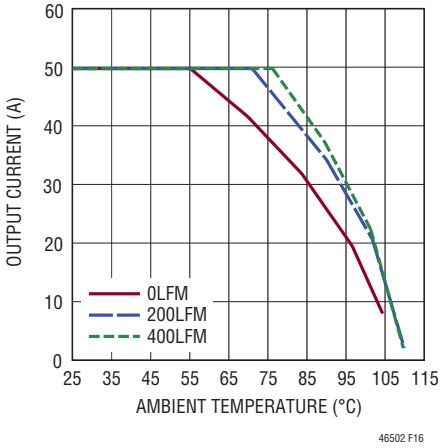

Figure 16. 12V to 0.9V Derating Curve, No Heat Sink

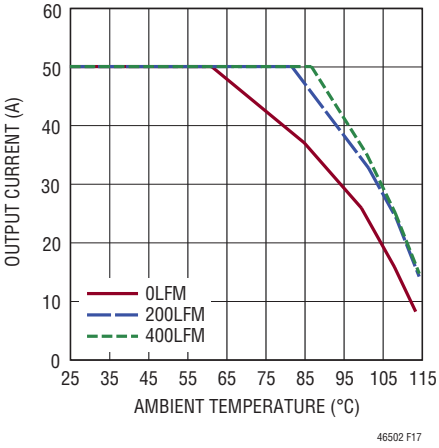

Figure 17. 5V to 0.9V Derating Curve, BGA Heat Sink

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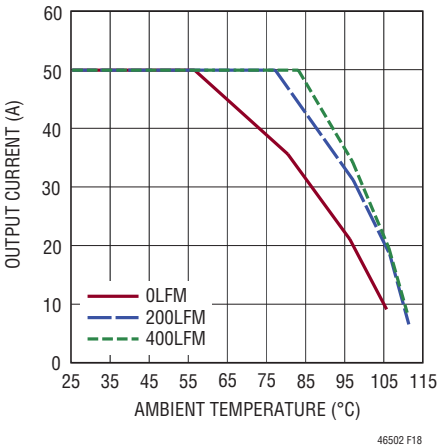

Figure 18. 12V to 0.9V Derating Curve, BGA Heat Sink

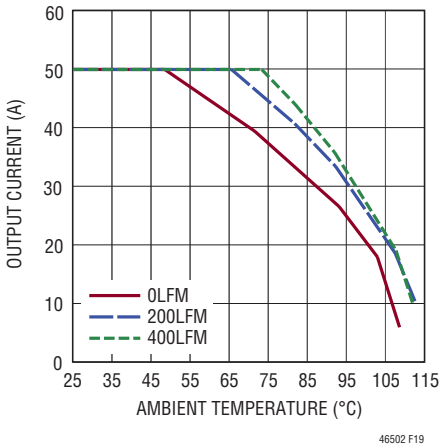

Figure 19. 5V to 1.5V Derating Curve, No Heat Sink

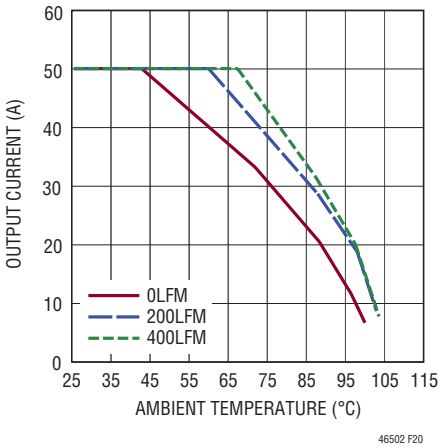

Figure 20. 12V to 1.5V Derating Curve, No Heat Sink

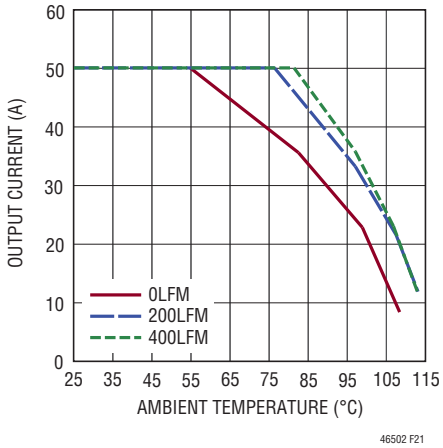

Figure 21. 5V to 1.5V Derating Curve, BGA Heat Sink

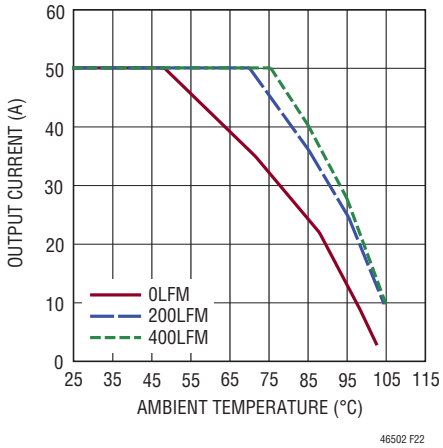

Figure 22. 12V to 1.5V Derating Curve, BGA Heat Sink

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the 120°C junction temperature, then the difference of 30°C divided by 5.5W equals a 5.4°C/W θ_{JA} thermal resistance. Table 2 specifies a 5.5°C/W value, which is pretty close. Table 2 and Table 3 provide equivalent thermal resistances for 0.9V and 1.5V outputs with and without airflow and heat sinking.

The derived thermal resistances in Table 2 and Table 3 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick 4-layer board with 2oz copper on each layer. The PCB dimensions are 101mm × 114mm. The BGA heat sinks are listed in Table 3.

Table 2. 0.9V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 15, Figure 16	5, 12	Figure 13	0	None	7.5
Figure 15, Figure 16	5, 12	Figure 13	200	None	5.5
Figure 15, Figure 16	5, 12	Figure 13	400	None	5
Figure 17, Figure 18	5, 12	Figure 13	0	BGA Heat Sink	7
Figure 17, Figure 18	5, 12	Figure 13	200	BGA Heat Sink	4.5
Figure 17, Figure 18	5, 12	Figure 13	400	BGA Heat Sink	4

Table 3. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 19, Figure 20	5, 12	Figure 14	0	None	7.5
Figure 19, Figure 20	5, 12	Figure 14	200	None	5.5
Figure 19, Figure 20	5, 12	Figure 14	400	None	5
Figure 21, Figure 22	5, 12	Figure 14	0	BGA Heat Sink	7
Figure 21, Figure 22	5, 12	Figure 14	200	BGA Heat Sink	4.5
Figure 21, Figure 22	5, 12	Figure 14	400	BGA Heat Sink	4

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Wakefield	LTN20069-T5	wakefield-vette.com

Table 4. Output Voltage Response vs Component Matrix (See Figure 25) Load Step Typical Measured Values

C_{IN} (CERAMIC)			C_{OUT} (CERAMIC)			C_{OUT} (BULK)		
VENDOR	VALUE	PART NUMBER	VENDOR	VALUE	PART NUMBER	VENDOR	VALUE	PART NUMBER
2-Phase Single Output Solution								
Murata	22µF, 16V, X5R, 1210	GRM32ER61C226KE20L	Murata	100µF, 6.3V, X5R, 1210	GRM32ER60J107ME20L	Panasonic	680µF, 2.5V, 6mΩ	2R5TPF680M6L
Murata	22µF, 16V, X5R, 1206	GRM31CR61C226KE15K	Murata	220µF, 4V, X5R, 1206	GRM31CR60G227M	Panasonic	470µF, 2.5V, 3mΩ	EEFGX0E471R
TDK	22µF, 16V, X5R, 1210	C3225X5R1C226M250AA	Taiyo Yuden	100µF, 6.3V, X5R, 1210	JMK325BJ107MM-T			
			Taiyo Yuden	220µF, 4V, X5R, 1210	AMK325ABJ227MM-T			

PEAK-PEAK DEVIATION PERCENTAGE	V_{IN} (V)	V_{OUT} (V)	C_{IN}* BULK (µF)	C_{IN} CERAMIC (µF)	C_{OUT} BULK (µF)	C_{OUT} CERAMIC (µF)	COMP PIN PARALLEL CAPACITOR C_{THP} (pF)	COMP PIN RESISTOR R_{TH} (kΩ)	COMP PIN CAPACITOR C_{TH}	FEED-FORWARD CAPACITOR $C_{FF\ (pF)}$	PEAK-PEAK DEVIATION V_{PK-PK} (mV)	SETTLING TIME t_{SETTLE} (µs)	CTRL LOOP BAND-WIDTH BW (kHz)	CTRL LOOP PHASE MARGIN (PM)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)	R_{FB} (kΩ)	FREQ (kHz)
25% Load Step (0A to 12.5A) Ceramic Output Capacitor Only Solutions																		
±3% (<60mV)	12	1	150	22 ×2	None	220 ×6	33	3.24	10nF	68	53	80	88	47 Deg	12.5	10	90.9	500
±3% (<72mV)	12	1.2	150	22 ×2	None	220 ×5	33	3.24	10nF	68	56	80	89	49 Deg	12.5	10	60.4	500
±3% (<90mV)	12	1.5	150	22 ×2	None	220 ×4	33	3.24	10nF	68	58	80	91	58 Deg	12.5	10	40.2	600
±3% (<108mV)	12	1.8	150	22 ×2	None	220 ×4	33	3.24	10nF	68	64	90	98	65 Deg	12.5	10	30.2	600
25% Load Step (0A to 9A) Bulk plus Ceramic Output Capacitor Solutions																		
±3% (<60mV)	12	1	150	22 ×2	470 ×2	100 ×4	33	3.16	3300pF	68	55	30	82	68 Deg	12.5	10	90.9	500
±3% (<72mV)	12	1.2	150	22 ×2	470 ×2	100 ×4	33	3.16	3300pF	68	55	30	82	73 Deg	12.5	10	60.4	500
±3% (<90mV)	12	1.5	150	22 ×2	470 ×2	100 ×4	82	4.12	3300pF	None	64	30	59	53 Deg	12.5	10	40.2	600
±3% (<108mV)	12	1.8	150	22 ×2	470 ×2	100 ×4	82	4.12	3300pF	None	75	30	51	58 Deg	12.5	10	30.2	600
50% Load Step (0A to 25A) Ceramic Output Capacitor Only Solutions																		
±3% (<60mV)	12	1	150	22 ×2	None	220 ×12	33	6.81	4.7nF	100	58	80	76	45 Deg	25	10	90.9	500
±3% (<72mV)	12	1.2	150	22 ×2	None	220 ×12	33	6.81	4.7nF	100	61	80	77	50 Deg	25	10	60.4	500
±3% (<90mV)	12	1.5	150	22 ×2	None	220 ×14	33	5.90	4.7nF	None	90	80	47	45 Deg	25	10	40.2	600
±3% (<108mV)	12	1.8	150	22 ×2	None	220 ×14	33	5.90	4.7nF	None	105	90	43	50 Deg	25	10	30.2	600
50% Load Step (0A to 25A) Bulk + Ceramic Output Capacitor Solutions																		
±3% (<60mV)	12	1	150	22 ×2	470 ×6	100 ×4	33	12.0k	3300pF	47	47	30	70	57 Deg	25	10	90.9	500
±3% (<72mV)	12	1.2	150	22 ×2	470 ×6	100 ×4	33	12.0k	3300pF	47	48	30	67	65 Deg	25	10	60.4	500
±3% (<90mV)	12	1.5	150	22 ×2	470 ×6	100 ×4	68	10.2k	3300pF	None	56	40	50	49 Deg	25	10	40.2	600
±3% (<108mV)	12	1.8	150	22 ×2	470 ×6	100 ×4	82	14.5k	3300pF	None	58	50	51	46 Deg	25	10	30.2	600

*Bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads.

APPLICATIONS INFORMATION

Layout Checklist/Example

The high integration of LTM4650-2 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, V_{OUT1} and V_{OUT2}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high-frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high-frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between the top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to the GND underneath the unit.
- For parallel modules, tie the V_{OUT}, V_{FB}, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied to a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 23 gives a good example of the recommended layout. LGA and BGA PCB layouts are identical, with the exception of circle pads for BGA (see Package Description section).

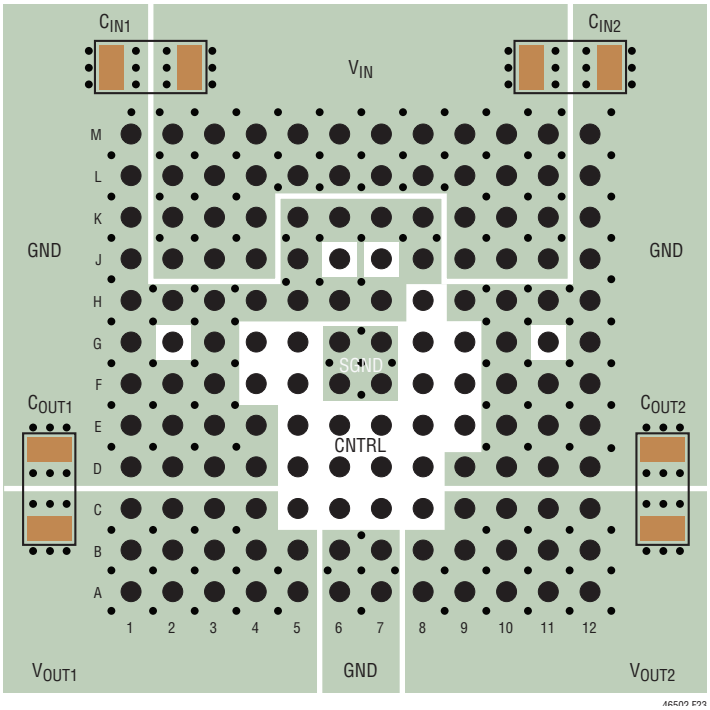


Figure 23. Recommended PCB Layout

TYPICAL APPLICATIONS

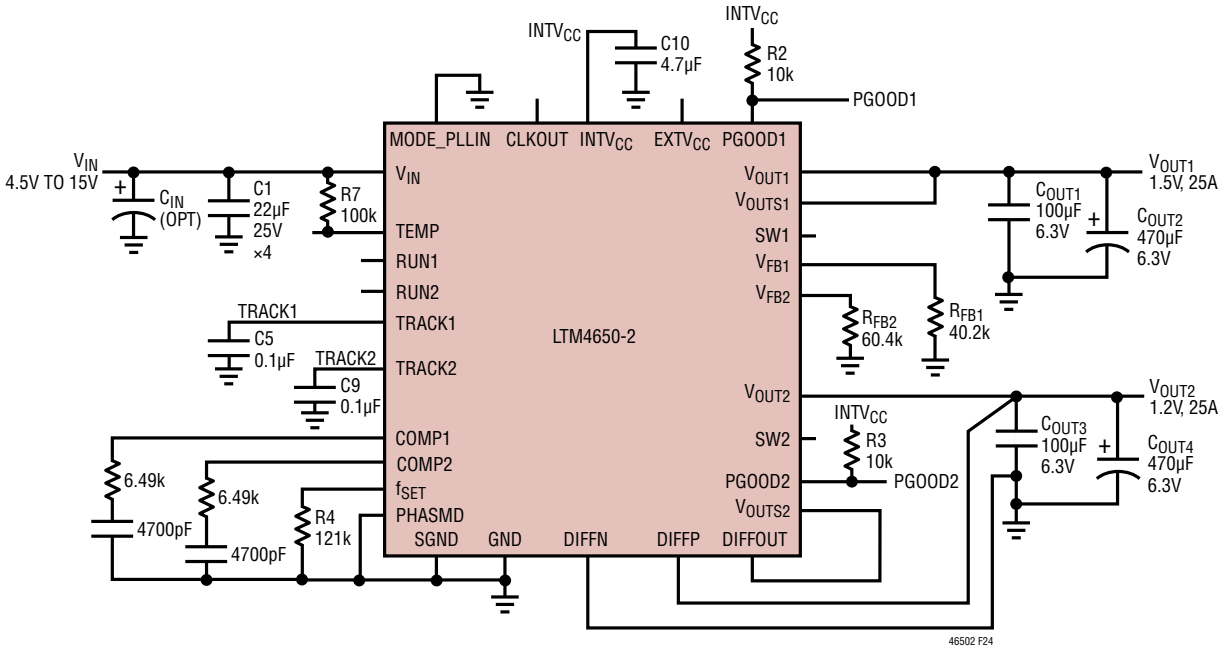


Figure 24. Typical 4.5V_{IN} to 15V_{IN}, 1.5V and 1.2V at 25A Outputs

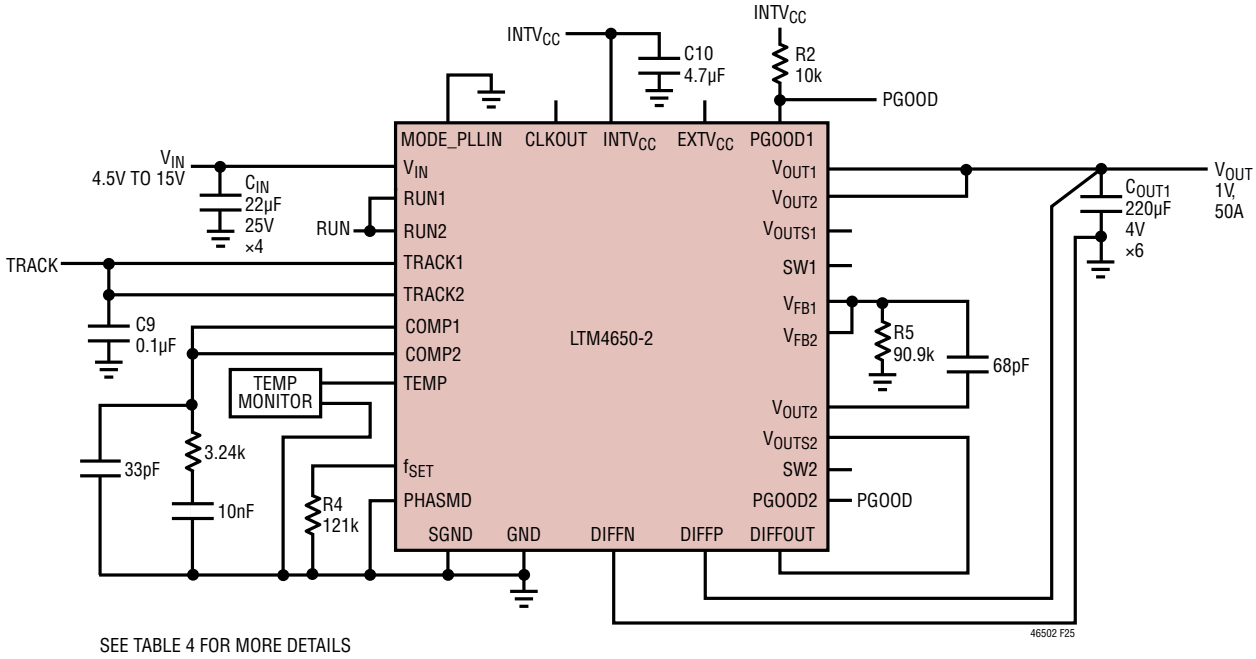


Figure 25. 2-Phase, 1V at 50A Design

TYPICAL APPLICATIONS

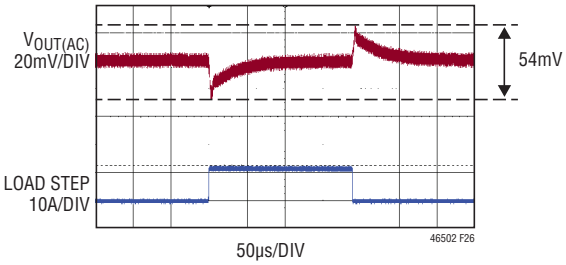


Figure 26. 25%, 12.5A Load Step Transient Waveform of Figure 25 Circuit

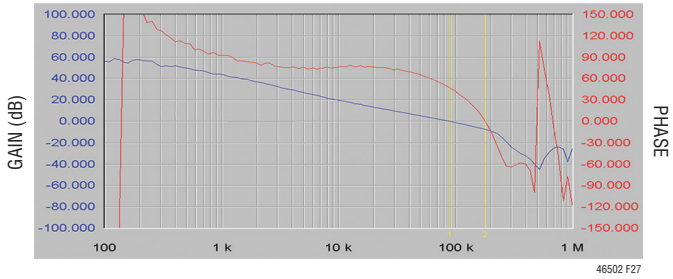


Figure 27. Bode Plot of Figure 25 Circuit

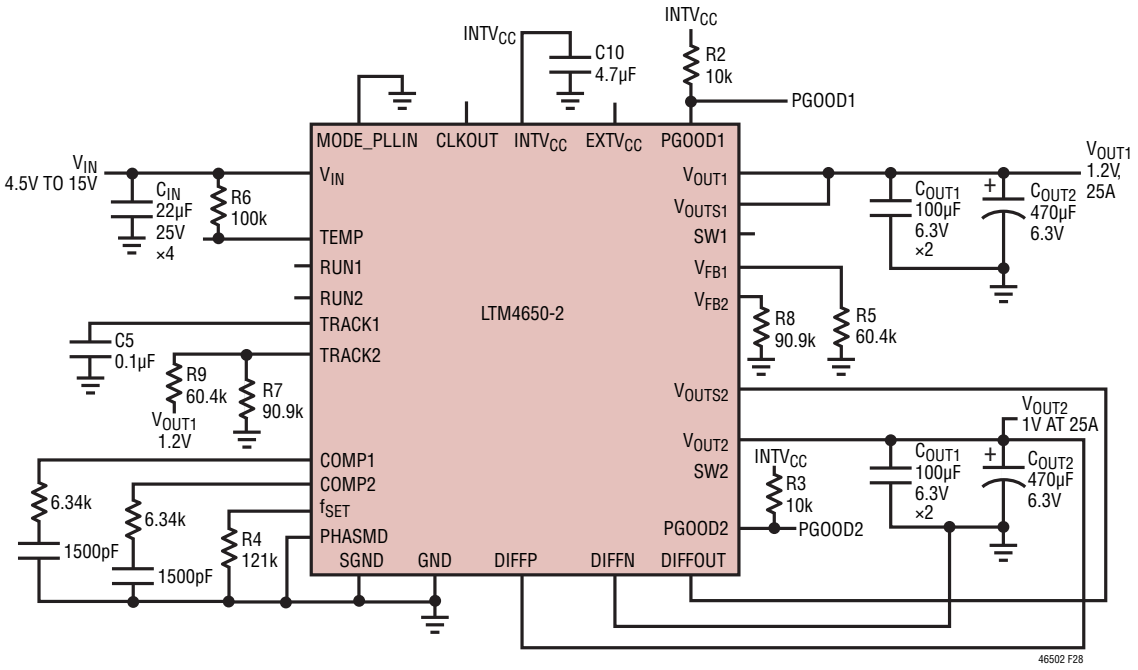


Figure 28. 1.2V and 1V Output Tracking

TYPICAL APPLICATION

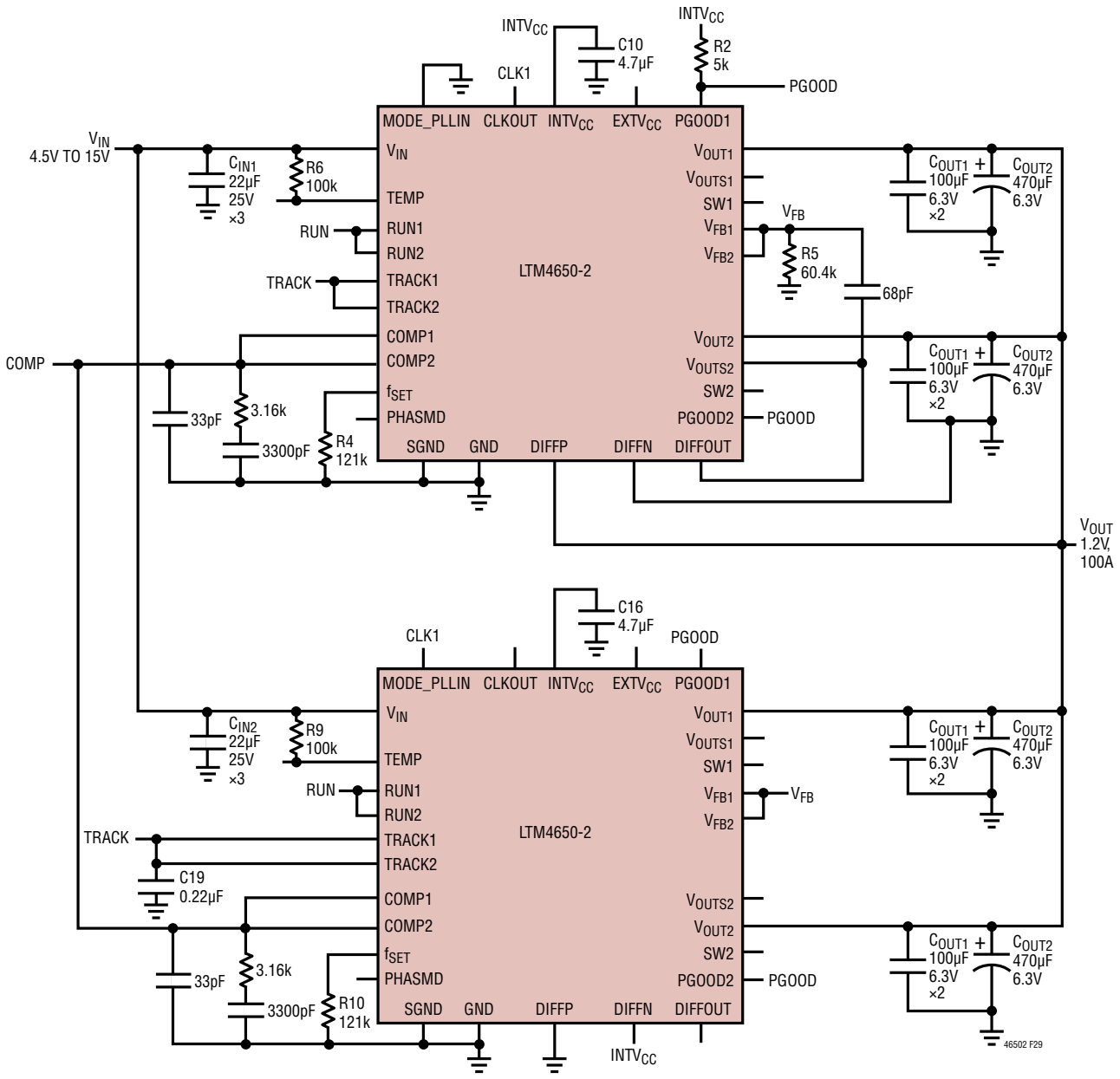


Figure 29. 4-Phase, 1.2V at 100A

TYPICAL APPLICATION

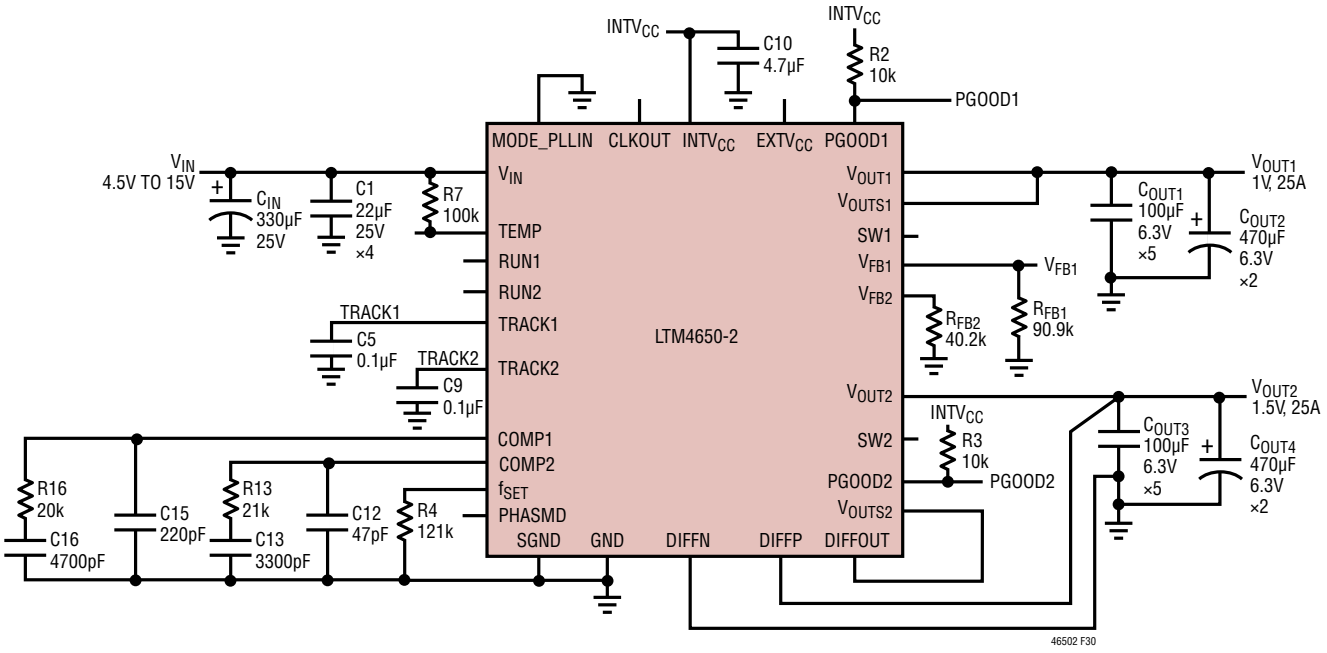


Figure 30. Circuit without AVP, Typical 4.5V_{IN} to 15V_{IN}, 1V_{OUT} and 1.5V_{OUT} at 25A

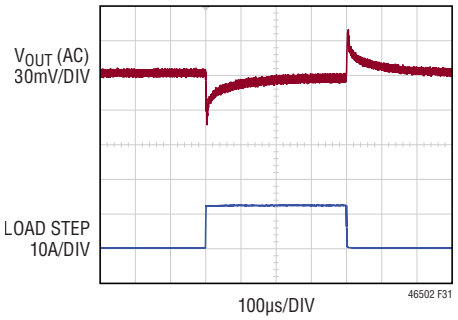


Figure 31. Load Transient Waveform of Figure 30 Circuit (without AVP), 12V_{IN}, 1V_{OUT}, 500kHz, 12.5A (50% of Full Load, Slew Rate 12.5A/µs), C_{OUT1} = 100µF ×5 Ceramic, C_{OUT2} = 470µF ×2 POSCAP

TYPICAL APPLICATION

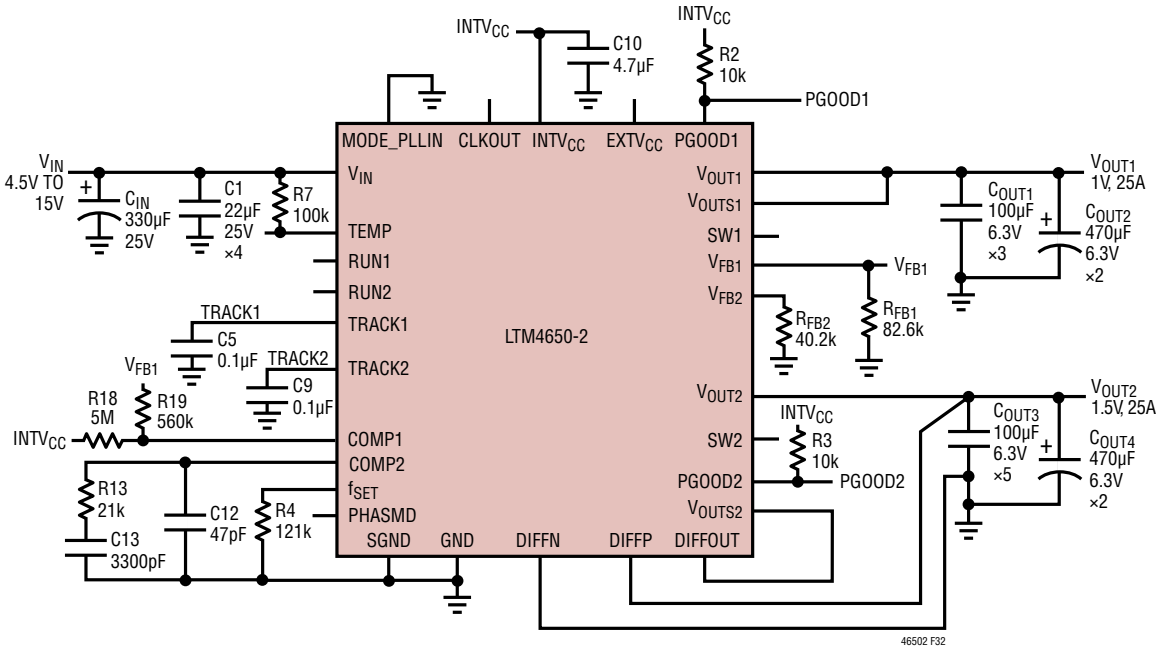


Figure 32. Circuit with AVP, Typical 4.5V_{IN} to 15V_{IN}, 1V_{OUT} (with AVP) and 1.5V_{OUT} at 25A with 12.5A Load Step Transient Response and 1V_{OUT} (with AVP), 4.5V_{IN} (78k R_{FB1}) to 15V_{IN} (84k R_{FB1})

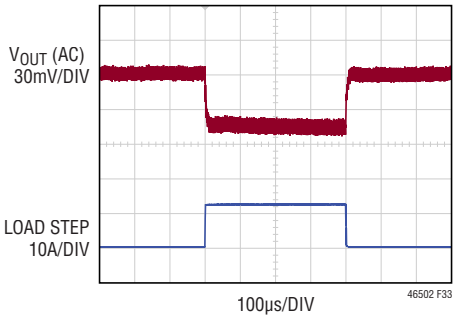


Figure 33. Load Transient Waveform of Figure 32 Circuit with AVP, 12V_{IN}, 1V_{OUT}, 500kHz, 12.5A (50% of Full Load, Slew Rate 12.5A/µs), C_{OUT1} = 100µF ×3 Ceramic, C_{OUT2} = 470µF ×2 POSCAP

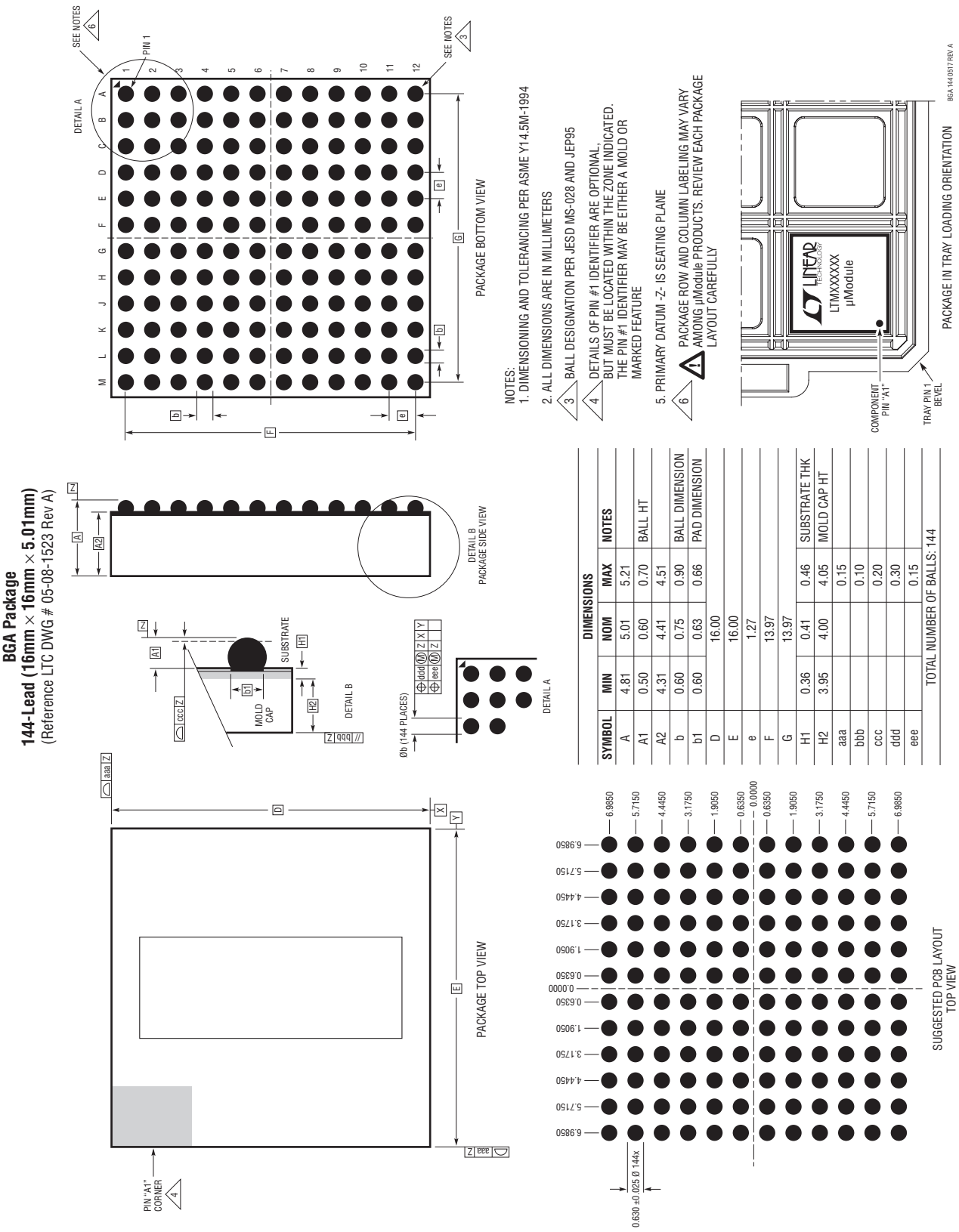
PACKAGE DESCRIPTION

Table 5. LTM4650-2 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT1}	B1	V_{OUT1}	C1	V_{OUT1}	D1	GND	E1	GND	F1	GND
A2	V_{OUT1}	B2	V_{OUT1}	C2	V_{OUT1}	D2	GND	E2	GND	F2	GND
A3	V_{OUT1}	B3	V_{OUT1}	C3	V_{OUT1}	D3	GND	E3	GND	F3	GND
A4	V_{OUT1}	B4	V_{OUT1}	C4	V_{OUT1}	D4	GND	E4	GND	F4	MODE_PLLIN
A5	V_{OUT1}	B5	V_{OUT1}	C5	V_{OUTS1}	D5	V_{FB1}	E5	TRACK1	F5	RUN1
A6	GND	B6	GND	C6	f_{SET}	D6	SGND	E6	COMP1	F6	SGND
A7	GND	B7	GND	C7	SGND	D7	V_{FB2}	E7	COMP2	F7	SGND
A8	V_{OUT2}	B8	V_{OUT2}	C8	V_{OUTS2}	D8	TRACK2	E8	DIFFP	F8	DIFFOUT
A9	V_{OUT2}	B9	V_{OUT2}	C9	V_{OUT2}	D9	GND	E9	DIFFN	F9	RUN2
A10	V_{OUT2}	B10	V_{OUT2}	C10	V_{OUT2}	D10	GND	E10	GND	F10	GND
A11	V_{OUT2}	B11	V_{OUT2}	C11	V_{OUT2}	D11	GND	E11	GND	F11	GND
A12	V_{OUT2}	B12	V_{OUT2}	C12	V_{OUT2}	D12	GND	E12	GND	F12	GND

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	GND	J1	GND	K1	GND	L1	GND	M1	GND
G2	SW1	H2	GND	J2	V_{IN}	K2	V_{IN}	L2	V_{IN}	M2	V_{IN}
G3	GND	H3	GND	J3	V_{IN}	K3	V_{IN}	L3	V_{IN}	M3	V_{IN}
G4	PHASMD	H4	GND	J4	V_{IN}	K4	V_{IN}	L4	V_{IN}	M4	V_{IN}
G5	CLKOUT	H5	GND	J5	GND	K5	GND	L5	V_{IN}	M5	V_{IN}
G6	SGND	H6	GND	J6	TEMP	K6	GND	L6	V_{IN}	M6	V_{IN}
G7	SGND	H7	GND	J7	$EXTV_{CC}$	K7	GND	L7	V_{IN}	M7	V_{IN}
G8	PGOOD2	H8	$INTV_{CC}$	J8	GND	K8	GND	L8	V_{IN}	M8	V_{IN}
G9	PGOOD1	H9	GND	J9	V_{IN}	K9	V_{IN}	L9	V_{IN}	M9	V_{IN}
G10	GND	H10	GND	J10	V_{IN}	K10	V_{IN}	L10	V_{IN}	M10	V_{IN}
G11	SW2	H11	GND	J11	V_{IN}	K11	V_{IN}	L11	V_{IN}	M11	V_{IN}
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND

PACKAGE DESCRIPTION



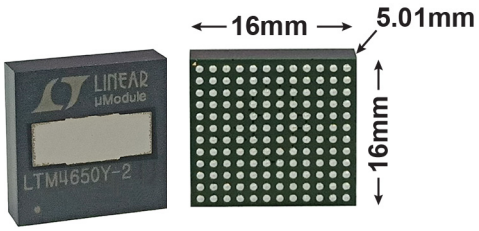
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.81	5.01	5.21	
A1	0.50	0.60	0.70	BALL HT
A2	4.31	4.41	4.51	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		16.00		
E		16.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.36	0.41	0.46	SUBSTRATE THK
H2	3.95	4.00	4.05	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 144				

Rev. 0

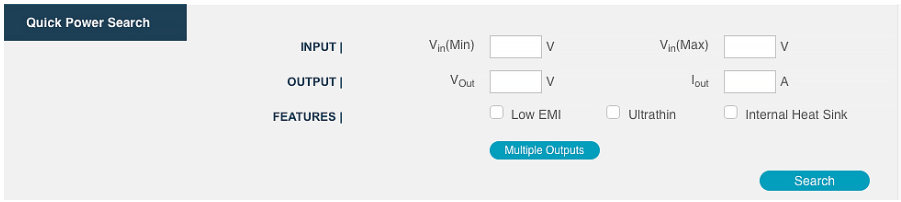
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	02/24	Initial Release.	—

PACKAGE PHOTOS



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4650-1	LTM4650-2 without AVP, External Compensation, ±0.8% (LTM4650-1A) or ±1.5% (LTM4650-1B) V_{OUT} Accuracy	Dual 25A or Single 50A, 4.5V ≤ V_{IN} ≤ 15V. 0.6V ≤ V_{OUT} ≤ 1.8V, 16mm × 16mm × 5.01mm BGA
LTM4650	Internal Compensation, ±1.5% V_{OUT} Accuracy.	Dual 25A or Single 50A, 4.5V ≤ V_{IN} ≤ 15V. 0.6V ≤ V_{OUT} ≤ 1.8V, 16mm × 16mm × 5.01mm BGA
LTM4650A	Internal Compensation, High V_{OUT} Up to 5.5V. ±1% V_{OUT} Accuracy	Dual 25A or Single 50A, 4.5V ≤ V_{IN} ≤ 16V, 0.6V ≤ V_{OUT} ≤ 5.5V, 16mm × 16mm × 4.41mm LGA and 5.01mm BGA
LTM4630	Lower Current than LTM4650, Dual 18A or Single 36A	Pin Compatible with LTM4650. 4.5V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 1.8V, 16mm × 16mm × 4.41mm LGA and 5.01mm BGA
LTM4630-1	Lower Current than LTM4650-1, External Compensation and ±0.8% (LTM4630-1A) or ±1.5% (LTM4630-1B) V_{OUT} Accuracy	Pin Compatible with LTM4650-1, 4.5V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 1.8V, 16mm × 16mm × 5.01mm BGA
LTM4630A	Lower Current and Higher V_{OUT} than LTM4650A, Up to 8V_{OUT}, Dual 18A or Single 36A	Pin Compatible with LTM4650A, 4.5V ≤ V_{IN} ≤ 18V, 0.6V ≤ V_{OUT} ≤ 8V, 16mm × 16mm × 4.41mm LGA and 5.01mm BGA
LTM4681	Quad 31.25A or Single 125A with PMBus Interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.3V, 15mm × 22mm × 8.17mm BGA
LTM4683	0.3V_{OUT} (Mini), Quad 31.25A or Single 125A with PMBus Interface	4.5V ≤ V_{IN} ≤ 14V, 0.3V ≤ V_{OUT} ≤ 0.7V, 15mm × 22mm × 5.71mm BGA
LTM4700	Dual 50A or Single 100A with PMBus Interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 1.8V, 15mm × 22mm × 7.87mm BGA
LTM4680	Dual 30A or Single 60A with PMBus Interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.3V, 16mm × 16mm × 7.82mm BGA
LTM4678	Dual 25A or Single 50A with PMBus Interface	4.5V ≤ V_{IN} ≤ 16V, 0.5V ≤ V_{OUT} ≤ 3.4V, 16mm × 16mm × 5.86mm BGA