SPI/Digital or I^2C μModule Isolator with Adjustable ±12.5V and 5V Regulated Power

FEATURES

- **$2500V_{RMS}$ for One Minute per UL1577 UL Recognized File #E151738**
- **Isolated Adjustable DC Power:**
  3V to 5V at Up to 30mA
  ±12.5V at Up to 20mA
- **No External Components Required**
- **SPI (LTM2883-S) or I^2C (LTM2883-I) Options**
- **High Common Mode Transient Immunity: 30kV/μs**
- **High Speed Operation:**
  10MHz Digital Isolation
  4MHz/8MHz SPI Isolation
  400kHz I^2C Isolation
- 3.3V (LTM2883-3) or 5V (LTM2883-5) Operation
- 1.62V to 5.5V Logic Supply
- ±10kV ESD HBM Across the Isolation Barrier
- Maximum Continuous Working Voltage: $560V_{PEAK}$
- Low Current Shutdown Mode (<10μA)
- Low Profile (15mm × 11.25mm × 3.42mm) BGA Package

APPLICATIONS

- Isolated SPI or I^2C Interfaces
- Industrial Systems
- Test and Measurement Equipment
- Breaking Ground Loops

DESCRIPTION

The LTM®2883 is a complete galvanic 6-channel digital μModule® (micromodule) isolator. No external components are required. A single 3.3V or 5V supply powers both sides of the interface through an integrated, isolated DC/DC converter. A logic supply pin allows easy interfacing with different logic levels from 1.62V to 5.5V, independent of the main supply.

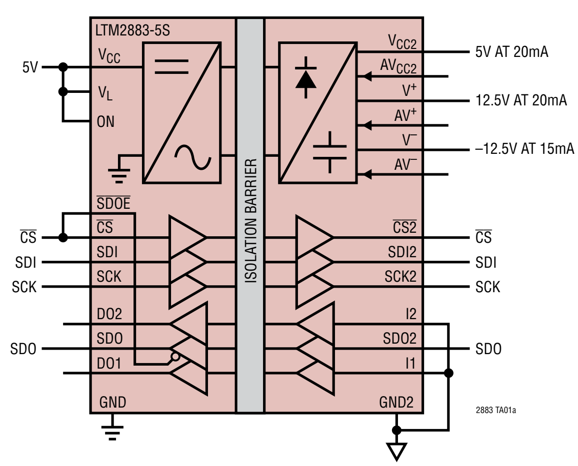
Available options are compliant with SPI and I^2C (master mode only) specifications.

The isolated side includes ±12.5V and 5V nominal power supplies, each capable of providing more than 20mA of load current. Each supply may be adjusted from its nominal value using a single external resistor.

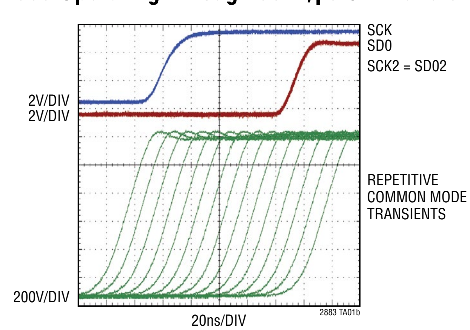
Coupled inductors and an isolation power transformer provide $2500V_{RMS}$ of isolation between the input and output logic interface. This device is ideal for systems where the ground loop is broken, allowing for a large common mode voltage range. Communication is uninterrupted for common mode transients greater than 30kV/μs.

TYPICAL APPLICATION

Isolated 4MHz SPI Interface



LTM2883 Operating Through 35kV/μs CM Transient



ABSOLUTE MAXIMUM RATINGS

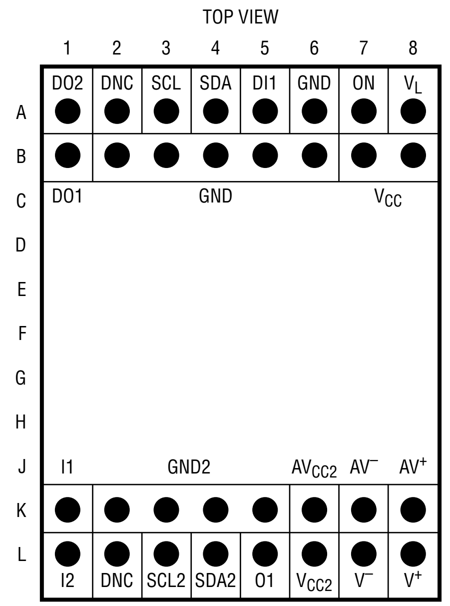
(Note 1)

V_{CC} to GND .... –0.3V to 6V
V_L to GND .... –0.3V to 6V
V_{CC2}, AV_{CC2}, AV^+ to GND2 .... –0.3V to 6V
V^+ to GND2 .... –0.3V to 16V
$V^–$, $AV^–$ to GND2 ....0.3V to –16V
Logic Inputs
DI1, SCK, SDI, $\overline{CS}$, SCL, SDA, $\overline{SDOE}$,
ON to GND ....–0.3V to (V_L + 0.3V)
I1, I2, SDA2,
SDO2 to GND2........................–0.3V to (V_{CC2} + 0.3V)

Logic Outputs
DO1, DO2, SDO to GND ....–0.3V to (V_L + 0.3V)
O1, SCK2, SDI2, $\overline{CS2}$,
SCL2 to GND2 ....–0.3V to (V_{CC2} + 0.3V)
Operating Temperature Range (Note 4)
LTM2883C ....0°C ≤ T_A ≤ 70°C
LTM2883I .... –40°C ≤ T_A ≤ 85°C
LTM2883H.................................–40°C ≤ T_A ≤ 105°C
Maximum Internal Operating Temperature............ 125°C
Storage Temperature Range ....–40°C to 125°C
Peak Body Reflow Temperature .... 245°C

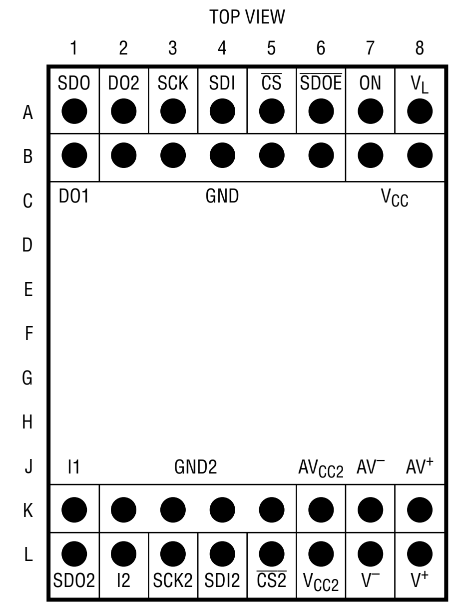
PIN CONFIGURATION

LTM2883-I



BGA PACKAGE
32-PIN (15mm × 11.25mm × 3.42mm)
T_{JMAX} = 125°C, θ_{JA} = 30°C/W, $\theta_{JC(BOTTOM)}$ = 15.7°C/W,
$\theta_{JC(TOP)}$ = 25°C/W, θ_{JBOARD} = 14.5°C/W
θ VALUES DETERMINED PER JESD51-9, WEIGHT = 1.2g

LTM2883-S



BGA PACKAGE
32-PIN (15mm × 11.25mm × 3.42mm)
T_{JMAX} = 125°C, θ_{JA} = 30°C/W, $\theta_{JC(BOTTOM)}$ = 15.7°C/W,
$\theta_{JC(TOP)}$ = 25°C/W, θ_{JBOARD} = 14.5°C/W
θ VALUES DETERMINED PER JESD51-9, WEIGHT = 1.2g

ORDER INFORMATION http://www.linear.com/product/LTM2883#orderinfo

PART NUMBER	INPUT VOLTAGE	PAD OR BALL FINISH	PART MARKING DEVICE	PART MARKING FINISH CODE	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
LTM2883CY-3S#PBF	3V TO 3.6V	SAC305 (RoHS)	LTM2883Y-3S	e1	BGA	4	0°C TO 70°C
LTM2883IY-3S#PBF							–40°C TO 85°C
LTM2883HY-3S#PBF							–40°C TO 105°C
LTM2883CY-5S#PBF	4.5V TO 5.5V		LTM2883Y-5S				0°C TO 70°C
LTM2883IY-5S#PBF							–40°C TO 85°C
LTM2883HY-5S#PBF							–40°C TO 105°C
LTM2883CY-3I#PBF	3V TO 3.6V		LTM2883Y-3I				0°C TO 70°C
LTM2883IY-3I#PBF							–40°C TO 85°C
LTM2883HY-3I#PBF							–40°C TO 105°C
LTM2883CY-5I#PBF	4.5V TO 5.5V		LTM2883Y-5I				0°C TO 70°C
LTM2883IY-5I#PBF							–40°C TO 85°C
LTM2883HY-5I#PBF							–40°C TO 105°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Terminal Finish Part Marking: www.linear.com/leadfree
- This product is not recommended for second side reflow. For more information, go to: www.linear.com/BGA-assy
- Recommended BGA PCB Assembly and Manufacturing Procedures: www.linear.com/BGA-assy
- BGA Package and Tray Drawings: www.linear.com/packaging
- This product is moisture sensitive. For more information, go to: www.linear.com/BGA-assy

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTM2883-3 V_{CC} = 3.3V, LTM2883-5 V_{CC} = 5V, V_L = 3.3V, and GND = GND2 = 0V, ON = V_L unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supplies							
V_{CC}	Input Supply Range	LTM2883-3 LTM2883-5	● ●	3 4.5	3.3 5	3.6 5.5	V V
V_L	Logic Supply Range	LTM2883-S LTM2883-I	● ●	1.62 3	 5	5.5 5.5	V V
I_{CC}	Input Supply Current	ON = 0V LTM2883-3, ON = V_L, No Load LTM2883-5, ON = V_L, No Load	● ● ●		0 25 19	10 35 28	µA mA mA
I_L	Logic Supply Current	ON = 0V LTM2883-S, ON = V_L LTM2883-I, ON = V_L	●		0 10 	10 150	µA µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTM2883-3 V_{CC} = 3.3V, LTM2883-5 V_{CC} = 5V, V_L = 3.3V, and GND = GND2 = 0V, ON = V_L unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Supplies							
V_{CC2}	Regulated Output Voltage	No Load	●	4.75	5	5.25	V
	Output Voltage Operating Range	(Note 2)		3		5.5	V
	Line Regulation	I_{LOAD} = 1mA, MIN ≤ V_{CC} ≤ MAX	●		25	100	mV
	Load Regulation	I_{LOAD} = 100µA to 20mA	●		8	80	mV
	ADJ Pin Voltage	I_{LOAD} = 100µA to 20mA	●	585	600	615	mV
	Voltage Ripple	I_{LOAD} = 20mA (Note 2)			1		mV_{RMS}
	Efficiency	I_{LOAD} = 20mA (Note 2)			45		%
I_{CC2}	Output Short Circuit Current	V_{CC2} = 0V			45		mA
	Current Limit	ΔV_{CC2} = –5%	●	20			mA
V^+	Regulated Output Voltage	No Load	●	12	12.5	13	V
	Line Regulation	I_{LOAD} = 1mA, MIN ≤ V_{CC} ≤ MAX	●		5	30	mV
	Load Regulation	I_{LOAD} = 100µA to 20mA	●			200	mV
	ADJ Pin Voltage	I_{LOAD} = 100µA to 20mA	●	1.170	1.220	1.260	mV
	Voltage Ripple	I_{LOAD} = 20mA (Note 2)			3		mV_{RMS}
	Efficiency	I_{LOAD} = 20mA (Note 2)			45		%
I^+	Output Short Circuit Current	V^+ = 0V			70		mA
	Current Limit	ΔV^+ = –0.5V	●	20			mA
$V^–$	Regulated Output Voltage	No Load	●	–12	–12.5	–13	V
	Line Regulation	I_{LOAD} = –1mA, MIN ≤ V_{CC} ≤ MAX	●		4	15	mV
	Load Regulation	I_{LOAD} = 100µA to 15mA, V^+_{LOAD} = 1.5mA				35	mV
	ADJ Pin Voltage	I_{LOAD} = 100µA to 15mA, V^+_{LOAD} = 1.5mA	●	–1.184	–1.220	–1.256	mV
	Voltage Ripple	I_{LOAD} = 15mA, V^+_{LOAD} = 1.5mA (Note 2)			2		mV_{RMS}
	Efficiency	I_{LOAD} = 15mA (Note 2)			45		%
$I^–$	Output Short-Circuit Current	$V^–$ = 0V			30		mA
	Current Limit	$\Delta V^–$ = 0.5V, V^+ = 1.5mA	●	10	15		mA
Logic/SPI							
V_{ITH}	Input Threshold Voltage	ON, DI1, $\overline{SDOE}$, SCK, SDI, $\overline{CS}$ 1.62V ≤ V_L < 2.35V ON, DI1, $\overline{SDOE}$, SCK, SDI, $\overline{CS}$ 2.35V ≤ V_L I1, I2, SDO2	● ● ●	0.25 • V_L 0.33 • V_L 0.33 • V_{CC2}		0.75 • V_L 0.67 • V_L 0.67 • V_{CC2}	V V V
I_{INL}	Input Current		●			±1	µA
V_{HYS}	Input Hysteresis	(Note 2)			150		mV
V_{OH}	Output High Voltage	DO1, DO2, SDO I_{LOAD} = –1mA, 1.62V ≤ V_L < 3V I_{LOAD} = –4mA, 3V ≤ V_L ≤ 5.5V	●	V_L – 0.4			V
		O1, SCK2, SDI2, $\overline{CS2}$, I_{LOAD} = –4mA	●	V_{CC2} – 0.4			V
V_{OL}	Output Low Voltage	DO1, DO2, SDO I_{LOAD} = 1mA, 1.62V ≤ V_L < 3V I_{LOAD} = 4mA, 3V ≤ V_L ≤ 5.5V	●			0.4	V
		O1, SCK2, SDI2, $\overline{CS2}$, I_{LOAD} = 4mA	●			0.4	V
I_{SC}	Short-Circuit Current	0V ≤ (DO1, DO2, SDO) ≤ V_L 0V ≤ (O1, SCK2, SDI2, $\overline{CS2}$) ≤ V_{CC2}	●		 ±60	±85 	mA mA

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I^2C							
V_{IL}	Low Level Input Voltage	SCL, SDA SDA2	● ●			0.3 • V_L 0.3 • V_{CC2}	V V
V_{IH}	High Level Input Voltage	SCL, SDA SDA2	● ●	0.7 • V_L 0.7 • V_{CC2}			V V
I_{INL}	Input Current	SCL, SDA = V_L or 0V	●			±1	µA
V_{HYS}	Input Hysteresis	SCL, SDA SDA2			0.05 • V_L 0.05 • V_{CC2}		mV mV
V_{OH}	Output High Voltage	SCL2, I_{LOAD} = –2mA DO2, I_{LOAD} = –2mA	● ●	V_{CC2} – 0.4 V_L – 0.4			V V
V_{OL}	Output Low Voltage	SDA, V_L = 3V, I_{LOAD} = 3mA DO2, V_L = 3V, I_{LOAD} = 2mA SCL2, I_{LOAD} = 2mA SDA2, No Load, SDA = 0V, 4.5V ≤ V_{CC2} < 5.5V SDA2, No Load, SDA = 0V, 3V < V_{CC2} < 4.5V	● ● ● ● ●		 0.3	0.4 0.4 0.4 0.45 0.55	V V V V V
C_{IN}	Input Pin Capacitance	SCL, SDA, SDA2 (Note 2)	●			10	pF
C_B	Bus Capacitive Load	SCL2, Standard Speed (Note 2) SCL2, Fast Speed SDA, SDA2, SR ≥ 1V/µs, Standard Speed (Note 2) SDA, SDA2, SR ≥ 1V/µs, Fast Speed	● ● ● ●			400 200 400 200	pF pF pF pF
	Minimum Bus Slew Rate	SDA, SDA2	●	1			V/µs
I_{SC}	Short-Circuit Current	SDA2 = 0, SDA = V_L 0V ≤ SCL2 ≤ V_{CC2} 0V ≤ DO2 ≤ V_L SDA = 0, SDA2 = V_{CC2} SDA = V_L, SDA2 = 0	●		 ±30 ±30 6 –1.8	100	mA mA mA mA mA
ESD (HBM) (Note 2)							
	Isolation Boundary	(V_{CC2}, V^+, V^-, GND2) to (V_{CC}, V_L, GND)			±10		kV

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTM2883-3 V_{CC} = 3.3V, LTM2883-5 V_{CC} = 5V, V_L = 3.3V, and GND = GND2 = 0V, ON = V_L unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic							
	Maximum Data Rate	Ix → DOx, C_L = 15pF (Note 3)	●	10			MHz
t_{PHL}, t_{PLH}	Propagation Delay	C_L = 15pF (Figure 1)	●	35	60	100	ns
t_R	Rise Time	C_L = 15pF (Figure 1) LTM2883-I, DO2, C_L = 15pF (Figure 1)	● ●		3 20	12.5 35	ns ns
t_F	Fall Time	C_L = 15pF (Figure 1) LTM2883-I, DO2, C_L = 15pF (Figure 1)	● ●		3 20	12.5 35	ns ns
SPI							
	Maximum Data Rate	Bidirectional Communication (Note 3) Unidirectional Communication (Note 3)	● ●	4 8			MHz MHz
t_{PHL}, t_{PLH}	Propagation Delay	C_L = 15pF (Figure 1)	●	35	60	100	ns
t_{PWU}	Output Pulse Width Uncertainty	SDI2, $\overline{CS2}$ (Note 2)		–20		50	ns

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTM2883-3 V_{CC} = 3.3V, LTM2883-5 V_{CC} = 5V, V_L = 3.3V, and GND = GND2 = 0V, ON = V_L unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_R	Rise Time	C_L = 15pF (Figure 1)	●		3	12.5	ns
t_F	Fall Time	C_L = 15pF (Figure 1)	●		3	12.5	ns
t_{PZH}, t_{PZL}	Output Enable Time	$\overline{SDOE}$ = ↓, R_L = 1kΩ, C_L = 15pF (Figure 2)	●			50	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	$\overline{SDOE}$ = ↑, R_L = 1kΩ, C_L = 15pF (Figure 2)	●			50	ns
I²C							
	Maximum Data Rate	(Note 3)	●	400			kHz
t_{PHL}, t_{PLH}	Propagation Delay	SCL → SCL2, C_L = 15pF (Figure 1) SDA → SDA2, R_L = Open, C_L = 15pF (Figure 3) SDA2 → SDA, R_L = 1.1kΩ, C_L = 15pF (Figure 3)	● ● ●		150 150 200	225 250 350	ns ns ns
t_{PWU}	Output Pulse Width Uncertainty	SDA, SDA2 (Note 2)		–20		50	ns
$t_{HD;DAT}$	Data Hold Time	(Note 2)			600		ns
t_R	Rise Time	SDA2, C_L = 200pF (Figure 3) SDA2, C_L = 200pF (Figure 3) SDA, R_L = 1.1kΩ, C_L = 200pF (Figure 3) SCL2, C_L = 200pF (Figure 1)	 ● ● ●	40 40 40		250 300 250 250	ns ns ns ns
t_F	Fall Time	SDA2, C_L = 200pF (Figure 3) SDA, R_L = 1.1kΩ, C_L = 200pF (Figure 3) SCL2, C_L = 200pF (Figure 1)	● ● ●	40 40		250 250 250	ns ns ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		●	0		50	ns
Power Supply							
	Power-Up Time	ON = ↑ to V_{CC2} (Min) ON = ↑ to V^+ (Min) ON = ↑ to V^- (Min)	● ● ●		0.6 0.6 0.6	2 2 2.5	ms ms ms

ISOLATION CHARACTERISTICS

T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ISO}	Rated Dielectric Insulation Voltage (Notes 5, 6, 7)	1 Minute, Derived from 1 Second Test	2500			V_{RMS}
		1 Second	±4400			V
	Common Mode Transient Immunity	LTM2883-3 V_{CC} = 3.3V, LTM2883-5 V_{CC} = 5V, V_L = ON = 3.3V, V_{CM} = 1kV, Δt = 33ns (Note 2)	30			kV/μs
V_{IORM}	Maximum Continuous Working Voltage	(Notes 2, 5)	560 400			V_{PEAK} V_{RMS}
	Partial Discharge	V_{PD} = 1050V_{PEAK} (Notes 2, 5)			5	pC
CTI	Comparative Tracking Index	IEC 60112 (Note 2)	600			V_{RMS}
	Depth of Erosion	IEC 60112 (Note 2)		0.017		mm
DTI	Distance Through Insulation	(Note 2)		0.06		mm
	Input to Output Resistance	(Notes 2, 5)	10^9			Ω
	Input to Output Capacitance	(Notes 2, 5)		6		pF
	Creepage Distance	(Note 2)		9.48		mm

ISOLATION CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and not subject to production test.

Note 3: Maximum data rate is guaranteed by other measured parameters and is not tested directly.

Note 4: This module includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

Note 5: Device considered a 2-terminal device. Pin group A1 through B8 shorted together and pin group K1 through L8 shorted together.

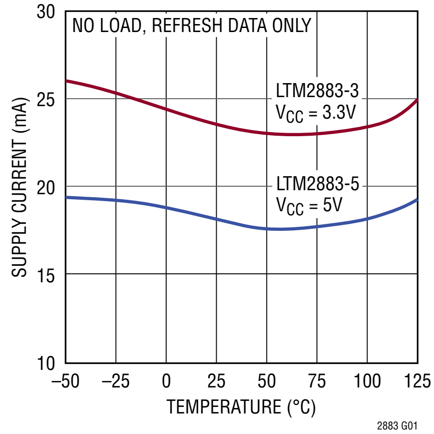
Note 6: The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

Note 7: In accordance with UL1577, each device is proof tested for the $2500V_{RMS}$ rating by applying the equivalent positive and negative peak voltage multiplied by an acceleration factor of 1.2 for one second.

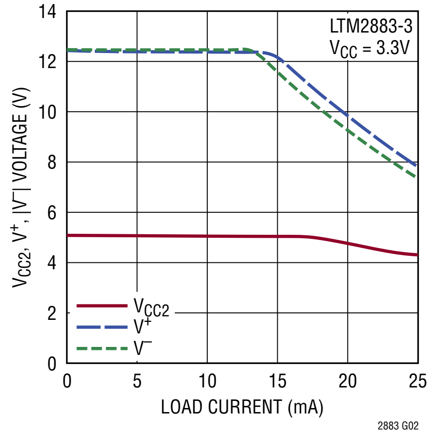
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, LTM2883-3 V_{CC} = 3.3V, LTM2883-5 V_{CC} = 5V, V_L = 3.3V, GND = GND2 = 0V, ON = V_L unless otherwise noted.

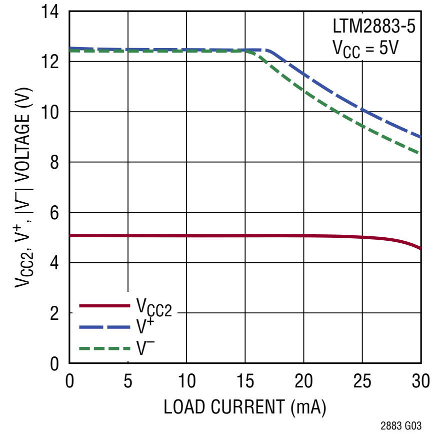
V_{CC} Supply Current vs Temperature



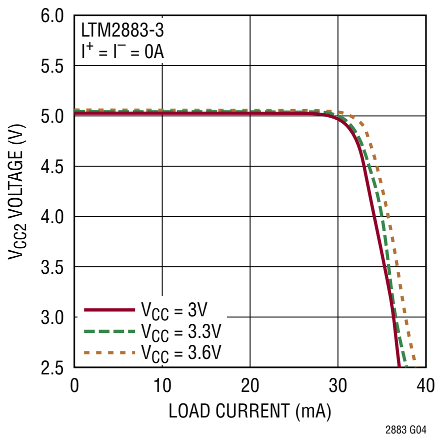
Isolated Supplies vs Equal Load Current



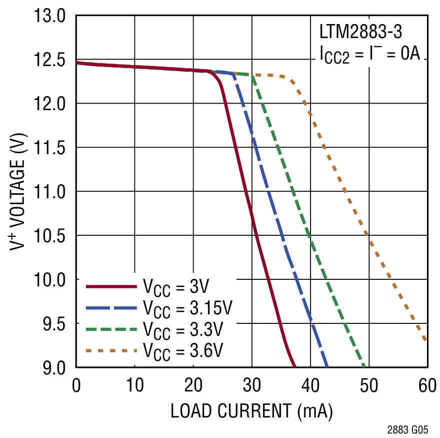
Isolated Supplies vs Equal Load Current



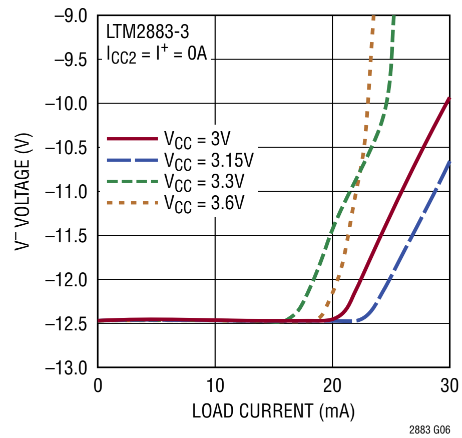
V_{CC2} Line Regulation vs Load Current



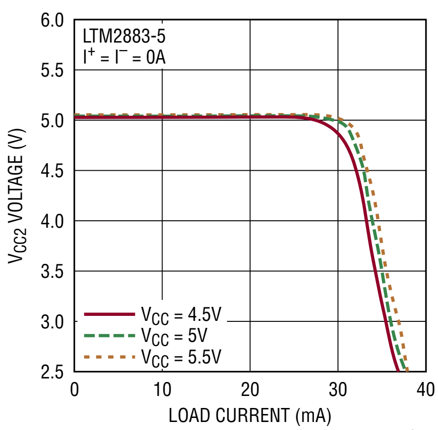
V⁺ Line Regulation vs Load Current



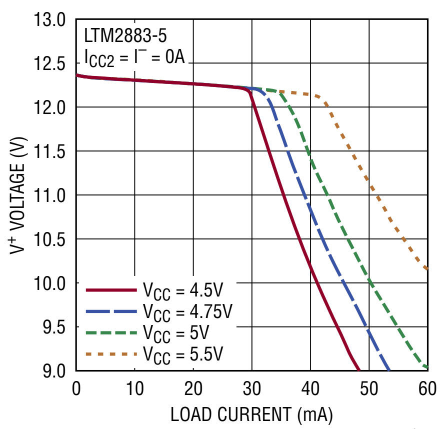
V⁻ Line Regulation vs Load Current



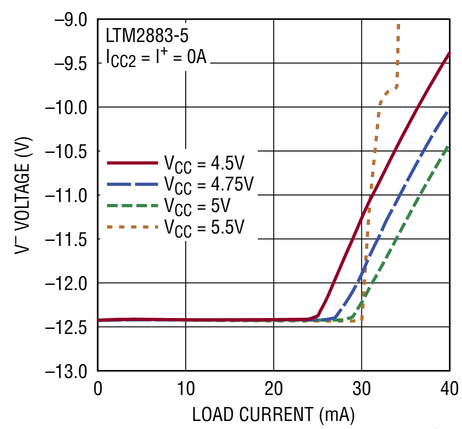
V_{CC2} Line Regulation vs Load Current



V⁺ Line Regulation vs Load Current



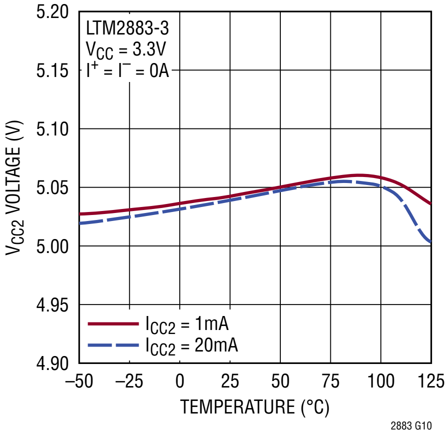
V⁻ Line Regulation vs Load Current



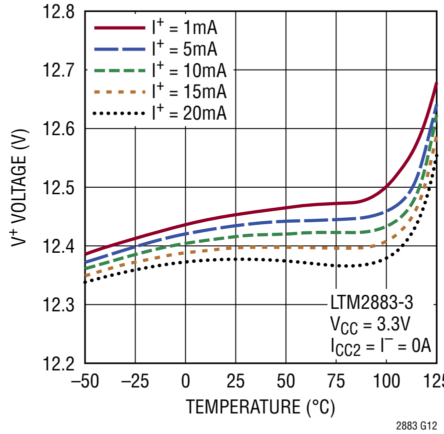
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, LTM2883-3 V_{CC} = 3.3V, LTM2883-5 V_{CC} = 5V, V_L = 3.3V, GND = GND2 = 0V, ON = V_L unless otherwise noted.

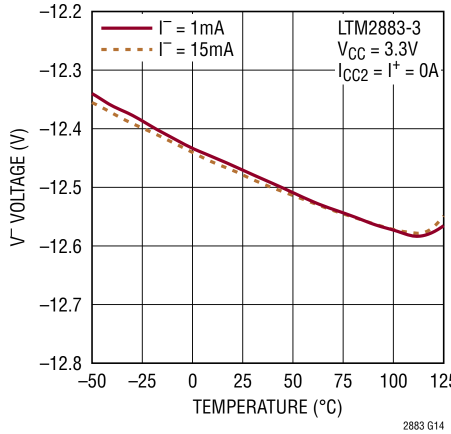
V_{CC2} Load Regulation vs Temperature



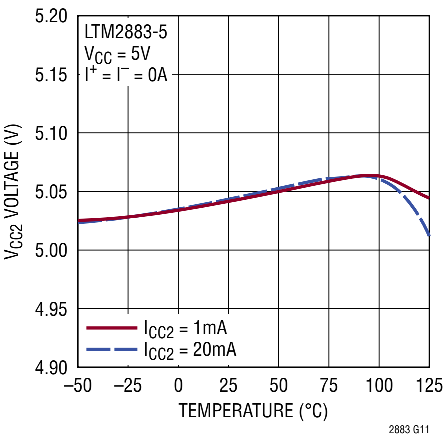
V+ Load Regulation vs Temperature



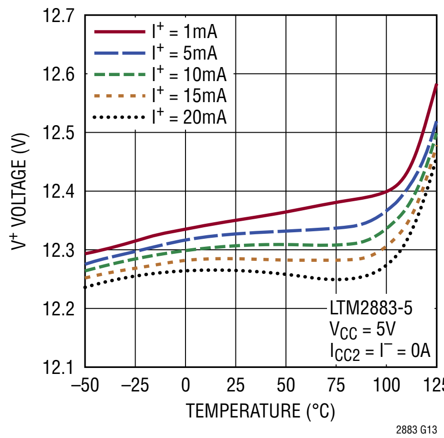
V– Load Regulation vs Temperature



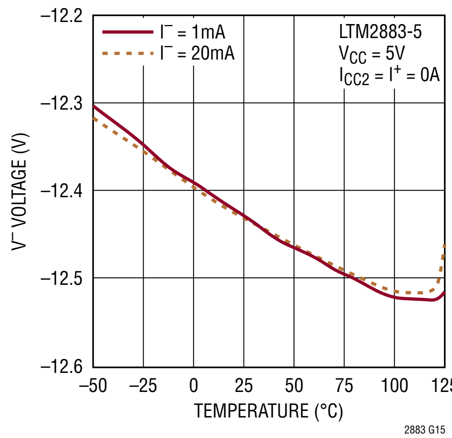
V_{CC2} Load Regulation vs Temperature



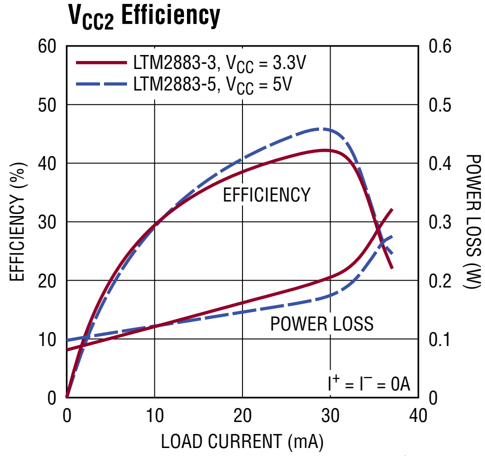
V+ Load Regulation vs Temperature



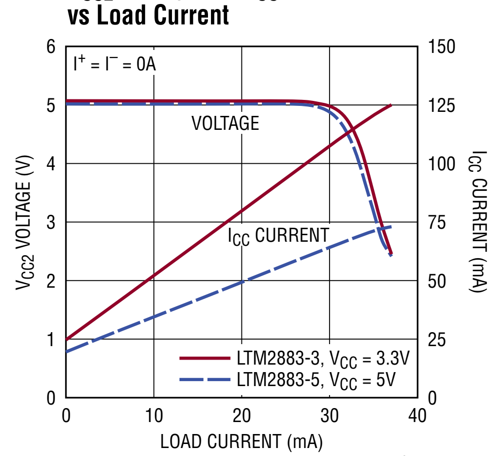
V– Load Regulation vs Temperature



V_{CC2} Efficiency



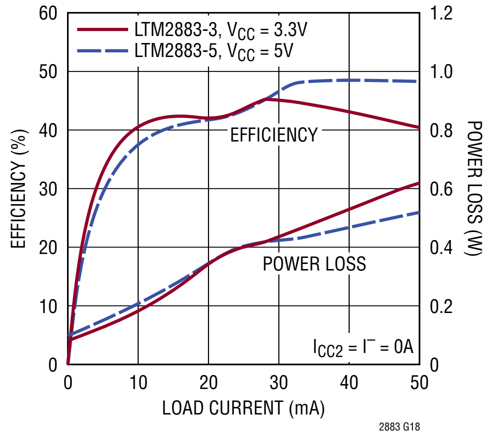
V_{CC2} Voltage and I_{CC} Current vs Load Current



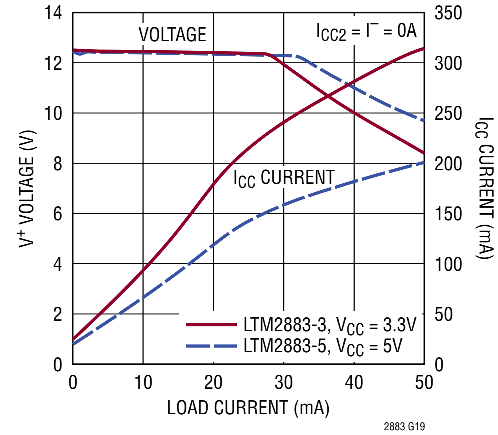
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, LTM2883-3 $V_{CC} = 3.3V$, LTM2883-5 $V_{CC} = 5V$, $V_L = 3.3V$, GND = GND2 = 0V, ON = V_L unless otherwise noted.

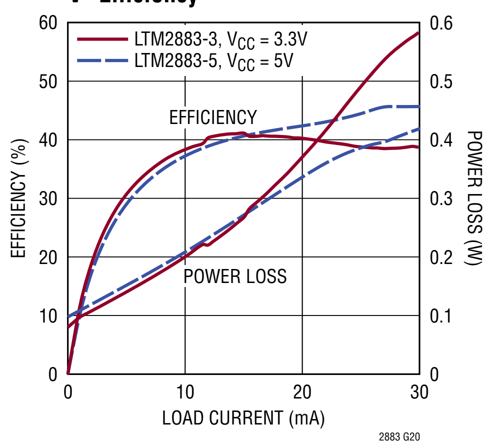
V+ Efficiency



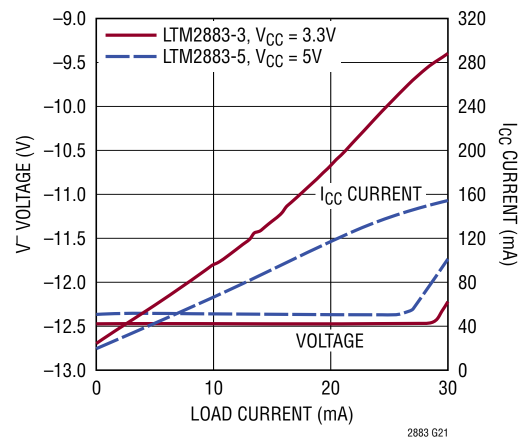
V+ Voltage and I_{CC} Current vs Load Current



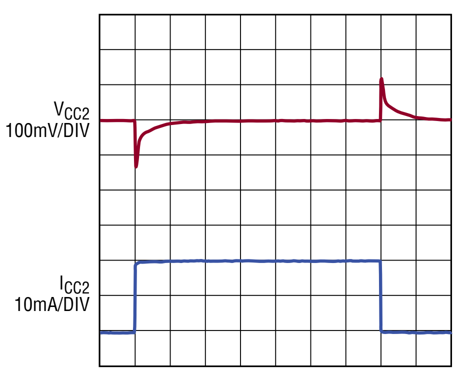
V– Efficiency



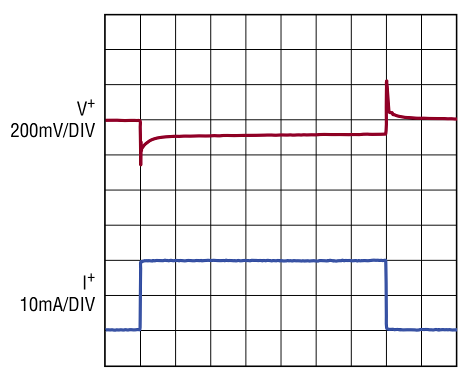
V– Voltage and I_{CC} Current vs Load Current



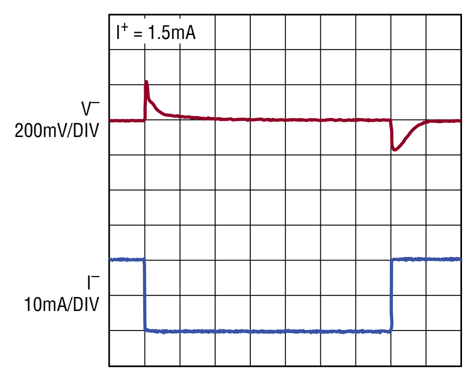
V_{CC2} Transient Response 20mA Load Step



V+ Transient Response 20mA Load Step



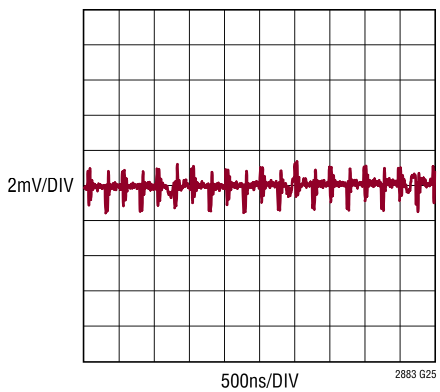
V– Transient Response 20mA Load Step



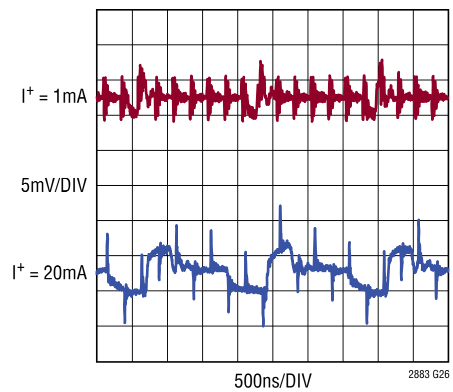
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, LTM2883-3 V_{CC} = 3.3V, LTM2883-5 V_{CC} = 5V, V_L = 3.3V, GND = GND2 = 0V, ON = V_L unless otherwise noted.

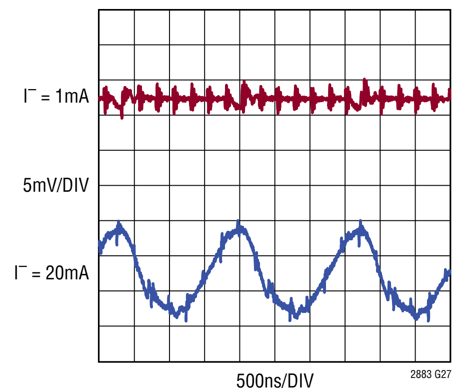
V_{CC2} Ripple



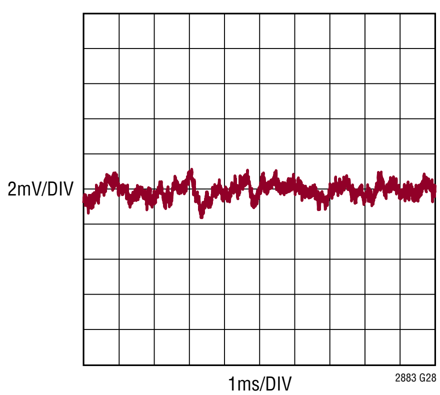
V^+ Ripple



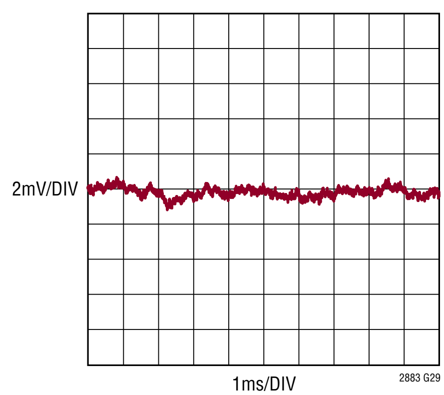
V^- Ripple



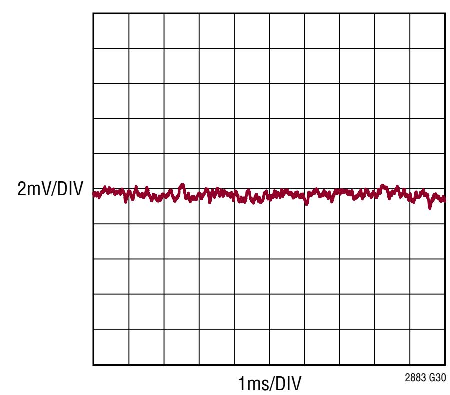
V_{CC2} Noise



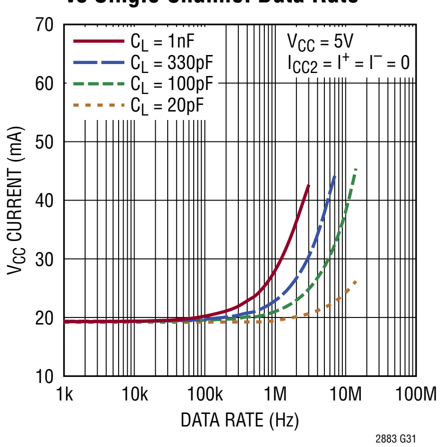
V^+ Noise



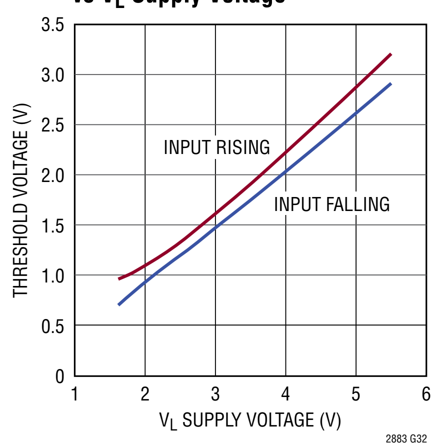
V^- Noise



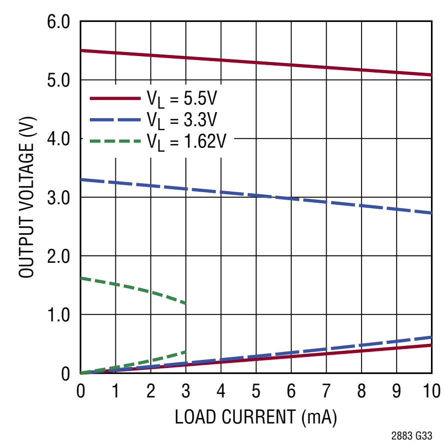
V_{CC} Supply Current vs Single Channel Data Rate



Logic Input Threshold vs V_L Supply Voltage



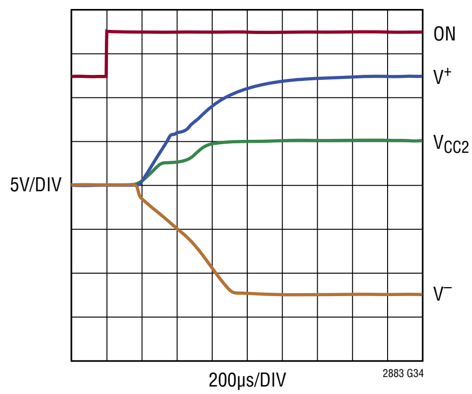
Logic Output Voltage vs Load Current



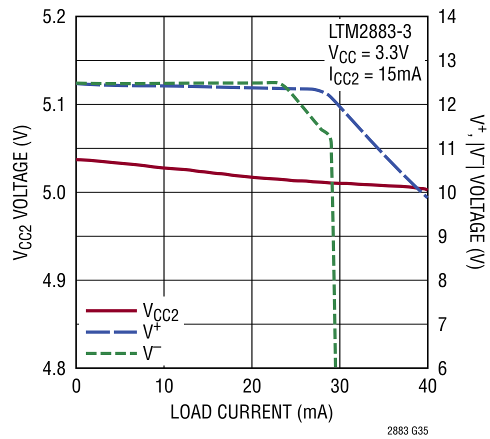
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, LTM2883-3 V_{CC} = 3.3V, LTM2883-5 V_{CC} = 5V, V_L = 3.3V, GND = GND2 = 0V, ON = V_L unless otherwise noted.

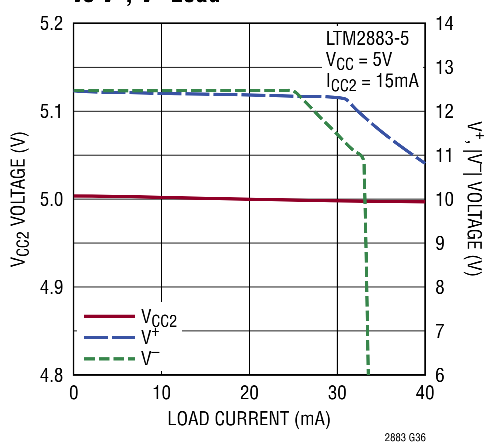
Power On Sequence



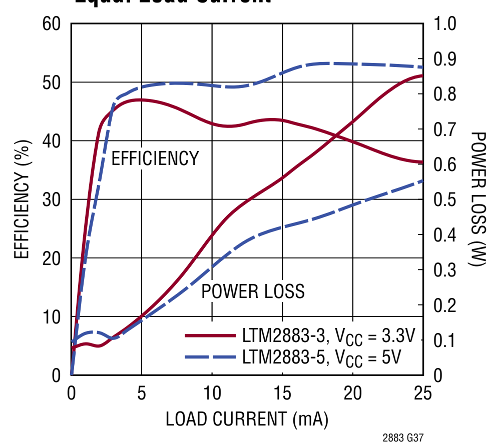
VCC2 Cross Regulation vs V+, V− Load



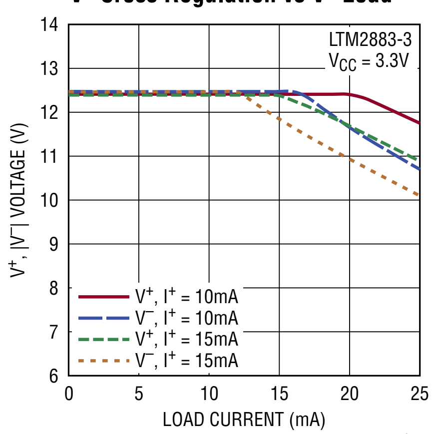
VCC2 Cross Regulation vs V+, V− Load



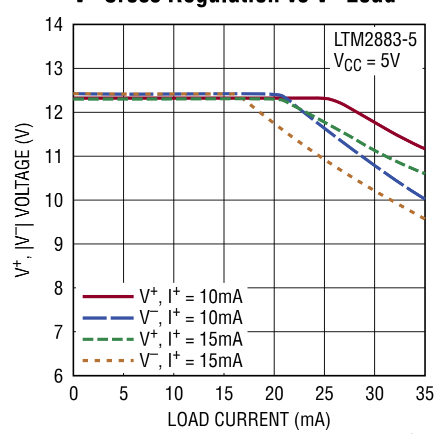
Isolated Supply Efficiency with Equal Load Current



V+ Cross Regulation vs V− Load



V+ Cross Regulation vs V− Load



PIN FUNCTIONS (LTM2883-I)

Logic Side

DO2 (A1): Digital Output, Referenced to V_L and GND. Logic output connected to I2 through isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

DNC (A2): Do Not Connect Pin. Pin connected internally.

SCL (A3): Serial I^2C Clock Input, Referenced to V_L and GND. Logic input connected to isolated side SCL2 pin through isolation barrier. Clock is unidirectional from logic to isolated side. Do not float.

SDA (A4): Serial I^2C Data Pin, Referenced to V_L and GND. Bidirectional logic pin connected to isolated side SDA2 pin through isolation barrier. Under the condition of an isolation communication failure this pin is in a high impedance state. Do not float.

DI1 (A5): Digital Input, Referenced to V_L and GND. Logic input connected to O1 through isolation barrier. The logic state on DI1 translates to the same logic state on O1. Do not float.

GND (A6, B2 to B6): Circuit Ground.

ON (A7): Enable. Enables power and data communication through the isolation barrier. If ON is high the part is enabled and power and communications are functional to the isolated side. If ON is low the logic side is held in reset, all digital outputs are in a high impedance state, and the isolated side is unpowered. Do not float.

V_L (A8): Logic Supply. Interface supply voltage for pins DI1, SCL, SDA, DO1, DO2, and ON. Operating voltage is 3V to 5.5V. Internally bypassed with 2.2µF.

DO1 (B1): Digital Output, Referenced to V_L and GND. Logic output connected to I1 through isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

V_{CC} (B7 to B8): Supply Voltage. Operating voltage is 3V to 3.6V for LTM2883-3 and 4.5V to 5.5V for LTM2883-5. Internally bypassed with 2.2µF.

Isolated Side

I2 (L1): Digital Input, Referenced to V_{CC2} and GND2. Logic input connected to DO2 through isolation barrier. The logic state on I2 translates to the same logic state on DO2. Do not float.

DNC (L2): Do Not Connect Pin. Pin connected internally.

SCL2 (L3): Serial I^2C Clock Output, Referenced to V_{CC2} and GND2. Logic output connected to logic side SCL pin through isolation barrier. Clock is unidirectional from logic to isolated side. SCL2 has a push-pull output stage, do not connect an external pull-up device. Under the condition of an isolation communication failure this output defaults to a high state.

SDA2 (L4): Serial I^2C Data Pin, Referenced to V_{CC2} and GND2. Bidirectional logic pin connected to logic side SDA pin through isolation barrier. Output is biased high by a 1.8mA current source. Do not connect an external pull-up device to SDA2. Under the condition of an isolation communication failure this output defaults to a high state.

O1 (L5): Digital Output, Referenced to V_{CC2} and GND2. Logic output connected to DI1 through isolation barrier. Under the condition of an isolation communication failure O1 defaults to a high state.

V_{CC2} (L6): 5V Nominal Isolated Supply Voltage. Internally generated from V_{CC} by an isolated DC/DC converter and regulated to 5V. Internally bypassed with 2.2µF.

V^- (L7): –12.5V Nominal Isolated Supply Voltage. Internally generated from V_{CC} by an isolated DC/DC converter and regulated to –12.5V. Internally bypassed with 1µF.

V^+ (L8): 12.5V Nominal Isolated Supply Voltage. Internally generated from V_{CC} by an isolated DC/DC converter and regulated to 12.5V. Internally bypassed with 1µF.

I1 (K1): Digital Input, Referenced to V_{CC2} and GND2. Logic input connected to DO1 through isolation barrier. The logic state on I1 translates to the same logic state on DO1. Do not float.

GND2 (K2 to K5): Isolated Ground.

AV_{CC2} (K6): 5V Nominal Isolated Supply Voltage Adjust. The adjust pin voltage is 600mV referenced to GND2.

AV^- (K7): –12.5V Nominal Isolated Supply Voltage Adjust. The adjust pin voltage is –1.22V referenced to GND2.

AV^+ (K8): 12.5V Nominal Isolated Supply Voltage Adjust. The adjust pin voltage is 1.22V referenced to GND2.

PIN FUNCTIONS (LTM2883-S)

Logic Side

SDO (A1): Serial SPI Digital Output, Referenced to V_L and GND. Logic output connected to isolated side SDO2 pin through isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

DO2 (A2): Digital Output, Referenced to V_L and GND. Logic output connected to I2 through isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

SCK (A3): Serial SPI Clock Input, Referenced to V_L and GND. Logic input connected to isolated side SCK2 pin through isolation barrier. Do not float.

SDI (A4): Serial SPI Data Input, Referenced to V_L and GND. Logic input connected to isolated side SDI2 pin through isolation barrier. Do not float.

$\overline{CS}$ (A5): Serial SPI Chip Select, Referenced to V_L and GND. Logic input connected to isolated side $\overline{CS2}$ pin through isolation barrier. Do not float.

$\overline{SDOE}$ (A6): Serial SPI Data Output Enable, Referenced to V_L and GND. A logic high on $\overline{SDOE}$ places the logic side SDO pin in a high impedance state, a logic low enables the output. Do not float.

ON (A7): Enable. Enables power and data communication through the isolation barrier. If ON is high the part is enabled and power and communications are functional to the isolated side. If ON is low the logic side is held in reset, all digital outputs are in a high impedance state, and the isolated side is unpowered. Do not float.

V_L (A8): Logic Supply. Interface supply voltage for pins SDI, SCK, SDO, DO1, DO2, $\overline{CS}$, and ON. Operating voltage is 1.62V to 5.5V. Internally bypassed with 2.2µF.

DO1 (B1): Digital Output, Referenced to V_L and GND. Logic output connected to I1 through isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

GND (B2 to B6): Circuit Ground.

V_{CC} (B7 to B8): Supply Voltage. Operating voltage is 3V to 3.6V for LTM2883-3 and 4.5V to 5.5V for LTM2883-5. Internally bypassed with 2.2µF.

Isolated Side

SDO2 (L1): Serial SPI Digital Input, Referenced to V_{CC2} and GND2. Logic input connected to logic side SDO pin through isolation barrier. Do not float.

I2 (L2): Digital Input, Referenced to V_{CC2} and GND2. Logic input connected to DO2 through isolation barrier. The logic state on I2 translates to the same logic state on DO2. Do not float.

SCK2 (L3): Serial SPI Clock Output, Referenced to V_{CC2} and GND2. Logic output connected to logic side SCK pin through isolation barrier. Under the condition of an isolation communication failure this output defaults to a low state.

SDI2 (L4): Serial SPI Data Output, Referenced to V_{CC2} and GND2. Logic output connected to logic side SDI pin through isolation barrier. Under the condition of an isolation communication failure this output defaults to a low state.

$\overline{CS2}$ (L5): Serial SPI Chip Select, Referenced to V_{CC2} and GND2. Logic output connected to logic side $\overline{CS}$ pin through isolation barrier. Under the condition of an isolation communication failure this output defaults to a high state.

V_{CC2} (L6): 5V Nominal Isolated Supply Voltage. Internally generated from V_{CC} by an isolated DC/DC converter and regulated to 5V. Internally bypassed with 2.2µF.

$V^–$ (L7): –12.5V Nominal Isolated Supply Voltage. Internally generated from V_{CC} by an isolated DC/DC converter and regulated to –12.5V. Internally bypassed with 1µF.

V^+ (L8): 12.5V Nominal Isolated Supply Voltage. Internally generated from V_{CC} by an isolated DC/DC converter and regulated to 12.5V. Internally bypassed with 1µF.

I1 (K1): Digital Input, Referenced to V_{CC2} and GND2. Logic input connected to DO1 through isolation barrier. The logic state on I1 translates to the same logic state on DO1. Do not float.

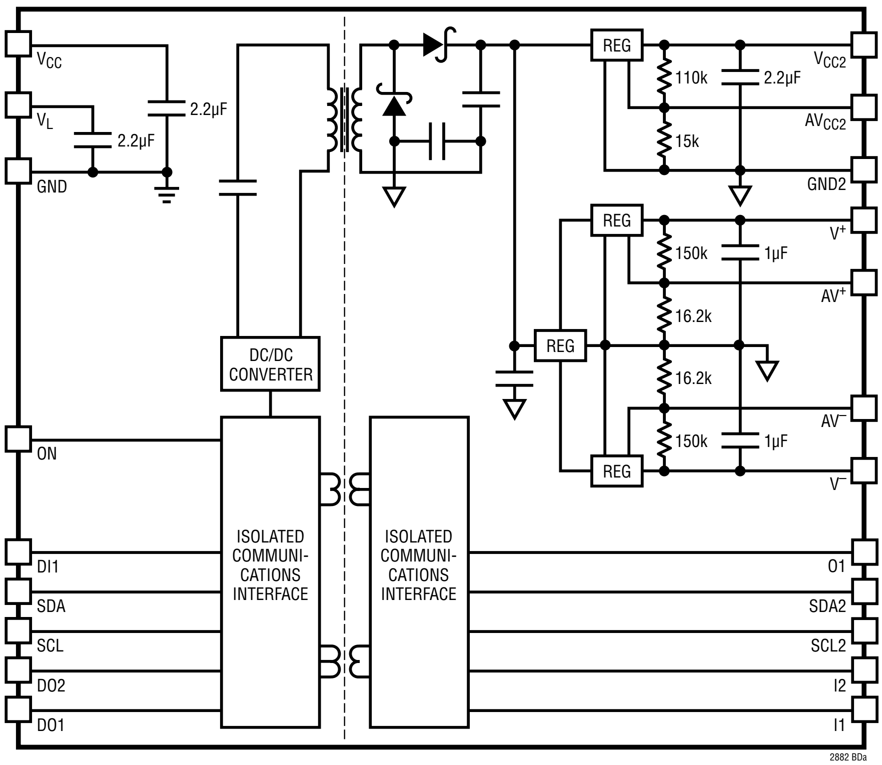
GND2 (K2 to K5): Isolated Ground.

AV_{CC2} (K6): 5V Nominal Isolated Supply Voltage Adjust. The adjust pin voltage is 600mV Referenced to GND2.

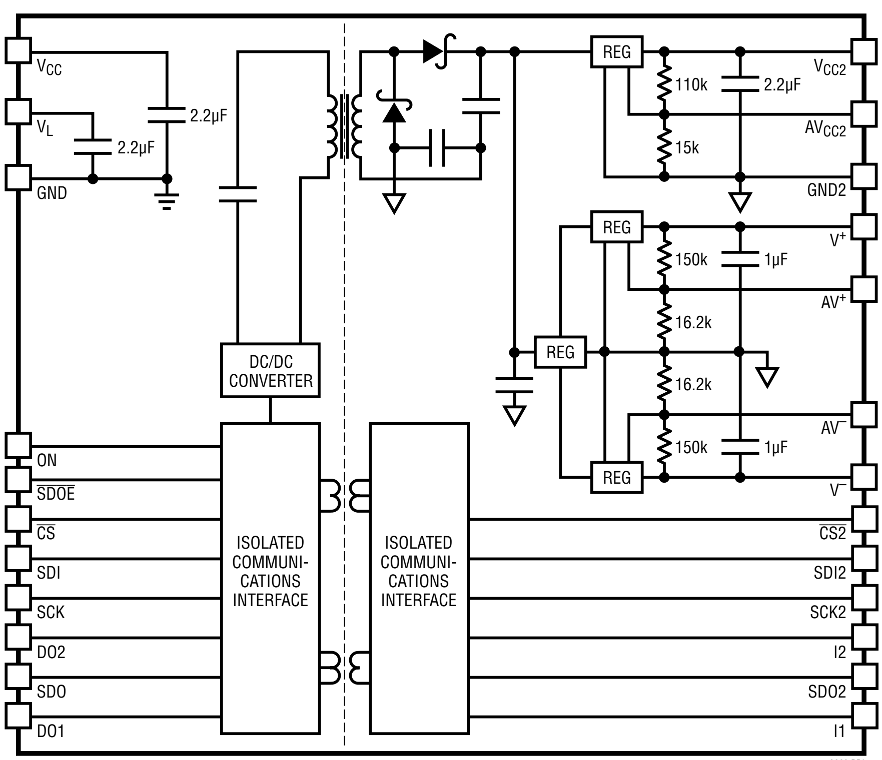
$AV^–$ (K7): –12.5V Nominal Isolated Supply Voltage Adjust. The adjust pin voltage is –1.22V Referenced to GND2.

AV^+ (K8): 12.5V Nominal Isolated Supply Voltage Adjust. The adjust pin voltage is 1.22V Referenced to GND2.

BLOCK DIAGRAM



LTM2883-I



LTM2883-S

TEST CIRCUITS

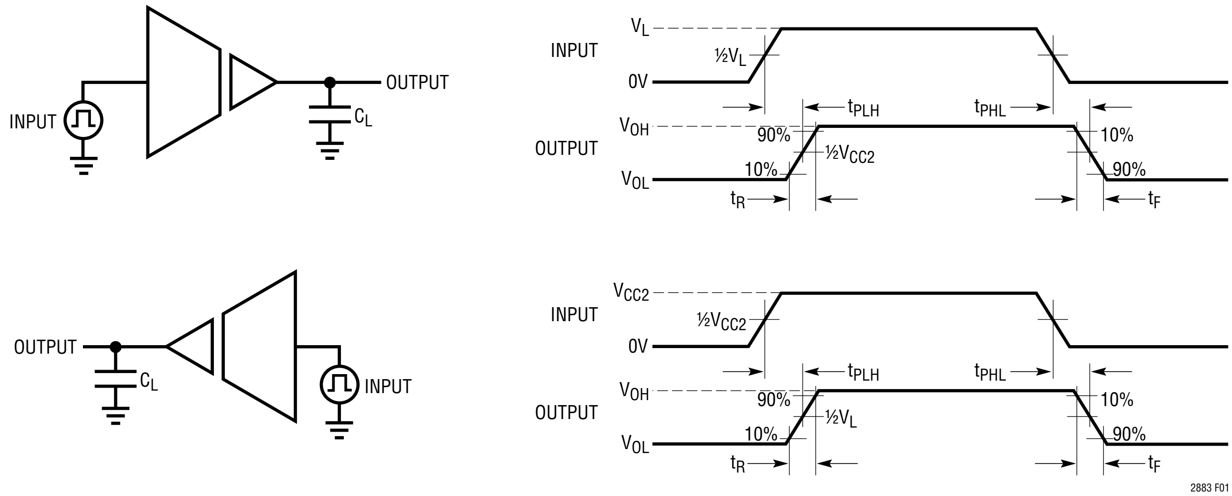


Figure 1. Logic Timing Measurements

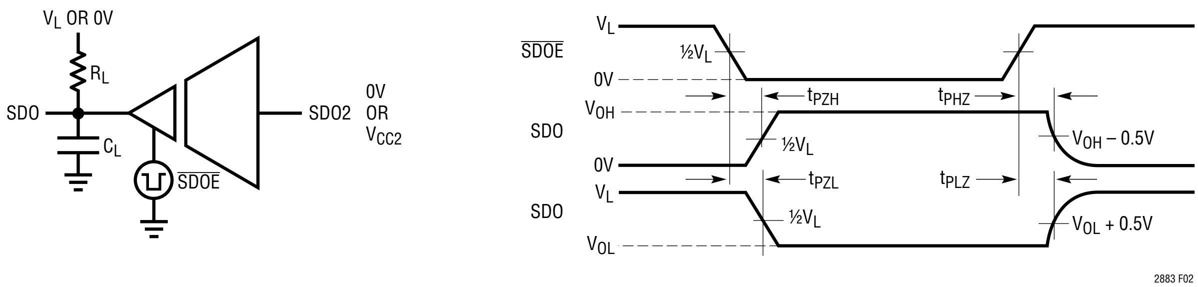


Figure 2. Logic Enable/Disable Time

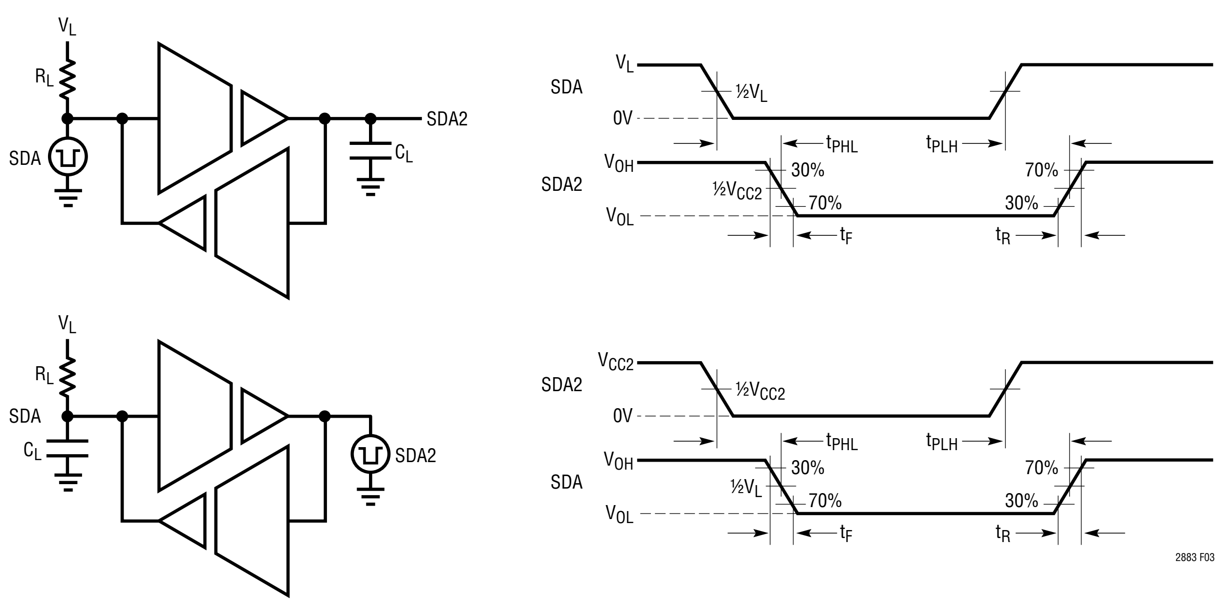


Figure 3. I²C Timing Measurements

APPLICATIONS INFORMATION

Overview

The LTM2883 digital μModule isolator provides a galvanically-isolated robust logic interface, powered by an integrated, regulated DC/DC converter, complete with decoupling capacitors. The LTM2883 is ideal for use in networks where grounds can take on different voltages. Isolation in the LTM2883 blocks high voltage differences, eliminates ground loops and is extremely tolerant of common mode transients between ground planes. Error-free operation is maintained through common mode events greater than 30kV/μs providing excellent noise isolation.

Isolator μModule Technology

The LTM2883 utilizes isolator μModule technology to translate signals and power across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using coreless transformers formed in the μModule substrate. This system, complete with data refresh, error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The μModule technology provides the means to combine the isolated signaling with multiple regulators and a powerful isolated DC/DC converter in one small package.

DC/DC Converter

The LTM2883 contains a fully integrated DC/DC converter, including the transformer, so that no external components are necessary. The logic side contains a full-bridge driver, running at 2MHz, and is AC-coupled to a single transformer primary. A series DC blocking capacitor prevents transformer saturation due to driver duty cycle imbalance. The transformer scales the primary voltage, and is rectified by a full-wave voltage doubler. This topology allows for a single diode drop, as in a center tapped full-wave bridge, and eliminates transformer saturation caused by secondary imbalances.

The DC/DC converter is connected to a low dropout regulator (LDO) to provide a regulated 5V output.

An integrated boost converter generates a regulated 14V supply and a charge pumped –14V supply. These rails are regulated to ±12.5V respectively by low dropout regulators. Performance of the –12.5V supply is enhanced by loading the 12.5V supply. A load current of 1.5mA is sufficient to improve static and dynamic load regulation characteristics of the –12.5V output. The increased load allows the boost regulator to operate continuously and in turn improves the regulation of the inverting charge pump.

The internal power solution is sufficient to provide a minimum of 20mA of current from V_{CC2} and V^+, and 15mA from $V^–$. V_{CC} and V_{CC2} are each bypassed with 2.2μF ceramic capacitors, and V^+ and $V^–$ are bypassed with 1μF ceramic capacitors.

V_L Logic Supply

A separate logic supply pin V_L allows the LTM2883 to interface with any logic signal from 1.62V to 5.5V as shown in Figure 4. Simply connect the desired logic supply to V_L.

There is no interdependency between V_{CC} and V_L; they may simultaneously operate at any voltage within their specified operating ranges and sequence in any order. V_L is bypassed internally by a 2.2μF capacitor.

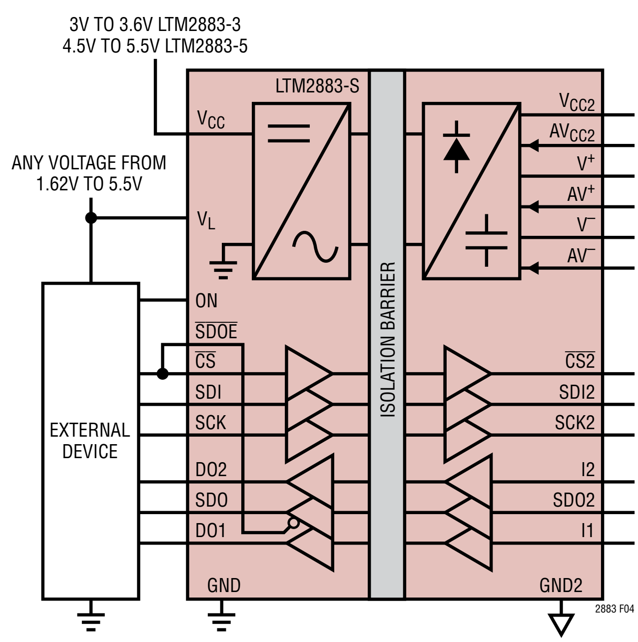


Figure 4. V_{CC} and V_L Are Independent

Hot-Plugging Safely

Caution must be exercised in applications where power is plugged into the LTM2883's power supplies, V_{CC} or V_L, due to the integrated ceramic decoupling capacitors. The

APPLICATIONS INFORMATION

parasitic cable inductance along with the high Q characteristics of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage ratings and damage the LTM2883. Refer to Analog Devices Application Note 88, entitled Ceramic Input Capacitors Can Cause Overvoltage Transients for a detailed discussion and mitigation of this phenomenon.

Isolated Supply Adjustable Operation

The three isolated power rails may be adjusted by connection of a single resistor from the adjust pin of each output to its associated output voltage or to GND2. The pre-configured voltages represent the maximums for guaranteed performance. Figure 5 illustrates configuration of the output power rails for V_{CC2} = 3.3V, V^+ = 10V, and V^- = –10V.

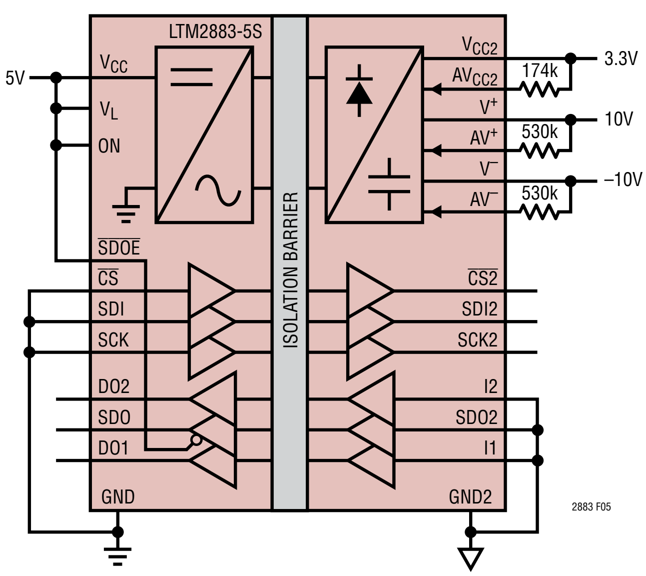


Figure 5. Adjustable Voltage Rails

To decrease the output voltage a resistor must be connected from the output voltage pin to the associated adjust pin. To increase the output voltage connect a resistor to the adjust pin to GND2. Use the equations listed in Table 1 to calculate the resistances required to adjust each output. The output voltage adjustment range for V_{CC2} is 3V to 5.5V. Adjustment range for V^+ and V^- is ±1.22V to approximately ±13.5V. Operation at low output voltages for V^+ or V^- may result in thermal shutdown due to low dropout regulator power dissipation.

Table 1. Voltage Adjustment Formula

OUTPUT VOLTAGE	RESISTOR (Ax TO Vx) TO REDUCE OUTPUT	RESISTOR (Ax TO GND2) TO INCREASE OUTPUT
V_{CC2}	$\frac{110k \bullet (V_{CC2} - 0.6)}{5 - V_{CC2}}$	$\frac{66k}{V_{CC2} - 5}$
V^+, V^-	$\frac{150k \bullet (\lvert V^+, V^- \rvert - 1.22)}{12.5 - \lvert V^+, V^- \rvert}$	$\frac{183k}{\lvert V^+, V^- \rvert - 12.5}$

Channel Timing Uncertainty

Multiple channels are supported across the isolation boundary by encoding and decoding of the inputs and outputs. Up to three signals in each direction are assembled as a serial packet and transferred across the isolation barrier. The time required to transfer all 3 bits is 100ns maximum, and sets the limit for how often a signal can change on the opposite side of the barrier. Encoding transmission is independent for each data direction. The technique used assigns SCK or SCL on the logic side, and SDO2 or I2 on the isolated side, the highest priority such that there is no jitter on the associated output channels, only delay. This preemptive scheme will produce a certain amount of uncertainty on the other isolation channels. The resulting pulse width uncertainty on these low priority channels is typically ±6ns, but may vary up to ±44ns if the low priority channels are not encoded within the same high priority serial packet.

Serial Peripheral Interface (SPI) Bus

The LTM2883-S provides a SPI compatible isolated interface. The maximum data rate is a function of the inherent channel propagation delays, channel to channel pulse width uncertainty, and data direction requirements. Channel timing is detailed in Figures 5 through 8 and Tables 3 and 4. The SPI protocol supports four unique timing configurations defined by the clock polarity (CPOL) and clock phase (CPHA) summarized in Table 2.

Table 2. SPI Mode

CPOL	CPHA	DATA TO (CLOCK) RELATIONSHIP	
0	0	Sample (Rising)	Set-Up (Falling)
0	1	Set-Up (Rising)	Sample (Falling)
1	0	Sample (Falling)	Set-Up (Rising)
1	1	Set-Up (Falling)	Sample (Rising)

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APPLICATIONS INFORMATION

The maximum data rate for bidirectional communication is 4MHz, based on a synchronous system, as detailed in the timing waveforms. Slightly higher data rates may be achieved by skewing the clock duty cycle and minimizing the SDO to SCK set-up time, however the clock rate is still dominated by the system propagation delays. A discussion of the critical timing paths relative to Figure 6 and 7 follows.

- $\overline{CS}$ to SCK (master sample SDO, 1st SDO valid)

  $t_0 \rightarrow t_1$ ≈50ns, $\overline{CS}$ to $\overline{CS2}$ propagation delay

  $t_1 \rightarrow t_{1+}$ Isolated slave device propagation (response time), asserts SDO2

  $t_1 \rightarrow t_3$ ≈50ns, SDO2 to SDO propagation delay

  $t_3 \rightarrow t_5$ Set-up time for master SDO to SCK

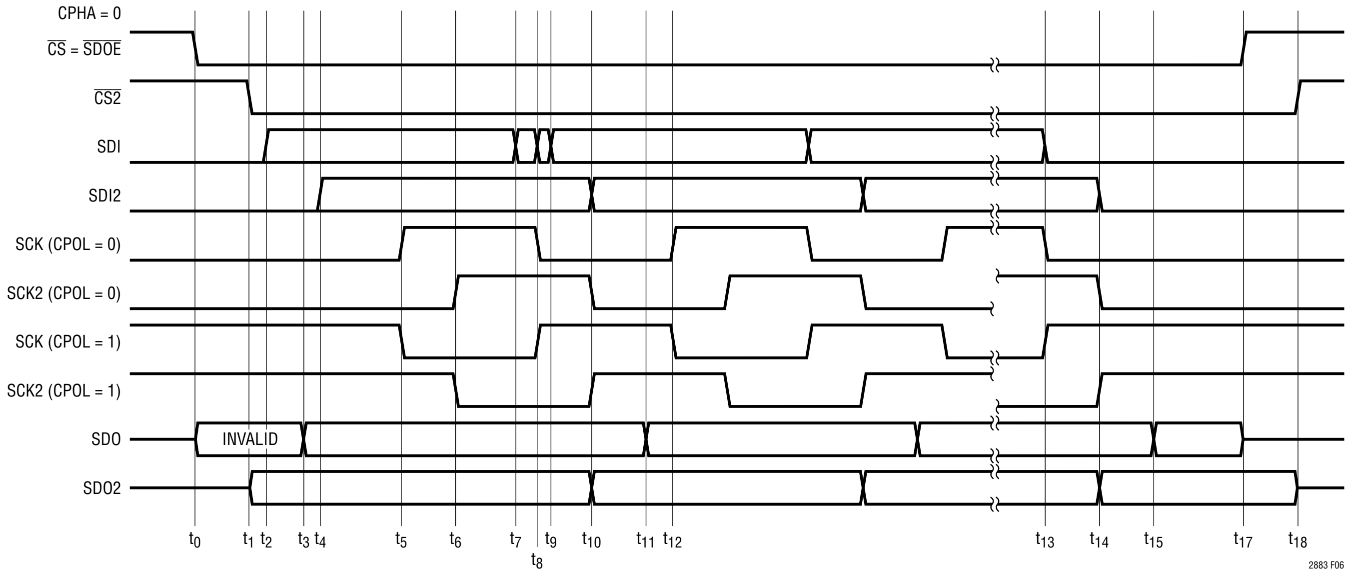

Figure 6. SPI Timing, Bidirectional, CPHA = 0

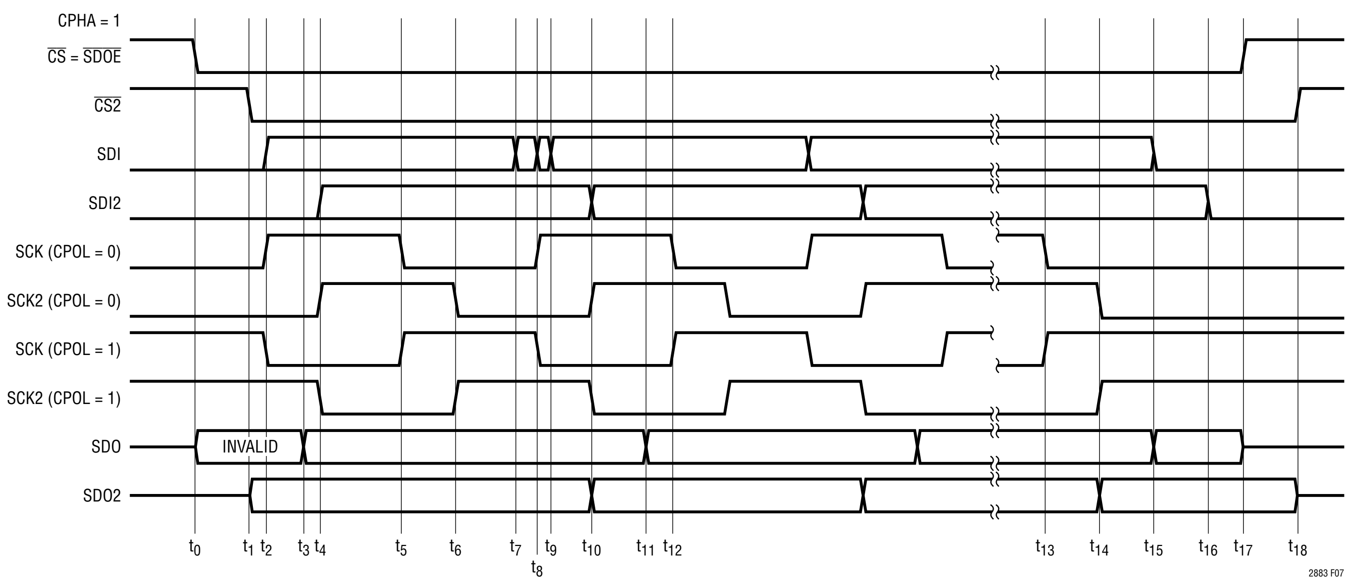

Figure 7. SPI Timing, Bidirectional, CPHA = 1

APPLICATIONS INFORMATION

- SDI to SCK (master data write to slave)

  $t_2 \rightarrow t_4$ ≈50ns, SDI to SDI2 propagation delay

  $t_5 \rightarrow t_6$ ≈50ns, SCK to SCK2 propagation delay

  $t_2 \rightarrow t_5$ ≥50ns, SDI to SCK, separate packet non-zero set-up time

  $t_4 \rightarrow t_6$ ≥50ns, SDI2 to SCK2, separate packet non-zero set-up time

- SDO to SCK (master sample SDO, subsequent SDO valid)

  t_8 set-up data transition SDI and SCK

  $t_8 \rightarrow t_{10}$ ≈50ns, SDI to SDI2 and SCK to SCK2 propagation delay

  t_{10} SDO2 data transition in response to SCK2

  $t_{10} \rightarrow t_{11}$ ≈50ns, SDO2 to SDO propagation delay

  $t_{11} \rightarrow t_{12}$ Set-up time for master SDO to SCK

Table 3. Bidirectional SPI Timing Event Description

TIME	CPHA	EVENT DESCRIPTION
t_0	0, 1	Asynchronous chip select, may be synchronous to SDI but may not lag by more than 3ns. Logic side slave data output enabled, initial data is not equivalent to slave device data output
t_0 to t_1, t_{17} to t_{18}	0, 1	Propagation delay chip select, logic to isolated side, 50ns typical
t_1	0, 1	Slave device chip select output data enable
t_2	0	Start of data transmission, data set-up
	1	Start of transmission, data and clock set-up. Data transition must be within –13ns to 3ns of clock edge
t_1 to t_3	0, 1	Propagation delay of slave data, isolated to logic side, 50ns typical
t_3	0, 1	Slave data output valid, logic side
t_2 to t_4	0	Propagation delay of data, logic side to isolated side
	1	Propagation delay of data and clock, logic side to isolated side
t_5	0, 1	Logic side data sample time, half clock period delay from data set-up transition
t_5 to t_6	0, 1	Propagation delay of clock, logic to isolated side
t_6	0, 1	Isolated side data sample time
t_8	0, 1	Synchronous data and clock transition, logic side
t_7 to t_8	0, 1	Data to clock delay, must be ≤13ns
t_8 to t_9	0, 1	Clock to data delay, must be ≤3ns
t_8 to t_{10}	0, 1	Propagation delay clock and data, logic to isolated side
t_{10}, t_{14}	0, 1	Slave device data transition
t_{10} to t_{11}, t_{14} to t_{15}	0, 1	Propagation delay slave data, isolated to logic side
t_{11} to t_{12}	0, 1	Slave data output to sample clock set-up time
t_{13}	0	Last data and clock transition logic side
	1	Last sample clock transition logic side
t_{13} to t_{14}	0	Propagation delay data and clock, logic to isolated side
	1	Propagation delay clock, logic to isolated side
t_{15}	0	Last slave data output transition logic side
	1	Last slave data output and data transition, logic side
t_{15} to t_{16}	1	Propagation delay data, logic to isolated side
t_{17}	0, 1	Asynchronous chip select transition, end of transmission. Disable slave data output logic side
t_{18}	0, 1	Chip select transition isolated side, slave data output disabled

APPLICATIONS INFORMATION

Maximum data rate for single direction communication, master to slave, is 8MHz, limited by the systems encoding/decoding scheme or propagation delay. Timing details for both variations of clock phase are shown in Figures 8 and 9 and Table 4.

Additional requirements to insure maximum data rate are:

- $\overline{CS}$ is transmitted prior to (asynchronous) or within the same (synchronous) data packet as SDI
- SDI and SCK set-up data transition occur within the same data packet. Referencing Figure 6, SDI can precede SCK by up to 13ns ($t_7 \rightarrow t_8$) or lag SCK by 3ns ($t_8 \rightarrow t_9$) and not violate this requirement. Similarly in Figure 8, SDI can precede SCK by up to 13ns ($t_4 \rightarrow t_5$) or lag SCK by 3ns ($t_5 \rightarrow t_6$).

Inter-IC Communication (I²C) Bus

The LTM2883-I provides an I²C compatible isolated interface, Clock (SCL) is unidirectional, supporting master mode only, and data (SDA) is bidirectional. The maximum

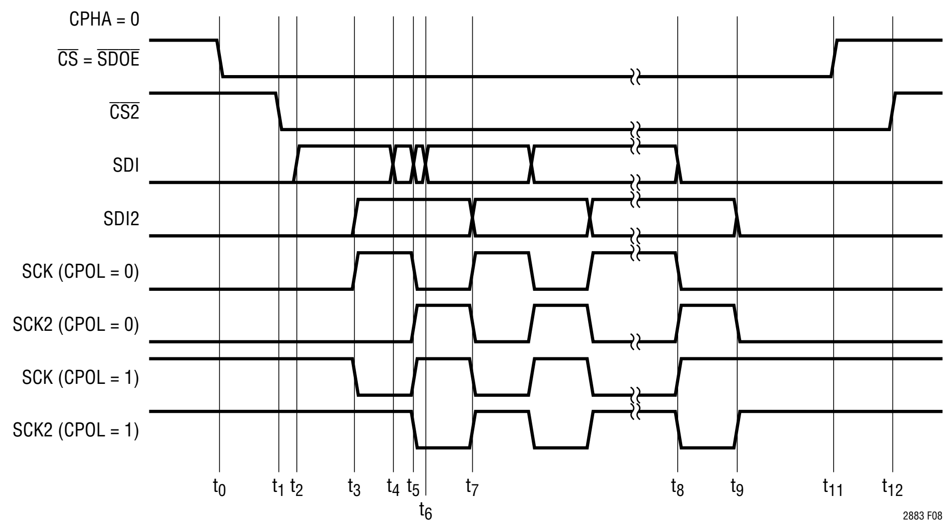

Figure 8. SPI Timing, Unidirectional, CPHA = 0

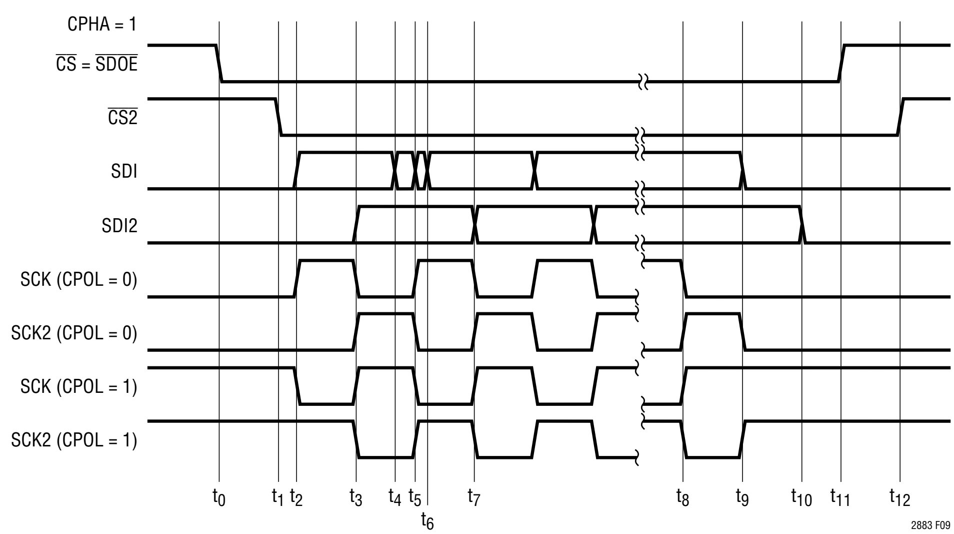

Figure 9. SPI Timing, Unidirectional, CPHA = 1

APPLICATIONS INFORMATION

Table 4. Unidirectional SPI Timing Event Description

TIME	CPHA	EVENT DESCRIPTION
t_0	0, 1	Asynchronous chip select, may be synchronous to SDI but may not lag by more than 3ns
t_0 to t_1	0, 1	Propagation delay chip select, logic to isolated side
t_2	0	Start of data transmission, data set-up
	1	Start of transmission, data and clock set-up. Data transition must be within –13ns to 3ns of clock edge
t_2 to t_3	0	Propagation delay of data, logic side to isolated side
	1	Propagation delay of data and clock, logic side to isolated side
t_3	0, 1	Logic side data sample time, half clock period delay from data set-up transition
t_3 to t_5	0, 1	Clock propagation delay, clock and data transition
t_4 to t_5	0, 1	Data to clock delay, must be ≤13ns
t_5 to t_6	0, 1	Clock to data delay, must be ≤3ns
t_5 to t_7	0, 1	Data and clock propagation delay
t_8	0	Last clock and data transition
	1	Last clock transition
t_8 to t_9	0	Clock and data propagation delay
	1	Clock propagation delay
t_9 to t_{10}	1	Data propagation delay
t_{11}	0, 1	Asynchronous chip select transition, end of transmission
t_{12}	0, 1	Chip select transition isolated side

data rate is 400kHz which supports fast-mode I^2C. Timing is detailed in Figure 10. The data rate is limited by the slave acknowledge setup time ($t_{SU;ACK}$), consisting of the I^2C standard minimum setup time ($t_{SU;DAT}$) of 100ns, maximum clock propagation delay of 225ns, glitch filter and isolated data delay of 350ns maximum, and the combined isolated and logic data fall time of 500ns at maximum bus loading. The total setup time reduces the I^2C data hold time ($t_{HD;DAT}$) to a maximum of 125ns, guaranteeing sufficient data setup time ($t_{SU;ACK}$).

The isolated side bidirectional serial data pin, SDA2, simplified schematic is shown in Figure 11. An internal 1.8mA current source provides a pull-up for SDA2. Do not connect any other pull-up device to SDA2. This current source is sufficient to satisfy the system requirements for bus capacitances greater than 200pF in FAST mode and greater than 400pF in STANDARD mode.

Additional proprietary circuitry monitors the slew rate on the SDA and SDA2 signals to manage directional control across the isolation barrier. Slew rates on both pins must be greater than 1V/μs for proper operation.

The logic side bidirectional serial data pin, SDA, requires a pull-up resistor or current source connected to V_L. Follow

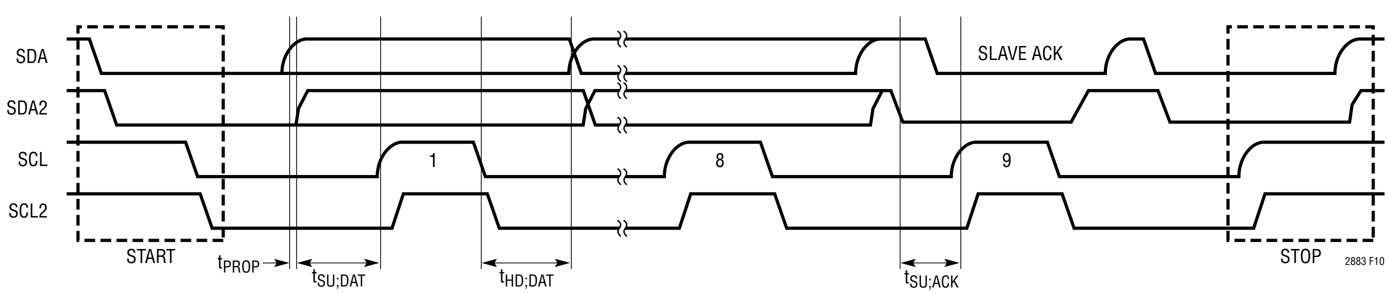

Figure 10. I^2C Timing Diagram

APPLICATIONS INFORMATION

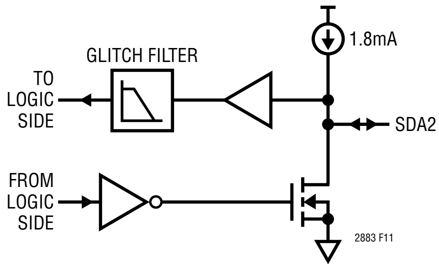

Figure 11. Isolated SDA2 Pin Schematic

the requirements in Figures 12 and 13 for the appropriate pull-up resistor on SDA that satisfies the desired rise time specifications and V_{OL} maximum limits for FAST and STANDARD modes. The resistance curves represent the maximum resistance boundary; any value may be used to the left of the appropriate curve.

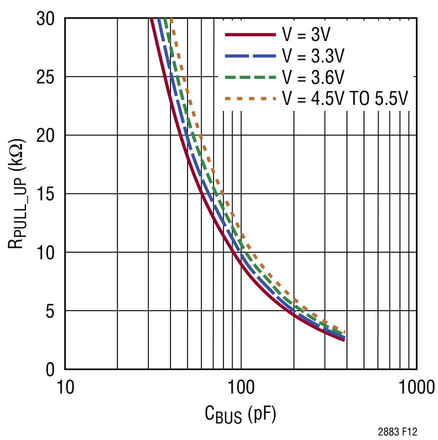

Figure 12. Maximum Standard Speed Pull-Up Resistance on SDA

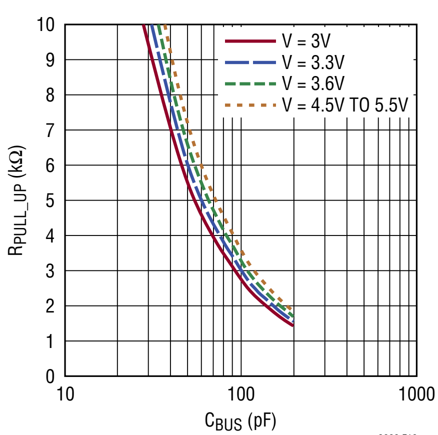

Figure 13. Maximum Fast Speed Pull-Up Resistance on SDA

The isolated side clock pin, SCL2, has a weak push-pull output driver; do not connect an external pull-up device. SCL2 is compatible with I^2C devices without clock stretching. On lightly loaded connections, a 100pF capacitor from SCL2 to GND2 or RC low-pass filter (R = 500Ω C = 100pF) can be used to increase the rise and fall times and minimize noise.

Some consideration must be given to signal coupling between SCL2 and SDA2. Separate these signals on a printed circuit board or route with ground between. If these signals are wired off board, twist SCL2 with V_{CC2} and/or GND2 and SDA2 with GND2 and/or V_{CC2}, do not twist SCL2 and SDA2 together. If coupling between SCL2 and SDA2 is unavoidable, place the aforementioned RC filter at the SCL2 pin to reduce noise injection onto SDA2.

RF, Magnetic Field Immunity

The isolator μModule technology used within the LTM2883 has been independently evaluated, and successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3	Radiated, Radio-Frequency, Electromagnetic Field Immunity
EN 61000-4-8	Power Frequency Magnetic Field Immunity
EN 61000-4-9	Pulsed Magnetic Field Immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 5.

Table 5.

TEST	FREQUENCY	FIELD STRENGTH
EN 61000-4-3 Annex D	80MHz to 1GHz	10V/m
	1.4MHz to 2GHz	3V/m
	2GHz to 2.7GHz	1V/m
EN 61000-4-8 Level 4	50Hz and 60Hz	30A/m
EN 61000-4-8 Level 5	60Hz	100A/m*
EN 61000-4-9 Level 5	Pulse	1000A/m

*non IEC method

APPLICATIONS INFORMATION

PCB Layout

The high integration of the LTM2883 makes PCB layout very simple. However, to optimize its electrical isolation characteristics, EMI, and thermal performance, some layout considerations are necessary.

- Under heavily loaded conditions V_{CC} and GND current can exceed 300mA. Sufficient copper must be used on the PCB to insure resistive losses do not cause the supply voltage to drop below the minimum allowed level. Similarly, the V_{CC2} and GND2 conductors must be sized to support any external load current. These heavy copper traces will also help to reduce thermal stress and improve the thermal conductivity.
- Input and output decoupling is not required, since these components are integrated within the package. An additional bulk capacitor with a value of 6.8µF to 22µF is recommended. The high ESR of this capacitor reduces board resonances and minimizes voltage spikes caused by hot plugging of the supply voltage. For EMI sensitive applications, an additional low ESL ceramic capacitor of 1µF to 4.7µF, placed as close to the power and ground terminals as possible, is recommended. Alternatively, a number of smaller value parallel capacitors may be used to reduce ESL and achieve the same net capacitance.
- Do not place copper on the PCB between the inner columns of pads. This area must remain open to withstand the rated isolation voltage.
- The use of solid ground planes for GND and GND2 is recommended for non-EMI critical applications to optimize signal fidelity, thermal performance, and to minimize RF emissions due to uncoupled PCB trace conduction. The drawback of using ground planes, where EMI is of concern, is the creation of a dipole antenna structure which can radiate differential voltages formed between GND and GND2. If ground planes are used it is recommended to minimize their area, and use contiguous planes as any openings or splits can exacerbate RF emissions.
- For large ground planes a small capacitance (≤330pF) from GND to GND2, either discrete or embedded within the substrate, provides a low impedance current return path for the module parasitic capacitance, minimizing any high frequency differential voltages and substantially reducing radiated emissions. Discrete capacitance will not be as effective due to parasitic ESL. In addition, voltage rating, leakage, and clearance must be considered for component selection. Embedding the capacitance within the PCB substrate provides a near ideal capacitor and eliminates component selection issues; however, the PCB must be 4 layers. Care must be exercised in applying either technique to insure the voltage rating of the barrier is not compromised.

The PCB layout in Figures 14a and 14b shows the low EMI demo board for the LTM2883. The demo board uses a combination of EMI mitigation techniques, including both embedded PCB bridge capacitance and discrete GND to GND2 capacitors. Two safety rated type Y2 capacitors are used in series, manufactured by MuRata, part number GA342QR7GF471KW01L. The embedded capacitor effectively suppresses emissions above 400MHz, whereas the discrete capacitors are more effective below 400MHz.

EMI performance is shown in Figure 15, measured using a Gigahertz Transverse Electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, Testing and Measurement Techniques – Emission and Immunity Testing in Transverse Electromagnetic Waveguides.

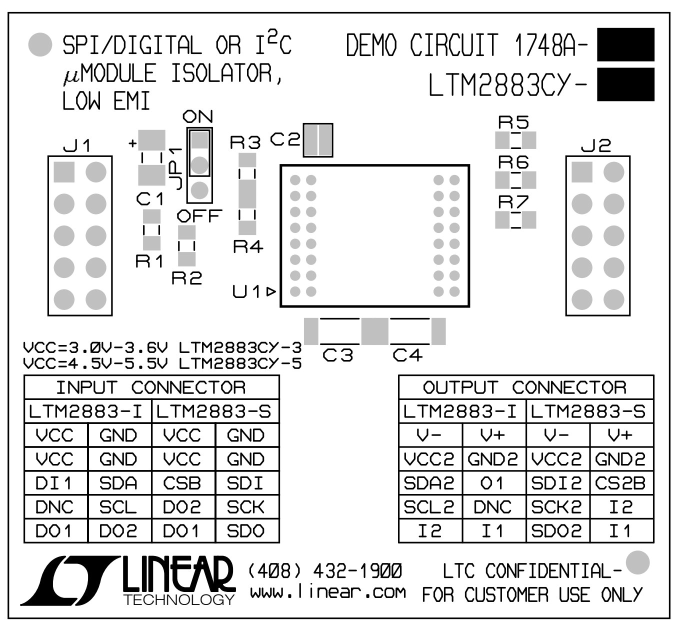

Figure 14a. LTM2883 Low EMI Demo Board Layout

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APPLICATIONS INFORMATION

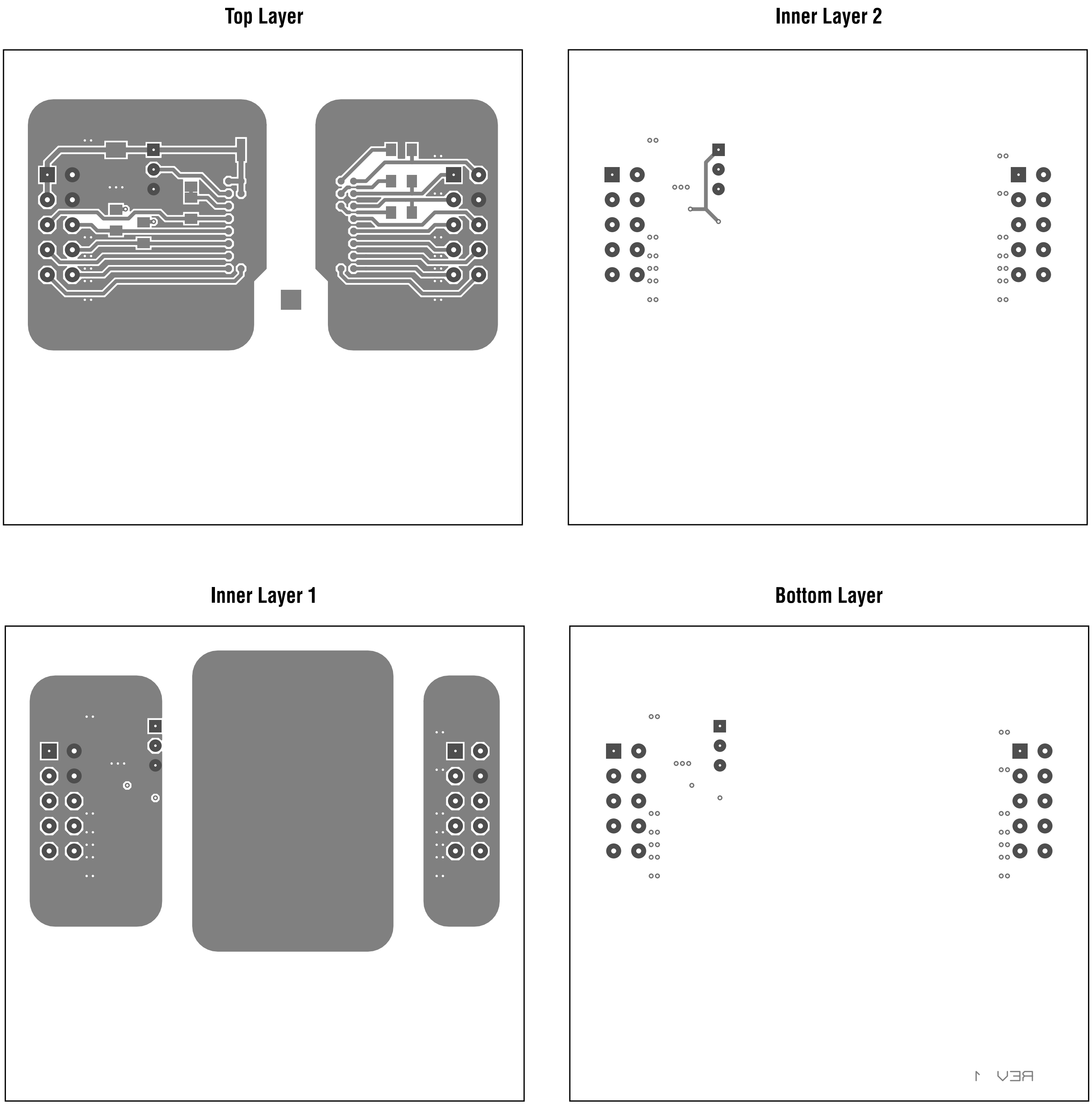

Figure 14b. LTM2883 Low EMI Demo Board Layout (DC1748A)

APPLICATIONS INFORMATION

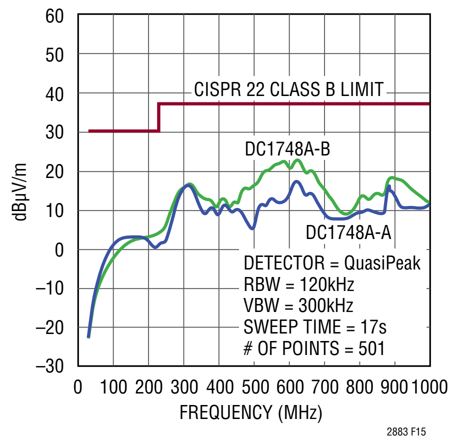

Figure 15. LTM2883 Low EMI Demo Board Emissions

TYPICAL APPLICATIONS

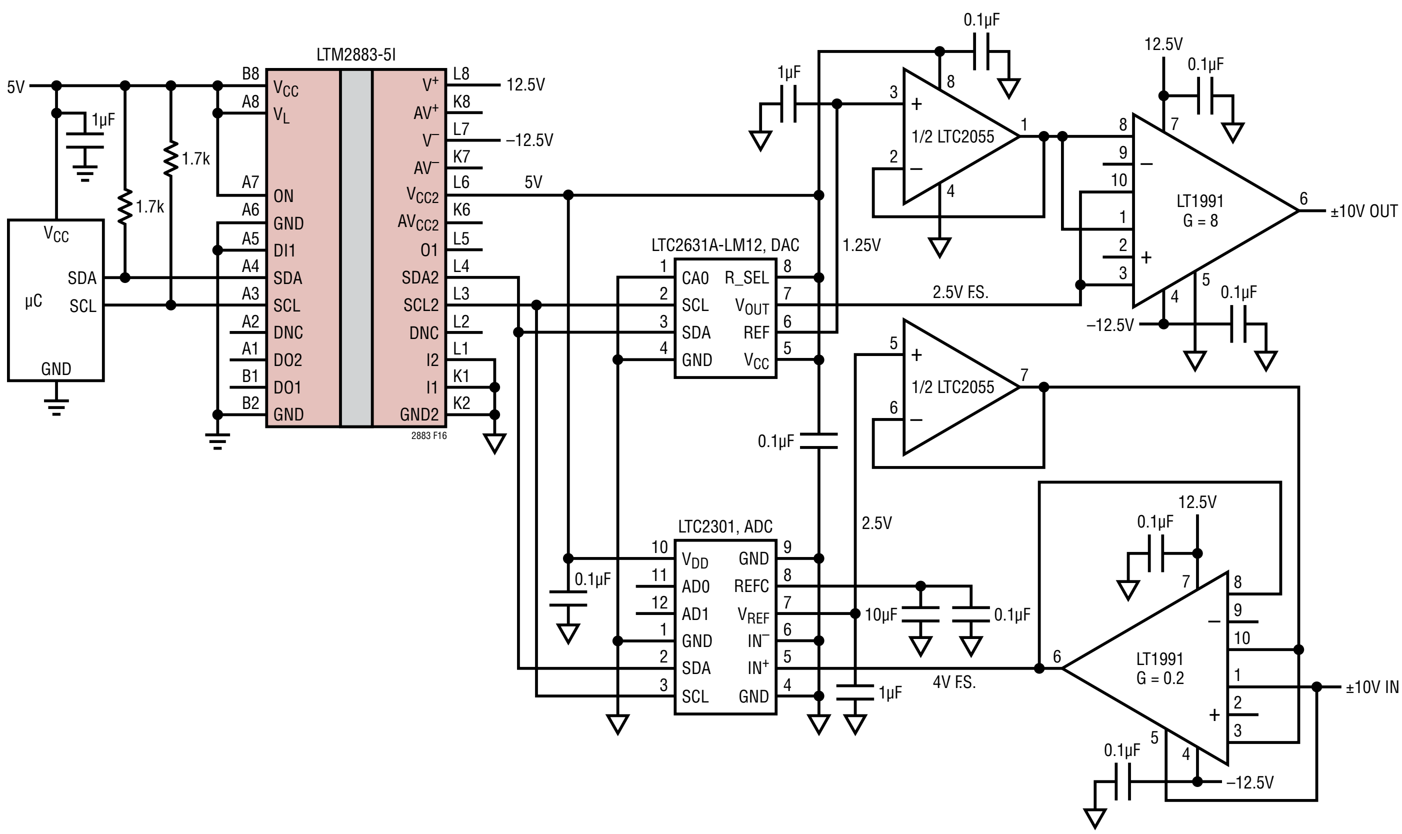

Figure 16. Isolated I²C 12-Bit, ±10V Analog Input and Output

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TYPICAL APPLICATIONS

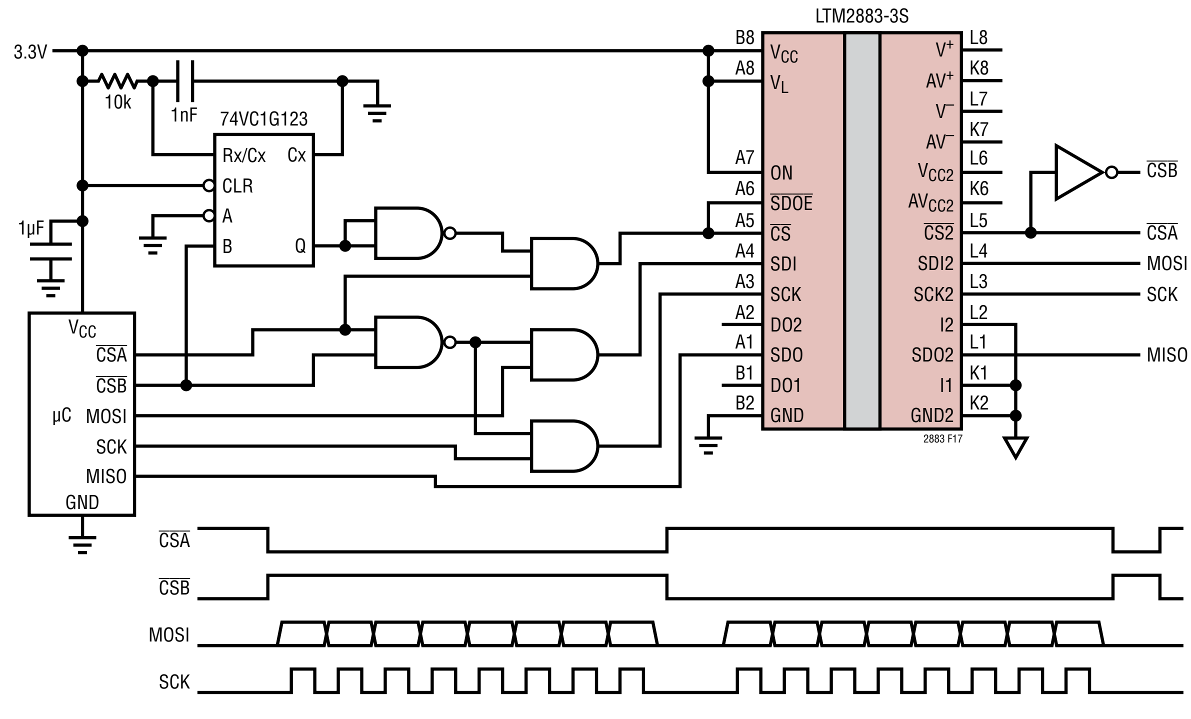


Figure 17. Isolated SPI Device Expansion

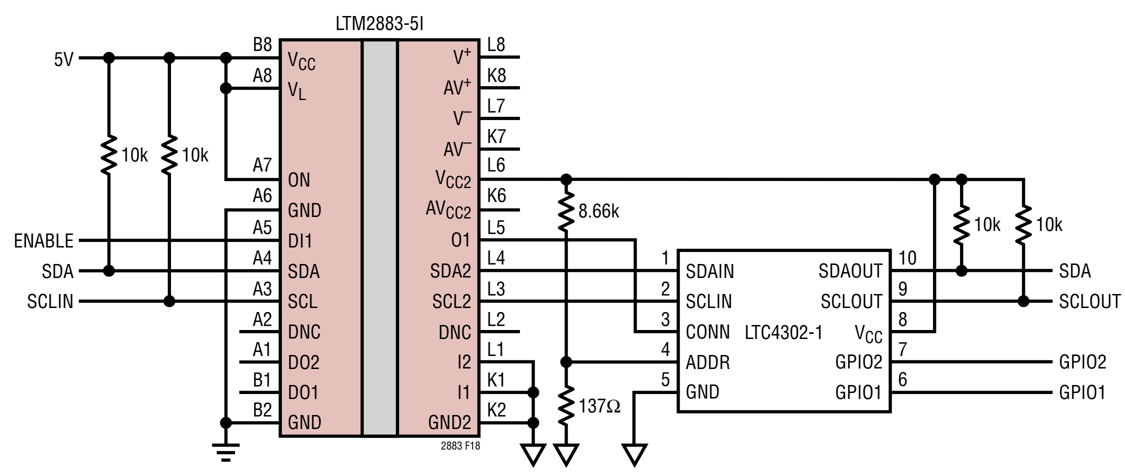
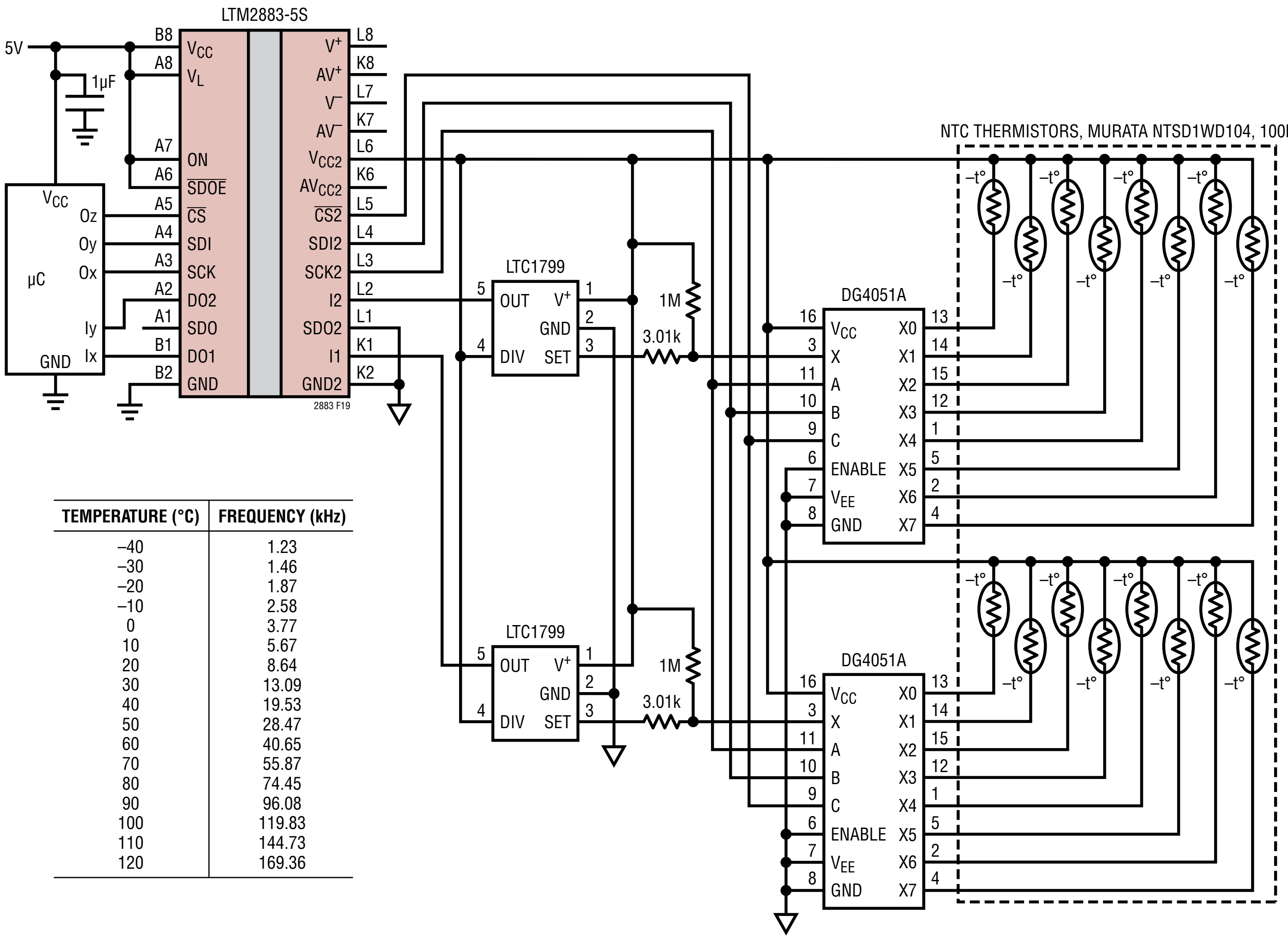


Figure 18. Isolated I^{2}C Buffer with Programmable Outputs

TYPICAL APPLICATIONS



TEMPERATURE (°C)	FREQUENCY (kHz)
–40	1.23
–30	1.46
–20	1.87
–10	2.58
0	3.77
10	5.67
20	8.64
30	13.09
40	19.53
50	28.47
60	40.65
70	55.87
80	74.45
90	96.08
100	119.83
110	144.73
120	169.36

Figure 19. 16-Channel Isolated Temperature to Frequency Converter

TYPICAL APPLICATIONS

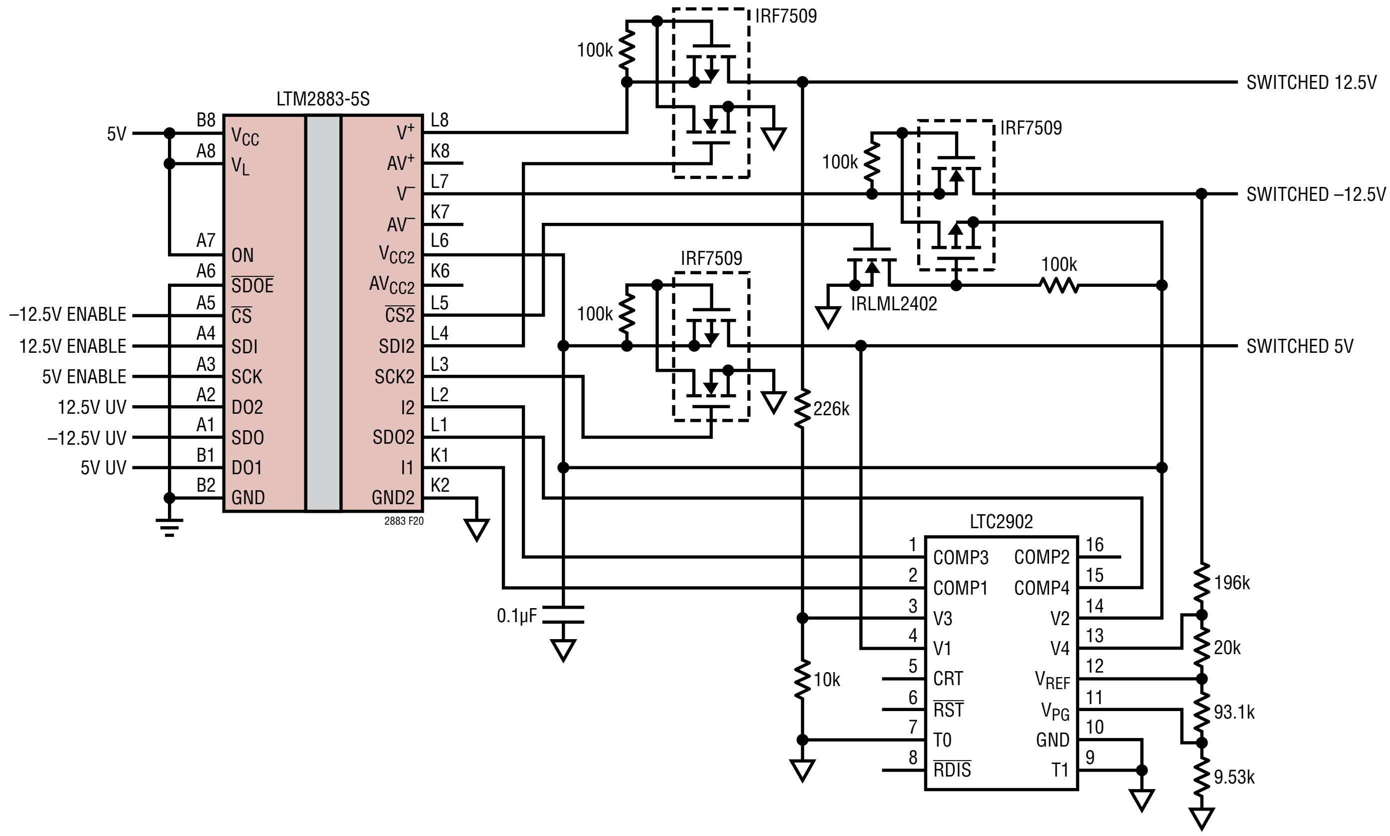


Figure 20. Digitally Switched Triple Power Supply with Undervoltage Monitor

TYPICAL APPLICATIONS

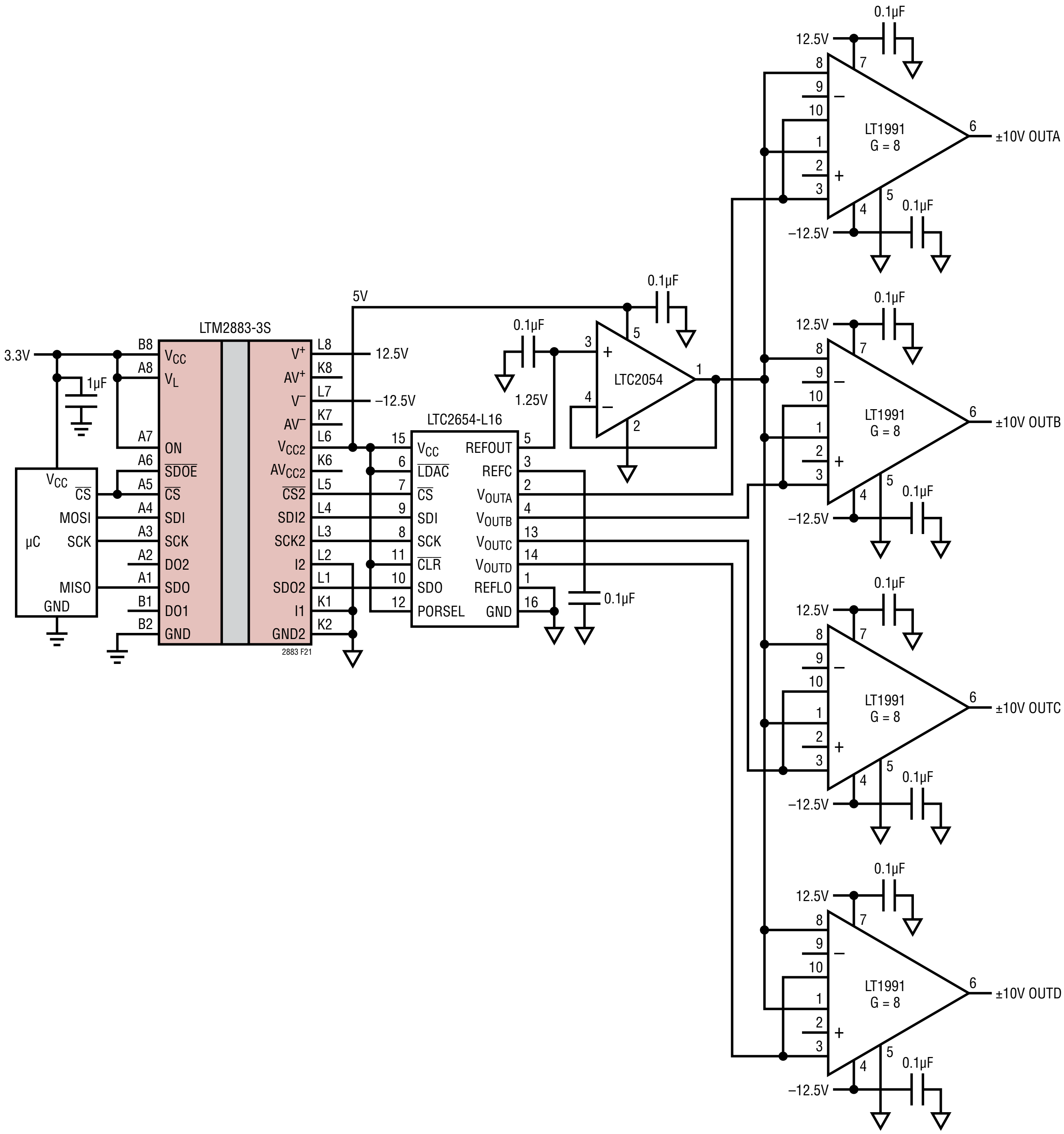


Figure 21. Quad 16-Bit ±10V Output Range DAC

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TYPICAL APPLICATIONS

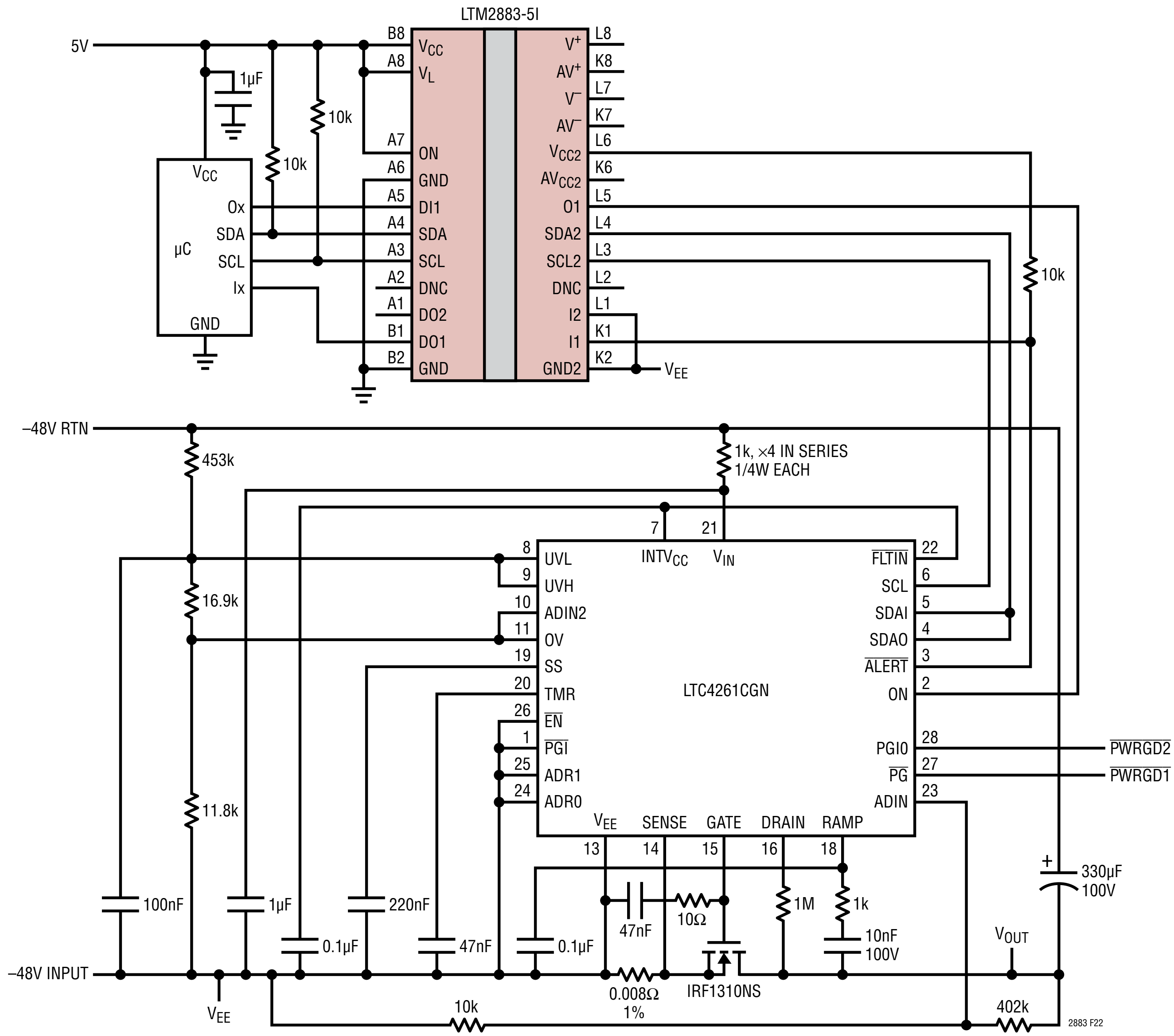


Figure 22. –48V, 200W Hot Swap Controller with Isolated I2C Interface

TYPICAL APPLICATIONS

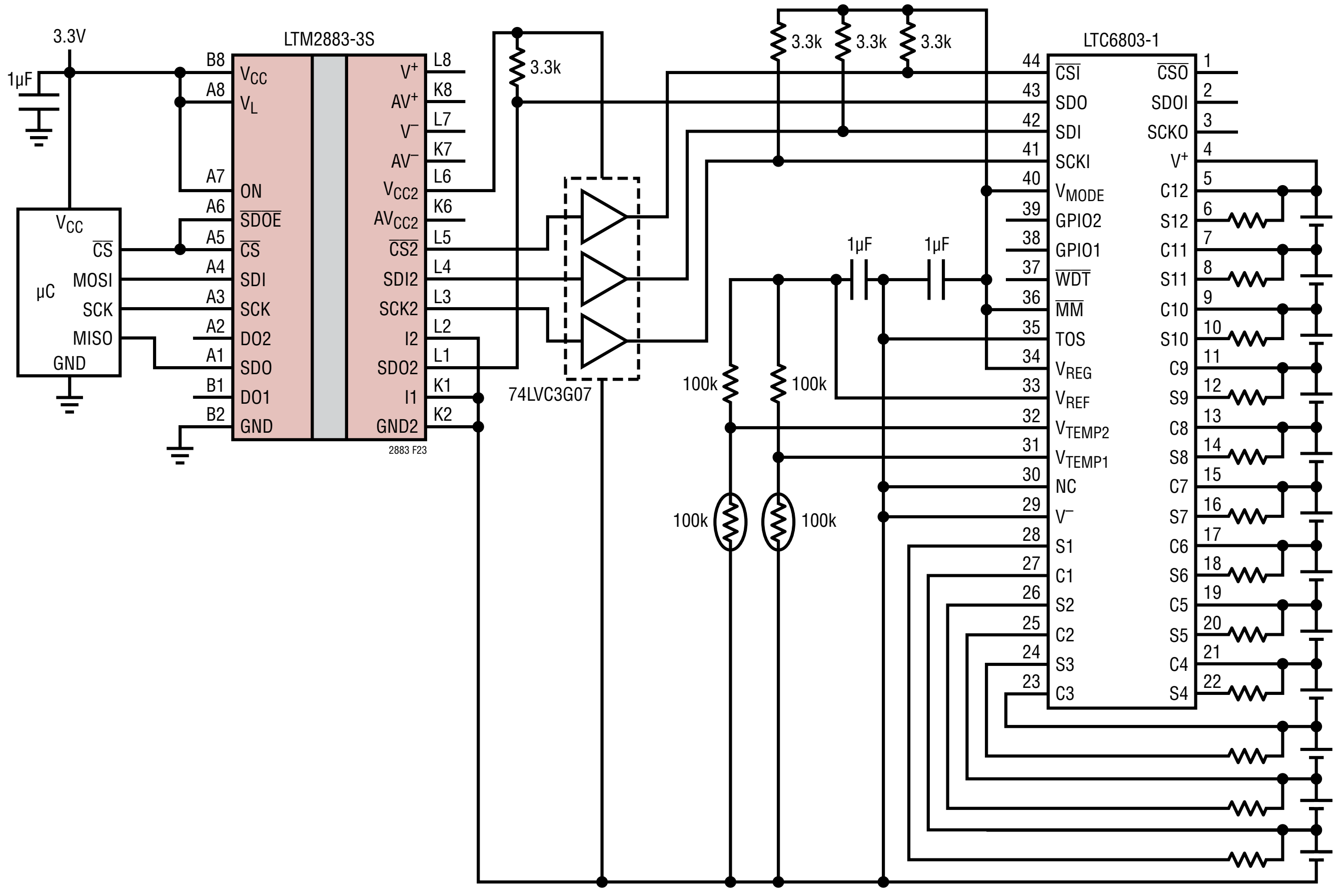
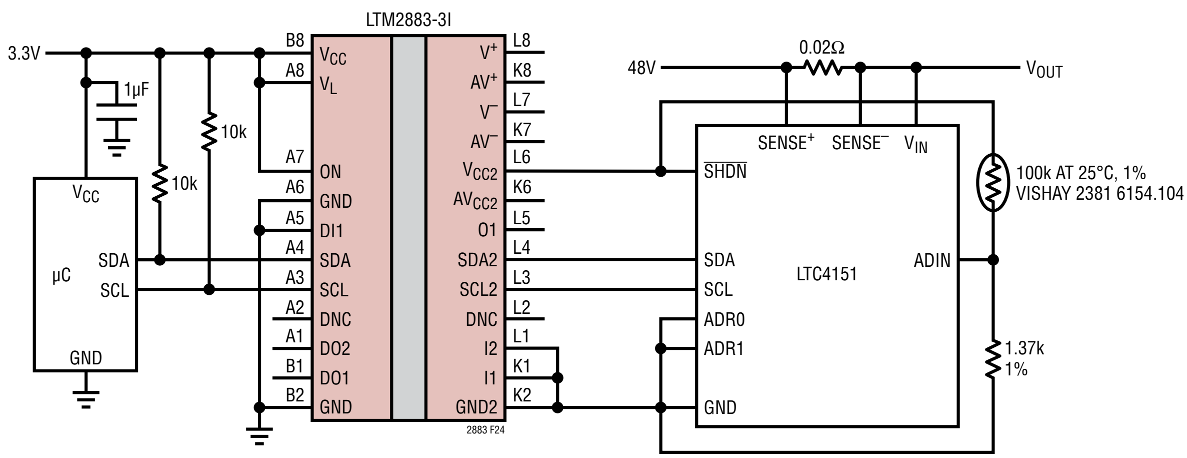


Figure 23. 12-Cell Battery Stack Monitor with Isolated SPI Interface and Low Power Shutdown



$$T(°C) = \frac{3950}{8.965 + LN\left(\frac{1000}{N_{ADIN}} - 1\right)} - 273, -40°C < T < 150°C$$

N_{ADIN} IS THE DIGITAL CODE MEASURED BY THE ADC AT THE ADIN PIN

Figure 24. Isolated I²C Voltage, Current and Temperature Power Supply Monitor

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TYPICAL APPLICATIONS

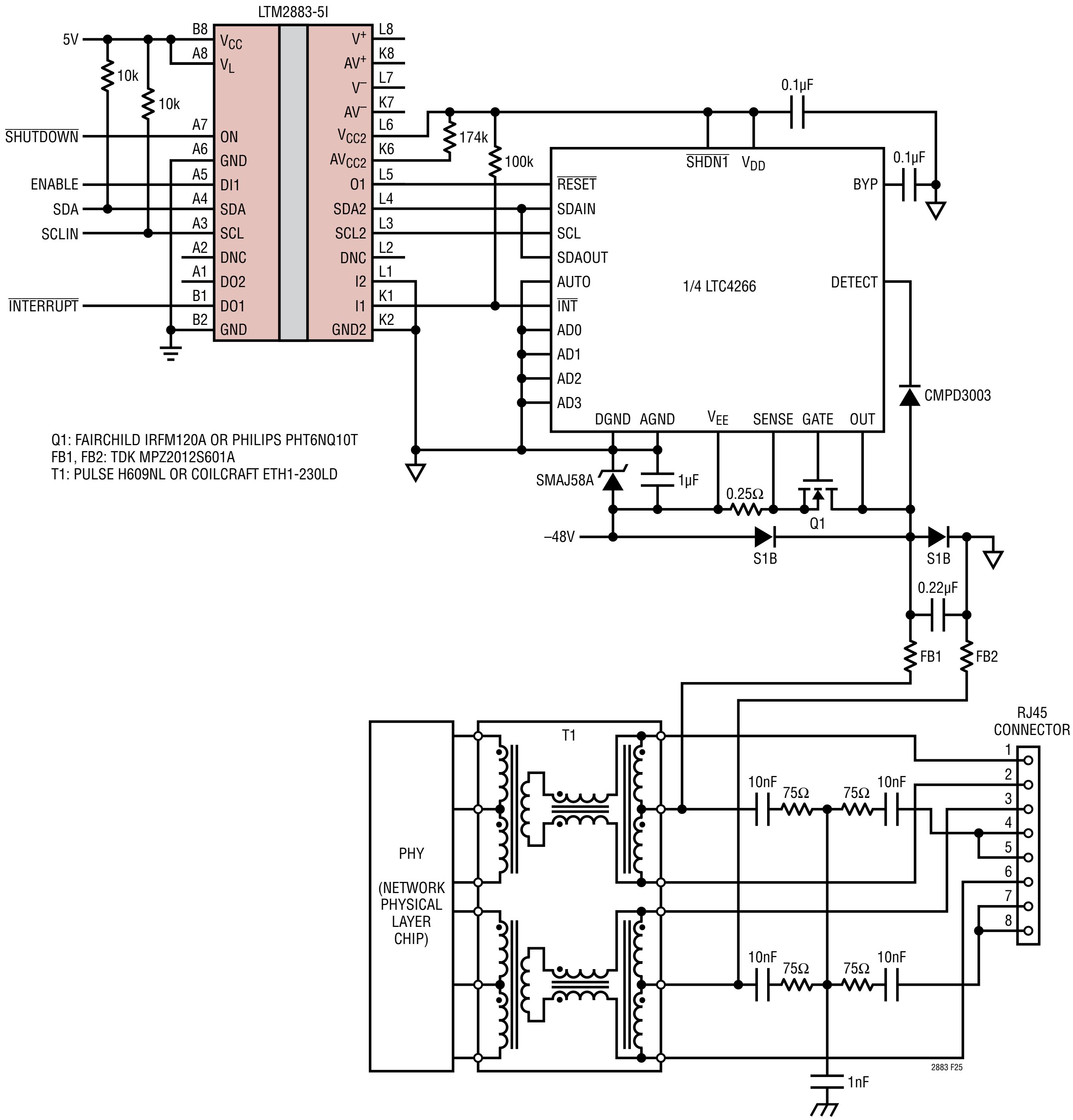
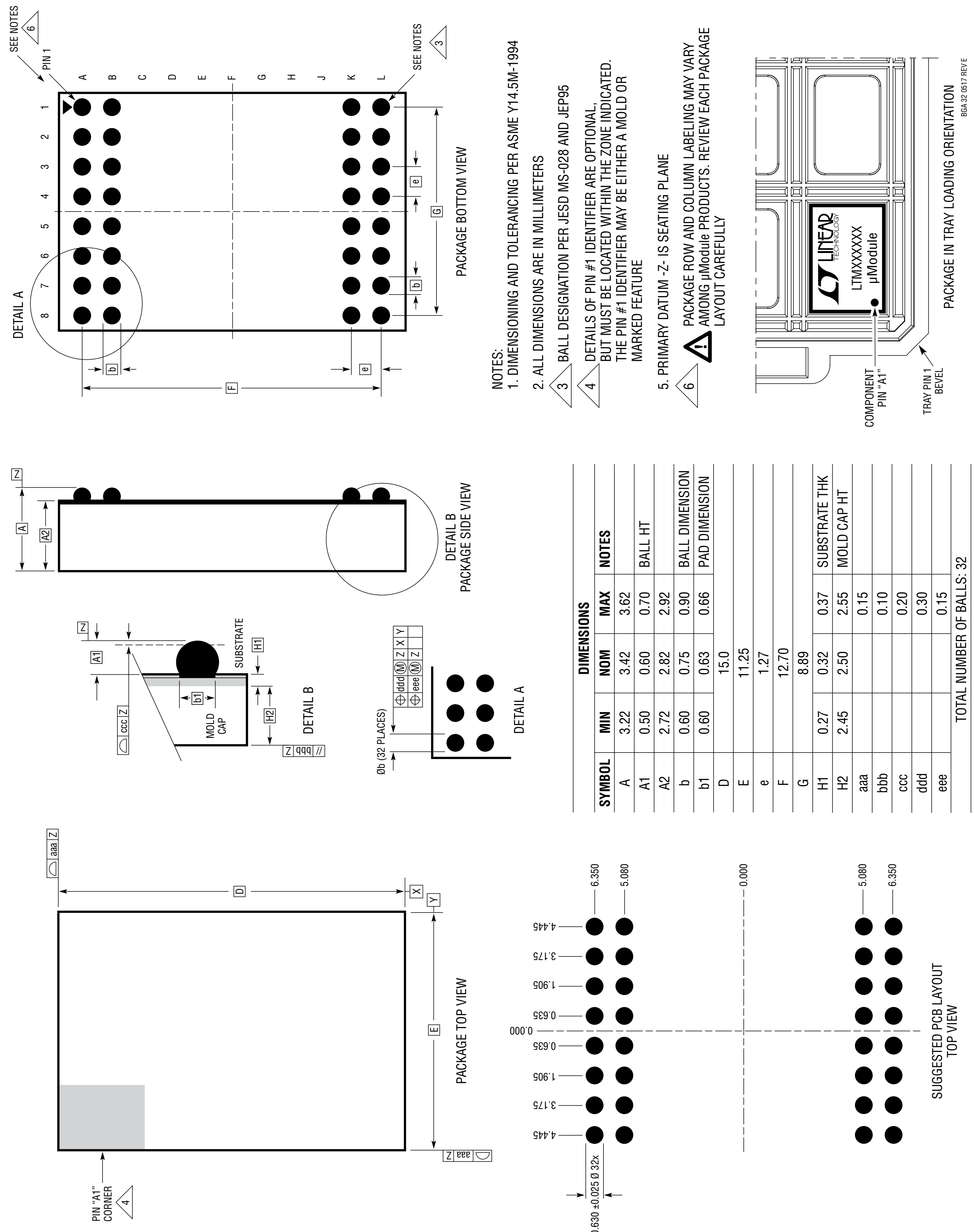


Figure 25. One Complete Isolated Powered Ethernet Port

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM2883#packaging for the most recent package drawings.

BGA Package
32-Lead (15mm × 11.25mm × 3.42mm)
(Reference LTC DWG # 05-08-1851 Rev E)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

SYMBOL	DIMENSIONS MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	BALL HT
A2	2.72	2.82	2.92	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		15.0		
E		11.25		
e		1.27		
F		12.70		
G		8.89		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	2.45	2.50	2.55	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	

TOTAL NUMBER OF BALLS: 32

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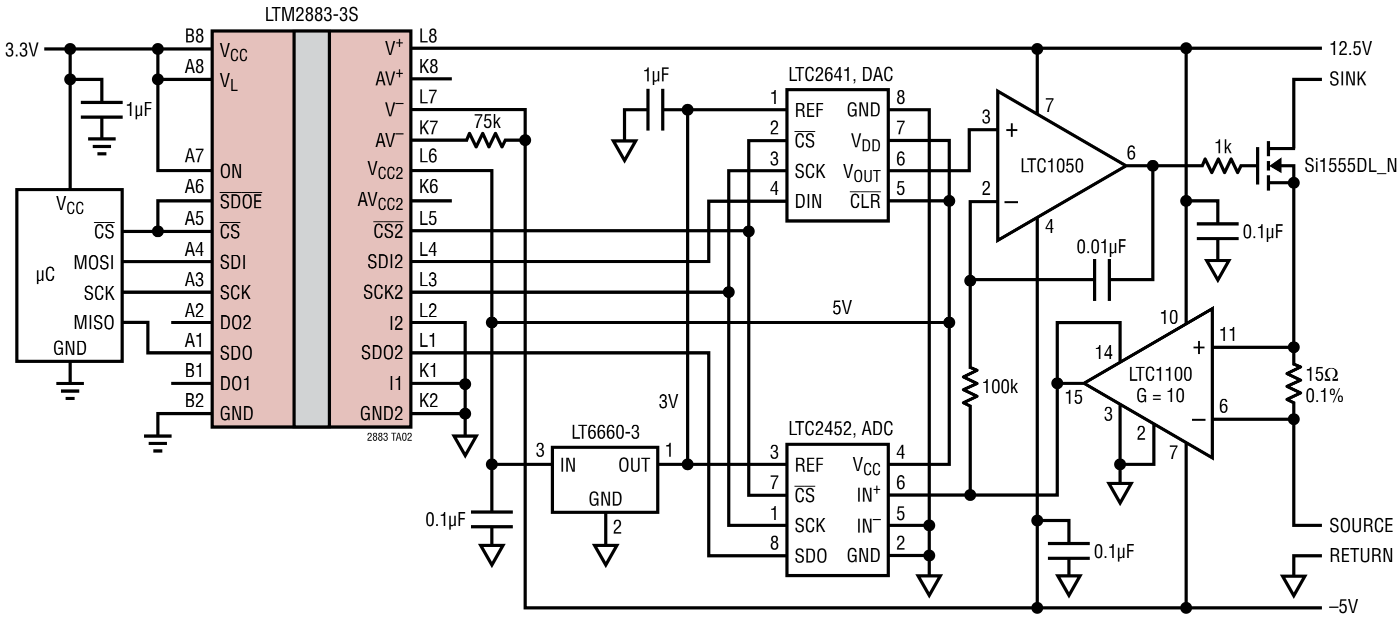
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/12	Storage temperature range updated.	2
B	8/13	Added CTI/DTI parameters and Notes 6, 7 to Isolation Characteristics table.	6, 7
C	5/14	Removed H-grade throughout data sheet.	1-36
		Changed Depth of Erosion parameter.	6
		Changed overtemperature protection threshold.	7
D	11/17	Added H-Grade; removed Obsolete mark from H-Grade.	2, 3
		Raised Maximum Internal Operating Temperature, Storage Temperature Range, and package T_{JMAX}.	2
		Updated graphs showing performance characteristics vs temperature.	8, 9

TYPICAL APPLICATION

Precision 4mA to 20mA Sink/Source with Current Monitor



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM2881	Isolated RS485/RS422 µModule Transceiver Plus Power	20Mbps 2500V_{RMS} Isolation with Power in LGA/BGA Package
LTM2882	Dual Isolated RS232 µModule Transceiver Plus Power	20Mbps 2500V_{RMS} Isolation with Power in LGA/BGA Package
LTC4310	Hot-Swappable I^2C Isolators	Bidirectional I^2C Communication, Low Voltage Level Shifting
LTC6803	Multistack Battery Monitor	Individual Battery Cell Monitoring of High Voltage Battery Stacks, Multiple Devices Interconnected via SPI
LTC2309/ LTC2305/LTC2301	12-Bit, 8-/2-/1-Channel, 14ksps SAR ADCs with I^2C	5V, Internal Reference, Software Compatible Family
LTC2631/LTC2630	Single 12-/10-/8-Bit I^2C or SPI V_{OUT} DACs with 10ppm/°C Reference	180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, Rail-to-Rail Output
LTC2641/LTC2642	16-/14-/12-Bit V_{OUT} DACs	±1LSB INL/DNL, 0.5nV • s Glitch, 1µs Settling, 3mm × 3mm DFN
LTC2452/LTC2453	Ultra-Tiny 16-Bit Differential ±5.5V ΔΣ ADCs, SPI/I^2C	2LSB INL, 50nA Sleep Current, Tiny 3mm × 2mm DFN-8 or TSOT Packages
LTC1859/ LTC1858/LTC1857	8-Channel 16-/14-/12-Bit, 100ksps, ±10V SoftSpan™ SAR ADCs with SPI	5V Supply, Up to ±10V Configurable Unipolar/Bipolar Input Range, Pin Compatible Family in SSOP-28 package
LTC2487/LTC2486	16-Bit 2- or 4-Channel ΔΣ ADCs with Easy Drive™ Inputs and I^2C/SPI Interface	16-Bit and 24-Bit ΔΣ ADC Family, Up to 16 Input Channels and Integrated Temperature Sensor
LTC4303/LTC4304	Hot Swappable I^2C Bus Buffers	2.7V to 5.5V Supply, Rise Time Acceleration, Stuck Bus Protection, ±15kV ESD
LTC1100	Zero-Drift Instrumentation Amplifier	Fixed Gain of 10 or 100
LT1991	Precision, Pin Configurable Gain Difference Amplifier	Gain Range –13 to +14
LTC2054/LTC2055	Micropower Zero-Drift Op Amps	3V/5V/±5V Supply
LTC4151	High Voltage I^2C Current and Voltage Monitor	Wide Operating Range: 7V to 80V
LTC4261	Negative Voltage Hot Swap Controller with ADC and I^2C Monitoring	Floating Topology Allows Very High Voltage Operation
LTC1799	Wide Frequency Range Silicon Oscillator	1kHz to 30MHz
LTC6990	TimerBlox™ Voltage Controlled Oscillator	488Hz to 2MHz
LTM2892	SPI/Digital or I^2C Isolated µModule	3500V_{RMS} Isolation, 6 Channels

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