55V Buck-Boost Multi-Chemistry Battery Charger

FEATURES

- **Wide Voltage Range: 4.5V to 55V Input, Up to 55V Output (60V Absolute Maximums)**
- **Synchronous Buck-Boost DC/DC Controller**
- **Li-Ion and Lead-Acid Charge Algorithms**
- **±0.5% Float Voltage Accuracy**
- **±5% Charge Current Accuracy**
- **Instant-On for Heavily Discharged Batteries**
- **Ideal Diode Controller Provides Low Loss PowerPath When Input Power Is Limited**
- **Input Voltage Regulation for High Impedance Input Supplies and Solar Panel Peak Power Operation**
- Onboard Timer for Protection and Termination
- Bad Battery Detection with Auto-Reset
- NTC Input for Temperature Qualified Charging
- Binary Coded Open-Collector Status Pins
- Low Profile (0.75mm) 38-Pin 5mm × 7mm QFN Package

APPLICATIONS

- Portable Industrial and Medical Equipment
- Solar-Powered Systems
- Military Communications Equipment
- 12V to 24V Embedded Automotive Systems

DESCRIPTION

The LTC®4020 is a high voltage power manager providing PowerPath™ instant-on operation and high efficiency battery charging over a wide voltage range. An onboard buck-boost DC/DC controller operates with battery and/or system voltages above, below, or equal to the input voltage.

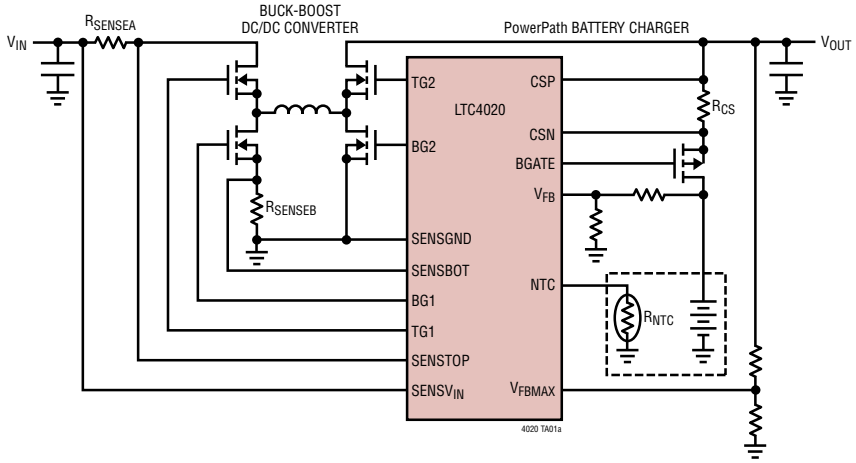
The LTC4020 seamlessly manages power distribution between battery and converter outputs in response to load variations, battery charge requirements and input power supply limitations.

The LTC4020 battery charger can provide a constant-current/constant-voltage charge algorithm (CC/CV), constant-current charging (CC), or charging with an optimized 4-step, 3-stage lead-acid battery charge profile. Maximum converter and battery charge currents are resistor programmable.

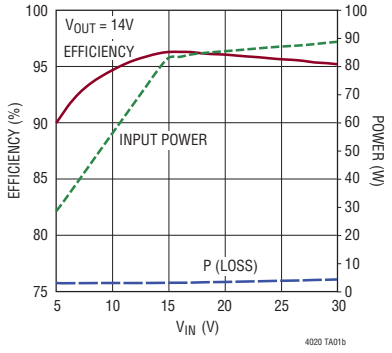
The IC's instant-on operation ensures system load power even with a fully discharged battery. Additional safety features include preconditioning for heavily discharged batteries and an integrated timer for termination and protection.

TYPICAL APPLICATION

Buck-Boost DC/DC Converter Controller with PowerPath Battery Charger Accepts Inputs from 4.5V to 55V and Produces Output Voltages Up to 55V



5V to 30V 6-Cell Lead-Acid Supply/Charger Maximum Power Efficiency vs V_{IN} (Application Circuit on Page 37)

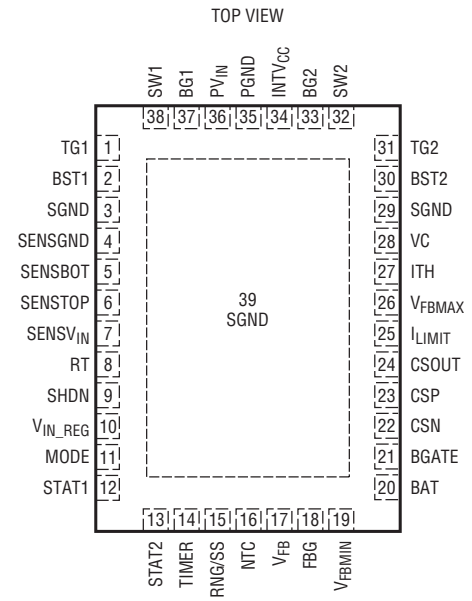


ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV_{IN}, $SENSV_{IN}$ ..... –0.3 to 60V
BST1, BST2..... –0.3 to 66V
SW1, SW2.....–2 to 60V
$SENSV_{IN}$ to PV_{IN} ..... –0.3 to 60V
BST1 to SW1, BST2 to SW2 ..... –0.3 to 6V
$SENSV_{IN}$ to SENSTOP, SENSBOT to SENSGND .....–0.3 to 0.3V
CSP, CSN ..... –0.3 to 60V
CSP to CSN.....–0.3 to 0.3V
STAT1, STAT2, SHDN ..... –0.3 to 60V
V_{FBMAX}, V_{INREG}, V_{FB}, V_{FBMIN}, BAT, FBG..... –0.3 to 60V
MODE..... –0.3 to 6V
Status Pin Currents
STAT1, STAT2 .....5mA
Operating Junction Temperature Range (Note 2).....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UHF PACKAGE
38-PIN PLASTIC QFN (5mm × 7mm)
T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 2°C/W
EXPOSED PAD (PIN 39) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4020EUHF#PBF	LTC4020EUHF#TRPBF	4020	38-Pin (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC4020IUHF#PBF	LTC4020IUHF#TRPBF	4020	38-Pin (5mm × 7mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). PV_{IN} = $SENSV_{IN}$ = CSP = CSN = BAT = 20V, SHDN = 2V, $C_{(TG1, BG1, TG2, BG2)}$ = 1000pF, $V_{RNG/SS}$ = 2V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Buck-Boost Switching Converter							
V_{IN}	Operating Voltage Range	PV_{IN}, $SENSV_{IN}$	●	4.5		55	V
UVLO	V_{IN} Supply UVLO (Rising) V_{IN} Supply UVLO Hysteresis	DC/DC Functions Enabled V_{IN} Falling	●	3.6	4.0 0.4	4.4	V V
	$SENSV_{IN}$ Supply UVLO (Rising) $SENSV_{IN}$ UVLO Hysteresis	$INTV_{CC}$ Enabled $SENSV_{IN}$ Falling			3.4 0.3		V V
	BST Supplies UVLO (Rising) BST Supplies UVLO Hysteresis	BST1 – SW1, BST2 – SW2 SW1, SW2 = 0V	●	3.0	3.3 0.4	3.8	V V
$INTV_{CC}$	Boost Refresh Supply Voltage	I_{LOAD} = 5mA	●	4.85	5.0	5.15	V
	Boost Refresh Supply Dropout	PV_{IN} = 4.5V, I_{INTVCC} = 5mA			4.46		V
	Boost Refresh Supply Short-Circuit Current Limit	V_{INTVCC} = 0V	●	85	150		mA
I_{PVIN}	PV_{IN} Operating Current	Note 3, ITH = 0V	●		1.6	3	mA
	Shutdown Current	V_{SHDN} = 0	●		3	6	µA
$I_{SENSVIN}$	$SENSEV_{IN}$ Operating Current		●		0.25	0.5	mA
	Shutdown Current	V_{SHDN} = 0	●		25	60	µA
$I_{SENSTOP}$	SENSETOP Operating Current				32.5		µA
	Shutdown Current	V_{SHDN} = 0			0.1		µA
V_{FBMAX}	DC/DC Converter Reference	Charging Terminated	●	2.7	2.75	2.8	V
SHDN	IC Enable Threshold (Rising) Threshold Hysteresis		●	1.175	1.225 100	1.275	V mV
	SHDN Pin Bias Current				10		nA
V_{SENS}	DC/DC Converter Inductor Current Limit (Average Value)	$V_{SENSVIN} – V_{SENSTOP}$, $V_{SENSGND} – V_{SENSBOT}$	●	45	50	60	mV
	Reverse Current Inhibit (Average Value)	V_{ITH} Falling (TG2 Disabled) V_{ITH} Rising (TG2 Enabled)	●	0	2 6		mV mV
I_{LIMIT}	Inductor Current Limit Programming	V_{ILIMIT} = 0.5V, $V_{ILIMIT}/V_{SENS(MAX)}$			20		V/V
	I_{LIMIT} Pin Bias Current		●	47.5	50	52.5	µA
RNG/SS	RNG/SS Pin Bias Current		●	47.5	50	52.5	µA
ITH	Error Amp Current Limit	V_{FBMAX} = 0, V_{ITH} = 1.3V			8		µA
	Error Amp Transconductance	V_{FBMAX} = 2.75V; V_{ITH} = 1.3V			95		µS
VC	High Side Current Sense Transconductance	($V_{SENSVIN} – V_{SENSETOP}$) to I_{VC}, V_C = 1.8V			200		µS
	Low Side Current Sense Transconductance	($V_{SENSGND} – V_{SENSEBOT}$) to I_{VC}, V_C = 1.8V			200		µS
DC_{MAX}	Maximum Duty Cycle	BG2: $t_{ON} • f_O$	●	70	80		%
f_O	Switching Frequency	R_{RT} = 100k R_{RT} = 50k R_{RT} = 250k	●	235	250 500 100	265	kHz kHz kHz
t_{ON}	Minimum On Time	BG2	●		150	250	ns
t_{OFF}	Minimum Off Time	TG1	●		300	500	ns
t_{TR}	Gate Drive Transition Time	TG1, BG1, TG2, BG2			5		ns
t_{NOL}	Gate Drive Non-Overlap time	(TG1 – SW1) to BG1, (TG2 – SW2) to BG2			75		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). PV_{IN} = $SENSV_{IN}$ = CSP = CSN = BAT = 20V, SHDN = 2V, $C_{(TG1, BG1, TG2, BG2)}$ = 1000pF, $V_{RNG/SS}$ = 2V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Charger							
V_{BAT}	Charger Output Voltage Range		●			55	V
V_{FB}	Float Reference	CC/CV Charging (MODE = 0V)		2.4875	2.5	2.5125	V
			●	2.475		2.525	V
	Auto Recharge Voltage	% of Float Reference	●	96.5	97.5	98.5	%
	Precondition Threshold (Rising)	% of Float Reference	●	68	70	72	%
	Precondition Hysteresis				85		mV
	Absorption Reference	Lead-Acid Charging (MODE = $INTV_{CC}$)		2.4875	2.5	2.5125	V
		% of Absorption Reference	●	2.475		2.525	V
	Float Reference	% of Absorption Reference	●	91.5	92.5	93.5	%
	Bulk Charge Threshold (Falling)	% of Absorption Reference	●	86	87.5	89	%
	Precondition Threshold (Rising)		●	68	70	72	%
	Precondition Hysteresis				85		mV
	Voltage Reference	CC Charging (MODE = NC)		2.4875	2.5	2.5125	V
			●	2.475		2.525	V
V_{IN_REG}	Input Regulation Reference	% of Float (CC/CV), Safety (CC), or Absorption (LA) Reference	●	98	100	102	%
V_{FBMIN}	Instant-On Reference	% of Float (CC/CV) or Absorption (LA) Reference	●	84	85	86	%
	C/10 Detection Enable (Rising)				2.175		V
	Hysteresis (Falling)				20		mV
	Instant-On Charge Current Reduction Threshold	$V_{CSN} – V_{BAT}$, Note 4			0.45		V
	C/10 Detection Enable	$V_{CSN} – V_{BAT}$ Falling			1.05		V
	C/10 Detection Hysteresis	$V_{CSN} – V_{BAT}$ Rising			150		mV
	Charge Current Reduction Gain	$\Delta V_{CS(MAX)}/\Delta(V_{CSN} – V_{BAT})$, Note 4			–33		mV/V
I_{BATQ}	Battery Bias Currents with PowerPath Switcher Disabled	$I_{CSP} + I_{CSN} + I_{BAT}$	●		9	18	µA
CSN, CSP	Charger Current Sense Pin Operating Bias Currents	$I_{CSP} = I_{CSN}$, Charging Enabled			40		µA
	Charger Current Sense Limit Voltage	$V_{CSP} – V_{CSN}$	●	47.5	50	52.5	mV
	Charger Current Sense Termination Voltage (C/10)	$V_{CSP} – V_{CSN}$, MODE = 0V	●	3	5	7	mV
	Charger Current Sense Precondition Voltage	$V_{CSP} – V_{CSN}$, V_{FB} = 1.5	●	1.5	3	4.5	mV
	Sense Input UVLO	V_{CSP} Rising (Charging Enabled)	●	1.6	1.75	1.9	V
	UVLO Hysteresis	V_{CSP} Falling (Charging Disabled)			100		mV
CSOUT	Offset	$V_{CSP} = V_{CSN}$	●	0.225	0.25	0.290	V
	Gain	$\Delta V_{CSOUT}/\Delta(V_{CSP} – V_{CSN})$	●	19	20	21	V/V
RNG/SS	Current Limit Programming	$V_{RNG/SS}$ = 0.5V, $V_{RNG/SS}/V_{CS(MAX)}$	●	18	20	22	V/V
NTC	NTC Range Limit (High)	V_{NTC} Rising	●	1.30	1.35	1.40	V
	NTC Range Limit (Low)	V_{NTC} Falling	●	0.27	0.3	0.33	V
	NTC Range Hysteresis	% of $V_{NTC(H,L)}$			20		%
I_{NTC}	NTC Pin Bias Current	V_{NTC} = 0.8V	●	47.5	50	52.5	µA
	NTC Disable Current	INTC Pin Current (Falling)			3.5		µA
	NTC Disable Current Hysteresis				2		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). PV_{IN} = $SENSV_{IN}$ = CSP = CSN = BAT = 20V, SHDN = 2V, $C_{(TG1, BG1, TG2, BG2)}$ = 1000pF, $V_{RNG/SS}$ = 2V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BGATE}	Gate Clamp Voltage	$V_{CSN} - V_{BGATE}$	●	7	9.5	12	V
	C/10 Detection Enable (Falling) C/10 Detection Enable Hysteresis	V_{CSN} < 7V			0.425 0.125		V V
BGATE	BGATE Pull-Down Current	Charging Enabled			15		µA
	BGATE Pull-Up Current	Charging Disabled, $V_{CSN} - V_{BGATE}$ = 2V			15		µA
	BGATE Standby Pull-Down Current	V_{SHDN} = 0V			120		µA
	Ideal Diode Pull-Down Current	Charging Disabled, $V_{BAT} - V_{CSN}$ = 0.5V			500		µA
	Ideal Diode Forward Voltage	$V_{BAT} - V_{CSN}$, V_{CSN} Measured Through 100Ω Series Resistor	●	5	14	20	mV
TIMER	Timer High Threshold				1.5		V
	Timer Low Threshold				1.0		V
	C/10 Mode Threshold (Rising)		●	0.4	0.5	0.6	V
	C/10 Mode Hysteresis				225		mV
	Timer Source/Sink Current	V_{TIMER} = 1.25V	●	8.5	10	11.5	µA
$V_{STAT(L)}$	Status Pins Enabled Voltage	I_{STAT1} = 1mA, I_{STAT2} = 1mA I_{STAT1} = 5mA, I_{STAT2} = 5mA	● ●		0.15 0.75	0.4 2.5	V V
I_{VFBMIN}	Instant-On Feedback Bias Current				10		nA
I_{VFB}	Feedback Pin Bias Current				10		nA
I_{VIN_REG}	Input Regulation Bias Current				10		nA
I_{FBG}	Pin Current (Disabled)	V_{SHDN} = 0V, V_{FBG} = 55V			10		nA
R_{NTC}	NTC Minimum Disable Resistance		●	250	400		kΩ
R_{FBG}	FBG Resistance to SGND	I_{FBG} = 1mA	●		20	50	Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4020 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4020E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LTC4020I is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) according to the formula $T_J = T_A + (P_D \bullet \theta_{JA})$. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors. This IC includes overtemperature protection that is intended to protect the device during momentary overload. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

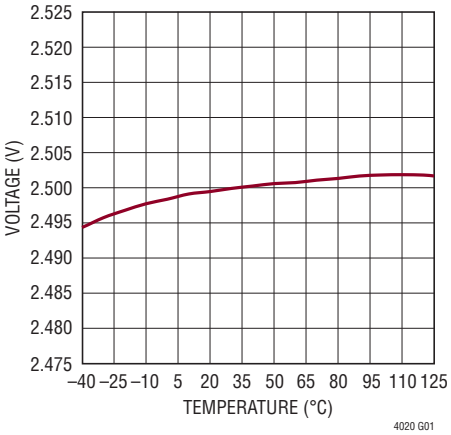
Note 3: ICC does not include switching currents. $V_{BST1} = V_{BST2} = V_{INTVCC}$ and $V_{SW1} = V_{SW2}$ = 0V for testing.

Note 4: See Typical Performance Characteristics.

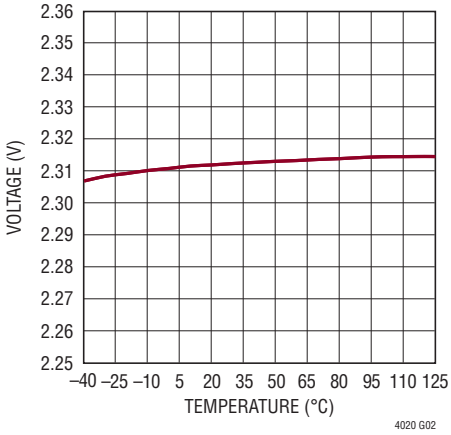
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

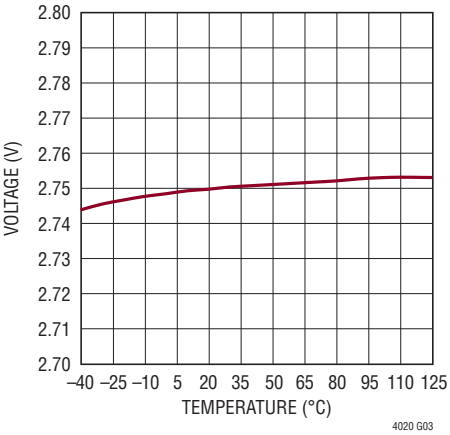
$V_{FLOAT(CC/CV)}$ or, $V_{ABSORB(LEAD-ACID)}$ Reference vs Temperature



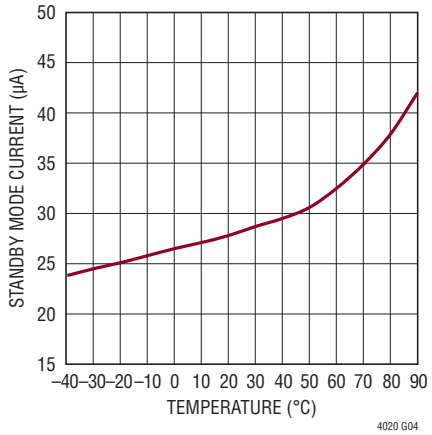
$V_{FLOAT(LEAD-ACID)}$ Reference vs Temperature



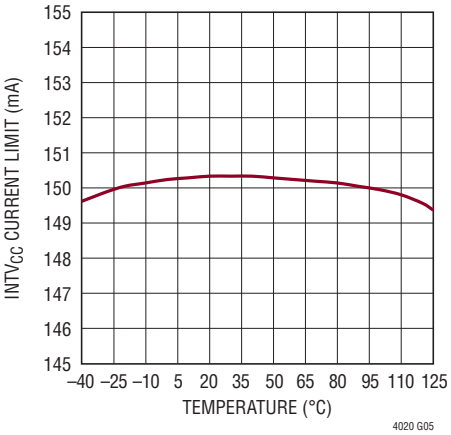
V_{FBMAX} Reference vs Temperature



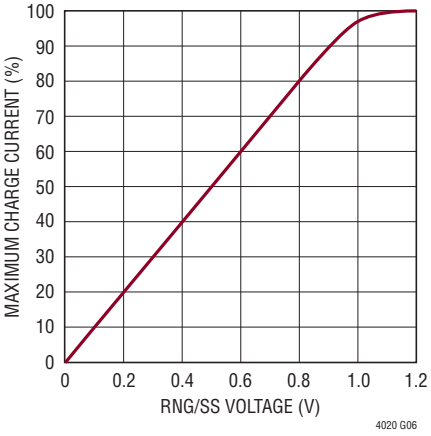
Shutdown Current vs Temperature (I_{PVIN} + $I_{SENSVIN}$ + $I_{SENSTOP}$)



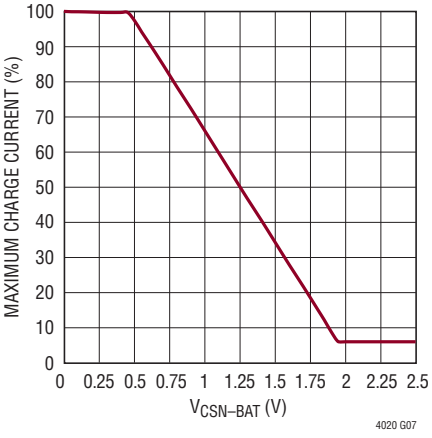
$INTV_{CC}$ Short-Circuit Current Limit vs Temperature



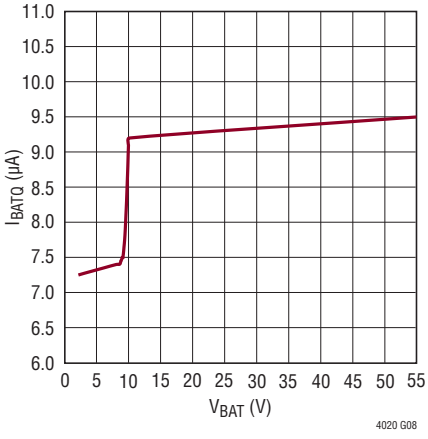
Maximum Charge Current (Percent of Programmed I_{CSMAX}) vs RNG/SS Voltage



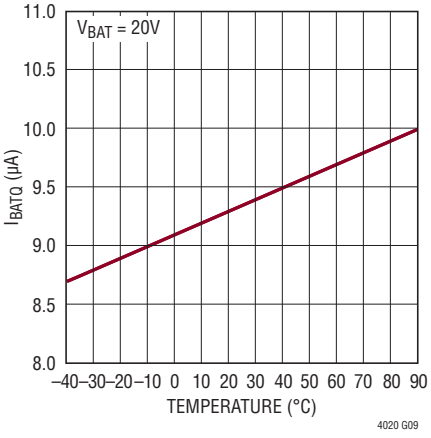
Instant-On: Maximum Charge Current (Percent of I_{CSMAX}) vs $V_{CSN–BAT}$



I_{BATQ} (I_{BAT} + I_{CSN} + I_{CSP}) vs V_{BAT} PowerPath Switcher Disabled



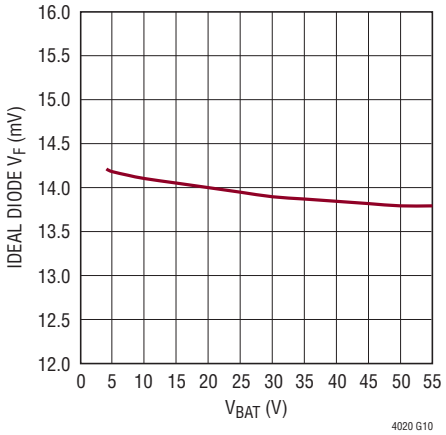
I_{BATQ} (I_{BAT} + I_{CSN} + I_{CSP}) vs Temperature PowerPath Switcher Disabled



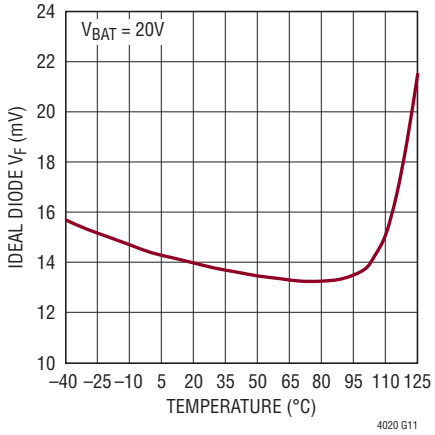
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

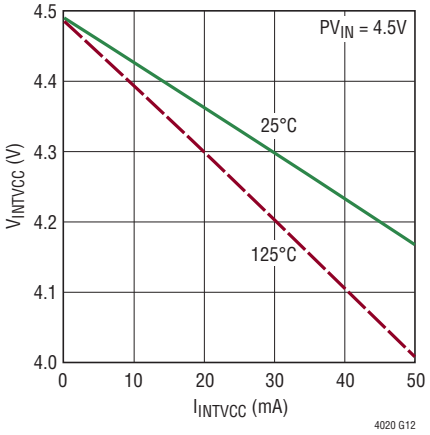
Ideal Diode V_F vs Battery Voltage



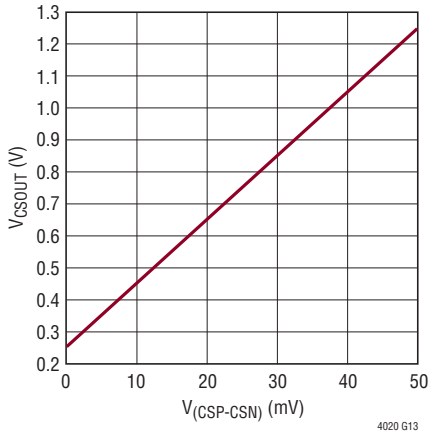
Ideal Diode V_F vs Temperature



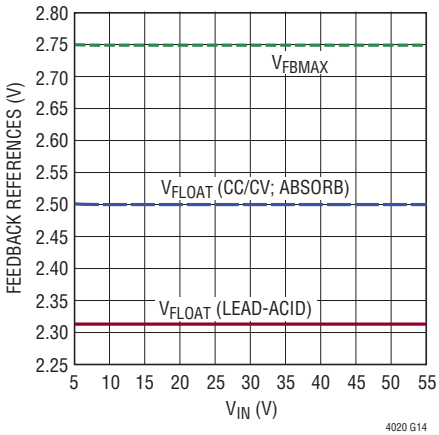
BST Refresh Regulator Dropout $INTV_{CC}$ vs I_{INTVCC}



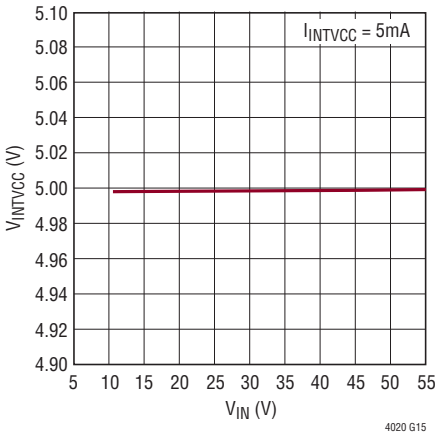
CSOUT vs CSP–CSN



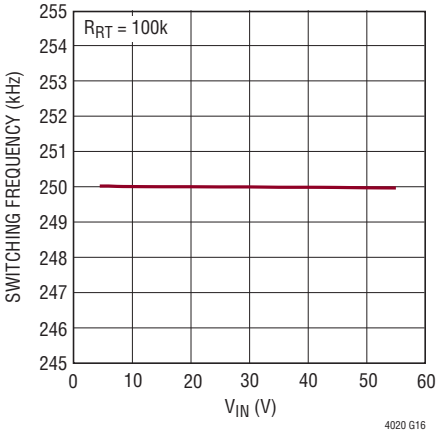
Feedback References vs Input Voltage



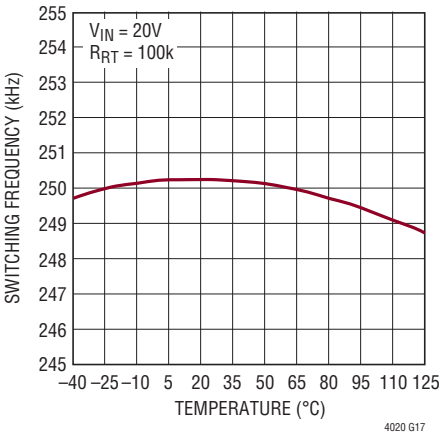
$INTV_{CC}$ vs V_{IN}



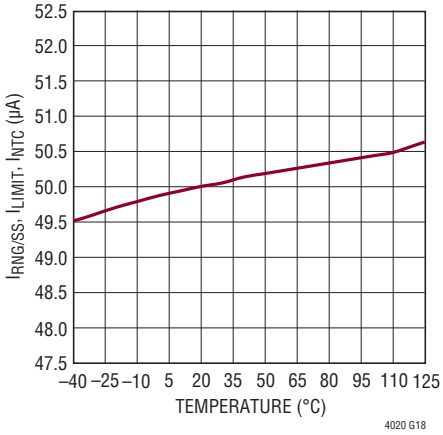
Switching Frequency vs Input Voltage



Switching Frequency vs Temperature



$I_{RNG/SS}$, I_{LIMIT}, I_{NTC} vs Temperature



PIN FUNCTIONS

TG1 (Pin 1): V_{IN} side (step-down) primary switch FET gate driver output.

BST1 (Pin 2): Boosted supply rail for V_{IN} side (step-down) switch FETs. Connect 1µF capacitor from this pin to SW1. Connect 1A Schottky diode cathode to this pin, anode to $INTV_{CC}$ pin.

SGND (Pins 3, 29, Exposed Pad 39): Signal Ground Reference. Connect to the output decoupling capacitor negative terminal and battery negative terminal. The exposed pad (39) must be soldered to PCB ground (SGND) for electrical connection and rated thermal performance.

SENSGND (Pin 4): Kelvin connection for PGND used for SENSBOT current sense reference.

SENSBOT (Pin 5): Ground Referred Current Sense Amplifier Input. Inductor current is monitored via a PGND referenced current sense resistor (R_{SENSEB}), typically in series with the source of the V_{IN} side synchronous switch FET. Kelvin connect this pin to the associated sense resistor. Inductor current is limited to a maximum average value (I_{LMAX}), and corresponds to 50mV across this sense resistor during normal operation.

$$R_{SENSEB} = 0.05/I_{LMAX}$$

Set $R_{SENSEB} = R_{SENSEA}$, as described in SENSTOP. A filter capacitor (C_{SENSB}) is typically connected from SENSBOT to SENSGND for noise reduction.

$$C_{SENSB} \sim 1ns/R_{SENSEB}$$

See Applications Information section.

SENSTOP (Pin 6): V_{IN} Referred Current Sense Amplifier Input. Inductor current is monitored via a V_{IN} referenced current sense resistor (R_{SENSEA}), typically in series with the drain of the V_{IN} side primary switch FET. Kelvin connect this pin to the associated sense resistor. Inductor current is limited to a maximum average value (I_{LMAX}), and corresponds to 50mV across this sense resistor during normal operation.

$$R_{SENSEA} = 0.05/I_{LMAX}$$

Set $R_{SENSEA} = R_{SENSEB}$, as described in SENSBOT.

$SENSV_{IN}$ (Pin 7): Kelvin connection for input supply (V_{IN}) used for SENSTOP current sense reference. Input power supply pin for most internal low current functions. Typical pin bias current is 0.25mA.

RT (Pin 8): System Oscillator Frequency Control Pin. Connect resistor (R_{RT}) from this pin to ground. Resistor value can range from 50k (500kHz) to 500k (50kHz). R_{RT} = 100k yields 250kHz operating frequency. See Applications Information.

SHDN (Pin 9): Precision Threshold Shutdown Pin. Enable threshold is 1.225V (rising), with 100mV of input hysteresis. When in shutdown, all charging functions are disabled and input supply current is reduced to 27.5µA. Typical SHDN pin input bias current is 10nA.

V_{IN_REG} (Pin 10): Input Voltage Regulation Reference. Battery charge current is reduced when the voltage on this pin falls below 2.5V. Connecting a resistor divider from V_{IN} to this pin enables programming of minimum operational V_{IN} voltage for the battery charging function. This is used to program the peak power voltage for a solar panel, or to help maintain a minimum voltage on a poorly regulated input supply. This pin should not be used to program minimum operational V_{IN} voltage with low impedance supplies. Should the input supply begin to collapse, the LTC4020 reduces the DC/DC converter input power such that programmed minimum V_{IN} operational voltage is maintained. If the voltage regulation feature is not used, connect the V_{IN_REG} pin to V_{IN} or $INTV_{CC}$. Typical V_{IN_REG} pin input bias current is 10nA. See Applications Information.

MODE (Pin 11): Charger Mode Control Pin. Short this pin to ground to enable a constant-current/constant-voltage (CC/CV) charging algorithm. Connect this pin to pin $INTV_{CC}$ to enable a 4-step, 3-stage lead-acid charging algorithm. Float this pin to force a constant-current (CC) charging function. See Applications Information section.

STAT1 (Pin 12): Open-collector status output, typically pulled up through a resistor to a supply voltage. This status pin can be pulled up to voltages as high as 55V when the pin is disabled, and can sink currents up to 1mA when logic low (<0.4V). Pull down currents as high

PIN FUNCTIONS

as 5mA (absolute maximum) are supported for higher current applications, such as lighting LEDs.

If the LTC4020 is configured for a CC/CV charging algorithm, the STAT1 pin is pulled low while battery charge currents exceed 10% of the programmed maximum (C/10). The STAT1 pin is also pulled low during NTC faults. The STAT1 pin becomes high impedance when a charge cycle is terminated or when charge current is below the C/10 threshold.

If the LTC4020 is configured for a CC charging algorithm, the STAT1 pin is pulled low during the entire charging cycle. The STAT1 pin becomes high impedance when the charge cycle is terminated.

If the LTC4020 is configured for a lead-acid charging algorithm, the STAT1 pin is used as a charge cycle stage indicator pin, and pulled low during the bulk and absorption charging stages. The pin is high impedance during the float charging period and during NTC or bad battery faults.

See Applications Information section.

STAT2 (Pin 13): Open-collector status output, typically pulled up through a resistor to a supply voltage. This status pin can be pulled up to voltages as high as 55V when disabled, and can sink currents up to 1mA when enabled (<0.4V). Pull down currents as high as 5mA (absolute maximum) are supported for higher current applications, such as lighting LEDs.

If the LTC4020 is configured for a CC/CV charging algorithms, the STAT2 pin is pulled low during NTC faults or after a bad battery fault occurs.

If the LTC4020 is configured for a CC charging algorithms, the STAT2 pin is pulled low during NTC faults.

If the LTC4020 is configured for a lead-acid charging algorithm, the STAT2 pin is used as a charge cycle stage indicator pin, and pulled low during the bulk and float charging stages. The pin is high impedance during the absorption charging stage and during NTC or bad battery faults.

See Applications Information section.

TIMER (Pin 14): End-Of-Cycle Timer Programming Pin. If a timer based charging algorithm is desired, connect a capacitor (C_{TIMER}) from this pin to ground. If no timer functions are desired, connect this pin to ground.

End-of-cycle time (in hours) is programmed with the value of C_{TIMER} following the equation:

$$T_{EOC} = C_{TIMER} \bullet 1.46 \bullet 10^7$$

During CC/CV or lead-acid charging algorithms, a bad battery fault is generated if the battery voltage does not reach the precondition threshold voltage within 1/8 of T_{EOC}, or:

$$T_{PRE} = C_{TIMER} \bullet 1.82 \bullet 10^6$$

A 0.2µF capacitor is typically used for CC/CV charging, which generates a 2.9 hour timer T_{EOC}, and a precondition limit time of 22 minutes. A 0.47µF capacitor is typically used for a lead-acid charger, which generates a 6.8 hour absorption stage safety timeout.

RNG/SS (Pin 15): Battery Charge Current Programming Pin. This pin allows dynamic adjustment of maximum charge current, and can be used to employ a soft-start function.

Setting the voltage on the RNG/SS pin reduces maximum charge current from the value programmed. The maximum charge current is reduced to the fraction of programmed current (as per the sense resistor, RCS) corresponding to the voltage set on the pin (in volts). This pin has an effective range from 0 to 1V.

For example, with 0.5V RNG/SS on the pin, the maximum charge current will be reduced to 50% of the programmed value set by the sense resistor values.

50µA is sourced from the RNG/SS pin, so maximum charge current can be programmed by connecting a single resistor ($R_{RNG/SS}$) from RNG/SS to ground, such that the voltage dropped across the resistor is equivalent to the desired pin voltage:

$$V_{RNG/SS} = 50\mu A \bullet R_{RNG/SS}$$

Soft-start functionality can be implemented by connecting a capacitor ($C_{RNG/SS}$) from RNG/SS to ground, such that the time required to charge the capacitor is the desired

PIN FUNCTIONS

soft-start interval (T_{SS1}). The voltage that corresponds to full programmed battery charge current on the RNG/SS pin is 1V, so the relation for this capacitor reduces to:

$C_{RNG/SS} = 50\mu A \bullet T_{SS1}$

The RNG/SS pin is pulled low during periods when charging is disabled, including NTC faults, bad battery faults, and normal charge cycle termination. This allows for a graceful start after faults and when initiating new charge cycles, should soft-start functionality be implemented.

Both a soft-start capacitor and a programming resistor can be implemented in parallel.

RNG/SS voltage can also be manipulated using an active device, such as employing a pull-down transistor to disable charge current or to dynamically servo maximum charging current. Because this pin is internally pulled to ground during fault conditions, active devices with low-impedance pull up capability cannot be used.

See Applications Information section.

NTC (Pin 16): Battery Temperature Monitor Pin. Connect a 10k, β = 3380 NTC thermistor from this pin to ground.

The NTC pin is the input to the negative temperature coefficient temperature monitoring circuit. This pin sources 50µA, and monitors the voltage created across the 10k thermistor. When the voltage on this pin is above 1.35V (0°C) or below 0.3V (40°C), charging is disabled and an NTC fault is signaled at the STAT1 and STAT2 status pins. If the internal timer is being used, the timer is paused, suspending the charging cycle until the NTC fault condition is relieved. There is approximately 5°C of temperature hysteresis associated with each of the temperature thresholds. The NTC function remains enabled while thermistor resistance to ground is less than 250k. If this function is not desired, leave the NTC pin unconnected or connect a 10k resistor from the NTC pin to ground. The NTC pin contains an internal clamp that prevents excursions above 2V, so the pin must not be pulled high with a low impedance source. A low impedance element can be used to pull the pin to ground.

V_{FB} (Pin 17): Battery Voltage Feedback Pin. Battery voltages are programmed through a feedback resistor divider placed from the BAT pin to FBG.

During CC/CV charging, the battery voltage references are:

Float Voltage (V_{FLOAT}) = 2.5V

Trickle Charge Voltage (V_{TRK}) = 1.75V

Auto-Restart Voltage ($V_{RESTART}$) = 2.4375

During lead-acid charging, the battery voltage references are:

Absorption Voltage (V_{ABSOR}) = 2.5V

Float Charge Voltage (V_{FLT}) = 2.3125V

Trickle Charge Voltage (V_{TRK}) = 1.75V

Bulk Recharge Voltage (V_{BULK}) = 2.1875V

With R_{FB1} connected from BAT to V_{FB} and R_{FB2} connected from V_{FB} to FBG, the ratio of (R_{FB1}/R_{FB2}) for the desired programmed battery float voltage (CC/CV charging) or absorption voltage (lead-acid charging) follows the relation:

$R_{FB1}/R_{FB2} = (V_{FLOAT/ABSORB})/2.5 – 1$

FBG (Pin 18): Voltage Feedback Divider Return. This pin contains a low impedance path to signal ground, used as the ground reference for voltage monitoring feedback resistor dividers. When V_{IN} is not present or the LTC4020 is in shutdown, this pin becomes high impedance, eliminating current drain from the battery associated with the feedback resistor dividers.

V_{FBMIN} (Pin 19): Minimum voltage feedback pin for instant-on operation. Minimum DC/DC converter output voltage (V_{OUTMIN}) is programmed using this pin for instant-on functionality. V_{OUTMIN} is programmed through a feedback resistor divider placed from the CSP pin to FBG.

If the battery voltage is below the voltage level programmed using this pin, the LTC4020 controls the external PowerPath FET as a linear pass element, allowing the DC/DC converter output to achieve the minimum

PIN FUNCTIONS

programmed voltage. Maximum battery charge current is reduced as the voltage across the PowerPath FET increases to control power dissipation.

The internal V_{FBMIN} voltage reference is 2.125V. With a resistor (R_{MIN1}) connected from CSP to V_{FBMIN}, and a resistor (R_{MIN2}) connected from V_{FBMIN} to FBG, the ratio of these resistors for the desired minimum converter output voltage follows the relation:

$$R_{MIN1}/R_{MIN2} = (V_{OUT(MIN)}/2.125) – 1$$

Using the same resistor values for battery voltage programming, or $R_{FB1} = R_{MIN1}$ and $R_{FB2} = R_{MIN2}$, yields an instant-on voltage that is 85% of V_{FLOAT} (CC/CV charging) or V_{ABSORB} (lead-acid charging):

$$V_{OUT(MIN)} = 0.85 • V_{FLOAT/ABSORB}$$

BAT (Pin 20): Battery Voltage Monitor Pin. This pin serves as the positive reference for the LTC4020 ideal diode function.

If a system load occurs that is large enough to collapse the DC/DC converter output while charging is terminated or disabled, and the battery is disconnected (PowerPath FET is high impedance), the ideal diode function engages the PowerPath. This function powers the system load from the battery, and modulates the PowerPath FET gate such that the system output voltage is maintained with 14mV across the PowerPath FET, provided the voltage drop due to $R_{DS(ON)}$ < 14mV. This allows large loads to be accommodated without excessive power dissipation in the body diode of the PowerPath FET.

BGATE (Pin 21): PowerPath FET Gate Driver Output.

This pin is controls the multiple functions of the PowerPath FET.

This pin is pulled low during a normal charging cycle, minimizing the FET series impedance between the DC/DC converter output and the battery.

The BGATE pin is also forced low when the DC/DC converter is disabled, maintaining a low impedance connection to power the system from the battery.

When BGATE is pulled low, CSP BGATE is limited internally to 9.5V, so if CSP > 9.5V, BGATE is maintained by an internal clamp at CSP – BGATE = 9.5V. The BGATE pin must be near ground or at the clamp voltage for C/10 detection to occur.

If the battery voltage is lower than the instant-on threshold (see V_{FBMIN}), BGATE servos the PowerPath FET impedance such that a voltage drop between the CSN pin and the BAT pin is created while battery charging continues. If the $V_{CSN} – V_{BAT}$ voltage exceeds 0.4V, maximum charge current is reduced to decrease power dissipation in the PowerPath FET.

When the DC/DC converter is enabled, but the battery charge cycle has terminated, BGATE is pulled high to disconnect the battery from the converter output. The battery is also disconnected in the same manner during NTC faults. The ideal diode function is active during these periods, however, so if a system load occurs that is larger than what the DC/DC converter can accommodate, the battery can supply the required current, and the BGATE pin will be servo controlled to force a voltage drop of only 14mV across the PowerPath FET. The ideal diode function is disabled during bad battery faults.

If a PowerPath FET is not being used, such as with a lead-acid charging application, connect a 0.1nF capacitor from BGATE to CSN.

CSN (Pin 22): Battery Charger Current Sense Negative Input. Connect this pin to the negative terminal of the battery charge current sense resistor (RCS) through a 100Ω resistor. Connect a filter capacitor between this pin and the CSP pin for ripple reduction. See Applications Information section.

The value of the sense resistor is related to the maximum battery charge current (I_{CSMAX}):

$$R_{CS} = 0.05/I_{CSMAX}$$

This pin also serves as the negative reference for the LTC4020 ideal diode function (see BAT).

PIN FUNCTIONS

CSP (Pin 23): Battery Charger Current Sense Positive Input. Connect this pin to the positive terminal of the battery charge current sense resistor (R_{CS}) through a 100Ω resistor. Connect a filter capacitor between this pin and the CSN pin for ripple reduction. See Applications Information section.

The value of the sense resistor is related to the maximum battery charge current (I_{CSMAX}) such that:

$$R_{CS} = 0.05/I_{CSMAX}$$

CSOUT (Pin 24): Current Sense Amplifier Output and Charge Current Monitor. Connect 100pF capacitor to ground.

Pin output impedance is 100k, so any loading for monitors must be high impedance. The sense output voltage follows the relation:

$$V_{CSOUT} = 0.25 + 20 \bullet (V_{CSP} – V_{CSN})$$

CSOUT is only active while battery charger functions are operating. CSOUT pin voltage is pulled to 0V after charge cycle termination or during fault conditions.

I_{LIMIT} (Pin 25): Switched Inductor Maximum Current Programming Pin. This pin allows dynamic adjustment of DC/DC converter maximum average inductor current, and can be used to employ a soft-start function.

Setting the voltage on the I_{LIMIT} pin reduces maximum average inductor current from the value programmed. The inductor current limit is reduced to the fraction of programmed current (as per the sense resistors) corresponding to the voltage set on the pin (in volts). This pin has an effective range from 0 to 1V.

For example, with 0.5V on the pin, the maximum inductor current will be reduced to 50% of the programmed value set by the sense resistor values.

50µA is sourced from this pin, so maximum inductor current can be programmed by connecting a single resistor (R_{ILIMIT}) from I_{LIMIT} to ground, such that the voltage dropped across the resistor is equivalent to the desired pin voltage:

$$V_{ILIMIT} = 50\mu A \bullet R_{ILIMIT}$$

Soft-start functionality can be implemented by connecting a capacitor (C_{ILIMIT}) from I_{LIMIT} to ground, such that the time required to charge the capacitor is the desired soft-start interval (T_{SS2}). The voltage that corresponds to full inductor current on the I_{LIMIT} pin is 1V, so the relation for this capacitor reduces to:

$$C_{ILIMIT} = 50\mu A \bullet T_{SS2}$$

I_{LIMIT} voltage can also be manipulated using an active device, such as employing a pull-down transistor to disable DC/DC converter current or to dynamically servo maximum current. Because this pin is internally pulled to ground during portions of the converter power-up cycle, active devices with low impedance pull-up capability cannot be used.

V_{FBMAX} (Pin 26): DC/DC Converter Output Feedback Pin. Maximum DC/DC converter output voltage (V_{OUTMAX}) is programmed using this pin. When a battery charge cycle is terminated or disabled, and the battery is disconnected (PowerPath FET is high impedance), the converter output will servo to this maximum voltage.

The internal V_{FBMAX} voltage reference is 2.75V. With a resistor (R_{MAX1}) connected from CSP to V_{FBMAX} and a resistor (R_{MAX2}) connected from V_{FBMAX} to FBG, the ratio of R_{MAX1}/R_{MAX2} for the desired maximum DC/DC converter output voltage follows the relation:

$$R_{MAX1}/R_{MAX2} = (V_{OUTMAX}/2.75) – 1$$

Using the same resistor values for battery voltage programming, or $R_{FB1} = R_{MAX1}$ and $R_{FB2} = R_{MAX2}$, yields a voltage while not charging that is 110% of V_{FLOAT} (CC/CV charging) or V_{ABSORB} (lead-acid charging):

$$V_{OUTMAX} = 1.1 \bullet V_{FLOAT/ABSORB}$$

If R_{MAX1}/R_{MAX2} are chosen for a not-charging power-stage output voltage (V_{OUTMAX}) of less than 110% of the full-charge voltage, be sure to choose R_{MAX1}/R_{MAX2} to allow adequate headroom between V_{OUTMAX} and the battery full-charge voltage to cover voltage drops in the battery-charge current-sense resistor (R_{CS}) and the PowerPath FET. Typically, at least 100mV to 200mV of headroom is required.

PIN FUNCTIONS

ITH (Pin 27): DC/DC Converter Voltage Loop Compensation Pin. See Applications Information section for compensation component selection details.

VC (Pin 28): DC/DC Converter Current Loop Compensation Pin. See Applications Information section for compensation component selection details.

BST2 (Pin 30): Boosted supply rail for V_{OUT} side (step-up) switch FETs. Connect a 1µF capacitor from this pin to SW2. Connect a 1A Schottky diode cathode to this pin, anode to $INTV_{CC}$ pin.

TG2 (Pin 31): V_{OUT} side (step-up) synchronous switch FET gate driver output.

SW2 (Pin 32): Switched node for step-up switches. Connect the switched inductor to this pin. Connect the primary switch FET drain and synchronous switch FET source to this pin.

BG2 (Pin 33): V_{OUT} side (step-up) primary switch FET gate driver output.

$INTV_{CC}$ (Pin 34): Boosted Driver Refresh Supply. This supply is regulated to 5V and is current limited to a typical value of 150mA. Connect a 2.2µF ceramic capacitor from this pin to PGND. Boosted supply refresh diode anodes are connected to this pin. Using this pin to power external 5V circuitry is not recommended.

Note that internal V_{CC} regulator has a minimum-specified current-limit value of 85mA. Since the internal regulator supplies gate drive to all four power-stage FETs, 85mA represents a maximum practical limit for total gate-drive current. See Applications Information section.

PGND (Pin 35): Switch high current return path for step-up primary and step-down synchronous switches.

PV_{IN} (Pin 36): High Current Input Supply Pin. Connect 10µF decoupling capacitor from this pin to PGND. The PV_{IN} pin provides input supply current for the $INTV_{CC}$ internal 5V linear regulator.

BG1 (Pin 37): V_{IN} side (step-down) synchronous switch FET gate driver output.

SW1 (Pin 38): Switched node for step-down switches. Connect the switched inductor to this pin. Connect the primary switch FET source and synchronous switch FET drain to this pin.

BLOCK DIAGRAM

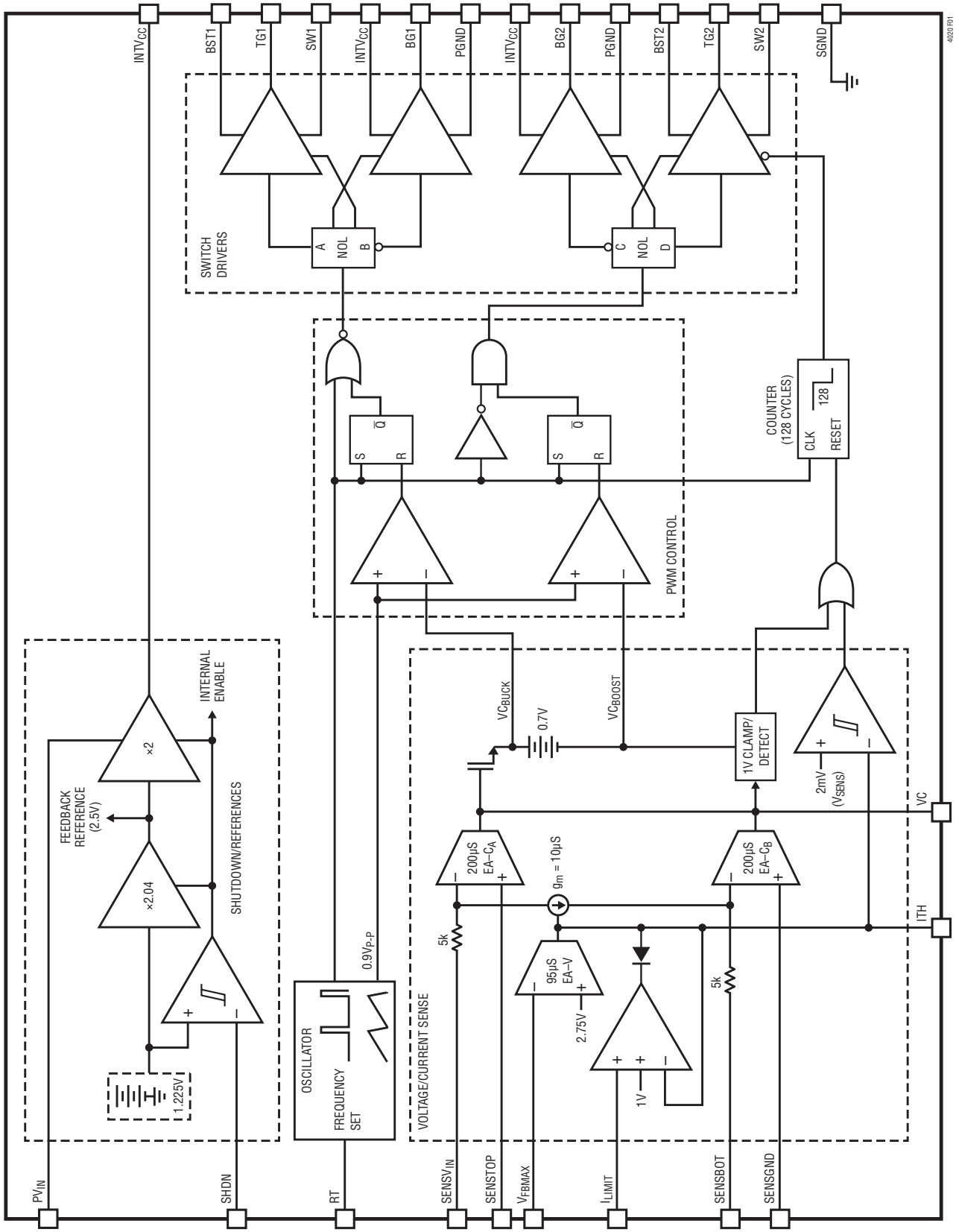


Figure 1. DC/DC Converter Block Diagram

BLOCK DIAGRAM

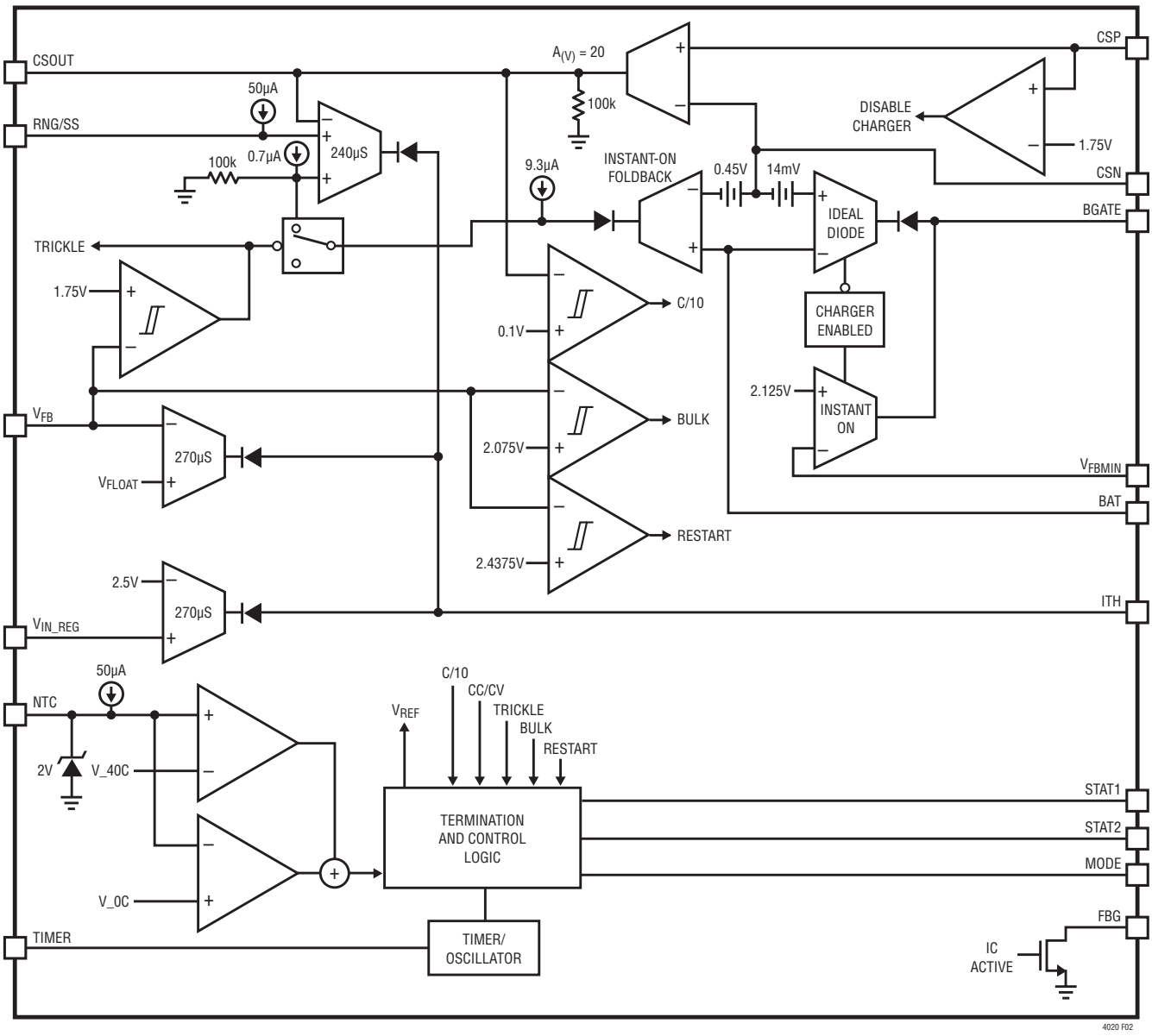


Figure 2. Battery Charger Block Diagram

OPERATION

Functional Overview

The LTC4020 is an advanced high voltage power manager and multi-chemistry battery charger designed to efficiently transfer power from a variety of sources to a system power supply rail and a battery.

The LTC4020 contains a step-up/step-down DC/DC controller that allows operation with battery and system voltages that are above, below, or equal to the input voltage (V_{IN}). A precision threshold shutdown feature allows incorporation of input voltage UVLO functionality using a simple resistor divider. When in low current shutdown mode, the IC input supply bias is reduced to only 27.5µA.

The LTC4020 charger is programmable to produce optimized charging profiles for a variety of battery chemistries. The LTC4020 can provide a constant-current/constant-voltage charge characteristic with either C/10 or timed termination for use with lithium based battery systems, a constant-current characteristic with timed termination, or an optimized 4-step, 3-stage lead-acid charge profile.

Maximum battery charge current is programmable using a sense resistor, and a charge current range adjust pin allows dynamic adjustment of maximum charge current. A switcher core current limit adjust pin also allows dynamic limiting of power available to the system by virtue of limiting maximum current in the DC/DC converter inductor.

The LTC4020 preconditions heavily discharged batteries by reducing charge current to one-fifteenth of the programmed maximum. Once the battery voltage climbs above an internally set threshold, the IC automatically increases maximum charging current to the full programmed value. A bad battery detection function signals a fault and suspends charging should a battery not respond to preconditioning.

Battery temperature is monitored using a thermistor measurement system. This feature monitors battery temperature during the charging cycle, suspending the charge cycle and signaling a fault condition if the battery temperature moves outside a safe charging range of 0°C to 40°C. The charge cycle automatically resumes when the temperature returns to that safe charging range.

Instant-on PowerPath architecture ensures that an application is powered immediately after an external voltage is applied, even with a completely dead battery, by prioritizing power to the application. Since the controller output (V_{OUT}) and the battery (BAT) are sometimes decoupled, the LTC4020 includes an ideal diode controller, which guarantees that ample power is always available to V_{OUT} if there is insufficient power available from the DC/DC converter. Should there be no input power available (V_{IN}), the LTC4020 makes a low impedance connection from the battery to V_{OUT} though the PowerPath FET. Battery life is maximized during periods of input supply disconnect by reducing the LTC4020 battery standby current to less than 10µA.

The LTC4020 contains two digital open-collector outputs that provide charger status and signal fault conditions. These binary coded pins signal battery charging, standby or shutdown modes, battery temperature faults, and bad battery faults.

DC/DC Converter Operation (See Figure 1, Block Diagram)

The LTC4020 uses a proprietary average current mode DC/DC converter architecture.

As shown in Figure 3, when V_{IN} is higher than V_{OUT} during step-down (buck) operation, switches A (driven by pin TG1) and B (driven by pin BG1) perform the PWM required for accommodating power conversion. Ideally, switch D (driven by pin TG2) would conduct continuously and switch C (driven by pin BG2) would stay off, making PWM switching action much like that in a synchronous buck topology. Switch D uses a bootstrapped driver, however, so switch C conducts for a minimum on time of 150ns each cycle to refresh the driver and switch D is disabled to accommodate this refresh time. A 75ns non-overlap period separates the conduction of the two switches preventing shoot-through currents.

When V_{IN} is lower than V_{OUT} during step-up (boost) operation, switches C and D perform the PWM required for accommodating power conversion. Ideally, switch A would conduct continuously and switch B would stay off, making PWM switching action much like that in a

OPERATION

synchronous boost topology. Since switch A also uses a bootstrapped drive, however, the B switch conducts for 100ns during this refresh period. A 75ns non-overlap period, separates the conduction of the two switches, preventing shoot-through currents.

If V_{IN} is close to V_{OUT}, the controller operates in 4-switch (buck-boost) mode, where both switch pairs PWM simultaneously to accommodate conversion requirements.

The LTC4020 senses the DC/DC converter output voltage using a resistor divider feedback network that drives the V_{FBMAX} pin. The difference between the voltage on the V_{FBMAX} pin and an internal 2.75V reference is converted into an error current by the voltage loop transconductance amplifier (EA–V). This error current is integrated by a compensation network to produce a voltage on pin ITH. The ITH compensation network is designed to optimize the response of the converter to changes in load current while the converter is in regulation. At regulation, the ITH pin will servo to a value that corresponds to the average inductor current of the DC/DC converter.

Inductor current is monitored through two like value sense resistors, placed in series with each of the V_{IN} side converter switches, A and B. The sum of these sensed currents yields a reasonably accurate continuous representation of inductor current.

The voltage produced on the ITH pin is translated into an offset at the input of the two current sense amplifiers. The difference between this offset voltage and the sum of the voltages is sensed on the SENSTOP and SENSBOT pins, then is converted to error currents by the current sense transconductance amplifiers (EA–C_A and EA–C_B). These error currents are summed and integrated by a compensation network to produce a voltage on the pin VC. This compensation network is designed to optimize the response of the converter duty cycle to required changes in inductor current.

The VC pin voltage is compared to an internally generated ramp, and the output of this comparison controls the duty cycle of the charger's switches.

Figure 3 shows a simplified diagram of the four power switches and their connections to the IC, inductor, V_{IN}, V_{OUT}, ground, and current sense elements.

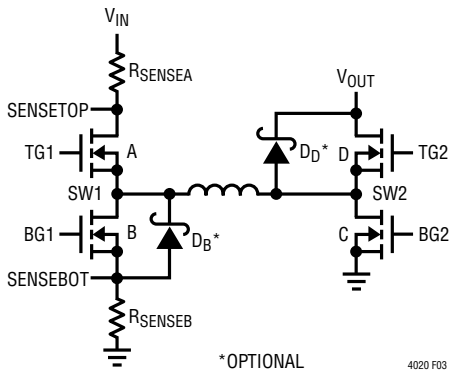


Figure 3. Converter Switch Diagram

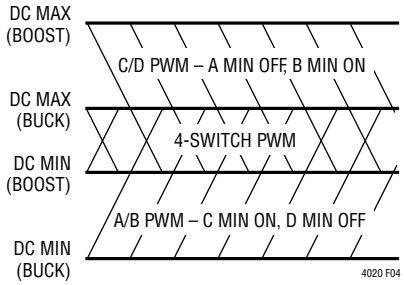


Figure 4. Operating Regions vs Duty Cycle (DC)

Reverse current protection is accomplished through disabling the V_{OUT} side synchronous switch (D) during initial power-up, when the converter is in step-up duty cycle limit, and when ITH falls to a voltage that corresponds to <1/25 of programmed I_{LMAX}. Once these conditions subside, the D switch remains disabled for an additional 128-clock cycles.

Battery Charger Operation (See Figure 2, Block Diagram)

During the majority of a normal battery charge cycle, the LTC4020 makes a low impedance connection between the battery and the DC/DC converter output through the PowerPath FET, as in Figure 5. This PFET is controlled by the LTC4020 through modulation of the BGATE pin, which is connected to the FET gate. When charging is disabled, the FET is disabled, disconnecting the battery from the converter output by pulling the gate of the PowerPath FET high via the BGATE pin. The converter output is regulated by V_{FBMAX} while the FET is disabled. When normal charger

OPERATION

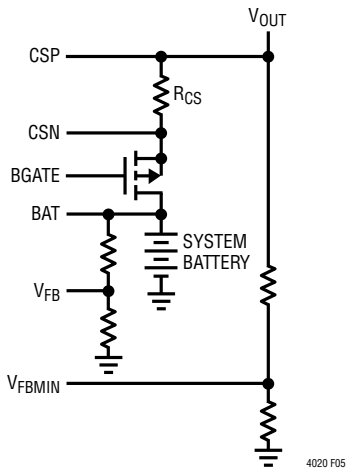


Figure 5. Battery Charger PowerPath Diagram

operation resumes, the gate is pulled low. As the BGATE pin is a slow-moving node, C/10 detection is disabled until the BGATE pin approaches its normal operating voltage, which prevents premature C/10 detection during reconnection of the battery. The slow movement of BGATE can also cause the converter output to regulate to V_{FBMAX} for a short time during start-up until the FET is enabled. This FET is also linearly controlled during low battery conditions to enable the instant-on function, where the converter output can be separated from a heavily discharged battery to power the rest of the system before the battery voltage responds to charging. C/10 detection is also disabled when the charger is operating in instant-on mode. This FET is also automatically configured as a 14mV ideal diode, which provides a low loss path from the battery to the output when system loads require power from the battery while the battery is disconnected from the converter output.

The battery charger takes control of the DC/DC converter operation by modulating the ITH pin voltage in response to sensed battery charge current, battery voltage, and input voltage. The converter thus provides exactly the amount of power required to satisfy both the system load and battery charger requirements.

Battery charge current is monitored via an external sense resistor connected to the pins CSP and CSN. The voltage across this resistor is amplified internally by a factor of 20, which is output onto pin CSOUT. This output voltage rides on top of a constant 250mV offset. The CSOUT pin voltage drives an internal transconductance amplifier that servos the DC/DC converter's ITH pin voltage in response to the current requirements of a charging battery. CSOUT voltage is also used internally as a charge current monitor to detect <C/10 current thresholds.

Battery voltage is monitored via the V_{FB} pin. This voltage drives a transconductance amplifier that servos the DC/DC converter ITH pin voltage in response to voltage developed on a charging battery. The transition from constant-current (CC) to constant-voltage (CV) charging modes is also detected using this transconductance amplifier. The V_{FB} voltage is used for all battery voltage monitor thresholds, each being defined as a percentage of the internal 2.5V reference voltage.

Input voltage regulation is implemented via the V_{IN_REG} pin for use with poorly regulated or high impedance supplies. This pin drives a transconductance amplifier that reduces the ITH pin voltage in response to voltage sensed on the V_{IN_REG} pin falling through 2.5V. This transconductance amplifier remains active even while battery charging is disabled, so the input regulation feature continues to operate regardless of the state of a charge cycle.

The LTC4020 contains an internal charge cycle timer that is used for time based control of a charge cycle. This function is enabled by connecting a capacitor to the TIMER pin. Grounding this pin disables all timer functions. The timer is used to terminate a successful CC or CC/CV charge cycle after a programmed end-of-cycle (T_{EOC}) time. This timer is also used to transition a lead-acid charger to float charging if charge current does not fall adequately during the absorption phase of the charge cycle within the programmed T_{EOC} time.

Use of the timer function also enables bad battery detection during CC/CV or lead-acid charging. This fault condition is achieved if the battery does not respond to preconditioning (V_{FB} < 1.75V), such that the charger remains in (or enters) precondition mode after one-eighth of the programmed T_{EOC} time. A bad battery fault halts the charging cycle, and the fault condition is reported on the status pins.

OPERATION

CC/CV Charging Overview (MODE = 0V)

To program the LTC4020 for CC/CV charging, connect the MODE pin to ground. This mode is commonly used for Li-Ion, Li-Polymer, and $LiFePO_4$ battery charging.

If the voltage on the V_{FB} pin is below 1.75V, the LTC4020 engages precondition mode, which provides low level charge currents to gently increase voltage on heavily discharged batteries. During preconditioning, the maximum charge current is reduced to one-fifteenth of the programmed value as set by R_{CS}, the battery charge current programming resistor. Full charge current capability is restored once the voltage on V_{FB} rises above 1.75V. Full charge current capability remains until the V_{FB} pin approaches the 2.5V float voltage. This is the constant-current (CC) portion of the charge cycle.

When the voltage on the V_{FB} pin approaches the 2.5V float voltage, the charger transitions into constant-voltage (CV) mode, and charge current is reduced from the maximum programmed value. If timer termination is used, the safety timer period starts when CV mode is initiated, and the charge cycle will terminate when the timer achieves end-of-cycle (T_{EOC}). This timer is typically programmed to achieve T_{EOC} in three hours, but can be configured for any amount of time by setting an appropriate timing capacitor value (C_{TIMER}).

During CV mode, the required charge current is steadily reduced as the battery voltage is maintained such that the voltage on the V_{FB} pin remains close to 2.5V. If the charger is configured for C/10 termination, when the battery charge current falls below one-tenth of the programmed maximum current (<C/10), the charge cycle will terminate and the charger indicates not charging on the status pins.

When timer termination is used, the charger continues to operate with charging current less than one-tenth of the programmed maximum current. The STAT1 status pin, however, responds to the <C/10 current level regardless of termination scheme, so the IC will indicate a not charging status when the charging current is below the C/10 current level. The charge cycle will continue, however, and the charger will source <C/10 current into the battery. Programmed float voltage is maintained while the charger tops-off the battery with low currents until the programmed T_{EOC} time has elapsed, at which time the charge cycle will terminate, charge current flow into the battery will be disabled, and the battery will be disconnected from the converter output.

After termination, if the battery discharges such that the voltage on the V_{FB} pin drops to 2.4375V, or 97.5% of the programmed float voltage, a new charge cycle is automatically initiated.

Table 1. Typical CC/CV Charge Cycle Voltages (per Cell)

	Li-Ion	$LiFePO_4$
Precondition	2.94V	2.52V
Float	4.2V	3.6V
Recharge	4.095V	3.51V

Lead-Acid Charging Overview (MODE = INT_VCC)

To program the LTC4020 for lead-acid charging, connect the MODE pin to the $INTV_{CC}$ pin. The LTC4020 supports a 4-step, 3-stage lead-acid charging profile.

The first step of the charging profile provides low level charge current to gently increase voltage on heavily discharged batteries. If the voltage on V_{FB} is below 1.75V, which corresponds to just over 10V for a 6-cell (12V) battery, the maximum charge current is reduced to one-fifteenth of the programmed value as set by RCS. Once the V_{FB} voltage rises above 1.75V, full charge current capability is restored, and the bulk charging stage begins.

The bulk charging stage of the charge profile, which is the first stage of 3-stage battery charging, is a constant-current charging stage, with the maximum programmed charge current forced into the battery. This continues until the battery voltage rises such that the V_{FB} pin approaches the 2.5V absorption reference voltage.

As the bulk charging stage completes and the voltage on the V_{FB} pin rises to approach 2.5V, the charger transitions into the absorption stage, which is the 2nd stage of 3-stage battery charging. During the absorption stage, the required charge current is steadily reduced as the battery voltage approaches the absorption voltage. This is a constant-voltage charging stage, as the battery voltage is maintained such that the V_{FB} pin remains close to the

OPERATION

2.5V absorption reference voltage. It is during this stage that the battery stored charge increases to 100% capacity. The 2.5V absorption reference typically corresponds to 14.4V for a 6-cell battery.

When the absorption stage charge current falls to one-tenth of the programmed maximum current, the charger will initiate the third stage in the charge profile, the float charging stage. The safety timer can be used with a lead-acid charger to limit the duration of the absorption stage of the charging profile. The timer is initiated at the start of the absorption stage, and forces the charger into float if the charge current does not fall to the required one-tenth of the programmed maximum current during the absorption stage before the timer reaches T_{EOC}. A 0.47µF capacitor on the TIMER pin is typically used, which generates a 6.8-hour absorption stage safety timeout.

Once the float charging stage is initiated, the battery reference voltage is reduced to 92.5% of the absorption voltage, or 2.3125V. The battery voltage is maintained at a voltage corresponding to this reference voltage, and maximum charge current is reduced to one-fifteenth of the programmed maximum. This level corresponds to 13.3V for a 6-cell battery.

Once float charging is achieved, the LTC4020 charger remains active and will attempt to maintain the float voltage on the battery indefinitely. During float charging, if a load on the battery exceeds the maintenance charge current of one-fifteenth of the programmed maximum, the battery voltage will begin to discharge. If a load discharges the battery such that the voltage on V_{FB} falls to 2.1875V, corresponding to 12.6V for a 6-cell battery, the LTC4020 restarts the full 3-stage charging cycle by reinitiating the bulk charging stage. Bulk charging is engaged by resetting the internal V_{FB} reference to the 2.5V absorption voltage reference and increasing the charge current capability to the programmed maximum.

Table 2. Typical Lead-Acid Charge Cycle Voltages (12V System)

Precondition	10.1V
Absorption	14.4V
Float	13.3V
Bulk Restart	12.6V

CC Charging Overview (MODE = NC)

To program the LTC4020 for CC charging, leave the MODE pin unconnected. This mode can be used for charging NiCd and NiMH batteries, supercap charging, or in any other application where a timed current source is desired. CC mode can also be used when the voltage dependent precondition mode is not desired.

In CC mode, the LTC4020 will maintain full programmed charge current capability for the duration of the timer period. The trickle charge function is disabled, although maximum charge current will be reduced during instant-on operation when the PowerPath FET is operating in linear mode. The charger will terminate the charge cycle and the PowerPath FET will become high-impedance once timer EOC is reached.

While the charge cycle is designed to be voltage independent, a maximum V_{BAT} voltage can be programmed corresponding to V_{FB} = 2.5V, allowing constant-voltage functionality at that level if desired.

Once the timer reaches T_{EOC} and the charge cycle terminates, input power or SHDN must be cycled to initiate another charge cycle. If the timer function is disabled (TIMER = 0V), the current source function remains active indefinitely.

Note: For nickel-chemistry batteries (e.g. NiCd or NiMH), the possibility of overcharging must be considered. A typical method is to charge with low currents for a long period of time. NiCd and NiMH batteries can absorb a C/300 charge rate indefinitely. Shorter duration charging is possible using a timed current source charge algorithm. It is recommended to ensure a depleted battery before charging, then subsequently charge the battery to no more than 125% capacity. For example, a depleted 2000mAh NiMH battery is charged with 2.5A for one hour.

APPLICATIONS INFORMATION

DC/DC CONVERTER SECTION

Output Voltage Programming

The LTC4020 DC/DC converter maximum output voltage, or voltage safety limit, is set by an external feedback resistive divider, providing feedback to the V_{FBMAX} pin. This divider sets the output voltage that the converter will servo to when the PowerPath FET is high impedance, which occurs after charge cycle termination or during a charge cycle fault.

The resultant feedback signal is compared with the internal 2.75V voltage reference by the converter error amplifier. The output voltage is given by the equation:

$$V_{OUT} = 2.75V \bullet \left(1 + \frac{R_{MAX1}}{R_{MAX2}}\right)$$

where R_{MAX1} and R_{MAX2} are defined as in Figure 6.

The values for R_{MAX1} and R_{MAX2} are typically the same as those used for the divider that programs battery voltage (to the V_{FB} pin; see Battery Charger Section), to yield a DC/DC converter maximum regulation voltage, or safety limit, that is 10% higher than the battery charge voltage.

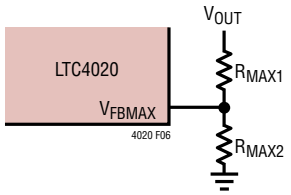


Figure 6. V_{OUT} Safety Limit Programming

R_{SENSEA}, R_{SENSEB}: DC/DC Converter Current Programming

The LTC4020 performs inductor current sensing via two resistors connected in series with the V_{IN} side switches (see Figure 3). The high side sense resistor (R_{SENSEA}) is connected between V_{IN} and the drain of the top side switch FET (A). Both nodes on the sense resistor must be Kelvin connected to the IC via the pins $SENSV_{IN}$ and SENSTOP. Likewise, the low side sense resistor (R_{SENSEB}) is connected between the source of the bottom side switch FET (B) and PGND. Both nodes on the sense resistor must be Kelvin connected to the IC, via the pins SENSBOT and SENSGND.

Both of these sense resistors must be of equal value, and that value programs the switched inductor maximum average current in the DC/DC converter inductor (I_{LMAX}) such that:

$$R_{SENSEA} = R_{SENSEB} = \frac{0.05}{I_{LMAX}}$$

When the converter is stepping down, or operating in buck mode, the inductor current will be roughly equivalent to the converter output current. Input supply current (I_{IN}) will be less than the inductor current (I_L), such that:

$$I_L \sim I_{IN} \bullet \left(\frac{V_{IN}}{V_{OUT}}\right)$$

When the converter is stepping up, or operating in boost mode, the inductor current will be roughly equivalent to the converter input current. Inductor current (I_L) will be greater than output current (I_{OUT}), such that:

$$I_L \sim I_{OUT} \bullet \left(\frac{V_{OUT}}{V_{IN}}\right)$$

Overcurrent Detection

The LTC4020 also contains an overcurrent detection circuit that monitors the low side current sense resistor, or SENSBOT–SENSGND input. Should that circuit detect a voltage on that input that is less than –150mV or greater than 100mV, or roughly 3x the maximum average current, all of the switches are disabled for four (4) clock cycles.

Parasitic inductances on non-ideal layouts and or body-diode commutation charge can cause voltage spikes across the sense resistor at the beginning of synchronous FET conduction. The LTC4020 overcurrent circuitry is somewhat resistant to these leading edge spikes but, in some cases, the overcurrent circuit can be prematurely triggered. This is identified by the repeated 4-cycle switch off-time that occurs should premature triggering occur. Placing a ceramic capacitor across the

APPLICATIONS INFORMATION

SENSBOT–SENSGND input pins near the IC will generally eliminate premature triggering by low pass filtering the current sense signal. Setting the τ of the effective filter in the range of 1ns is generally sufficient to shunt errant signals, such that:

$$C_{SENSB} \sim \frac{1ns}{R_{SENSEB}}$$

Programming Switching Frequency

The RT frequency adjust pin allows the user to program the LTC4020 DC/DC converter operating frequency from 50kHz to 500kHz.

Higher frequency operation is desirable for smaller external inductor and capacitor values, but at the expense of increased switching losses and higher gate drive currents. Higher frequencies may also not allow sufficiently high or low duty cycle operation due to minimum on/off time constraints. Lower operating frequencies require larger external component values, but result in reduced switching losses yielding higher conversion efficiencies.

Operating frequency (f_O) is set by choosing an appropriate frequency setting resistor (R_{RT}), connected from the RT pin to ground. This resistor is required for operation; do not leave this pin open. For a desired operating frequency, R_{RT} follows the relation:

$$R_{RT} = 100k\Omega \bullet \left(\frac{f_O}{250kHz}\right)^{-1.0695}$$

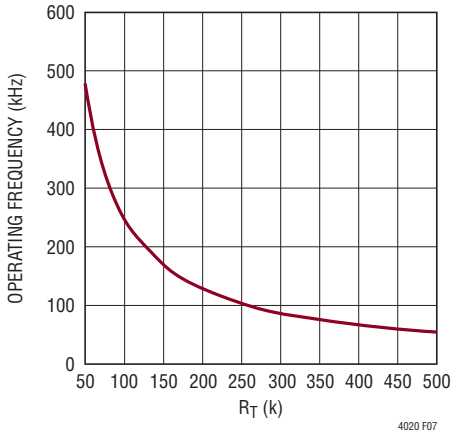


Figure 7. R_T vs Operating Frequency

Input Supply Decoupling

The LTC4020 is typically biased directly from the charger input supply through the PV_{IN} and $SENSV_{IN}$ pins. This supply provides large switched currents, so a high quality, low ESR decoupling capacitor is recommended to minimize voltage glitches on the V_{IN} supply. Placing a smaller ceramic capacitor (0.1µF to 10µF) close to the IC in parallel with the input decoupling capacitor is also recommended for high frequency noise reduction. The $SENSV_{IN}$ pin is a Kelvin connection from the V_{IN} supply at the primary V_{IN} side switch FET (A); separate decoupling for that pin is not recommended. The charger input supply decoupling capacitor (C_{VIN}) absorbs all input switching ripple current in the charger, so it must have an adequate ripple current rating. RMS ripple current ($I_{CVIN(RMS)}$) is highest during step down operation, and follows the relation:

$$I_{CVIN(RMS)} \sim I_{MAX} \bullet DC \bullet \sqrt{\frac{1}{DC} - 1}$$

which has a maximum at DC = 0.5, or $V_{IN} = 2 \bullet V_{OUT}$, where:

$$I_{CVIN(RMS)} = \frac{I_{MAX}}{2}$$

The simple worst-case of ½ • I_{MAX} is commonly used for design, where I_{MAX} is the programmed inductor current limit.

Bulk capacitance ($C_{IN(BULK)}$) is a function of desired input ripple voltage (ΔV_{IN}). For step-down operation, $C_{IN(BULK)}$ follows the relation:

$$C_{IN(BULK)} \geq I_{MAX} \bullet \frac{V_{OUT(MAX)}}{V_{IN(MIN)}} \bullet \frac{1}{\Delta V_{IN} \bullet f_O}$$

where f_O is the operating frequency, $V_{OUT(MAX)}$ is the DC/DC converter maximum output voltage and $V_{IN(MIN)}$ is the regulation voltage corresponding to 2.5V on V_{IN_REG}. If the input regulation feature is not being used, use the minimum expected input operating voltage.

If an application does not require step-down operation, during step-up operation, input ripple current is equivalent

APPLICATIONS INFORMATION

to inductor ripple current (ΔI_{MAX}), so $C_{IN(BULK)}$ follows the relation:

$$C_{IN(BULK)} = \frac{\Delta I_{MAX}}{\Delta V_{IN} \bullet f_O}$$

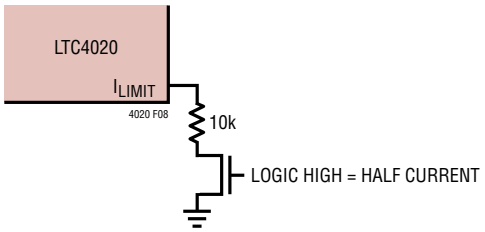


Figure 8. Using the I_{LIMIT} Pin for Digital Control of Maximum Average Inductor Current

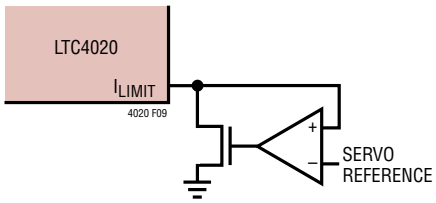


Figure 9. Driving the I_{LIMIT} Pin with a Current Sink Active Servo Amplifier

I_{LIMIT} Pin

Maximum average inductor current can be dynamically adjusted using the I_{LIMIT} pin as described in the Pin Functions section. Active servos can also be used to impose voltages on the I_{LIMIT} pin, provided they can only sink current. Active circuits that source current must not be used to drive the I_{LIMIT} pin.

Inductor Selection

The primary criterion for inductor value selection in an LTC4020 charger is the ripple current created in that inductor. Once the inductance value is determined, an inductor must also have a saturation current equal to or exceeding the maximum peak current in the inductor.

An inductor value (L) is calculated based on the maximum desired amount of peak-to-peak ripple current, ΔI_{MAX}. The ripple current can be expressed as α, the ratio of the peak-to-peak ripple current to the maximum average inductor current, I_{MAX}.

$$\alpha \equiv \frac{\Delta I_{MAX}}{I_{MAX}}$$

A range of 0.2 to 0.5 for α is typical. When stepping down, ripple current gets larger with increased V_{IN}, and is maximized when $V_{OUT} = V_{IN}/2$. When stepping up, ripple current gets larger with increased V_{OUT}, and is maximized when $V_{IN} = V_{OUT}/2$. The inductor value must be chosen using the greatest expected operational difference between these values.

A minimum inductor value for a given maximum ripple current and operating frequency (f_O) can be determined using whichever relation yields the largest inductor value for L_{MIN}:

If $V_{IN} > V_{OUT}$ (step-down conversion):

$$L_{MIN} = \frac{V_{OUT} \bullet \left(1 - \left[V_{OUT} / V_{IN(MAX)}\right]\right)}{f_O \bullet \alpha \bullet I_{MAX}}$$

If $V_{IN} < V_{OUT}$ (step-up conversion):

$$L_{MIN} = \frac{V_{IN} \bullet \left(1 - \left[V_{IN} / V_{OUT(MAX)}\right]\right)}{f_O \bullet \alpha \bullet I_{MAX}}$$

For step-down conversion, use the maximum expected operating voltage for $V_{IN(MAX)}$. If the expected V_{OUT} operating range (typically from V_{FBMIN} = 2.125V to V_{FBMAX} = 2.75V) includes $V_{IN(MAX)}/2$, use that value for V_{OUT}. If the entire operating range is below $V_{IN(MAX)}/2$, use the value corresponding to V_{FBMAX} = 2.75V. If the entire operating range is above $V_{IN(MAX)}/2$, use the value corresponding to V_{FBMIN} = 2.125V.

For step-up conversion, use the maximum output voltage (typically corresponding to pin V_{FBMAX} = 2.75V) for $V_{OUT(MAX)}$. If the expected V_{IN} operating range includes $V_{OUT(MAX)}/2$, use that value for V_{IN}. If the entire input operating range is below $V_{OUT(MAX)}/2$, use the maximum operating voltage for V_{IN}. If the entire input operating range is above $V_{OUT(MAX)}/2$, use the minimum input operating voltage for V_{IN}.

APPLICATIONS INFORMATION

Magnetics vendors typically specify inductors with maximum RMS and saturation current ratings. Select an inductor that has a saturation current rating at or above 1.25 • I_{MAX}, and an RMS rating above I_{MAX}.

Output Decoupling

During periods when the LTC4020 DC/DC converter output is not connected to the battery through the PowerPath FET, the system load is driven directly by the converter. The converter creates large switched currents, so a high quality, low ESR decoupling capacitor is recommended to minimize voltage glitches on the V_{OUT} supply. Placing a smaller ceramic decoupling capacitor (0.1µF to 10µF) in parallel with the output decoupling capacitor is also recommended for high frequency noise reduction. The V_{OUT} decoupling capacitor (C_{VOUT}) absorbs the majority of the converter ripple current, so it must have an adequate ripple current rating. RMS ripple current ($I_{\Delta RMS}$) is highest during step up operation, and follows the relation:

$$I_{\Delta RMS} \sim I_{MAX} \bullet DC \bullet \sqrt{\frac{1}{DC} - 1}$$

having a maximum at DC = 0.5, or $V_{OUT} = 2 \bullet V_{IN}$, where:

$$I_{CVOUT(RMS)} = \frac{I_{MAX}}{2}$$

The simple worst-case of ½ • I_{MAX} is commonly used for design, where I_{MAX} is the programmed inductor current limit.

Bulk capacitance is a function of desired output ripple voltage (ΔV_{OUT}), and follows the relations:

For step-up operation:

$$C_{OUT(BULK)} \geq I_{MAX} \bullet \frac{V_{OUT(MAX)} - V_{IN(MIN)}}{V_{OUT(MAX)}} \bullet \frac{1}{\Delta V_{OUT} \bullet f_O}$$

where $V_{OUT(MAX)}$ is the DC/DC converter safety limit, and $V_{IN(MIN)}$ is the V_{IN} regulation threshold. If the V_{IN} regulation feature is not being used, use the minimum expected operating voltage.

For step-down operation, output ripple current is equivalent to inductor ripple current (ΔI_{MAX}), so $C_{OUT(BULK)}$ follows the relation:

$$C_{OUT(BULK)} \geq \frac{\Delta I_{MAX}}{\Delta V_{OUT} \bullet f_O}$$

Switch FET Selection

The LTC4020 requires four external N-channel power MOSFETs, as shown in Figure 3.

Specified parameters used for power MOSFET selection are: breakdown voltage ($V_{BR(DSS)}$), threshold voltage ($V_{GS(TH)}$), on-resistance ($R_{DS(ON)}$), reverse transfer capacitance (C_{RSS}), and maximum inductor current (I_{LMAX}).

The drive voltage is set by the $INTV_{CC}$ supply pin, which is typically 5V. Consequently, logic-level threshold MOSFETs must be used in LTC4020 applications.

Transition Losses (P_{TR}): During maximum power operation, all 4 switches change state once per oscillator cycle, so the maximum switching transient power losses (P_{TR}) remain constant over condition.

$$P_{TR(A, B)} \approx (k)(V_{IN})^2 (I_{LMAX})(C_{RSS})(f_O)$$

$$P_{TR(C, D)} \approx (k)(V_{OUT})^2 (I_{LMAX})(C_{RSS})(f_O)$$

$P_{TR(A, B)}$ is the transition loss for the V_{IN} side switch FETs A and B, and $P_{TR(C,D)}$ is the transition loss for V_{OUT} side switch FETs C and D, with the switch FETs designated as in Figure 3. The constant *k*, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has a empirical value approximated by *k* = 1 in LTC4020 applications. I_{LMAX} is the converter maximum inductor current as programmed by the two sense resistors. C_{RSS}, the MOSFET reverse transfer capacitance, is specified by the MOSFET manufacturer.

Conductive Losses (P_{ON}): Conductive losses are proportional to switch duty cycle. The average conductive losses in a switch at maximum inductor current (I_{LMAX})is:

$$P_{ON} = I_{LMAX}^2 \bullet \rho T \bullet R_{DS(ON)} \bullet (T_{ON} \bullet f_O)$$

where ρT is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance

APPLICATIONS INFORMATION

with temperature. For a maximum junction temperature of 125°C, using a value of $\rho T = 1.5$ is reasonable.

If $V_{IN} > V_{OUT}$ (step-down conversion):

$$P_{ON(A)} = I_{LMAX}^2 \bullet \rho T \bullet R_{DS(ON(A))} \bullet (V_{OUT}/V_{IN})$$

$$P_{ON(B)} = I_{LMAX}^2 \bullet \rho T \bullet R_{DS(ON(B))} \bullet (1 - V_{OUT}/V_{IN})$$

$$P_{ON(C+D)} = I_{LMAX}^2 \bullet \rho T \bullet R_{DS(ON(C, D))}$$

If $V_{IN} < V_{OUT}$ (step-up conversion):

$$P_{ON(A+B)} = I_{LMAX}^2 \bullet \rho T \bullet R_{DS(ON(A, B))}$$

$$P_{ON(C)} = I_{LMAX}^2 \bullet \rho T \bullet R_{DS(ON(C))} \bullet (1 - V_{IN}/V_{OUT})$$

$$P_{ON(D)} = I_{LMAX}^2 \bullet \rho T \bullet R_{DS(ON(D))} \bullet (V_{IN}/V_{OUT})$$

Optional Schottky Diode (Db, Dd) Selection

Schottky diodes can be placed in parallel with the synchronous FETs B and D, as shown in Figure 3 as Db and Dd. These diodes conduct during the dead time between the conduction of the power MOSFET switches and are intended to prevent the body diode of synchronous switches from storing charge.

To maximize effectiveness of the diodes, the inductance between the switches and the synchronous switches must be minimized, so the diodes should be placed adjacent to their corresponding FET switch.

The Dd diode also reduces power dissipation in the D switch during periods of reverse current inhibit operation, during which time the D switch is disabled. Load currents are low during reverse inhibit, and diode Db only conducts during switch dead times, so both can have current ratings well below the DC/DC converter inductor current maximum. Typically, a diode with an average current rating at or above one-tenth of I_{LMAX} is adequate, provided the diode has an instantaneous current rating that exceeds the maximum inductor current, or $I_{LMAX} + \frac{1}{2} \Delta I_{MAX}$.

Db reverse voltage rating must exceed V_{IN}. Dd reverse voltage rating must exceed V_{OUT}.

$INTV_{CC}$ LDO Output, and BST1 and BST2 Supplies

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. An internal 5V low dropout regulator (LDO) supplies $INTV_{CC}$ power from the PV_{IN} pin. $INTV_{CC}$ is decoupled to PGND using a 2.2µF ceramic capacitor.

The BST1 and BST2 bootstrapped supply pins power internal high side FET gate drivers, which output to pins TG1 and TG2. BST1 provides switch gate drive above the input power supply voltage for switch FET A, and BST2 provides switch gate drive above the output power supply voltage for switch FET D, as designated in Figure 3. These boosted supply pins allows the use of NFET switches for increased conversion efficiency. These bootstrapped supplies are regenerated through external Schottky diodes from the $INTV_{CC}$ pin.

Connect two low leakage 1A Schottky diode anodes to the $INTV_{CC}$ pin. Connect one Schottky cathode to the BST1 pin. This diode must be rated for reverse voltage standoff exceeding the maximum input supply voltage. Connect the other diode cathode to the BST2 pin. This diode must be rated for reverse voltage standoff exceeding the converter safety limit output, $V_{OUT(MAX)}$.

Connect a ceramic capacitor from the BST1 pin to the SW1 pin and another from BST2 pin to the SW2 pin. The value of these two capacitors should be at least 50 times greater than the equivalent total gate capacitance of the corresponding switch FET. Total FET gate charge ($Q_{G(TOT)}$) is typically specified at a specific gate-source voltage ($V_{GS(Q)}$). Using those parameters, the required boost capacitor values (C_{BST}) follow the relation:

$$C_{BST} > 50 \bullet Q_{G(TOT)}/V_{GS(Q)}$$

C_{BST} = 1µF is typically adequate for most applications.

During low load operation, start-up, and nonoverlap periods, inductor current is conducted by the silicon body diode of the synchronous FET. This diode stores a significant amount of charge, so when the primary switch turns on for the next switch cycle, reverse recovery current is conducted by the main switch to discharge this diode. The resultant short-duration current spike can be orders of magnitude greater than the inductor current itself, resulting in an extremely fast dV/dt on the switched node. Consequently, parasitic inductance associated with the switch FET packaging and/or less-than-ideal layout can induce a voltage spike of 10 or more volts at the leading edge of a switching cycle. This can be particularly

APPLICATIONS INFORMATION

problematic on the step-up side of the inductor, as these voltage spikes are negative, and can cause a build-up of voltage on the BST2-SW2 capacitor. This would generally occur when the step-up synchronous switch (D) is disabled, such as during low load operation and during start-up. If voltage build-up on the boosted supply proves excessive, it could potentially violate absolute maximum voltage ratings of the IC and cause damage. This effect can be greatly reduced by implementing a Schottky diode across the step-up synchronous FET, shown as D_D in Figure 3, which reduces reverse recovery charge in the synchronous FET body diode. A low current 6V Zener (0.1A) in parallel with the BST2-SW2 capacitor will also effectively shunt any errant charge and prevent excessive voltage build-up.

External Power for BST1 and BST2 Supplies

Power for the top and bottom MOSFET drivers can be supplied by an external supply, provided that a precision 5V supply is available (±5%).

The $INTV_{CC}$ internal supply is a linear regulator, which transfers current from the V_{IN} pin. As such, power dissipation can be excessive with high V_{IN} pin voltages and/or large gate drive requirements. The power dissipation in the linear pass element (P_{INTVCC}) is:

$$P_{INTVCC} = (V_{IN} - 5V) \bullet Q_{G(TOT)ABCD} \bullet f_O$$

where $Q_{G(TOT)ABCD}$ is the sum of all four switch total gate charges, and f_O is the LTC4020 switching frequency.

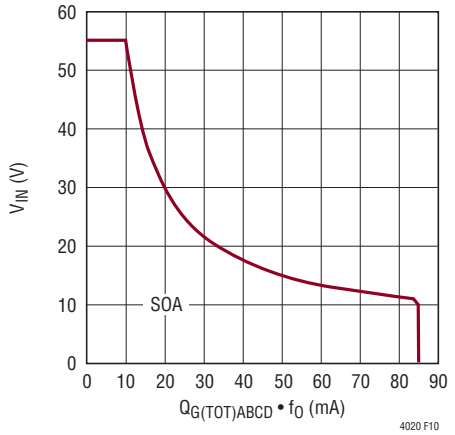


Figure 10. $INTV_{CC}$ Pass Element SOA (Safe Operating Area)

The SOA curve is bounded by the LTC4020 operating voltage of 55V, the linear-pass-device power dissipation of 500mW and the linear-regulator minimum dropout current of 85mA. If desired operation places the internal 5V regulator out of the allowable SOA region, deriving gate drive power externally is required. The circuit in Figure 11 uses an external regulator to offload the power dissipation to an external regulator. With 5.5V output, the LTC4020 easily handles internal power dissipation while allowing plenty of overhead for regulator dropout voltage.

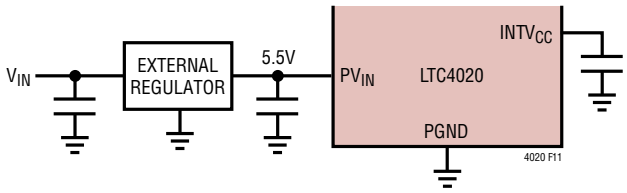


Figure 11. Connection of External Voltage Regulator for Reduced Internal Power Dissipation

BATTERY CHARGER SECTION

Battery Charge Voltage Programming

The LTC4020 uses an external feedback resistive divider from the BAT pin to ground to program battery voltages. This divider provides feedback to the V_{FB} pin, and sets the final voltage that the battery charger will achieve at the end of a charge cycle. The feedback reference of 2.5V corresponds to the battery float voltage during CC/CV mode charging (MODE = 0V).

The resultant feedback signal is compared with the internal 2.5V voltage reference by the converter error amplifier. The output voltage is given by the equation:

$$V_{(FLOAT(CC/CV)} = 2.5V\left(1+\frac{R_{FB1}}{R_{FB2}}\right)$$

where R_{FB1} and R_{FB2} are defined as in Figure 12.

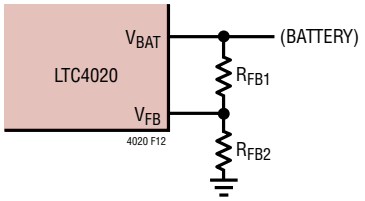


Figure 12. Battery Voltage Programming

APPLICATIONS INFORMATION

If charging in CC mode (MODE = NC), R_{FB1} and R_{FB2} corresponding to V_{FB} = 2.5V programs a maximum V_{BAT} voltage, if constant-voltage functionality at that level if desired.

During lead-acid charging (MODE = $INTV_{CC}$), the absorption mode voltage corresponds to 2.5V on the V_{FB} pin. Battery float voltage (maintenance) corresponds to 2.3125V on the V_{FB} pin, or 92.5% of the absorption voltage. These voltages typically correspond to 14.4V and 13.3V respectively for a 6-cell (12V) battery.

The values for R_{FB1} and R_{FB2} are typically the same as those used for the divider that programs the converter safety limit (converter output to the V_{FBMAX} pin; see DC/DC Converter Section), which yields a DC/DC converter maximum regulation voltage, or safety limit, that is 10% higher than the maximum battery charge voltage.

Table 3. Common Battery Types: Normalized R_{FB1} Resistor Values (R_{FB2} = 1)

BATTERY TYPE	VOLTAGE	R_{FB1}
1-Cell $LiFePO_4$	3.6V Float	0.44
1-Cell Li-Ion	4.2V Float	0.68
2-Cell $LiFePO_4$	7.2V Float	1.88
2-Cell Li-Ion	8.4V Float	2.36
6-Cell Lead-Acid	12V Battery	4.76
3-Cell $LiFePO_4$	10.8V Float	3.32
3-Cell Li-Ion	12.6V Float	4.04
4-Cell $LiFePO_4$	14.4V Float	4.76
6-Cell $LiFePO_4$	21.6V Float	7.64
12-Cell Lead-Acid	24V Battery	10.52

R_{CS}: Battery Charge Current Programming

The LTC4020 senses battery charge current using a sense resistor that is connected between the CSP and CSN pins. Maximum average battery charge current (I_{CSMAX}) is programmed by setting the value of this current sense resistor. The resistor value is selected so the desired maximum charge current through that sense resistor creates a 50mV drop, or:

$$R_{CS} = \frac{0.05V}{I_{CSMAX}}$$

For example, for a maximum average charge current of 5A, use a 0.01Ω sense resistor.

PowerPath FET Function and Instant-On

The LTC4020 controls an external PMOS with its gate connected to the BGATE pin. This PowerPath FET controls current flow to and from the battery.

During a normal battery charge cycle, the BGATE pin is pulled low (clamped at V_{GS} = 9.5V), which operates the FET as a low impedance connection from the DC/DC converter output to the battery, effectively shorting the battery to the converter output. This minimizes power dissipation from charge current passing thorough the FET. When there is no V_{IN} power or when the IC is in shutdown, LTC4020 connects the battery to the converter output by holding the BGATE pin low, again effectively shorting the battery to the converter output. This minimizes power dissipation while the output is powered by the battery.

The LTC4020 controls the PowerPath FET to perform instant-on operation when a charge cycle is initiated into a heavily discharged battery. If the battery voltage is below a programmed minimum operational output voltage, corresponding to V_{FBMIN} = 2.125V, the PowerPath FET is configured as a linear regulator, allowing the DC/DC converter output to rise above the battery voltage while still providing charge current into the battery. During instant-on operation, the BGATE pin is driven by the LTC4020 to maintain the minimum programmed voltage on the PowerPath FET source, the FET acting as a high

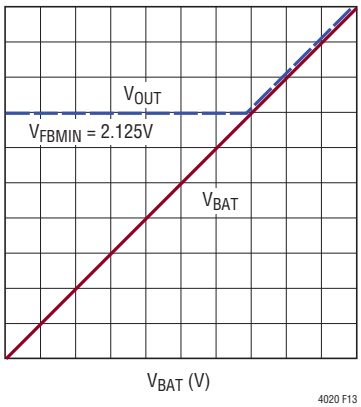


Figure 13. Instant-On DC/DC Converter Output vs Battery Voltage Characteristics

APPLICATIONS INFORMATION

impedance current source, providing charge current to the battery, independent of the battery voltage.

The resultant feedback signal is compared with the internal 2.125V voltage reference by a dedicated instant-on error amplifier, the output of which servos the BGATE pin. The output voltage is given by the equation:

$$V_{OUT} = 2.125V\left(1+\frac{R_{MIN1}}{R_{MIN2}}\right)$$

where R_{MIN1} and R_{MIN2} are defined as in Figure 14.

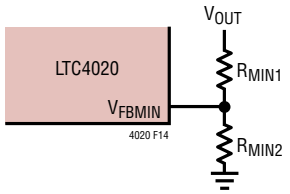


Figure 14. V_{OUT} Instant-On Programming

The values for R_{MIN1} and R_{MIN2} are typically the same as those used for the divider that programs battery voltage (to the V_{FB} pin; see Battery Charger Section), to yield a DC/DC converter minimum operational regulation voltage corresponding to 85% of the battery charge voltage.

During instant-on operation, if the drain-to-source voltage across the PowerPath FET ($V_{CSN} – V_{BAT}$) exceeds 0.45V, the maximum charge current is automatically reduced. Maximum charge current is reduced linearly across the range of $0.45V < V_{CSN} – V_{BAT} < 1.95V$ to one-fifteenth of the current programmed by the battery charger sense resistor, RCS. This reduction in charge current helps to prevent excessive power dissipation in the PowerPath FET.

When the DC/DC converter is operating, but the battery charger is not in a charging cycle, the PowerPath FET is automatically configured as an ideal diode between the BAT pin (anode) and the CSN pin (cathode). The ideal diode function allows the battery to remain disconnected from the converter output while the converter is supplying power, but also allows the battery to be efficiently engaged for additional power should a load exceed the DC/DC converter's capability. This ideal diode circuit regulates the external FET to achieve low loss conduction, maintaining a voltage drop of 14mV across from the BAT pin to the CSN pin, provided the battery current load though the ideal diode does not exceed $14mV/R_{DS(ON)}$. With larger currents, the FET will behave like a fixed value resistor equal to $R_{DS(ON)}$.

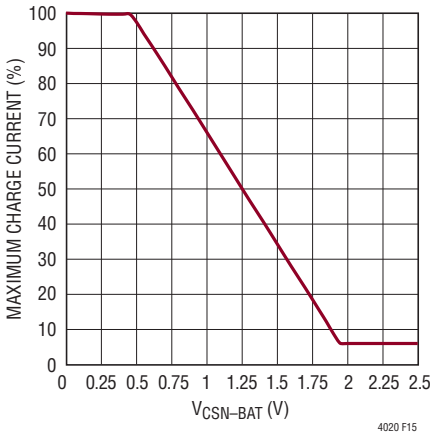


Figure 15. Instant-On Charger Current Sense Limit Reduction

In certain applications, the PowerPath function is not required. For example, lead-acid chargers do not terminate (they remain in float charging mode indefinitely), so the battery need never be disconnected from the output, provided the instant-on feature is not desired. The PowerPath FET can be eliminated in these applications by tying the CSN side of the sense resistor to BAT, connecting V_{FBMIN} to ground, and connecting a 100pF capacitor from the BGATE pin to CSN. See Typical Application Circuits section.

RNG/SS: Dynamic Current Limit Adjust

Maximum charge current can be dynamically adjusted using the RNG/SS pin as described in the Pin Functions section. Active servos can also be used to impose voltages on the RNG/SS pin, provided they can only sink current. Active circuits that source current cannot be used to drive the RNG/SS pin.

APPLICATIONS INFORMATION

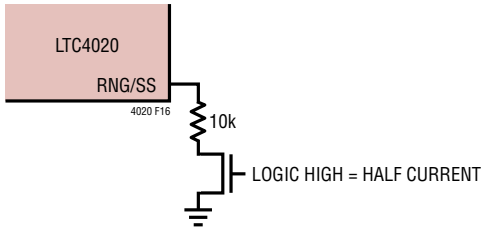


Figure 16. Using the RNG/SS Pin for Digital Control of Maximum Charge Current

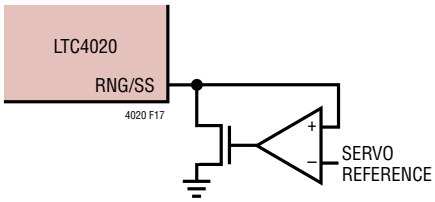


Figure 17. Driving the RNG/SS Pin with a Current Sink Active Servo Amplifier

RNG/SS: Soft-Start

Soft-start functionality is also supported by the RNG/SS pin. 50µA is sourced from the RNG/SS pin, so connecting a capacitor from the RNG/SS pin to ground ($C_{RNG/SS}$) creates a linear voltage ramp. The maximum charge current follows this voltage, thus increasing the charge current capability from zero to the full programmed value as the capacitor gets charged from 0 to 1V. The value of $C_{RNG/SS}$ is calculated based on the desired time to full current (T_{SS}) following the relation:

$$C_{RNG/SS} = 50\mu A \bullet T_{SS}$$

The RNG/SS pin is pulled to ground internally when charging is terminated so each new charging cycle begins with a soft-start cycle. RNG/SS is also pulled to ground during bad battery and NTC fault conditions.

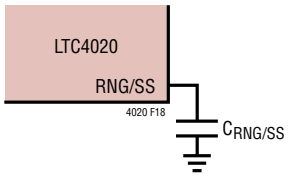


Figure 18. Using the RNG/SS Pin for Soft-Start

Status Pins

The LTC4020 reports charger status through two open collector outputs, the STAT1 and STAT2 pins. These pins can accept voltages as high as 55V when disabled, and can sink up to 5mA when enabled.

If the LTC4020 is configured for a CC/CV charging algorithm, the STAT1 pin is pulled low while battery charge currents exceed 10% of the programmed maximum (C/10). The STAT1 pin is also pulled low during NTC faults. The STAT2 pin is pulled low during NTC faults or after a bad battery fault occurs. The STAT1 pin becomes high impedance when a charge cycle is terminated or when charge current is below the C/10 threshold, and the STAT2 pin remains high impedance if no fault conditions are present.

If the LTC4020 is configured for a CC charging algorithm, the STAT1 pin is pulled low during the entire charging cycle, and the STAT2 pin is pulled low during NTC faults. The STAT1 pin becomes high impedance when the charge cycle is terminated.

If the LTC4020 is configured for a lead-acid charging algorithm, the STAT1 and STAT2 pins are used as charge cycle stage indicator pins. The STAT1 pin is pulled low during the bulk and absorption charging stages and is

Table 4. Status Pins Charging State

STATUS PINS STATE		CC/CV	LEAD-ACID	CC
STAT1	STAT2	(MODE = 0V)	(MODE = $INTV_{CC}$)	(MODE = NC)
OFF	OFF	Not Charging — Standby or Shutdown Mode, I_{CS} < C/10	Not Charging — NTC/Bad Battery Fault or Shutdown	Not Charging — Standby or Shutdown Mode, I_{CS} < C/10
OFF	ON	Bad Battery Fault	Float Charge	Not Used
ON	OFF	Charging Cycle OK: Trickle Charge or I_{CS} > C/10	Absorption Charge	Charge Cycle OK
ON	ON	NTC Fault	Bulk Charge	NTC Fault

APPLICATIONS INFORMATION

high impedance during the float charging period and during NTC or bad battery faults. The STAT2 pin is pulled low during bulk and float charging stages, and is high impedance during the absorption charging stage and during NTC or bad battery faults.

The STAT1 and STAT2 status pins are binary coded, and signal following the table below, where ON indicates pin pulled low, and OFF indicates pin high impedance:

TIMER: C/10 Termination

The LTC4020 supports a low current based termination scheme. This termination mode is engaged by shorting the TIMER pin to ground.

When in CC/CV charge mode, a battery charge cycle terminates when the current output from the charger falls to below one-tenth the maximum charge current, or I_{CSMAX}, as programmed with R_{CS}. The C/10 threshold current corresponds to 5mV across R_{CS}.

During lead-acid charging, the LTC4020 initiates float charging when the absorption stage charge current is reduced to one-tenth of the programmed maximum current.

When charging in CC mode, the current source function remains active indefinitely.

There is no provision for bad battery detection if C/10 termination is used.

TIMER: Timed Functions

The LTC4020 supports timer based functions, where battery charge cycle control occurs after a specific amount of time elapses. Timer termination is engaged when a capacitor (C_{TIMER}) is connected from the TIMER pin to ground. C_{TIMER} for a desired end-of-cycle time (T_{EOC}) follows the relation:

$$C_{TIMER} = T_{EOC} \bullet 6.87 \bullet 10^{-2}\ (\mu F)$$

where T_{EOC} is hours.

A typical timer T_{EOC} for Li-Ion charge cycle termination is three hours, which requires a 0.2µF timer capacitor. The timer cycle starts when the charger transitions from constant-current to constant-voltage charging, thus, termination at the end of the timer cycle only occurs if the charging cycle was successful. When timer termination is used, the STAT1 status pin is pulled low during a charging cycle until the battery charge current falls below the C/10 threshold. The STAT1 pin stays high impedance with charge currents below C/10, but the charger continues to top off the battery until timer T_{EOC}, when the LTC4020 terminates the charging cycle and the PowerPath FET disconnects the battery from the DC/DC converter output.

During lead-acid charging, the timer acts as an absorption mode safety timer. Normally, the LTC4020 initiates float charging when the absorption stage charge current is reduced to one-tenth of the programmed maximum current, however, the maximum duration of absorption charging is limited by the timer. If the charge current does not fall to one-tenth of the programmed maximum current by T_{EOC}, the LTC4020 forces the battery charger to begin float mode charging. A typical timer T_{EOC} for lead-acid charging is six to eight hours, which is accommodated by a 0.47µF timer capacitor.

When charging in CC mode, after charge termination, once the timer reaches T_{EOC} and the charge cycle terminates, input power or SHDN must be cycled to initiate another battery charge cycle.

A bad battery detection function is available during CC/CV or lead-acid charging. This fault condition is achieved if the battery does not respond to preconditioning (V_{FB} < 1.75V), such that the charger remains in (or enters) precondition mode after one-eighth of the programmed T_{EOC} time. A bad battery fault halts the charging cycle, and the fault condition is reported on the status pins. The bad battery fault remains active until the battery voltage rises above the precondition threshold, or until power or SHDN is cycled.

Battery Temperature Qualified Charging: NTC

The LTC4020 can accommodate battery temperature monitoring by using an NTC (negative temperature coefficient) thermistor close to the battery pack. The temperature monitoring function is enabled by connecting a 10k, β = 3380 NTC thermistor from the NTC pin to ground. If the NTC function is not desired, leave the pin unconnected.

APPLICATIONS INFORMATION

The NTC pin sources 50µA, and monitors the voltage dropped across the 10k thermistor. When the voltage on this pin is above 1.35V (0°C) or below 0.3V (40°C), the battery temperature is out of range, and the LTC4020 triggers an NTC fault. The NTC fault condition remains until the voltage on the NTC pin corresponds to a temperature within the 0°C to 40°C range. Both hot and cold thresholds incorporate hysteresis that corresponds to 5°C.

If higher operational charging temperatures are desired, the temperature range can be expanded by adding series resistance to the 10k NTC resistor. Adding a 910Ω resistor will increase the effective HOT temperature threshold to 45°C. The effect of this additional resistance on the COLD threshold is negligible.

During an NTC fault, charging is halted and an NTC fault is indicated on the status pins. If timer termination is enabled, the timer count is suspended and held until the fault condition is relieved. The RNG/SS pin is also pulled low during this fault, to accommodate a graceful restart, in the event that a soft-start function is being incorporated (see DRNG/SS: Dynamic Current Limit Adjust and RNG/SS: Soft-Start section).

DC/DC CONVERTER: EXTERNAL COMPENSATION AND FILTERING COMPONENTS

The LTC4020 average current mode architecture employs two integrating compensation nodes. The current setting loop is compensated at the output of the current sense amplifier on the VC pin, generally with a series R-C network (R_{VC}, C_{VC}). The voltage generated on the VC pin is compared with an internal ramp, providing control of the converter duty cycle.

The voltage loop is compensated at the output of the error amplifier on the ITH pin, generally with a series R-C network (R_{ITH}, C_{ITH}). The voltage on the ITH pin is imposed onto the current sense amplifier, setting the current level to which the current loop will servo.

While determining compensation components, the LTC4020 should initially be configured to eliminate any functional contribution from the Battery Charger Section. This can be easily accomplished by connecting the NTC pin to ground, which disables all battery charging functions and puts the PowerPath FET into a high impedance state.

The current loop compensation (VC pin) transfer function crossover frequency is typically set to approximately one-half of the switching frequency; the voltage loop compensation (ITH pin) transfer function crossover frequency is typically set to approximately one-tenth of the switching frequency.

Compensation values must be tested at high and low input voltage operational limits, and also V_{IN} ~ V_{OUT}, so that stable operation during all switching modes (buck, boost, buck-boost) is verified.

If a network analyzer is not available for determining compensation values, use procedures as outlined in Application Note 19 for adjusting compensation.

VC pin compensation:

1. V_{NTC} = V_{FBMAX} = 0V
2. Fix V_{IN} at typical voltage.
3. Fix V_{OUT} at V_{FB} regulation voltage. A charged battery, battery simulator, or a 2-quadrant power supply can be used for V_{OUT}.
4. Impose 1V to 1.5V square wave (1kHz) on ITH pin
5. Monitor inductor current using current probe
6. Adjust compensation values as per Application Note 19 until response is critically damped

ITH pin compensation:

1. V_{NTC} = 0V (disables charger)
2. Bring to regulation (V_{FBMAX} = 2.75V)
3. Step load current on output (25% to 75% of I_{MAX})
4. Monitor V_{OUT} voltage
5. Adjust compensation values as per Application Note 19 until response is critically damped and settled in ~10 to 25 cycles
6. V_{NTC} = 0.8 (enable charger)
7. Exercise battery charger and verify stability in all modes

APPLICATIONS INFORMATION

BATTERY CHARGER FUNCTIONS: FILTERING COMPONENTS

Voltage Regulation Loop (V_{FB})

The charger voltage regulation loop monitors battery voltage, and as such is controlled by a very slow moving node. Battery ESR, however, can produce significant AC voltages due to ripple currents, which can cause unstable operation. This ESR effect can be reduced by adding a capacitor to the V_{FB} input, producing a low frequency pole.

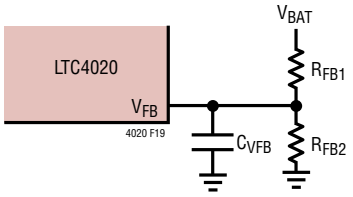


Figure 19. V_{FB} Ripple Suppression

Current Sense Regulation Loop (CSN, CSP)

The charger current regulation loop monitors and regulates battery charge current. Ripple voltage on the DC/DC converter output, however, gets directly imposed across the charger sense resistor, and can produce significant ripple currents. Large ripple currents can corrupt low level current sensing, and can also cause unstable operation. This ripple current effect can be greatly reduced by adding a capacitor (C_{CS}) across the CSN and CSP pins, producing a low frequency pole with the two 100Ω resistors that are required for those pins. The filter frequency is typically set to reduce voltage ripple across the current sense inputs at the CSP and CSN pins to less than $1mV_{P-P}$.

The ripple-reduction filter on the current sense inputs creates a phase shift in the charger current loop response, which can result in instability. A resistor (R_{CSZ}) in series with C_{CS} creates a zero that can be employed to recover phase margin. This zero setting resistor will reintroduce ripple error, so R_{CS} should be minimized. CSOUT can be coupled into ITH for a similar feedforward zero with $R_{CS} = 0$.

Current sense information, or differential voltage at the CSN to CSP pins, is amplified by a factor of 20 then output on pin CSOUT. This signal is compared to a reference voltage that is proportional to the maximum charge current at the input of a transconductance amplifier, which creates an error current that modulates the ITH compensation pin. A feedforward zero can be employed to recover phase margin by putting a capacitor from the CSOUT pin to the ITH pin (C_{CSOUT}). The output impedance of the CSOUT pin is ~100k, so if compensation requirements are appropriate, the C_{CSOUT} capacitor can perform double-duty as both the primary pole ITH capacitor along with a 100k zero-setting resistance, and as feed forward coupling from CSOUT to ITH.

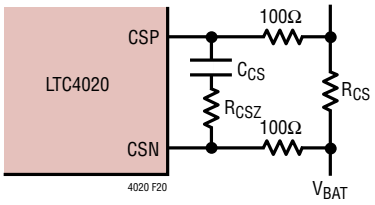


Figure 20. CSN/CSP Ripple Suppression

Instant-On/Ideal Diode Regulation Loop (BGATE)

The instant-on function regulates the voltage across the PowerPath FET by servoing the voltage at the BGATE pin. Gate capacitance of the PowerPath FET is typically sufficient to stabilize this loop. Additional capacitance can be added to the BGATE pin (C_{BGATE}) to stabilize the current foldback loop during instant-on operation if necessary:

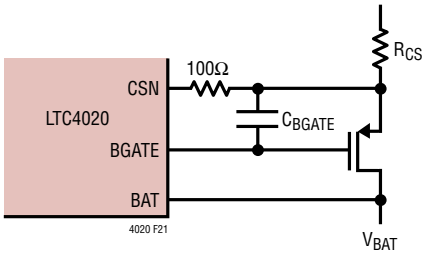


Figure 21. Instant-On/Ideal Diode Compensation

LAYOUT CONSIDERATIONS

The LTC4020 is typically used in designs that involve substantial switching transients. The switch drivers on the IC are designed to drive large capacitances and, as such, generate significant transient currents themselves. Supply bypass capacitor locations must be carefully considered to avoid corrupting the signal ground reference (SGND)

APPLICATIONS INFORMATION

used by the IC. Typically, high current paths and transients from the input supply and any local drive supplies must be kept isolated from SGND, to which sensitive circuits such as the error amp reference and the current sense circuits are referred.

Effective grounding can be achieved by considering switch current in the ground plane, and the return current paths of each respective bypass capacitor. The V_{IN} bypass return, $INTV_{CC}$ bypass return, and the sources of the ground-referred switch FETs carry PGND currents. SGND originates at the negative terminal of the V_{OUT} bypass capacitor, and is the small signal reference for the LTC4020.

Do not be tempted to run small traces to separate ground paths. A good ground plane is important as always, but PGND referred bypass elements must be oriented such that transient currents in these return paths do not corrupt the SGND reference.

During the dead time between synchronous switch and main switch conduction, the body diode of the synchronous FET conducts inductor current. Commutating the body diode requires a significant charge contribution from the main switch during initiation of main switch, creating a current spike in the main switch. At the instant the body diode commutates, a current discontinuity is created between the inductor and main switch, with parasitic inductance causing the switch node to transition in response to this discontinuity. High currents and excessive parasitic inductance can generate extremely fast $\delta V/\delta t$ times during this transition. These fast $\delta V/\delta t$ transitions can sometimes cause avalanche breakdown in the synchronous FET body diode, generating shoot-through currents via parasitic turn-on of the synchronous FET. Layout practices and component orientations that minimize parasitic inductance on the switched nodes is critical for reducing these effects.

Orient power path components such that current paths in the ground plane do not cross through signal ground areas. Power ground currents are controlled on the LTC4020 via the PGND pin, and this ground references the high current synchronous switch drive components, as well as the local $INTV_{CC}$ supply. It is important to keep PGND and SGND voltages consistent with each other. Separating these grounds with thin traces is not recommended.

When a ground referenced switch FET is turned off, gate drive currents return to the LTC4020 PGND pin from the switch FET source. The BOOST supply refresh surge currents also return through this same path. The switch FETs must be oriented such that these PGND return currents do not corrupt the SGND reference.

The high $\delta i/\delta t$ loop formed by the switch MOSFETs and the input capacitor (CV_{IN}) should have short wide traces to minimize high frequency noise and voltage stress from inductive ringing. Surface mount components are preferred to reduce parasitic inductances from component leads. Switch path currents can be controlled by orienting switch FETs, the switched inductor, and input and output decoupling capacitors in close proximity to each other. Locate the $INTV_{CC}$, BST1, and BST2 decoupling capacitors in close proximity to the IC. These capacitors carry the switch FET gate drive currents. Locate the small signal components away from high frequency switching nodes (TG1, BG1, TG2, BG2, SW1, SW2, BST1, BST2, and $INTV_{CC}$). High current switching nodes are oriented across the top of the LTC4020 package to simplify layout and prevent corruption of the SGND reference.

Locate the output and battery charger feedback resistors in close proximity to the LTC4020 and minimize the length of the high impedance feedback nodes.

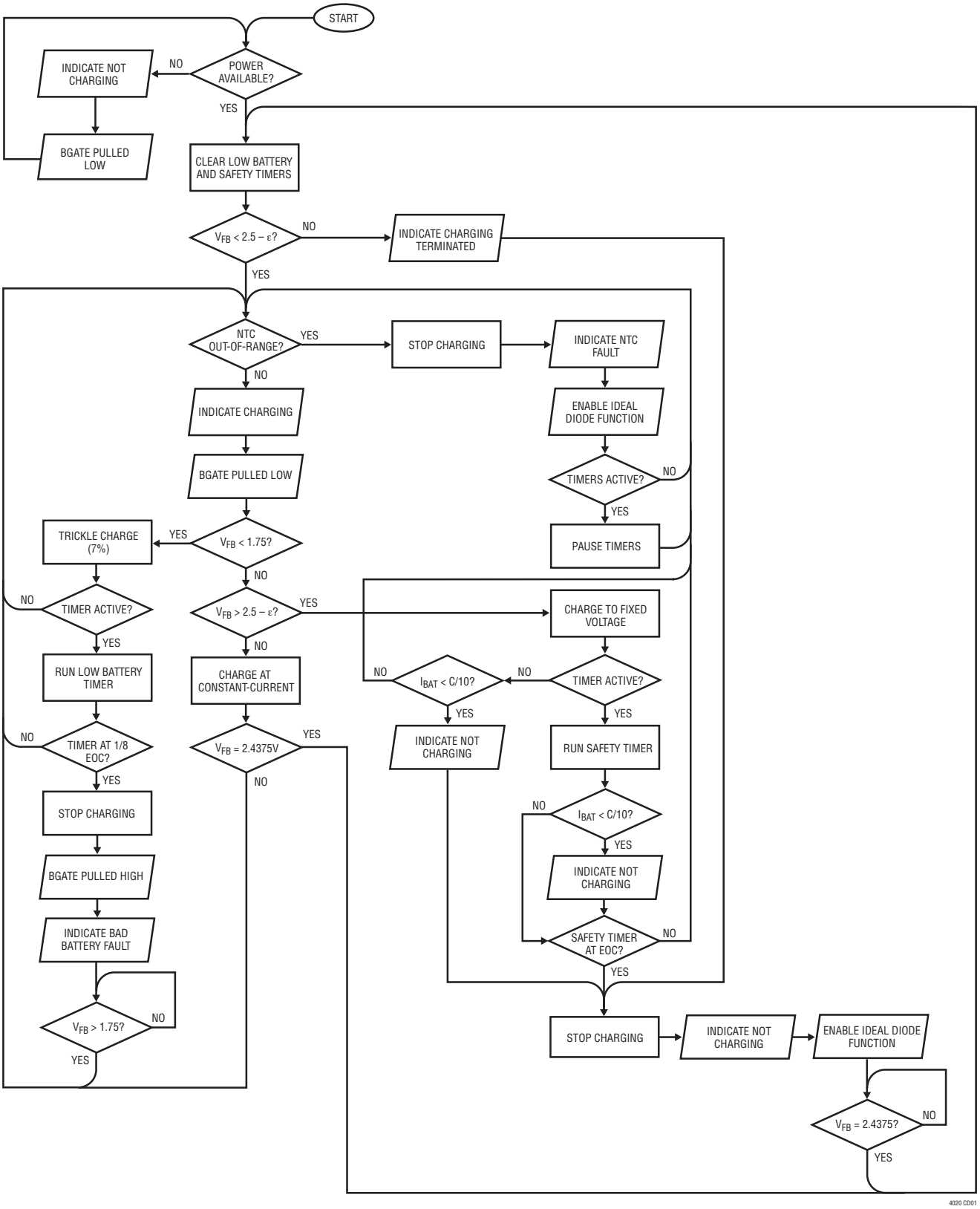
The $SENSV_{IN}$ and SENSTOP traces should be routed together and SENSBOT and SENSGND should be routed together. Keep these traces as short as possible, and avoid corruption of these lines by high current switching nodes.

The LTC4020 packaging has been designed to efficiently remove heat from the IC via the exposed pad on the backside of the package. The exposed pad is soldered to a copper footprint on the PCB. The exposed pad is electrically connected to SGND, so a good connection to a PCB ground plane effectively reduces the thermal resistance of the IC case to ambient air.

Please refer to Application Note 136, which discusses guidelines, techniques, and considerations for switching power supply PCB design and layout.

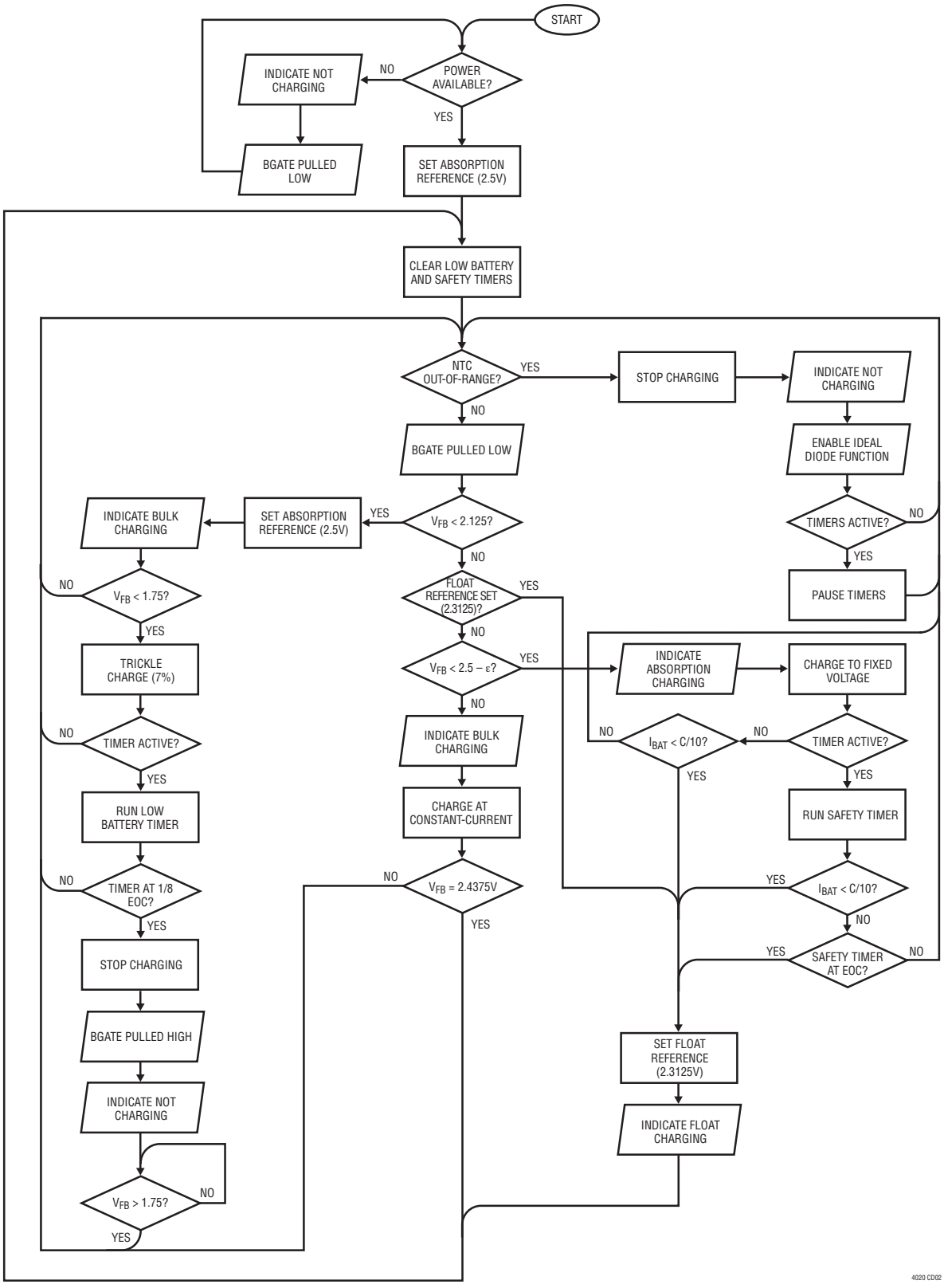
APPLICATIONS INFORMATION

LTC4020 Constant-Current/Constant-Voltage (CC/CV) Charging Diagram



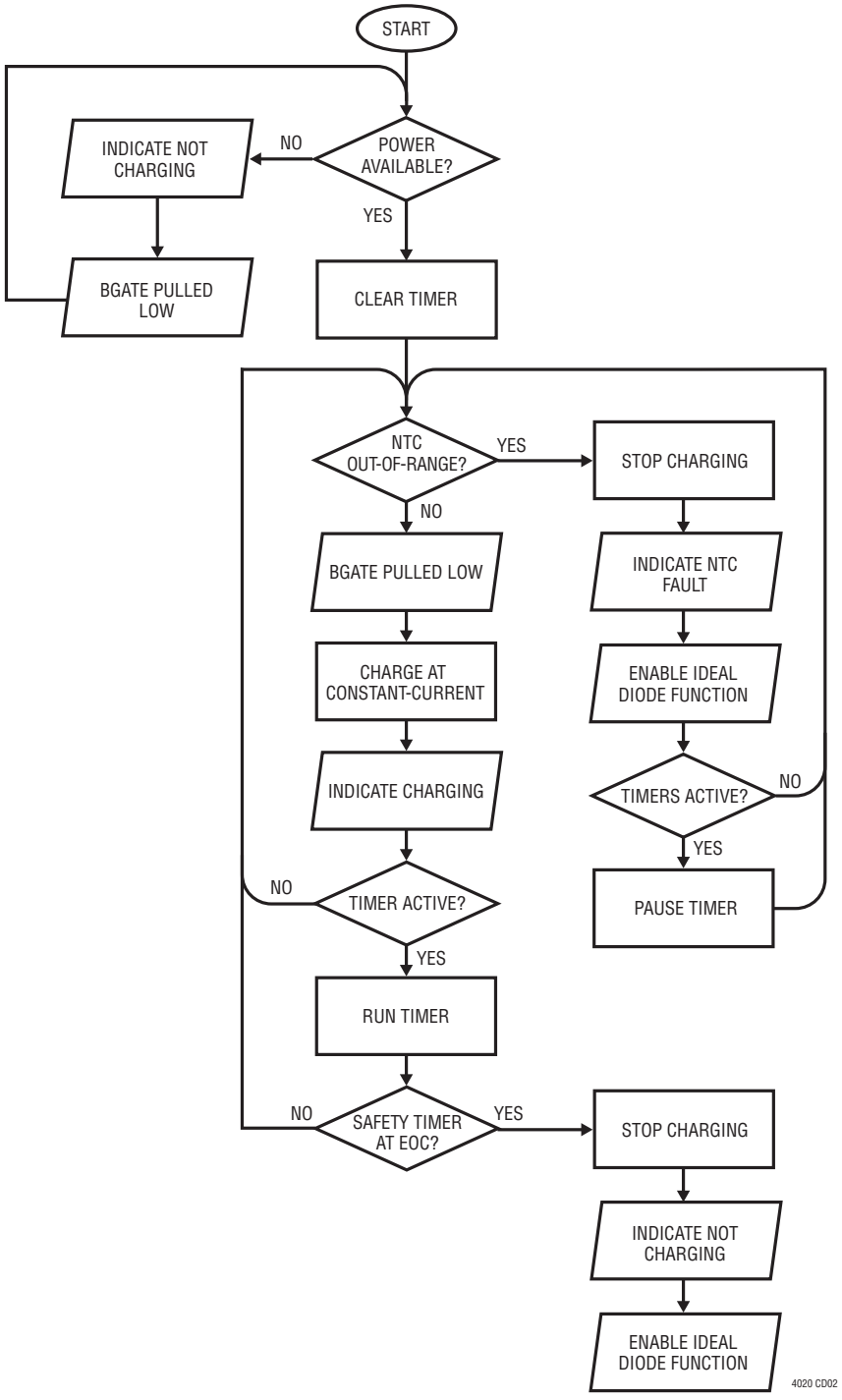
APPLICATIONS INFORMATION

LTC4020 Lead-Acid Charging Diagram



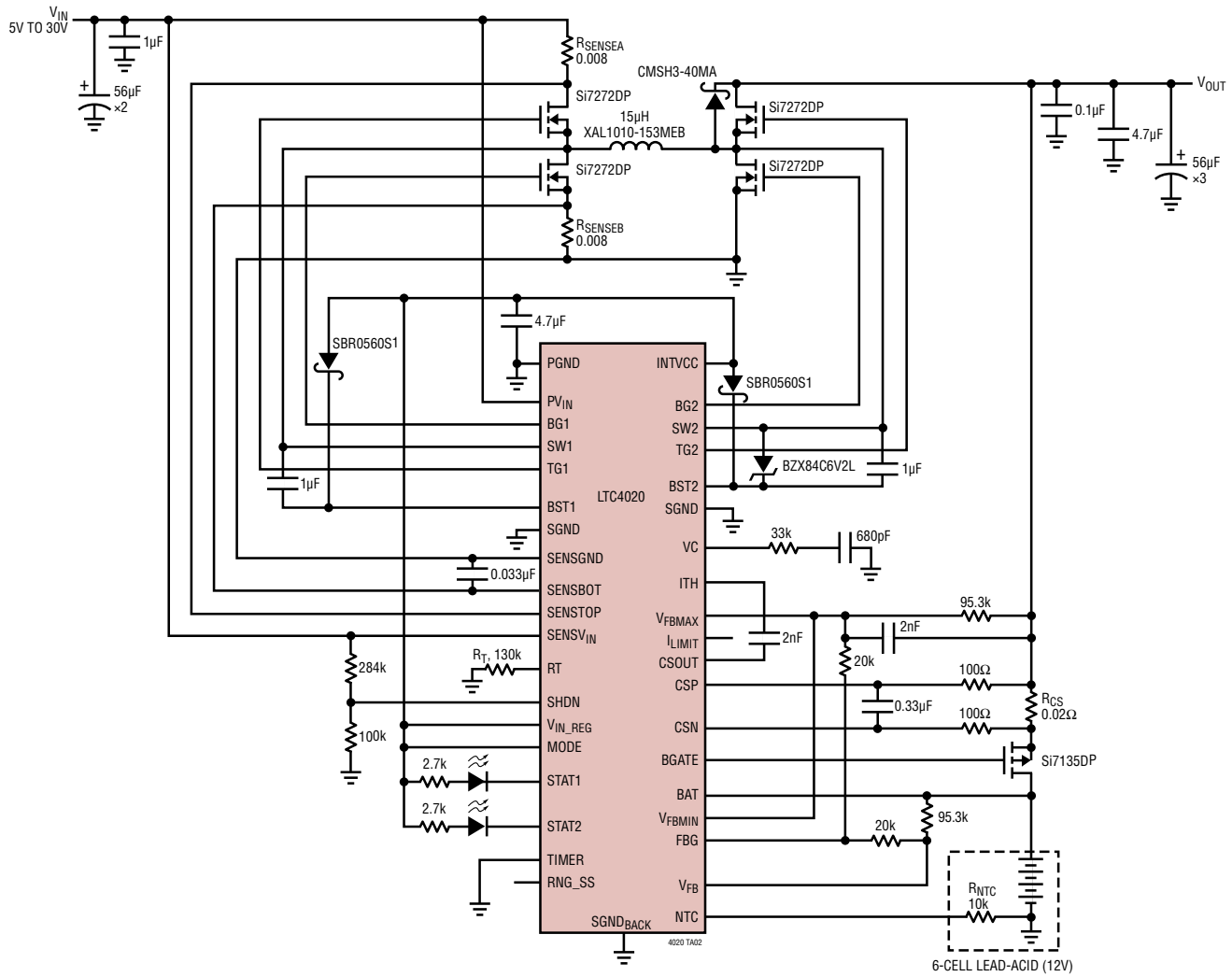
APPLICATIONS INFORMATION

LTC4020 Constant-Current Charging Diagram



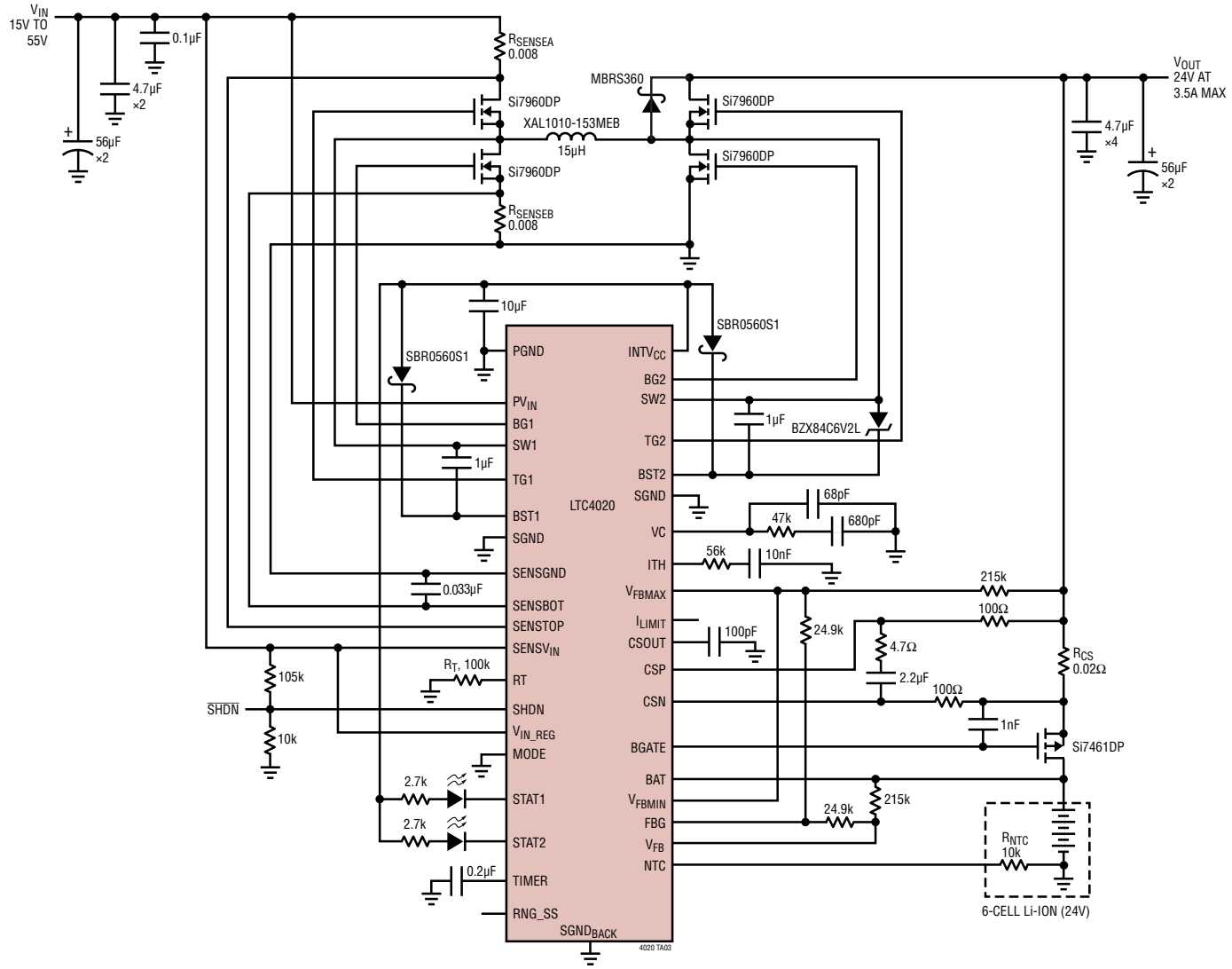
TYPICAL APPLICATION

5V to 30V to 6-cell lead-acid PowerPath charger/system supply. 6A inductor current limit with 2.5A battery charge current limit. Instant-on functionality incorporated for battery voltages below 12.25V, 14.4V absorption voltage, 13.3V float voltage,and 15.6V maximum output voltage (Instant-On and NTC fault only). Status pins light LEDs for visible charge-state monitoring



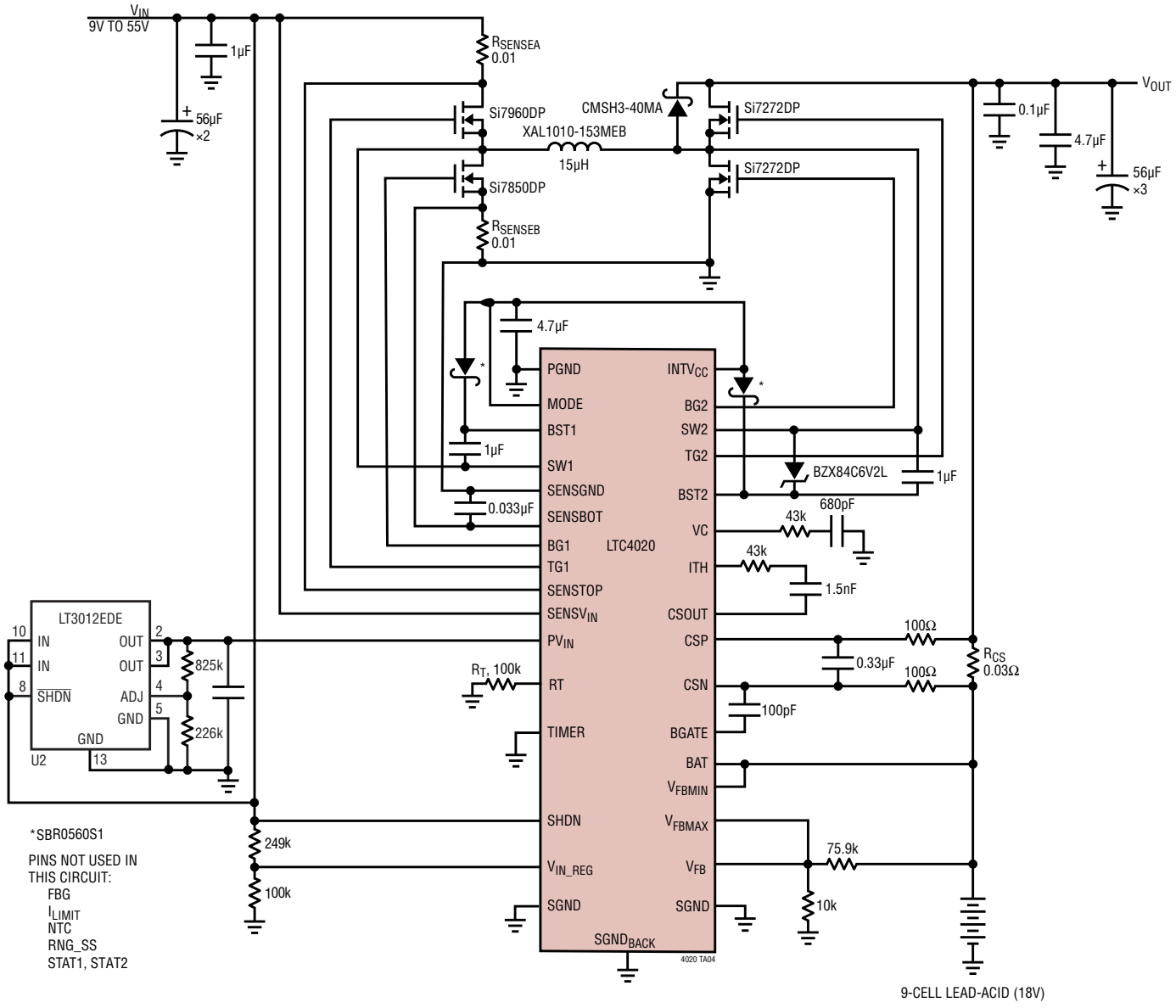
TYPICAL APPLICATION

15V to 55V to 6-cell Li-Ion PowerPath charger/system supply. 6A inductor current limit with 2.5A battery charge current limit. Instant-on functionality for battery voltages below 20.4V, 24V charge termination voltage, and 26.4V maximum output voltage. Status pins light LEDs for visible charge-state monitoring



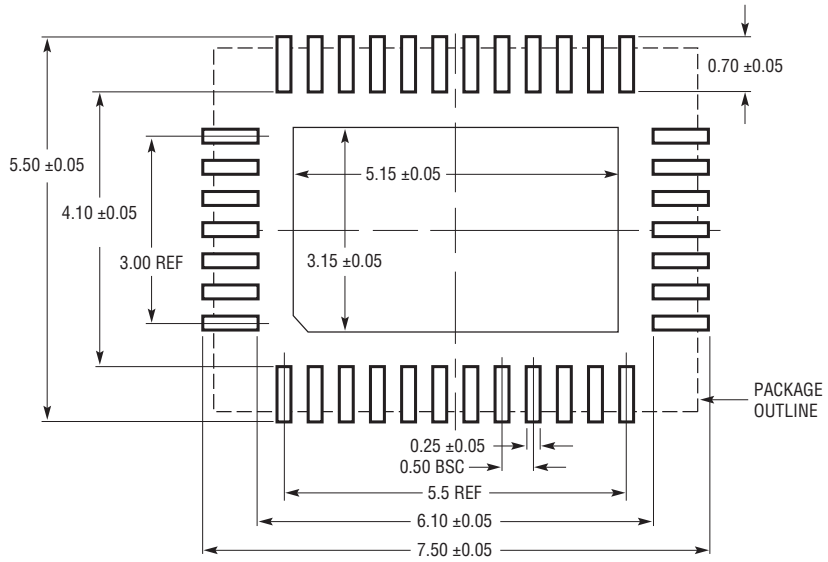
TYPICAL APPLICATION

9V to 55V to 9-cell lead-acid (18V) charger/system supply with no PowerPath. External 5V regulator for boosted supplies. 5A inductor current limit with 1.67A battery charge current limit. 21.5V absorption voltage output, 19.9V float voltage output

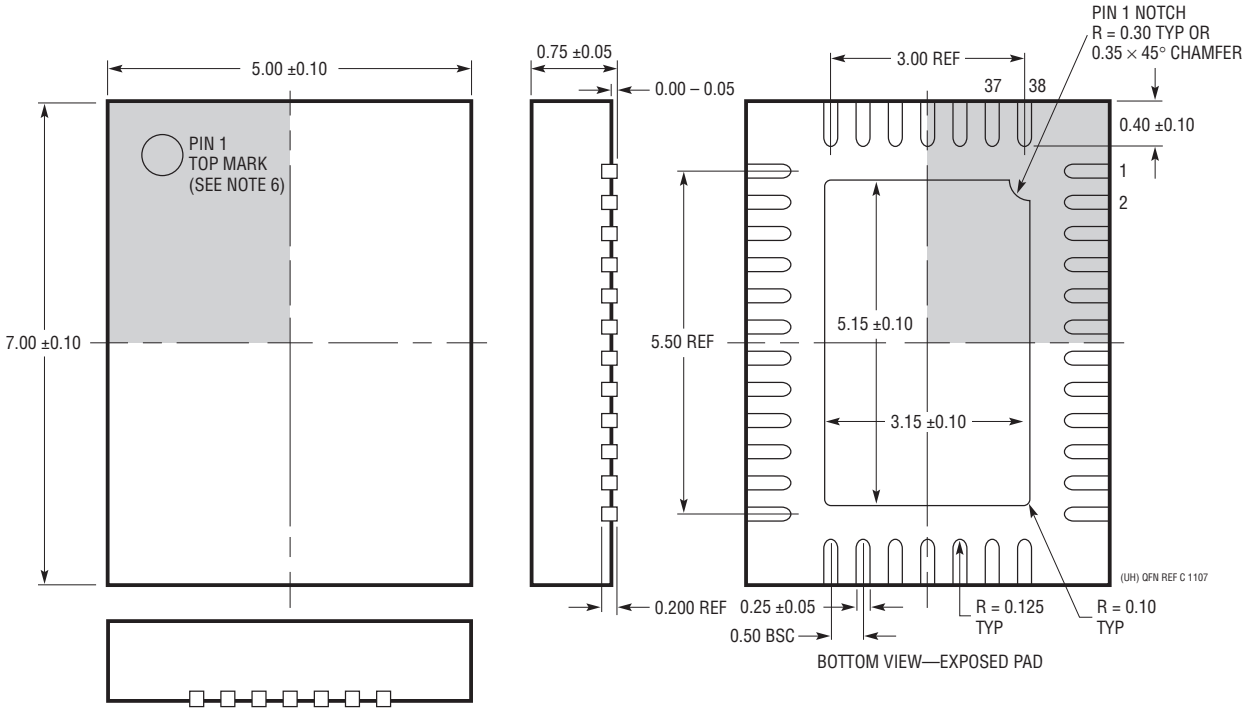


PACKAGE DESCRIPTION

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



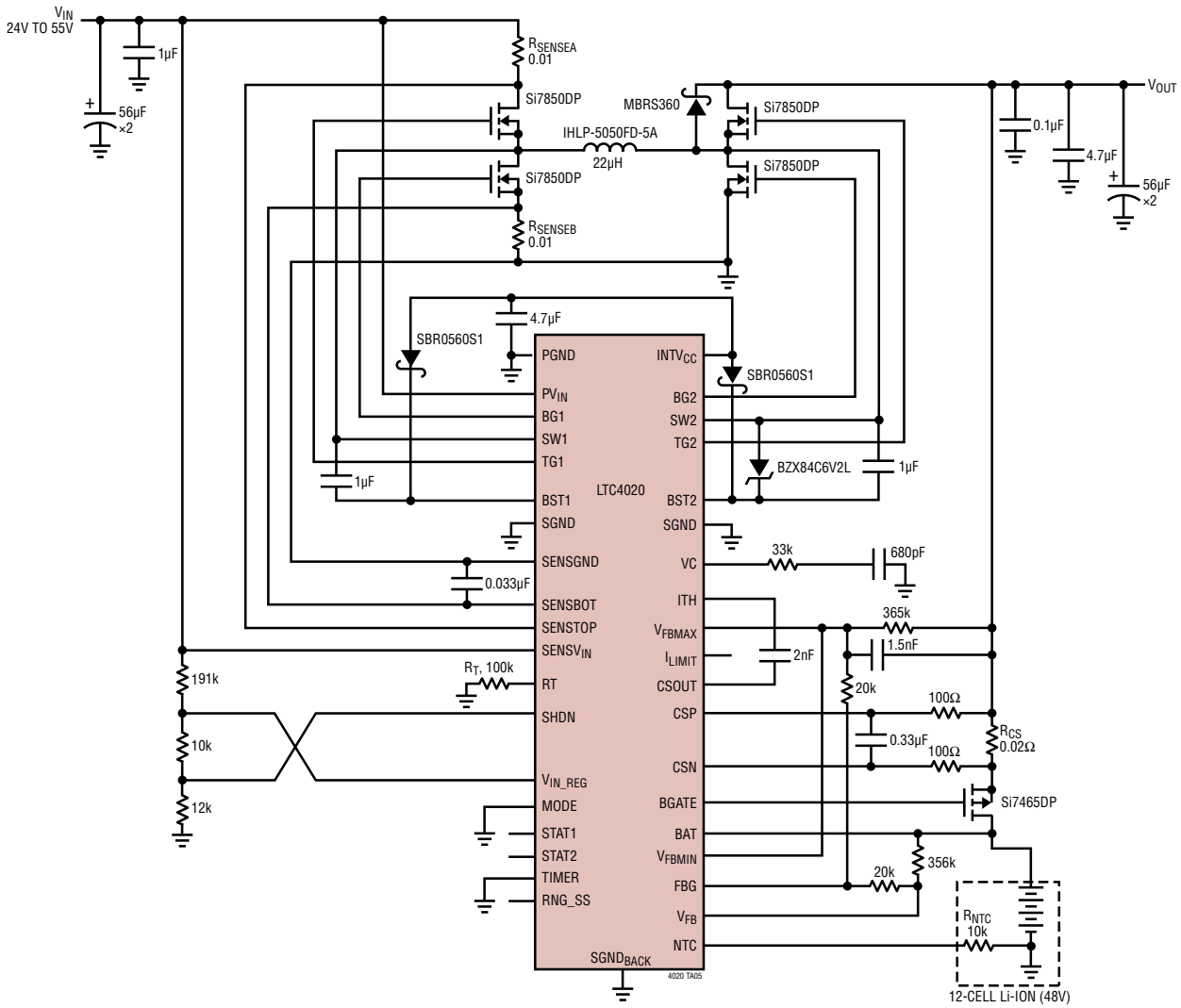
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/14	Changed V_{IN} to PV_{IN}. Modified $I_{SENSTOP}$ Operating Current spec and Error Amp Transconductance spec. Changed C/10 Detection Enable Units, C/10 Detection Hysteresis spec, and conditions for Gate Clamp Voltage. Changed Conditions for BGATE tests and conditions for Pin Current (Disabled) spec. Changed cathode to anode for BST1 and anode to cathode for BST1. Modified equations for T_{EOC} and T_{PRE} and associated TIMER text. Modified equations for R_{FB1}/R_{FB2} and R_{MIN1}/R_{MIN2}. Changed cathode to anode for BST2 and anode to cathode for BST2. Modified Error Amplified Transconductance. Modified step-up and step-down equations in Switch FET section. Modified C_{TIMER} equation and associated text. Modified Typical Applications circuit. Modified Typical Application circuit to 12-cell.	3-5 3 4 5 8 9 10 12 14 24 30 38 42
B	09/14	Added (Application Circuit on Page 37) to efficiency curve title. Added Ω unit to R_{FBG} specification. Changed $INTV_{CC}$ Short-Circuit Current Limit vs Temperature curve y-axis units to mA. Added text to the end of the NTC (Pin 16) section. Corrected formula: $(V_{OUTMAX}/2.75) – 1$. Changed BST1 on lower-right of block diagram to BST2; Insert (V_{SENS}) below 2mV near VC pin. Added 2V Zener diode symbol from NTC pin (cathode) to ground (anode). Added average to first line; changed Charge to Average Inductor in Figure 8 title. Changed inductor to charge. Added ground symbol to bottom of IC symbol (backside connection). Flipped PMOS symbol vertically (Si7461DP); add ground symbol to bottom of IC symbol (backside connection). Added ground symbol to bottom of IC symbol (backside connection). Moved connection of BZX84C6V2L anode from BG2 to SW2 (diode between BST2 and SW2); add ground symbol to bottom of IC symbol (backside connection).	1 5 6 10 12 14 15 23 28 37 38 39 42
C	09/15	Added pin names to Typical Application IC drawing. Added text to end of SENSBOT (5) Pin Functions section. Changed text in RNG/SS section: Inductor to Charge. Changed I_{LIMIT} text, ...pin, so maximum charge current... to ...pin, so maximum inductor current... Changed Operation section to a 0.47µF capacitor on the TIMER pin is typically used, which generates a 6.8-hour absorption stage safety timeout. Changed $C_{SENSBOT,SENSGND}$ to C_{SENSB}. Changed ...BGATE pin to ground to ...BGATE pit to CSN. Changed CSN to CSN. Replaced R_{CS} with R_{CSZ} in the text and in Figure 21. Replaced R_{SENSE} with R_{CS} in Figure 21. Replaced R_{SENSE} with R_{CS} in schematic.	1 8 9 12 20 22 28 32 37-39, 42
D	04/16	Modified bulk capacitance equation.	24
E	3/23	Fixed major formatting issues (renumbered figures, added table titles, fixed crossed references). Changed umho to µS and added RNG/SS pin specifications in the Electrical Characteristics table. Changed inductor to battery charge in the RNG/SS (Pin 15) description. Removed (V) in the absorption voltage equation. Modified the V_{FBMAX} (Pin 26) description. Modified the $INTV_{CC}$ (Pin 34) description. Changed µohm to µS in Figure 1 and Figure 2 (Block Diagrams). Modified second paragraph in the CC Charging Overview (MODE = NC) section. Changed high pass to low-pass in the Overcurrent Detection section. Changed cannot to must not. Changed Inductor Selection section (added I_{MAX} equation, modified L_{MIN} equations). Added C_{RSS} description to the P_{TR} equation description paragraph. Implemented major modifications to the External Power for BST1 and BST2 Supplies section. Corrected typical application schematic.	All 3 9 10 12 13 14-15 20 22 23 24 26 39

TYPICAL APPLICATION

Remote 24V to 55V (48V system) input to 12-cell Li-Ion (48V) PowerPath charger/system supply. 5A inductor current limit with 2.5A battery charge current limit. Minimum V_{IN} is 24V as input regulation limits voltage loss due to line impedance. Battery termination voltage is 48V with maximum output voltage of 52.8V. Instant-on functionality limits minimum regulated output voltage to 40.8V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3789	High Efficiency, Synchronous, 4-Switch Buck-Boost Controller	Improved LTC3780 with More Features
LT3845	High Voltage Synchronous Current Mode Step-Down Controller	For Medium/High Power, High Efficiency Supplies
LT3650	High Voltage 2A Monolithic Li-Ion Battery Charger	3mm × 3mm DFN-12 and MSOP-12 Packages
LT3651	High Voltage 4A Monolithic Li-Ion Battery Charger	4A Synchronous Version of LT3650 Family
LT3652/LT3652HV	Power Tracking 2A Battery Chargers	Multi-Chemistry, Onboard Termination
LTC4009	High Efficiency, Multi-Chemistry Battery Charger	Low Cost Version of LTC4008, 4mm × 4mm QFN-20
LTC4012	High Efficiency, Multi-Chemistry Battery Charger with PowerPath Control	Similar to LTC4009 Adding PowerPath Control
LT3741	High Power, Constant-Current, Constant-Voltage, Step-Down Controller	Thermally Enhanced 4mm × 4mm QFN and 20-Pin TSSOP
LT8705	80V_{IN}/V_{OUT} Synchronous Buck-Boost 4-Switch Controller	Single Inductor, TSSOP-38 and 5mm × 7mm QFN-38