# 60V Low $I_Q$, Triple Output, Buck/Buck/Boost Synchronous Controller

## FEATURES

- **Dual Buck Plus Single Boost Synchronous Controllers**
- **Wide Bias Input Voltage Range: 4.5V to 60V**
- **Outputs Remain in Regulation Through Cold Crank Down to a 2.2V Input Supply Voltage**
- **Buck and Boost Output Voltages Up to 60V**
- **Adjustable Gate Drive Level 5V to 10V (OPTI-DRIVE)**
- **No External Bootstrap Diodes Required**
- **Low Operating $I_Q$: 29µA (One Channel On)**
- **100% Duty Cycle for Boost Synchronous MOSFET**
- Phase-Lockable Frequency (75kHz to 850kHz)
- Programmable Fixed Frequency (50kHz to 900kHz)
- Very Low Dropout Operation: 99% Duty Cycle (Bucks)
- Low Shutdown $I_Q$: 3.6µA
- Fixed or Adjustable Boost Output Voltage Saves $I_Q$
- Small 38-Lead 5mm × 7mm QFN and TSSOP Packages
- AEC-Q100 Qualified for Automotive Applications

## APPLICATIONS

- Automotive Always-On and Start-Stop Systems
- Distributed DC Power Systems
- Multioutput Buck-Boost Applications

## DESCRIPTION

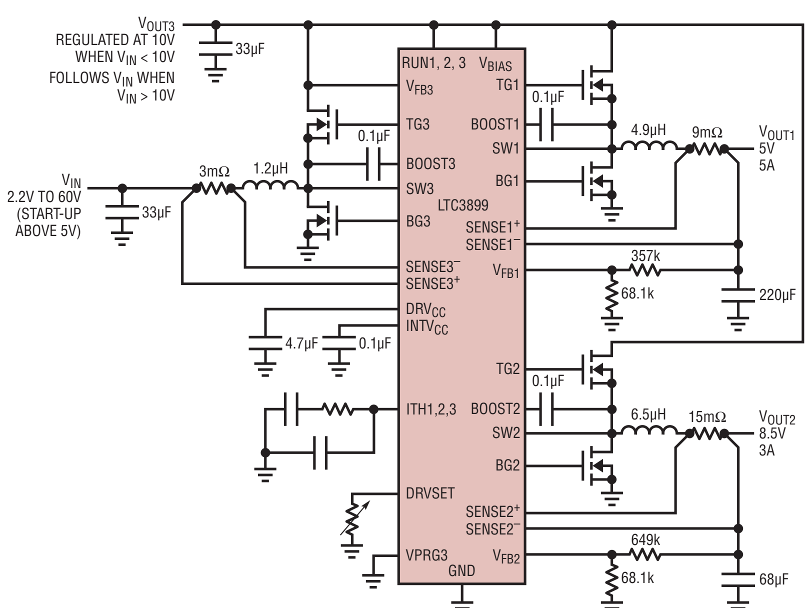
The LTC®3899 is a high performance triple output (buck/buck/boost) DC/DC switching regulator controller that drives all N-channel synchronous power MOSFET stages. The constant frequency current mode architecture allows a phase-lockable frequency of up to 850kHz. The LTC3899 operates from a wide 4.5V to 60V input supply range. When biased from the output of the boost converter or another auxiliary supply, the LTC3899 can operate from an input supply as low as 2.2V after start-up.

The gate drive for the LTC3899 can be programmed from 5V to 10V to allow the use of logic-level or standard-level FETs and to maximize efficiency. Internal switches in the top gate drivers eliminate the need for external bootstrap diodes. The 29µA no-load quiescent current extends operating run time in battery-powered systems. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

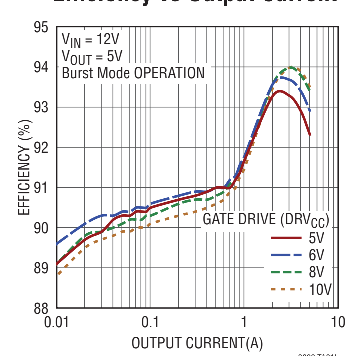


## TYPICAL APPLICATION

**High Efficiency Wide Input Range Dual 5V/8.5V Converter**




**Efficiency vs Output Current**

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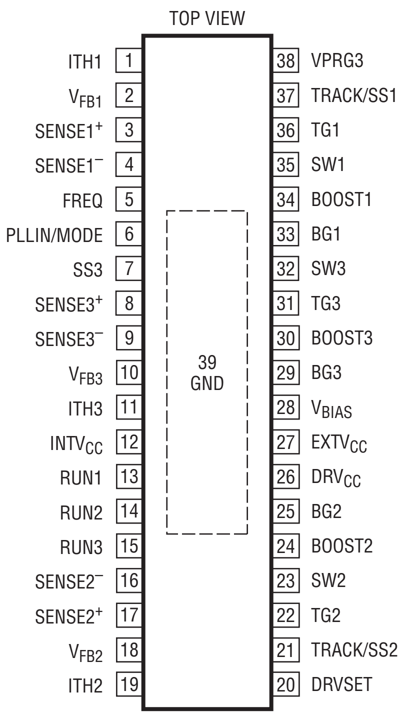
## ABSOLUTE MAXIMUM RATINGS (Notes 1, 3)

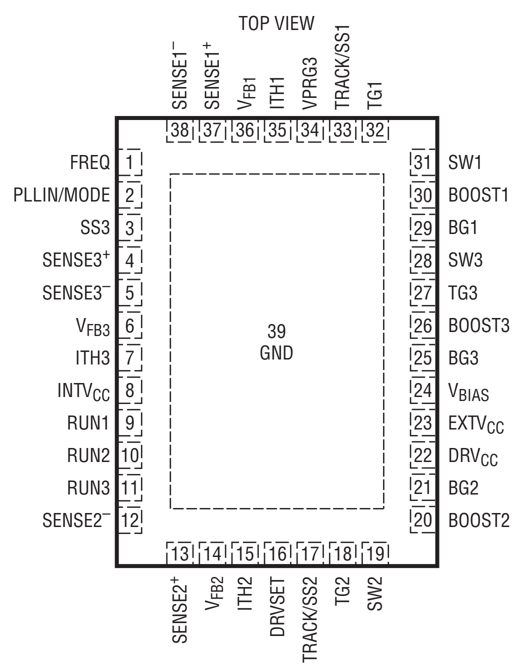
Bias Input Supply Voltage ($V_{BIAS}$) .............. –0.3V to 65V
Topside Driver Voltages
BOOST1, BOOST2, BOOST3 .................. –0.3V to 76V
Switch Voltage (SW1, SW2, SW3) ................ –5V to 70V
$DRV_{CC}$, (BOOST1-SW1), (BOOST2-SW2),
(BOOST3-SW3) .......................................... –0.3V to 11V
BG1, BG2, BG3, TG1, TG2, TG3 .......................... (Note 8)
RUN1, RUN2, RUN3 Voltages ..................... –0.3V to 65V
SENSE1⁺, SENSE2⁺, SENSE1⁻
SENSE2⁻ Voltages ..................................... –0.3V to 65V
SENSE3⁺, SENSE3⁻ Voltages ..................... –0.3V to 65V
PLLIN/MODE, FREQ, DRVSET Voltages ....... –0.3V to 6V
$EXTV_{CC}$ Voltage ........................................ –0.3V to 14V
ITH1, ITH2, ITH3, $V_{FB1}$, $V_{FB2}$ Voltages ......... –0.3V to 6V
$V_{FB3}$ Voltage ............................................. –0.3V to 65V
VPRG3, Voltage .......................................... –0.3V to 6V
TRACK/SS1, TRACK/SS2, SS3 Voltages ...... –0.3V to 6V
Operating Junction Temperature Range (Note 2)
LTC3899E, LTC3899I ......................... –40°C to 125°C
LTC3899H ......................................... –40°C to 150°C
LTC3899MP ...................................... –55°C to 150°C
Storage Temperature Range .................. –65°C to 150°C

## PIN CONFIGURATION




FE PACKAGE
38-LEAD PLASTIC TSSOP

$T_{JMAX}$ = 150°C, $θ_{JA}$ = 25°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB




UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN

$T_{JMAX}$ = 150°C, $θ_{JA}$ = 34°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

# ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3899EFE#PBF | LTC3899EFE#TRPBF | LTC3899FE | 38-Lead Plastic TSSOP | –40°C to 125°C |
| LTC3899IFE#PBF | LTC3899IFE#TRPBF | LTC3899FE | 38-Lead Plastic TSSOP | –40°C to 125°C |
| LTC3899HFE#PBF | LTC3899HFE#TRPBF | LTC3899FE | 38-Lead Plastic TSSOP | –40°C to 150°C |
| LTC3899MPFE#PBF | LTC3899MPFE#TRPBF | LTC3899FE | 38-Lead Plastic TSSOP | –55°C to 150°C |
| LTC3899EUHF#PBF | LTC3899EUHF#TRPBF | 3899 | 38-Lead (5mm × 7mm) Plastic QFN | –40°C to 125°C |
| LTC3899IUHF#PBF | LTC3899IUHF#TRPBF | 3899 | 38-Lead (5mm × 7mm) Plastic QFN | –40°C to 125°C |
| LTC3899HUHF#PBF | LTC3899HUHF#TRPBF | 3899 | 38-Lead (5mm × 7mm) Plastic QFN | –40°C to 150°C |
| LTC3899MPUHF#PBF | LTC3899MPUHF#TRPBF | 3899 | 38-Lead (5mm × 7mm) Plastic QFN | –55°C to 150°C |
| **AUTOMOTIVE PRODUCTS**** | | | | |
| LTC3899IFE#WPBF | LTC3899IFE#WTRPBF | LTC3899FE | 38-Lead Plastic TSSOP | –40°C to 125°C |
| LTC3899HFE#WPBF | LTC3899HFE#WTRPBF | LTC3899FE | 38-Lead Plastic TSSOP | –40°C to 150°C |
| LTC3899IUHF#WPBF | LTC3899IUHF#WTRPBF | 3899 | 38-Lead (5mm × 7mm) Plastic QFN | –40°C to 125°C |
| LTC3899HUHF#WPBF | LTC3899HUHF#WTRPBF | 3899 | 38-Lead (5mm × 7mm) Plastic QFN | –40°C to 150°C |

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

# ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 2) $V_{BIAS}$ = 12V, $V_{RUN1,2,3}$ = 5V, $V_{EXTVCC}$ = 0V, $V_{DRVSET}$ = 0V, VPRG3 = Float unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{BIAS}$ | Bias Input Supply Operating Voltage Range | | | 4.5 | | 60 | V |
| $V_{FB1,2}$ | Buck Regulated Feedback Voltage | (Note 4) ITH1,2 Voltage = 1.2V<br>0°C to 85°C | <br><br>● | <br>0.792<br>0.788 | <br>0.800<br>0.800 | <br>0.808<br>0.812 | <br>V<br>V |
| $V_{FB3}$ | Boost Regulated Feedback Voltage | (Note 4) ITH3 Voltage = 1.2V<br>VPRG3 = FLOAT<br>VPRG3 = 0V<br>VPRG3 = $INTV_{CC}$ | <br>●<br>●<br>● | <br>1.182<br>9.78<br>11.74 | <br>1.200<br>10.00<br>12.00 | <br>1.218<br>10.22<br>12.26 | <br>V<br>V<br>V |
| $I_{FB1,2}$ | Buck Feedback Current | (Note 4) | | | –2 | ±50 | nA |
| $I_{FB3}$ | Boost Feedback Current | (Note 4)<br>VPRG3 = FLOAT<br>VPRG3 = 0V<br>VPRG3 = $INTV_{CC}$ | | | <br>±0.01<br>4<br>5 | <br>±0.05<br>6<br>7 | <br>µA<br>µA<br>µA |
| $V_{REFLNREG}$ | Reference Voltage Line Regulation | (Note 4) $V_{BIAS}$ = 4.5V to 60V | | | 0.002 | 0.02 | %/V |
| $V_{LOADREG}$ | Output Voltage Load Regulation | (Note 4) Measured in Servo Loop, ∆ITH Voltage = 1.2V to 0.7V | ● | | 0.01 | 0.1 | % |
| | | (Note 4) Measured in Servo Loop, ∆ITH Voltage = 1.2V to 2V | ● | | –0.01 | –0.1 | % |
| $g_{m1,2,3}$ | Transconductance Amplifier $g_m$ | (Note 4) ITH1,2,3 = 1.2V, Sink/Source 5µA | | | 2 | | mmho |

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## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 2) $V_{BIAS}$ = 12V, $V_{RUN1,2,3}$ = 5V, $V_{EXTVCC}$ = 0V, $V_{DRVSET}$ = 0V, VPRG3 = Float unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_Q$ | Input DC Supply Current | (Note 5), $V_{DRVSET}$ = 0V | | | | | |
| | Pulse-Skipping or Forced Continuous Mode (One Channel On) | RUN1 = 5V and RUN2,3 = 0V or<br>RUN2 = 5V and RUN1,3 = 0V or<br>RUN3 = 5V and RUN1,2 = 0V,<br>$V_{FB1,2}$ = 0.83V (No Load), $V_{FB3}$ = 1.25V | | | 1.6<br>1.6<br>0.8 | | mA |
| | Pulse-Skipping or Forced Continuous Mode (All Channels On) | RUN1,2,3 = 5V, $V_{FB1,2}$ = 0.83V (No Load),<br>$V_{FB3}$ = 1.25V | | | 3 | | mA |
| | Sleep Mode (One Channel On, Buck) | RUN1 = 5V and RUN2,3 = 0V or<br>RUN2 = 5V and RUN1,3 = 0V<br>$V_{FB1,2}$ = 0.83V (No Load) | ● | | 29 | 55 | μA |
| | Sleep Mode (One Channel On, Boost) | RUN3 = 5V and RUN1,2 = 0V, $V_{FB3}$ = 1.25V | | | 29 | 50 | μA |
| | Sleep Mode (Buck and Boost Channel On) | RUN1 = 5V and RUN2 = 0V or<br>RUN2 = 5V and RUN1 = 0V, RUN3 = 5V,<br>$V_{FB1,2}$ = 0.83V (No Load), $V_{FB3}$ = 1.25V | | | 34 | 55 | μA |
| | Sleep Mode (All Three Channels On) | RUN1,2,3 = 5V, $V_{FB1,2}$ = 0.83V (No Load),<br>$V_{FB3}$ = 1.25V | | | 39 | 60 | μA |
| | Shutdown | RUN1,2,3 = 0V | | | 3.6 | 10 | μA |
| UVLO | Undervoltage Lockout | $DRV_{CC}$ Ramping Up<br>DRVSET = 0V or $R_{DRVSET}$ ≤ 100kΩ<br>DRVSET = $INTV_{CC}$ | <br>●<br>● | | <br>4.0<br>7.5 | <br>4.2<br>7.8 | <br>V<br>V |
| | | $DRV_{CC}$ Ramping Down<br>DRVSET = 0V or $R_{DRVSET}$ ≤ 100kΩ<br>DRVSET = $INTV_{CC}$ | <br>●<br>● | <br>3.6<br>6.4 | <br>3.8<br>6.7 | <br>4.0<br>7.0 | <br>V<br>V |
| $V_{OVL1,2}$ | Buck Feedback Overvoltage Protection | Measured at $V_{FB1,2}$ Relative to Regulated $V_{FB1,2}$ | | 7 | 10 | 13 | % |
| $I_{SENSE1,2+}$ | $SENSE^+$ Pin Current | Bucks (Channels 1 and 2) | | | | ±1 | μA |
| $I_{SENSE3+}$ | $SENSE^+$ Pin Current | Boost (Channel 3) | | | 170 | | μA |
| $I_{SENSE1,2-}$ | $SENSE^-$ Pins Current | Bucks (Channels 1 and 2)<br>$V_{OUT1,2}$ < $V_{INTVCC}$ – 0.5V<br>$V_{OUT1,2}$ > $V_{INTVCC}$ + 0.5V | | | <br><br>700 | <br>±1<br> | <br>μA<br>μA |
| $I_{SENSE3-}$ | $SENSE^-$ Pin Current | Boost (Channel 3) $V_{SENSE+}$, $V_{SENSE-}$ = 12V | | | | ±1 | μA |
| $DF_{MAX(TG)}$ | Maximum Duty Factor for TG | Bucks (Channels 1,2) in Dropout, FREQ = 0V<br>Boost (Channel 3) in Overvoltage | | 97.5 | 99<br>100 | | %<br>% |
| $DF_{MAX(BG)}$ | Maximum Duty Factor for BG | Bucks (Channels 1,2) in Overvoltage<br>Boost (Channel 3) | | | 100<br>96 | | %<br>% |
| $I_{TRACK/SS1,2}$ | Soft-Start Charge Current | $V_{TRACK/SS1,2}$ = 0V | | 8 | 10 | 12 | μA |
| $I_{SS}$ | Soft-Start Charge Current | $V_{SS3}$ = 0V | | 8 | 10 | 12 | μA |
| $V_{RUN1,2,3}$ ON | RUN Pin On Threshold | $V_{RUN1}$, $V_{RUN2}$, $V_{RUN3}$ Rising | ● | 1.22 | 1.275 | 1.33 | V |
| $V_{RUN1,2,3}$ Hyst | RUN Pin Hysteresis | | | | 75 | | mV |
| $V_{SENSE(MAX)}$ | Maximum Current Sense Threshold | $V_{FB1,2}$ = 0.7V, $V_{SENSE1,2-}$ = 3.3V,<br>$V_{FB3}$ = 1.1V, $V_{SENSE3+}$ = 12V | ● | 65 | 75 | 85 | mV |
| $V_{SENSE(CM)}$ | SENSE3 Pins Common Mode Range (BOOST Converter Input Supply Voltage) | | | 2.2 | | 60 | V |
| **Gate Driver** | | | | | | | |
| TG1,2,3 | Pull-Up On-Resistance<br>Pull-Down On-Resistance | $V_{DRVSET}$ = $INTV_{CC}$ | | | 2.2<br>1.0 | | Ω<br>Ω |
| BG1,2,3 | Pull-Up On-Resistance<br>Pull-Down On-Resistance | $V_{DRVSET}$ = $INTV_{CC}$ | | | 2.2<br>1.0 | | Ω<br>Ω |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 2) $V_{BIAS}$ = 12V, $V_{RUN1,2,3}$ = 5V, $V_{EXTVCC}$ = 0V, $V_{DRVSET}$ = 0V, VPRG3 = Float unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| BDSW1,2,3 | BOOST to $DRV_{CC}$ Switch On-Resistance | $V_{SW}$ = 0V, $V_{DRVSET}$ = $INTV_{CC}$ | | | 3.7 | | Ω |
| <br>TG1,2,3 $t_r$<br>TG1,2,3 $t_f$ | TG Transition Time:<br>Rise Time<br>Fall Time | (Note 6) $V_{DRVSET}$ = $INTV_{CC}$<br>$C_{LOAD}$ = 3300pF<br>$C_{LOAD}$ = 3300pF | | | <br>25<br>15 | | <br>ns<br>ns |
| <br>BG1,2,3 $t_r$<br>BG1,2,3 $t_f$ | BG Transition Time:<br>Rise Time<br>Fall Time | (Note 6) $V_{DRVSET}$ = $INTV_{CC}$<br>$C_{LOAD}$ = 3300pF<br>$C_{LOAD}$ = 3300pF | | | <br>25<br>15 | | <br>ns<br>ns |
| TG1,2/BG1,2 $t_{1D}$ | Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time | $C_{LOAD}$ = 3300pF Each Driver, $V_{DRVSET}$ = $INTV_{CC}$ | | | 55 | | ns |
| BG1,2/TG1,2 $t_{1D}$ | Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time | $C_{LOAD}$ = 3300pF Each Driver, $V_{DRVSET}$ = $INTV_{CC}$ | | | 50 | | ns |
| TG3/BG3 $t_{1D}$ | CH3 Top Gate Off to Bottom Gate On Delay Bottom Switch-On Delay Time | $C_{LOAD}$ = 3300pF Each Driver, $V_{DRVSET}$ = $INTV_{CC}$ | | | 85 | | ns |
| BG3/TG3 $t_{1D}$ | CH3 Bottom Gate Off to Top Gate On Delay Synchronous Switch-On Delay Time | $C_{LOAD}$ = 3300pF Each Driver, $V_{DRVSET}$ = $INTV_{CC}$ | | | 80 | | ns |
| $t_{ON(MIN)1,2}$ | Buck Minimum On-Time | (Note 7) $V_{DRVSET}$ = $INTV_{CC}$ | | | 80 | | ns |
| $t_{ON(MIN)3}$ | Boost Minimum On-Time | (Note 7) $V_{DRVSET}$ = $INTV_{CC}$ | | | 120 | | ns |
| **$DRV_{CC}$ Linear Regulator** | | | | | | | |
| $V_{DRVCC(INT)}$ | $DRV_{CC}$ Voltage from Internal $V_{BIAS}$ LDO | $V_{EXTVCC}$ = 0V<br>7V < $V_{BIAS}$ < 60V, DRVSET = 0V<br>11V < $V_{BIAS}$ < 60V, DRVSET = $INTV_{CC}$ | | <br>5.8<br>9.6 | <br>6.0<br>10.0 | <br>6.2<br>10.4 | <br>V<br>V |
| $V_{LDOREG(INT)}$ | $DRV_{CC}$ Load Regulation from $V_{BIAS}$ LDO | $I_{CC}$ = 0mA to 50mA, $V_{EXTVCC}$ = 0V | | | 0.9 | 2.0 | % |
| $V_{DRVCC(EXT)}$ | $DRV_{CC}$ Voltage from Internal $EXTV_{CC}$ LDO | 7V < $V_{EXTVCC}$ < 13V, DRVSET = 0V<br>11V < $V_{EXTVCC}$ < 13V, DRVSET = $INTV_{CC}$ | | 5.8<br>9.6 | 6.0<br>10.0 | 6.2<br>10.4 | V<br>V |
| $V_{LDOREG(EXT)}$ | $DRV_{CC}$ Load Regulation from Internal $EXTV_{CC}$ LDO | $I_{CC}$ = 0mA to 50mA, $V_{EXTVCC}$ = 8.5V, $V_{DRVSET}$ = 0V | | | 0.7 | 2.0 | % |
| $V_{EXTVCC}$ | $EXTV_{CC}$ LDO Switchover Voltage | $EXTV_{CC}$ Ramping Positive<br>DRVSET = 0V or $R_{DRVSET}$ ≤ 100kΩ<br>DRVSET = $INTV_{CC}$ | | <br>4.5<br>7.4 | <br>4.7<br>7.7 | <br>4.9<br>8.0 | <br>V<br>V |
| $V_{LDOHYS}$ | $EXTV_{CC}$ Hysteresis | | | | 250 | | mV |
| $V_{DRVCC(50kΩ)}$ | Programmable $DRV_{CC}$ | $R_{DRVSET}$ = 50kΩ, $V_{EXTVCC}$ = 0V | | | 5.0 | | V |
| $V_{DRVCC(70kΩ)}$ | Programmable $DRV_{CC}$ | $R_{DRVSET}$ = 70kΩ, $V_{EXTVCC}$ = 0V | | 6.4 | 7.0 | 7.6 | V |
| $V_{DRVCC(90kΩ)}$ | Programmable $DRV_{CC}$ | $R_{DRVSET}$ = 90kΩ, $V_{EXTVCC}$ = 0V | | | 9.0 | | V |
| **Oscillator and Phase-Locked Loop** | | | | | | | |
| $f_{25kΩ}$ | Programmable Frequency | $R_{FREQ}$ =25kΩ, PLLIN/MODE = DC Voltage | | | 105 | | kHz |
| $f_{65kΩ}$ | Programmable Frequency | $R_{FREQ}$ = 65kΩ, PLLIN/MODE = DC Voltage | | 375 | 440 | 505 | kHz |
| $f_{105kΩ}$ | Programmable Frequency | $R_{FREQ}$ = 105kΩ, PLLIN/MODE = DC Voltage | | | 835 | | kHz |
| $f_{LOW}$ | Low Fixed Frequency | $V_{FREQ}$ = 0V, PLLIN/MODE = DC Voltage | | 320 | 350 | 380 | kHz |
| $f_{HIGH}$ | High Fixed Frequency | $V_{FREQ}$ = $INTV_{CC}$, PLLIN/MODE = DC Voltage | | 485 | 535 | 585 | kHz |
| $f_{SYNC}$ | Synchronizable Frequency | PLLIN/MODE = External Clock | ● | 75 | | 850 | kHz |
| PLLIN $V_{IH}$<br>PLLIN $V_{IL}$ | PLLIN/MODE Input High Level<br>PLLIN/MODE Input Low Level | PLLIN/MODE = External Clock<br>PLLIN/MODE = External Clock | ●<br>● | 2.5 | | <br>0.5 | V<br>V |
| **BOOST3 Charge Pump** | | | | | | | |
| $I_{BST3}$ | BOOST3 Charge Pump Available Output Current | FREQ = 0V, PLLIN/MODE = $INTV_{CC}$<br>$V_{BOOST3}$ = 16.5V, $V_{SW3}$ = 12V<br>$V_{BOOST3}$ = 19V, $V_{SW3}$ = 12V | | | <br>75<br>35 | | <br>µA<br>µA |

# ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3899 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3899E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3899I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3899H is guaranteed over the –40°C to 150°C operating junction temperature range, and the LTC3899MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature ($T_J$, in °C) is calculated from the ambient temperature ($T_A$, in °C) and power dissipation ($P_D$, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where $\theta_{JA}$ = 34°C/W for the QFN package and where $\theta_{JA}$ = 25°C/W for the TSSOP package.

**Note 3:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

**Note 4:** The LTC3899 is tested in a feedback loop that servos $V_{ITH1,2,3}$ to a specified voltage and measures the resultant $V_{FB1,2,3}$. The specification at 85°C is not tested in production and is assured by design, characterization and correlation to production testing at other temperatures (125°C for the LTC3899E and LTC3899I, 150°C for the LTC3899H and LTC3899MP). For the LTC3899I and LTC3899H, the specification at 0°C is not tested in production and is assured by design, characterization and correlation to production testing at –40°C. For the LTC3899MP, the specification at 0°C is not tested in production and is assured by design, characterization and correlation to production testing at –55°C.

**Note 5:** Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications information.

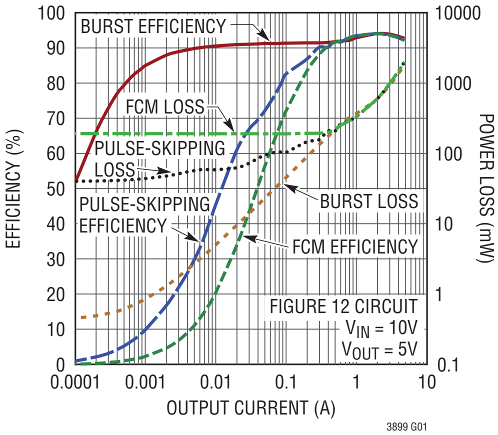
**Note 6:** Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels

**Note 7:** The minimum on-time condition is specified for an inductor peak-to-peak ripple current >40% of $I_{MAX}$ (See Minimum On-Time Considerations in the Applications Information section).

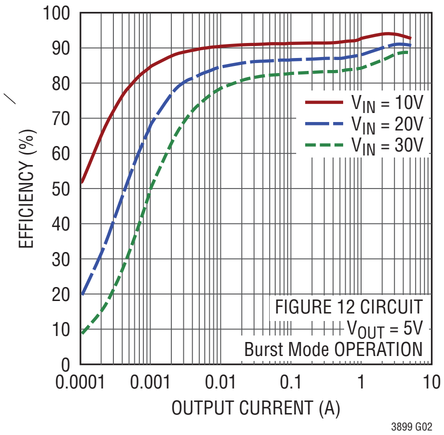
**Note 8:** Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

## TYPICAL PERFORMANCE CHARACTERISTICS

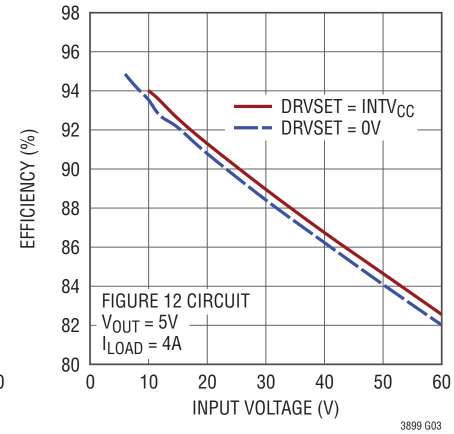
**Efficiency and Power Loss vs Output Current (Buck)**



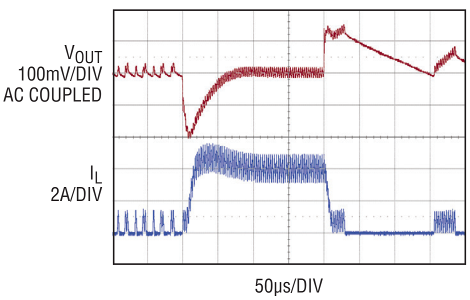

**Efficiency vs Output Current (Buck)**




**Efficiency vs Input Voltage (Buck)**

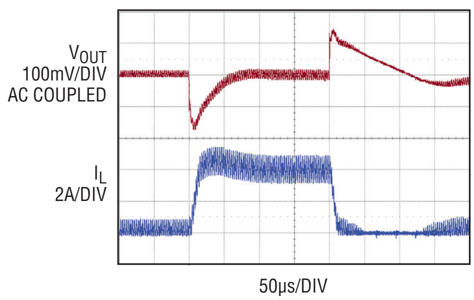



**Load Step (Buck) Burst Mode Operation**



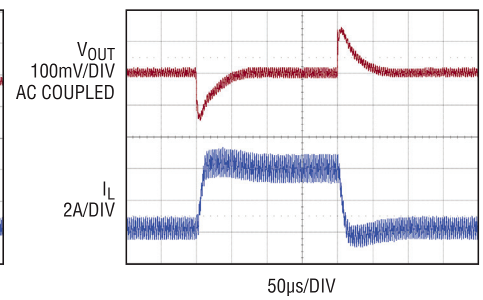

$V_{IN}$ = 12V
$V_{OUT}$ = 5V
FIGURE 12 CIRCUIT

**Load Step (Buck) Pulse-Skipping Mode**



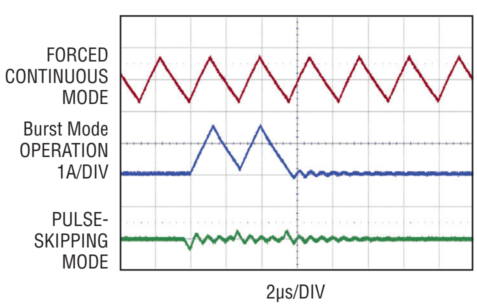

$V_{IN}$ = 12V
$V_{OUT}$ = 5V
FIGURE 12 CIRCUIT

**Load Step (Buck) Forced Continuous Mode**




$V_{IN}$ = 12V
$V_{OUT}$ = 5V
FIGURE 12 CIRCUIT

**Inductor Current at Light Load (Buck)**




$V_{IN}$ = 12V
$V_{OUT}$ = 5V
$I_{LOAD}$ = 1mA
FIGURE 12 CIRCUIT

**Soft Start-Up (Buck)**

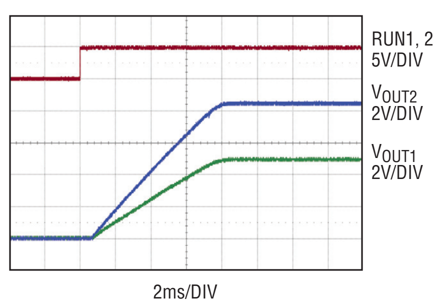
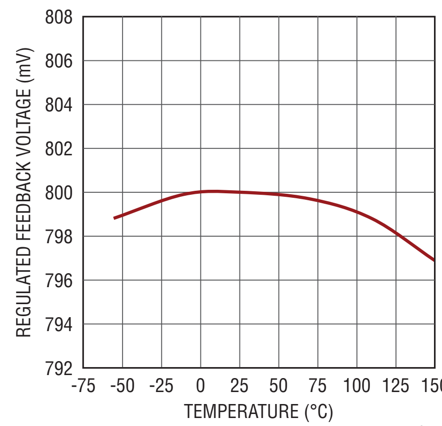


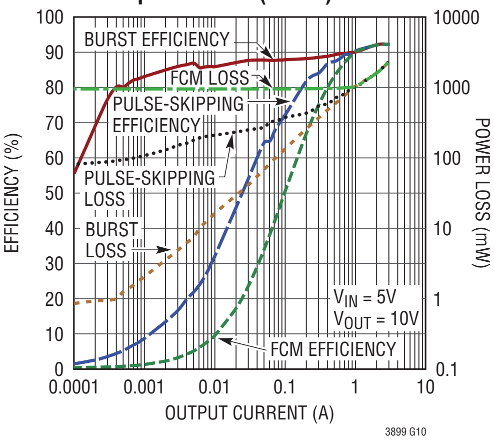

FIGURE 12 CIRCUIT

**Buck Regulated Feedback Voltage vs Temperature**

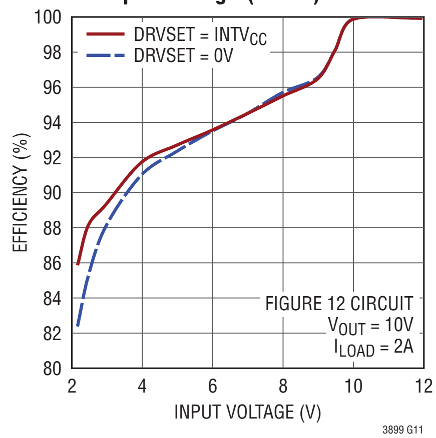


## TYPICAL PERFORMANCE CHARACTERISTICS

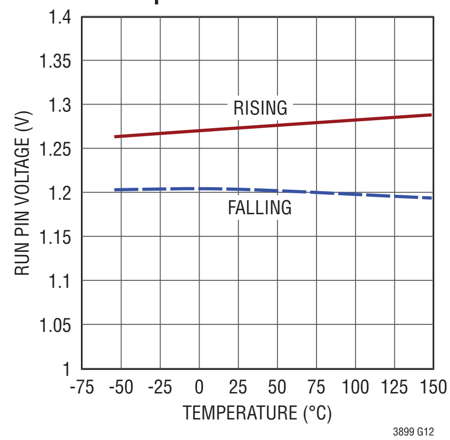
### Efficiency and Power Loss vs Output Current (Boost)



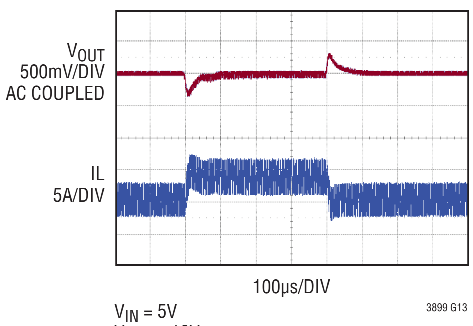

### Efficiency vs Input Voltage (Boost)




### Shutdown (RUN) Threshold vs Temperature

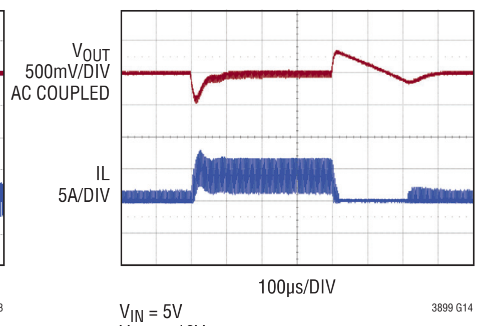



### Load Step (Boost) Forced Continuous Mode



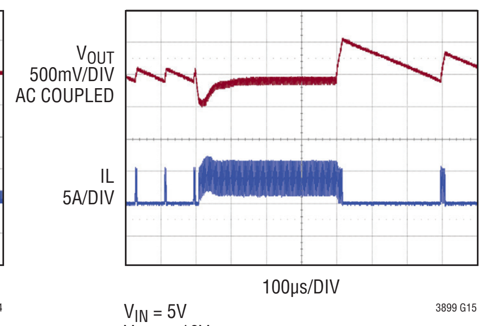

$V_{IN}$ = 5V
$V_{OUT}$ = 10V
FIGURE 12 CIRCUIT

### Load Step (Boost) Pulse-Skipping Mode



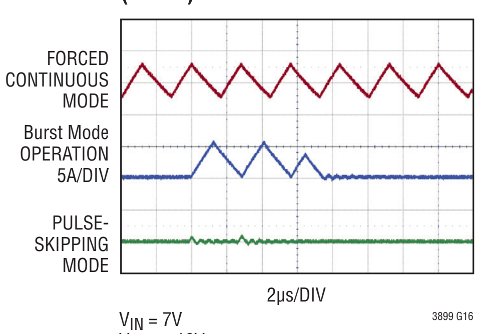

$V_{IN}$ = 5V
$V_{OUT}$ = 10V
FIGURE 12 CIRCUIT

### Load Step (Boost) Burst Mode Operation




$V_{IN}$ = 5V
$V_{OUT}$ = 10V
FIGURE 12 CIRCUIT

### Inductor Current at Light Load (Boost)




$V_{IN}$ = 7V
$V_{OUT}$ = 10V
$I_{LOAD}$ = 1mA
FIGURE 12 CIRCUIT

### Soft Start-Up (Boost)

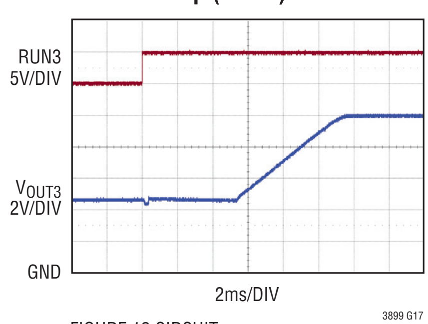
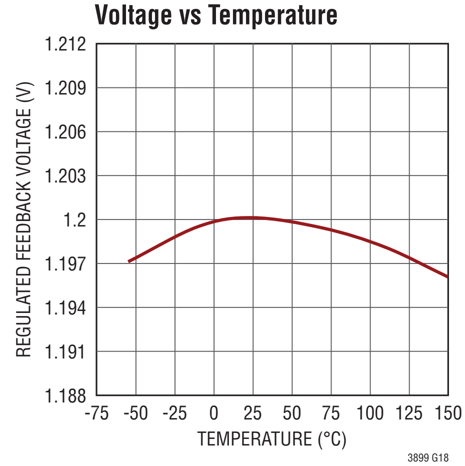



FIGURE 12 CIRCUIT

### Boost Regulated Feedback Voltage vs Temperature

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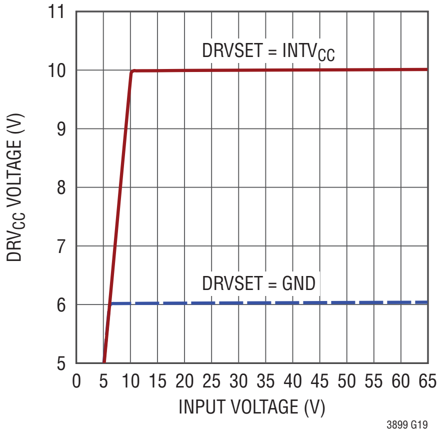
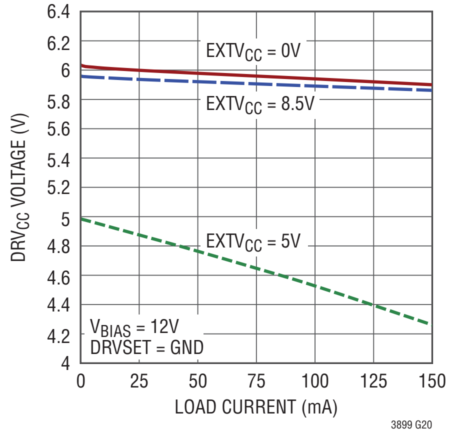
# TYPICAL PERFORMANCE CHARACTERISTICS

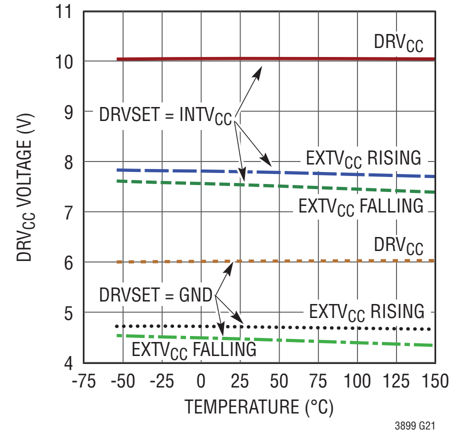
### $DRV_{CC}$ Line Regulation



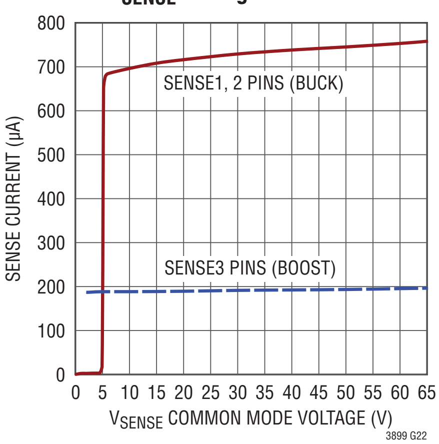

### $DRV_{CC}$ and $EXTV_{CC}$ vs Load Current



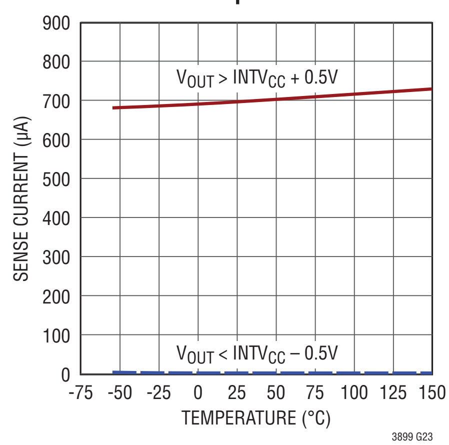

### $EXTV_{CC}$ Switchover and $DRV_{CC}$ Voltages vs Temperature



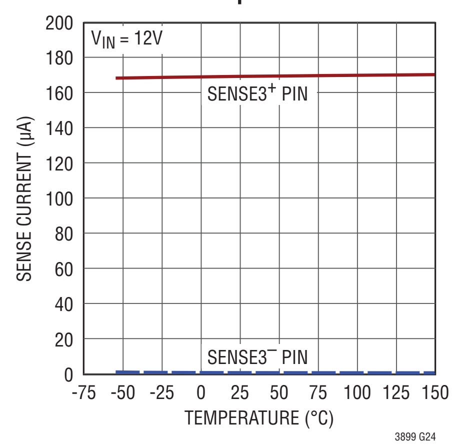

### SENSE Pins Total Input Current vs $V_{SENSE}$ Voltage



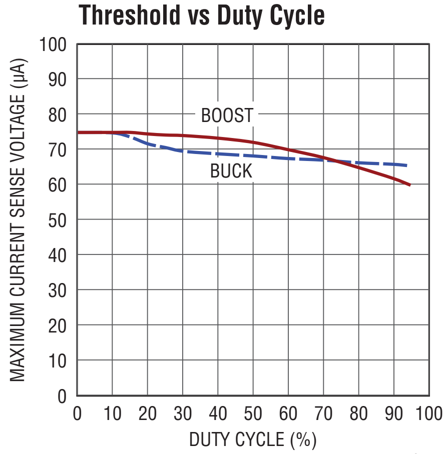

### Buck SENSE⁻ Pin Input Bias Current vs Temperature



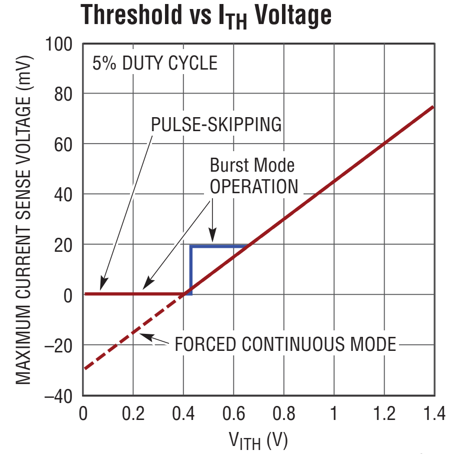

### Boost SENSE Pin Total Input Current vs Temperature



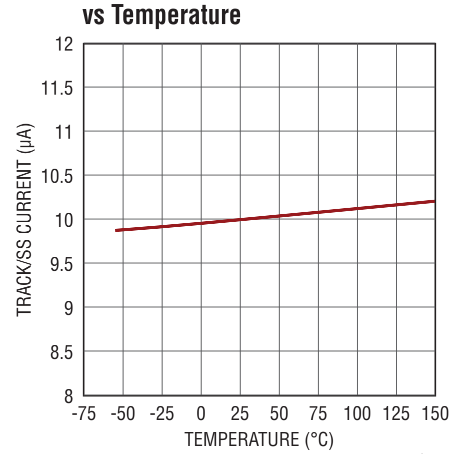

### Maximum Current Sense Threshold vs Duty Cycle




### Maximum Current Sense Threshold vs $I_{TH}$ Voltage



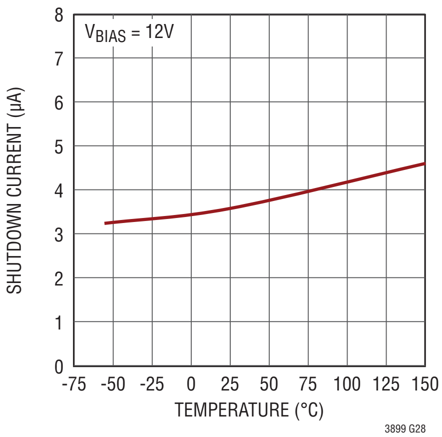

### TRACK/SS Pull-Up Current vs Temperature



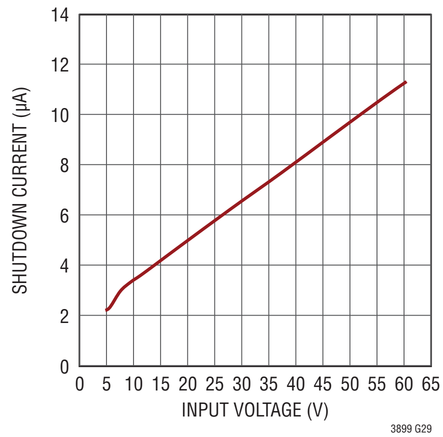

Rev. B

# TYPICAL PERFORMANCE CHARACTERISTICS

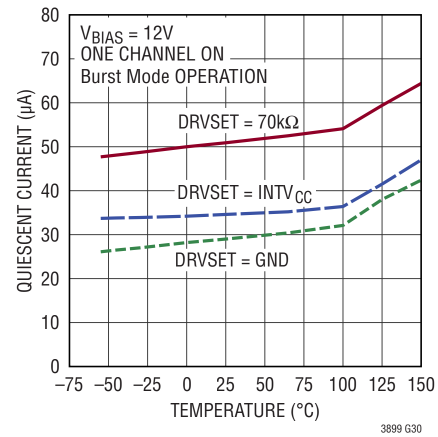
### Shutdown Current vs Temperature



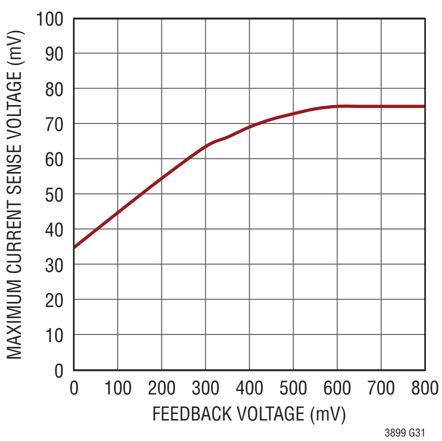

### Shutdown Current vs Input Voltage



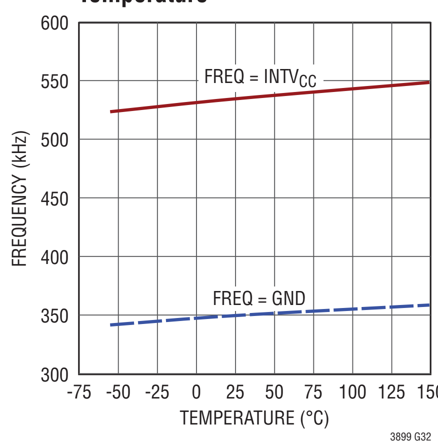

### Quiescent Current vs Temperature



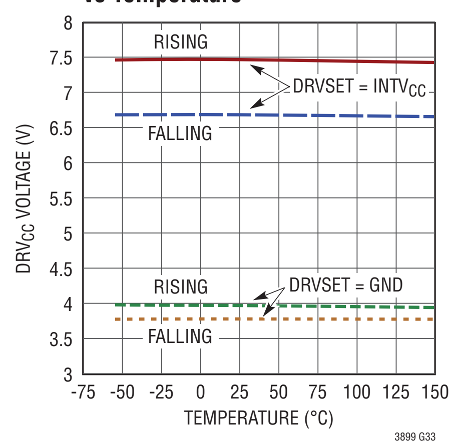

### Buck Foldback Current



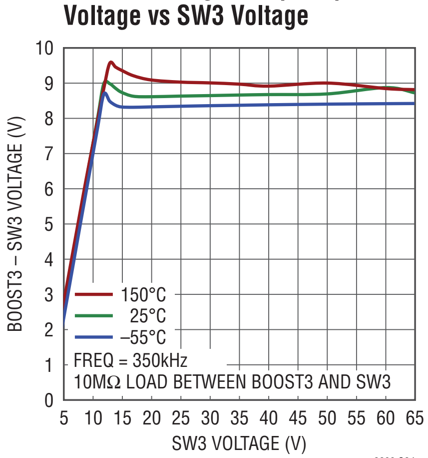

### Oscillator Frequency vs Temperature



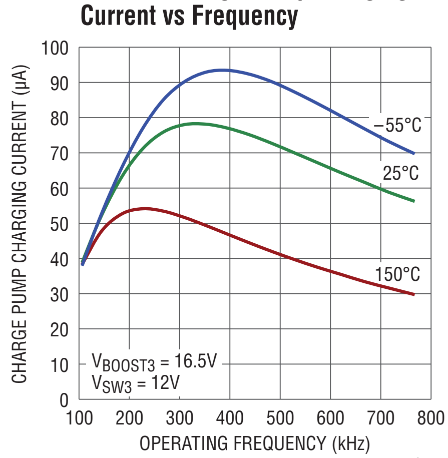

### Undervoltage Lockout Threshold vs Temperature



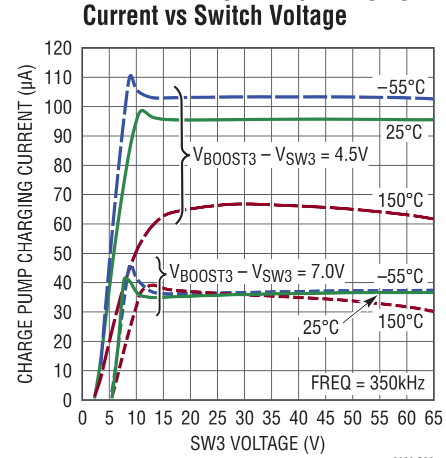

### BOOST3 Charge Pump Output Voltage vs SW3 Voltage




### BOOST3 Charge Pump Charging Current vs Frequency




### BOOST3 Charge Pump Charging Current vs Switch Voltage

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## PIN FUNCTIONS (QFN/TSSOP)

**FREQ (Pin 1/Pin 5):** The frequency control pin for the internal VCO. Connecting this pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting this pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. Other frequencies between 50kHz and 900kHz can be programmed using a resistor between FREQ and GND. The resistor and an internal 20μA source current create a voltage used by the internal oscillator to set the frequency.

**PLLIN/MODE (Pin 2/Pin 6):** External Synchronization Input to Phase Detector and Forced Continuous Mode Input. When an external clock is applied to this pin, the phase-locked loop will force the rising TG1 signal to be synchronized with the rising edge of the external clock, and the regulators will operate in forced continuous mode. When not synchronizing to an external clock, this input, which acts on all three controllers, determines how the LTC3899 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floated. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 1.1V and less than $INTV_{CC}$ – 1.3V selects pulse-skipping operation. This can be done by connecting a 100k resistor from this pin to $INTV_{CC}$.

**$INTV_{CC}$ (Pin 8/Pin 12):** Output of the Internal 5V Low Dropout Regulator. The low voltage analog and digital circuits are powered from this voltage source. A low ESR 0.1μF ceramic bypass capacitor should be connected between $INTV_{CC}$ and GND, as close as possible to the IC. $INTV_{CC}$ should not be used to power or bias any external circuitry other than to configure FREQ, PLLIN/MODE, DRVSET AND VPRG3 pins.

**RUN1, RUN2, RUN3 (Pins 9, 10, 11/Pins 13, 14, 15):** Run Control Inputs for Each Controller. Forcing any of these pins below 1.2V shuts down that controller. Forcing all of these pins below 0.7V shuts down the entire LTC3899, reducing quiescent current to approximately 3.6μA.

**DRVSET (Pin 16/Pin 20):** Sets the regulated output voltage of the $DRV_{CC}$ LDO regulator. Connecting this pin to GND sets $DRV_{CC}$ to 6V whereas connecting it to $INTV_{CC}$ sets $DRV_{CC}$ to 10V. Voltages between 5V and 10V can be programmed by placing a resistor (50k to 100k) between the DRVSET pin and GND. The DRVSET pin also determines the higher or lower $DRV_{CC}$ UVLO and $EXTV_{CC}$ switchover thresholds, as listed on the Electrical Characteristics table. Connecting DRVSET to GND or programming DRVSET with a resistor chooses the lower thresholds whereas tying DRVSET to $INTV_{CC}$ chooses the higher thresholds. When programming DRVSET with a resistor, do not choose a resistor value less than 50k (unless shorting DRVSET to GND) or higher than 100k.

**$DRV_{CC}$ (Pin 22/Pin 26):** Output of the Internal or External Low Dropout (LDO) Regulator. The gate drivers are powered from this voltage source. The $DRV_{CC}$ voltage is set by the DRVSET pin. Must be decoupled to ground with a minimum of 4.7μF ceramic or other low ESR capacitor. Do not use the $DRV_{CC}$ pin for any other purpose.

**$EXTV_{CC}$ (Pin 23/Pin 27):** External Power Input to an Internal LDO Connected to $DRV_{CC}$. This LDO supplies $DRV_{CC}$ power, bypassing the internal LDO powered from $V_{BIAS}$ whenever $EXTV_{CC}$ is higher than its switchover threshold (4.7V or 7.7V depending on the DRVSET pin). See $EXTV_{CC}$ Connection in the Applications Information section. Do not float or exceed 14V on this pin. Do not connect $EXTV_{CC}$ to a voltage greater than $V_{BIAS}$. Connect to GND if not used.

**$V_{BIAS}$ (Pin 24/Pin 28):** Main Supply Pin. A bypass capacitor should be tied between this pin and the GND pin.

**BG1, BG2, BG3 (Pins 29, 21, 25/Pins 33, 25, 29):** High Current Gate Drives for Bottom N-Channel MOSFETs. Voltage swing at these pins is from ground to $DRV_{CC}$.

**BOOST1, BOOST2, BOOST3 (Pins 30, 20, 26/Pins 34, 24, 30):** Bootstrapped Supplies to the Topside Floating Drivers. Capacitors are connected between the BOOST and SW pins. Voltage swing at BOOST1 and BOOST2 pins is from approximately $DRV_{CC}$ to ($V_{IN1,2}$ + $DRV_{CC}$). Voltage swing at BOOST3 is from $DRV_{CC}$ to ($V_{OUT3}$ + $DRV_{CC}$).

**SW1, SW2, SW3 (Pins 31, 19, 28/Pins 35, 23, 32):** Switch Node Connections to Inductors.

**TG1, TG2, TG3 (Pins 32, 18, 27/Pins 36, 22, 31):** High Current Gate Drives for Top N-Channel MOSFETs. These

## PIN FUNCTIONS (QFN/TSSOP)

are the outputs of floating drivers with a voltage swing equal to $DRV_{CC}$ superimposed on the switch node voltage SW.

**TRACK/SS1, TRACK/SS2, SS3 (Pins 33, 17, 3/Pins 37, 21, 7):** External Tracking and Soft-Start Input. For the buck channels, the LTC3899 regulates the $V_{FB1,2}$ voltage to the smaller of 0.8V, or the voltage on the TRACK/SS1,2 pin. For the boost channel, the LTC3899 regulates the $V_{FB3}$ voltage to the smaller of 1.2V, or the voltage on the SS3 pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage. Alternatively, a resistor divider on another voltage supply connected to the TRACK/SS pins of the buck channels allow the LTC3899 buck outputs to track the other supply during start-up.

**VPRG3 (Pin 34/Pin 38):** Channel 3 Output Control Pin. This pin sets the boost channel to adjustable output mode using external feedback resistors or fixed 10V/12V output mode. Floating this pin allows the output to be programmed through the $V_{FB3}$ pin using external resistors, regulating $V_{FB3}$ to the 1.2V reference. Connecting this pin to GND or $INTV_{CC}$ programs the output to 10V or 12V (respectively), and $V_{FB3}$ is used to sense the output voltage.

**ITH1, ITH2, ITH3 (Pins 35, 15, 7/Pins 1, 19, 11):** Error Amplifier Outputs and Switching Regulator Compensation Points. Each associated channel's current comparator trip point increases with this control voltage.

**$V_{FB1}$, $V_{FB2}$ (Pins 36, 14/Pins 2, 18):** These pins receive the remotely sensed feedback voltage for each buck controller from an external resistive divider across the output.

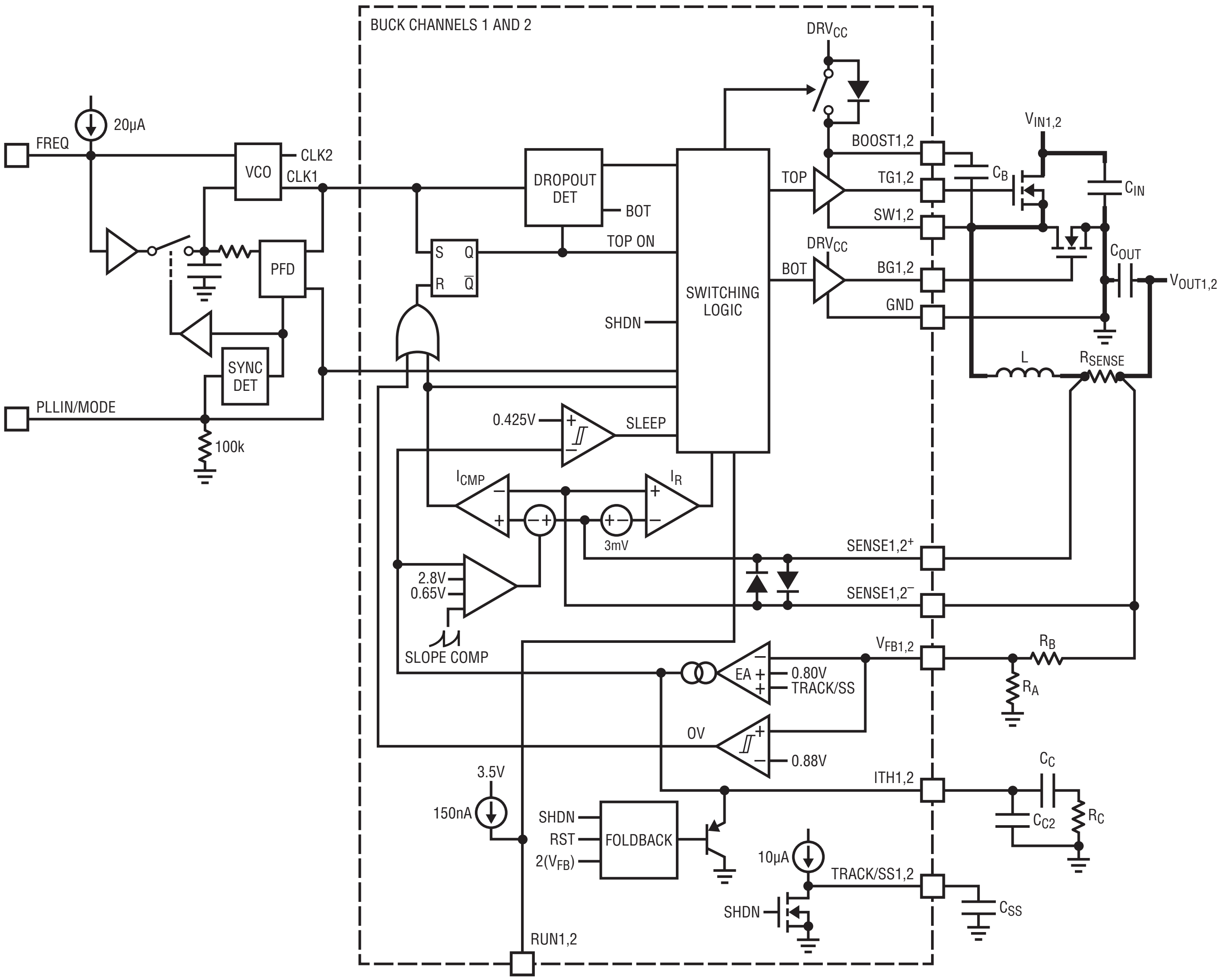
**$V_{FB3}$ (Pins 6/Pins 10):** If VPRG3 is floating, this pin receives the remotely sensed feedback voltage for the boost controller from an external resistive divider across the output. If VPRG3 is tied to GND or $INTV_{CC}$, this pin receives the remotely sensed output voltage of the boost controller.

**$SENSE1^+$, $SENSE2^+$, $SENSE3^+$ (Pins 37, 13, 4/Pins 3, 17, 8):** The (+) Input to the Differential Current Comparators. The ITH pin voltage and controlled offsets between the $SENSE^–$ and $SENSE^+$ pins in conjunction with $R_{SENSE}$ set the current trip threshold. For the boost channel, the $SENSE3^+$ pin supplies current to the current comparator.

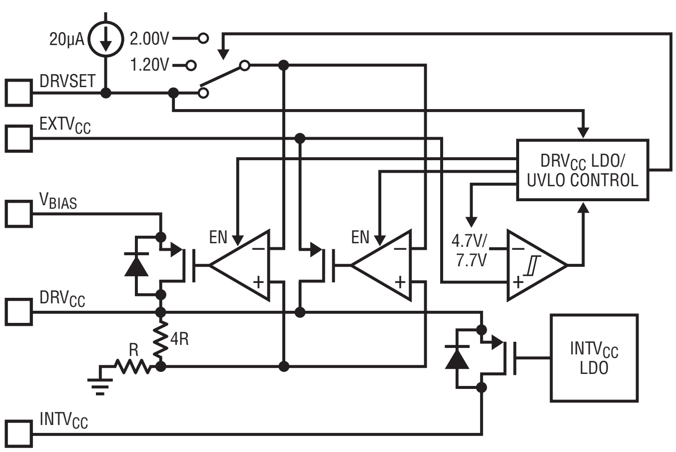
**$SENSE1^–$, $SENSE2^–$, $SENSE3^–$ (Pins 38, 12, 5/Pins 4, 16, 9):** The (–) Input to the Differential Current Comparators. When $SENSE1,2^–$ for the buck channels is greater than $INTV_{CC}$, then $SENSE1,2^–$ pin supplies current to the current comparator.

**GND (Exposed Pad Pin 39/Exposed Pad Pin 39):** Ground. The exposed pad must be soldered to the PCB for rated electrical and thermal performance.

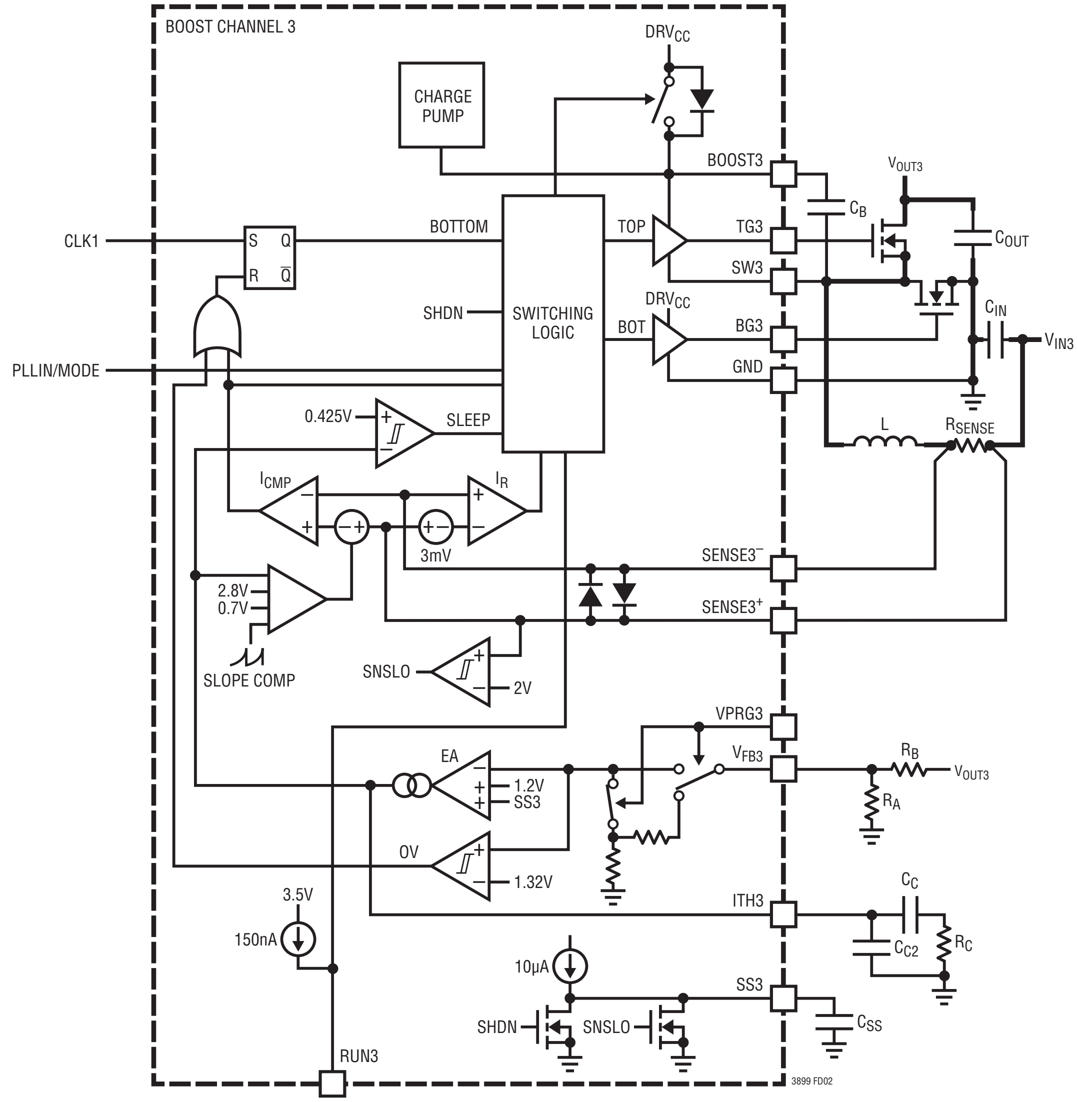
# FUNCTIONAL DIAGRAMS




3899 FD



## FUNCTIONAL DIAGRAMS




## OPERATION (Refer to the Functional Diagrams)

### Main Control Loop

The LTC3899 uses a constant frequency, current mode step-down architecture. The two buck controllers, channels 1 and 2, operate 180° out of phase with each other. The boost controller, channel 3, operates in phase with channel 1. During normal operation, the external top MOSFET for the buck channels (the external bottom MOSFET for the boost controller) is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, $I_{CMP}$, resets the RS latch. The peak inductor current at which $I_{CMP}$ trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output voltage feedback signal at the $V_{FB}$ pin (which is generated with an external resistor divider connected across the output voltage, $V_{OUT}$, to ground) to the internal 0.800V reference voltage (1.2V reference voltage for the boost). When the load current increases, it causes a slight decrease in $V_{FB}$ relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

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## OPERATION (Refer to the Functional Diagrams)

After the top MOSFET for the bucks (the bottom MOSFET for the boost) is turned off each cycle, the bottom MOSFET is turned on (the top MOSFET for the boost) until either the inductor current starts to reverse, as indicated by the current comparator $I_R$, or the beginning of the next clock cycle.

### $DRV_{CC}$/$EXTV_{CC}$/$INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers is derived from the $DRV_{CC}$ pin. The $DRV_{CC}$ supply voltage can be programmed from 5V to 10V through control of the DRVSET pin. When the $EXTV_{CC}$ pin is tied to a voltage below its switchover voltage (4.7V or 7.7V depending on the DRVSET voltage), the $V_{BIAS}$ LDO (low dropout linear regulator) supplies power from $V_{BIAS}$ to $DRV_{CC}$. If $EXTV_{CC}$ is taken above its switchover voltage, the $V_{BIAS}$ LDO is turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies power from $EXTV_{CC}$ to $DRV_{CC}$. Using the $EXTV_{CC}$ pin allows the $DRV_{CC}$ power to be derived from a high efficiency external source such as one of the LTC3899 buck regulator outputs.

Each top MOSFET driver is biased from the floating bootstrap capacitor, $C_B$, which normally recharges during each cycle through an internal switch whenever SW goes low.

For buck channels 1 and 2, if the input voltage decreases to a voltage close to its output, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period every tenth cycle to allow $C_B$ to recharge, resulting in about 99% duty cycle.

The $INTV_{CC}$ supply powers most of the other internal circuits in the LTC3899. The $INTV_{CC}$ LDO regulates to a fixed value of 5V and its power is derived from the $DRV_{CC}$ supply.

### Shutdown and Start-Up (RUN, TRACK/SS Pins)

The three channels of the LTC3899 can be independently shut down using the RUN1, RUN2 and RUN3 pins. Pulling a RUN pin below 1.20V shuts down the main control loop for that channel. Pulling all three pins below 0.7V disables all controllers and most internal circuits, including the $DRV_{CC}$ and $INTV_{CC}$ LDOs. In this state, the LTC3899 draws only 3.6μA of quiescent current.

Releasing a RUN pin allows a small 150nA internal current to pull up the pin to enable that controller. Each RUN pin may be externally pulled up or driven directly by logic. Each RUN pin can tolerate up to 65V (absolute maximum), so it can be conveniently tied to $V_{BIAS}$ in always-on applications where one or more controllers are enabled continuously and never shut down.

The start-up of each controller's output voltage $V_{OUT}$ is controlled by the voltage on the TRACK/SS pin (TRACK/SS1 for channel 1, TRACK/SS2 for channel 2, SS3 for channel 3). When the voltage on the TRACK/SS pin is less than the 0.8V internal reference for the bucks and the 1.2V internal reference for the boost, the LTC3899 regulates the $V_{FB}$ voltage to the TRACK/SS pin voltage instead of the corresponding reference voltage. This allows the TRACK/SS pin to be used to program a soft-start by connecting an external capacitor from the TRACK/SS pin to GND. An internal 10μA pull-up current charges this capacitor creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 0.8V/1.2V (and beyond up to about 4V), the output voltage $V_{OUT}$ rises smoothly from zero ($V_{IN}$ for the boost) to its final value.

Alternatively the TRACK/SS pins for buck channels 1 and 2 can be used to cause the start-up of $V_{OUT}$ to track that of another supply. Typically, this requires connecting to the TRACK/SS pin an external resistor divider from the other supply to ground (see Applications Information section).

### Light Load Current Operation (Burst Mode Operation, Pulse-Skipping or Forced Continuous Mode) (PLLIN/MODE Pin)

The LTC3899 can be enabled to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode, or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to GND. To select forced continuous operation, tie the PLLIN/MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 1.1V and less than $INTV_{CC}$ – 1.3V. This can be done by connecting a 100kΩ resistor between PLLIN/MODE and $INTV_{CC}$.

## OPERATION (Refer to the Functional Diagrams)

When a controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of the maximum sense voltage (30% for the boost) even though the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.450V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC3899 draws. If one channel is in sleep mode and the other two are shut down, the LTC3899 draws only 29µA of quiescent current (with DRVSET = 0V). If two channels are in sleep mode and the other shut down, it draws only 34µA of quiescent current. If all three controllers are enabled in sleep mode, the LTC3899 draws only 39µA of quiescent current. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET (the bottom external MOSFET for the boost) on the next cycle of the internal oscillator.

When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator ($I_R$) turns off the bottom external MOSFET (the top external MOSFET for the boost) just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates discontinuously.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current. Clocking the LTC3899 from an external source enables forced continuous mode (see the Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins) section).

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC3899 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator, $I_{CMP}$, may remain tripped for several cycles and force the external top MOSFET (bottom for the boost) to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

### Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3899's controllers can be selected using the FREQ pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to GND, tied to $INTV_{CC}$ or programmed through an external resistor. Tying FREQ to GND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 10.

A phase-locked loop (PLL) is available on the LTC3899 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The LTC3899's phase detector adjusts the voltage (through an internal lowpass filter) of the VCO input to align the turn-on of controller 1's external top MOSFET (and controller 3's external bottom MOSFET) to the rising edge of the synchronizing signal. Thus, the turn-on of controller 2's

## OPERATION (Refer to the Functional Diagrams)

external top MOSFET is 180° out of phase to the rising edge of the external clock source.

The VCO input voltage is prebiased to the operating frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of TG1. The ability to prebias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency.

The typical capture range of the LTC3899's phase-locked loop is from approximately 55kHz to 1MHz, with a guarantee to be between 75kHz and 850kHz. In other words, the LTC3899's PLL is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.1V (falling). It is recommended that the external clock source swings from ground (0V) to at least 2.5V.

### Boost Controller Operation When $V_{IN} > V_{OUT}$

When the input voltage to the boost channel rises above its regulated $V_{OUT}$ voltage, the controller can behave differently depending on the mode, inductor current and $V_{IN}$ voltage. In forced continuous mode, the loop works to keep the top MOSFET on continuously once $V_{IN}$ rises above $V_{OUT}$. An internal charge pump delivers current to the boost capacitor from the BOOST3 pin to maintain a sufficiently high TG voltage. Because the LTC3899 uses internal switches and does not require external bootstrap diodes, the charge pump only has to overcome small leakage currents (board leakage, etc.).

In pulse-skipping mode, if $V_{IN}$ is between 0% and 10% above the regulated $V_{OUT}$ voltage, TG3 turns on if the inductor current rises above approximately 3% of the programmed $I_{LIM}$ current. If the part is programmed in Burst Mode operation under this same $V_{IN}$ window, then TG3 turns on at the same threshold current as long as the chip is awake (one of the buck channels is awake and switching). If both buck channels are asleep or shut down in this $V_{IN}$ window, then TG3 will remain off regardless of the inductor current.

If $V_{IN}$ rises more than 10% above the regulated $V_{OUT}$ voltage in any mode, the controller turns on TG3 regardless of the inductor current. In Burst Mode operation, however, the internal charge pump turns off if the entire chip is asleep (if the two buck channels are also asleep or shut down). With the charge pump off, there would be nothing to prevent the boost capacitor from discharging, resulting in an insufficient TG voltage needed to keep the top MOSFET completely on. The charge pump turns back on when the chip wakes up, and it remains on as long as one of the buck channels is actively switching.

### Boost Controller at Low SENSE Pin Common Voltage

The current comparator of the boost controller is powered directly from the $SENSE3^+$ pin and can operate to voltages as low as 2.2V. Since this is lower than the $V_{BIAS}$ UVLO of the chip, $V_{BIAS}$ can be connected to the output of the boost controller, as illustrated in the typical application circuit in Figure 12. This allows the boost controller to handle input voltage transients down to 2.2V while maintaining output voltage regulation. If $SENSE3^+$ falls below 2.0V, then switching stops and SS3 is pulled low. If $SENSE3^+$ rises back above 2.2V, the SS3 pin will be released, initiating a new soft-start sequence.

### Buck Controller Output Overvoltage Protection

The two buck channels have an overvoltage comparator that guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the $V_{FB1,2}$ pin rises by more than 10% above its regulation point of 0.800V, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

### Buck Foldback Current

When the buck output voltage falls to less than 70% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the $V_{FB1,2}$ voltage is keeping up with the TRACK/SS1,2 voltage). There is no foldback current limiting for the boost channel.

## APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC3899 application circuit. LTC3899 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of $R_{SENSE}$ (if $R_{SENSE}$ is used) and inductor value. Next, the power MOSFETs and Schottky diodes are selected. Finally, input and output capacitors are selected.

### SENSE$^+$ and SENSE$^–$ Pins

The SENSE$^+$ and SENSE$^–$ pins are the inputs to the current comparators.

*Buck Controllers* (SENSE1$^+$/SENSE1$^–$, SENSE2$^+$/SENSE2$^–$): The common mode voltage range on these pins is 0V to 65V (absolute maximum), enabling the LTC3899 to regulate buck output voltages up to a nominal 60V (allowing margin for tolerances and transients). The SENSE$^+$ pin is high impedance over the full common mode range, drawing at most ±1μA. This high impedance allows the current comparators to be used in inductor DCR sensing. The impedance of the SENSE$^–$ pin changes depending on the common mode voltage. When SENSE$^–$ is less than $INTV_{CC}$ – 0.5V, a small current of less than 1μA flows out of the pin. When SENSE$^–$ is above $INTV_{CC}$ + 0.5V, a higher current (≈700μA) flows into the pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current.

*Boost Controller* (SENSE3$^+$/SENSE3$^–$): The common mode input range for these pins is 2.2V to 60V, allowing the boost converter to operate from inputs over this full range. The SENSE3$^+$ pin also provides power to the current comparator and draws about 170μA during normal operation (when not shut down or asleep in Burst Mode operation). There is a small bias current of less than 1μA that flows into the SENSE3$^–$ pin. This high impedance on the SENSE3$^–$ pin allows the current comparator to be used in inductor DCR sensing.

Filter components mutual to the sense lines should be placed close to the LTC3899, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

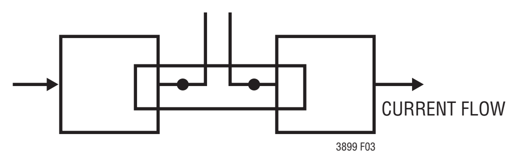



**Figure 1. Sense Lines Placement with Inductor or Sense Resistor**

### Low Value Resistor Current Sensing

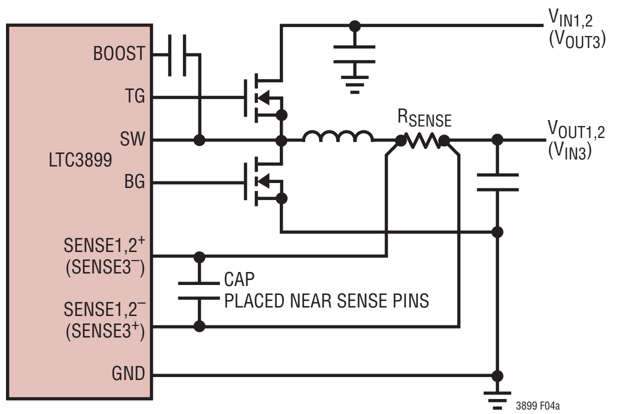
A typical sensing circuit using a discrete resistor is shown in Figure 2a. $R_{SENSE}$ is chosen based on the required output current.

The current comparators have a maximum threshold $V_{SENSE(MAX)}$ of 75mV. The current comparator threshold voltage sets the peak of the inductor current, yielding a maximum average output current, $I_{MAX}$, equal to the peak value less half the peak-to-peak ripple current, $\Delta I_L$. To calculate the sense resistor value, use the equation:

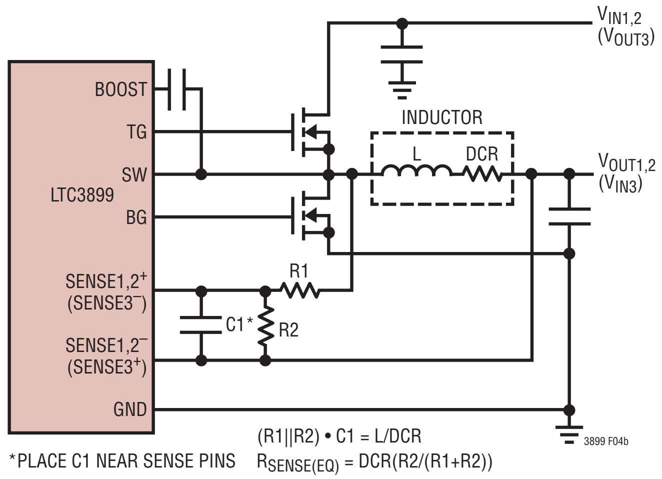
$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

When using the buck controllers in very low dropout conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criteria for buck regulators operating at greater than 50%

## APPLICATIONS INFORMATION




**(2a) Using a Resistor to Sense Current**




**(2b) Using the Inductor DCR to Sense Current**

**Figure 2. Current Sensing Methods**

duty factor. A curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak inductor current depending upon the operating duty factor.

### Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3899 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, determine $R_{SENSE(EQUIV)}$, keeping in mind that the minimum value for the maximum current sense threshold ($V_{SENSE(MAX)}$) for the LTC3899 is 65mV.

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value ($R_D$), use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}}$$

## APPLICATIONS INFORMATION

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the SENSE+ pin's ±1µA current.

The equivalent resistance R1||R2 is scaled to the temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR\ at\ 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D}; \quad R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}\ R1 = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R1}$$

For the boost controller, the maximum power loss in R1 will occur in continuous mode at $V_{IN}$ = 1/2 • $V_{OUT}$:

$$P_{LOSS}\ R1 = \frac{\left(V_{OUT(MAX)} - V_{IN}\right) \bullet V_{IN}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

### Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current, $\Delta I_L$, decreases with higher inductance or higher frequency. For the buck controllers, $\Delta I_L$ increases with higher $V_{IN}$:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For the boost controller, $\Delta I_L$ increases with higher $V_{OUT}$:

$$\Delta I_L = \frac{1}{(f)(L)} V_{IN} \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

Accepting larger values of $\Delta I_L$ allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum $\Delta I_L$ occurs at the maximum input voltage for the bucks and $V_{IN}$ = 1/2 • $V_{OUT}$ for the boost.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit (30% for the boost) determined by $R_{SENSE}$. Lower inductor values (higher $\Delta I_L$) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

### Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

## APPLICATIONS INFORMATION

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

**Power MOSFET and Schottky Diode (Optional) Selection**

Two external power MOSFETs must be selected for each controller in the LTC3899: one N-channel MOSFET for the top switch (main switch for the bucks, synchronous for the boost), and one N-channel MOSFET for the bottom switch (main switch for the boost, synchronous for the bucks).

The peak-to-peak drive levels are set by the $DRV_{CC}$ voltage. This voltage can range from 5V to 10V depending on configuration of the DRVSET pin. Therefore, both logic-level and standard-level threshold MOSFETs can be used in most applications depending on the programmed $DRV_{CC}$ voltage. Pay close attention to the $BV_{DSS}$ specification for the MOSFETs as well.

The LTC3899's unique ability to adjust the gate drive level between 5V to 10V (OPTI-DRIVE) allows an application circuit to be precisely optimized for efficiency. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance $C_{MILLER}$, input voltage and maximum output current. Miller capacitance, $C_{MILLER}$, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. $C_{MILLER}$ is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in $V_{DS}$. This result is then multiplied by the ratio of the application applied $V_{DS}$ to the gate charge curve specified $V_{DS}$. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Buck Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Buck Sync Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

$$\text{Boost Main Switch Duty Cycle} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\text{Boost Sync Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN\_BUCK} = \frac{V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{OUT(MAX)}}{2}\right)(R_{DR})(C_{MILLER}) \bullet \left[\frac{1}{V_{DRVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC\_BUCK} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)}$$

$$P_{MAIN\_BOOST} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V_{IN}^2}\left(I_{OUT(MAX)}\right)^2 \bullet (1+\delta)R_{DS(ON)} + \left(\frac{V_{OUT}^3}{V_{IN}}\right)\left(\frac{I_{OUT(MAX)}}{2}\right) \bullet (R_{DR})(C_{MILLER}) \bullet \left[\frac{1}{V_{DRVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC\_BOOST} = \frac{V_{IN}}{V_{OUT}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)}$$

where $\delta$ is the temperature dependency of $R_{DS(ON)}$ and $R_{DR}$ (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. $V_{THMIN}$ is the typical MOSFET minimum threshold voltage.

## APPLICATIONS INFORMATION

Both MOSFETs have $I^2R$ losses while the main N-channel equations for the buck and boost controllers include an additional term for transition losses, which are highest at high input voltages for the bucks and low input voltages for the boost. For $V_{IN}$ < 20V (higher $V_{IN}$ for the boost) the high current efficiency generally improves with larger MOSFETs, while for $V_{IN}$ > 20V (lower $V_{IN}$ for the boost) the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower $C_{MILLER}$ actually provides higher efficiency. The synchronous MOSFET losses for the buck controllers are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1 + $\delta$) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta$ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

Optional Schottky diodes placed across the synchronous MOSFET conduct during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the synchronous MOSFET from turning on, storing charge during the dead-time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high $V_{IN}$. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

### Boost $C_{IN}$, $C_{OUT}$ Selection

The input ripple current in a boost converter is relatively low (compared with the output ripple current), because this current is continuous. The boost input capacitor $C_{IN}$ voltage rating should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of $C_{IN}$ is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

In a boost converter, the output has a discontinuous current, so $C_{OUT}$ must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$\text{Ripple} = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f} V$$

where $C_{OUT}$ is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR} = I_{L(MAX)} \bullet ESR$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings such as OS-CON and POSCAP.

### Buck $C_{IN}$, $C_{OUT}$ Selection

The selection of $C_{IN}$ for the two buck controllers is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula shown in Equation 1 to determine the maximum RMS

## APPLICATIONS INFORMATION

capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The opt-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN}-V_{OUT})\right]^{1/2} \quad (1)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3899, ceramic capacitors can also be used for $C_{IN}$. Always consult the manufacturer if there is any question.

The benefit of the LTC3899 2-phase operation can be calculated by using Equation 1 for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing.

The drains of the top MOSFETs should be placed within 1cm of each other and share a common $C_{IN}$(s). Separating the drains and $C_{IN}$ may produce undesirable voltage and current resonances at $V_{IN}$.

A small (0.1µF to 1µF) bypass capacitor between the chip $V_{BIAS}$ pin and ground, placed close to the LTC3899, is also suggested. A 10Ω resistor placed between $C_{IN}$ (C1) and the $V_{BIAS}$ pin provides further isolation.

The selection of $C_{OUT}$ is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple ($\Delta V_{OUT}$) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}}\right)$$

where f is the operating frequency, $C_{OUT}$ is the output capacitance and $\Delta I_L$ is the ripple current in the inductor. The output ripple is highest at maximum input voltage since $\Delta I_L$ increases with input voltage.

### Setting Buck Output Voltage

The LTC3899 output voltages for the buck controllers are set by an external feedback resistor divider carefully placed across the output, as shown in Figure 3. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V\left(1+\frac{R_B}{R_A}\right)$$

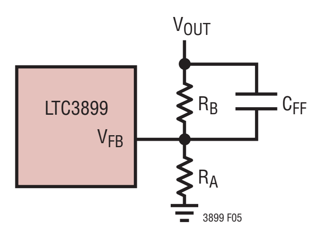



**Figure 3. Setting Buck Output Voltage**

## APPLICATIONS INFORMATION

To improve the frequency response, a feedforward capacitor, $C_{FF}$, may be used. Great care should be taken to route the $V_{FB}$ line away from noise sources, such as the inductor or the SW line.

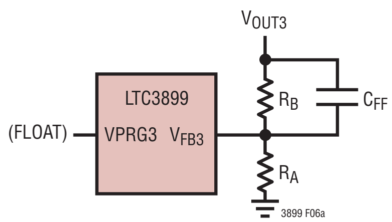
**Setting Boost Output Voltage (VPRG3 Pin)**

Through control of the VPRG3 pin the boost controller output voltage can be set by an external feedback resistor divider or programmed to a fixed 10V or 12V output.

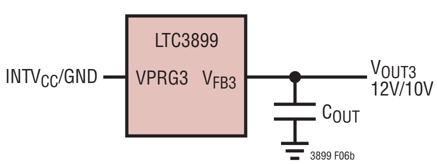
Floating VPRG3 allows the boost output voltage to be set by an external feedback resistor divider placed across the output, as shown in Figure 4a. The regulated output voltage is determined by:

$$V_{OUT(BOOST)} = 1.2V\left(1+\frac{R_B}{R_A}\right)$$

Tying the VPRG3 to $INTV_{CC}$ or GND configures the boost




**(4a) Setting Boost Output Using External Resistors**




**(4b) Setting Boost to Fixed 12V/10V Output**

**Figure 4. Setting CH3 Output Voltage**

controller in fixed output voltage mode. Figure 4b shows how the $V_{FB3}$ pin is used to sense the output voltage in this mode. Tying VPRG3 to $INTV_{CC}$ programs the boost output to 12V, whereas tying VPRG3 to GND programs the output to 10V.

**RUN Pins**

The LTC3899 is enabled using the RUN1, RUN2 and RUN3 pins. The RUN pins have a rising threshold of 1.275V with 75mV of hysteresis. Pulling a RUN pin below 1.2V shuts down the main control loop for that channel. Pulling all three RUN pins below 0.7V disables the controllers and most internal circuits, including the $DRV_{CC}$ and $INTV_{CC}$ LDOs. In this state, the LTC3899 draws only 3.6µA of quiescent current.

Releasing a RUN pin allows a small 150nA internal current to pull up the pin to enable that controller. Because of condensation or other small board leakage pulling the pin down, it is recommended the RUN pins be externally pulled up or driven directly by logic. Each RUN pin can tolerate up to 65V (absolute maximum), so it can

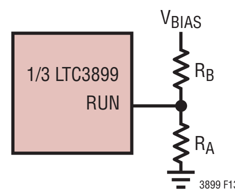



**Figure 5. Using the RUN Pins as a UVLO**

be conveniently tied to $V_{BIAS}$ in always-on applications where one or more controllers are enabled continuously and never shut down.

The RUN pins can be implemented as a UVLO by connecting them to the output of an external resistor divider network off $V_{BIAS}$, as shown in Figure 5.

The rising and falling UVLO thresholds are calculated using the RUN pin thresholds and pull-up current:

$$V_{UVLO(RISING)} = 1.275V\left(1+\frac{R_B}{R_A}\right) - 150nA \cdot R_B$$

$$V_{UVLO(FALLING)} = 1.20V\left(1+\frac{R_B}{R_A}\right) - 150nA \cdot R_B$$

**Tracking and Soft-Start (TRACK/SS1, TRACK/SS2, SS3 Pins)**

The start-up of each $V_{OUT}$ is controlled by the voltage on the TRACK/SS pin (TRACK/SS1 for channel 1, TRACK/SS2 for channel 2, SS3 for channel 3). When the

## APPLICATIONS INFORMATION

voltage on the TRACK/SS pin is less than the internal 0.8V reference (1.2V reference for the boost channel), the LTC3899 regulates the $V_{FB}$ pin voltage to the voltage on the TRACK/SS pin instead of the internal reference. The TRACK/SS pin can be used to program an external soft-start function or to allow $V_{OUT}$ to track another supply during start-up.

Soft-start is enabled by simply connecting a capacitor from the TRACK/SS pin to ground, as shown in Figure 6. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The LTC3899 will regulate its feedback voltage (and hence $V_{OUT}$) according to the voltage on the TRACK/SS pin, allowing $V_{OUT}$ to rise smoothly from 0V ($V_{IN}$ for the boost) to its final regulated value. The total soft-start time will be approximately:

$$t_{SS\_BUCK} = C_{SS} \bullet \frac{0.8V}{10\mu A}$$

$$t_{SS\_BOOST} = C_{SS} \bullet \frac{1.2V}{10\mu A}$$

Alternatively, the TRACK/SS1 and TRACK/SS2 pins for the two buck controllers can be used to track two (or more) supplies during start-up, as shown qualitatively in Figure 7a and Figure 7b. To do this, a resistor divider should be connected from the master supply ($V_X$) to the TRACK/SS pin of the slave supply ($V_{OUT}$), as shown in Figure 8. During start-up $V_{OUT}$ will track $V_X$ according to the ratio set by the resistor divider:

$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B}$$

For coincident tracking ($V_{OUT} = V_X$ during start-up),

$R_A = R_{TRACKA}$

$R_B = R_{TRACKB}$

### $DRV_{CC}$ and $INTV_{CC}$ Regulators (OPTI-DRIVE)

The LTC3899 features two separate internal P-channel low dropout linear regulators (LDO) that supply power at the $DRV_{CC}$ pin from either the $V_{BIAS}$ supply pin or the $EXTV_{CC}$

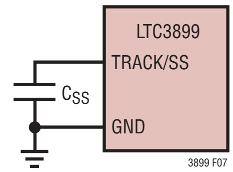
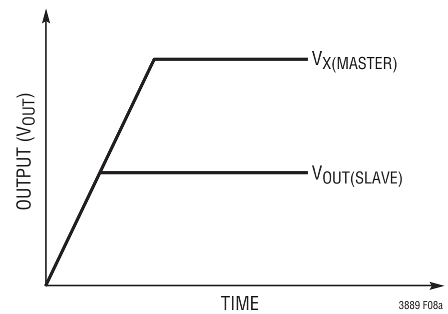
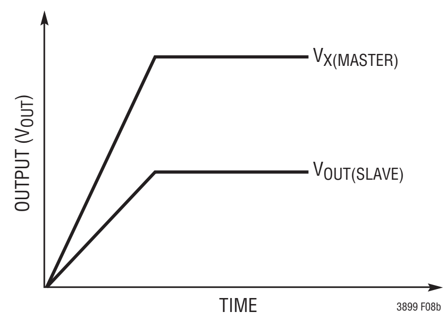



**Figure 6. Using the TRACK/SS Pin to Program Soft-Start**




**(7a) Coincident Tracking**




**(7b) Ratiometric Tracking**

**Figure 7. Two Different Modes of Output Voltage Tracking**

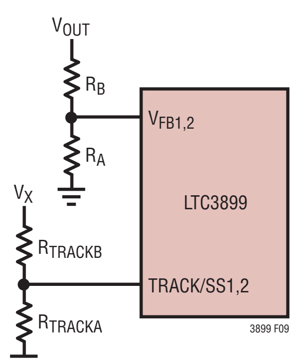



**Figure 8. Using the TRACK/SS Pin for Tracking**

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pin depending on the connections of the $EXTV_{CC}$ and DRVSET pins. A third P-channel LDO supplies power at the $INTV_{CC}$ pin from the $DRV_{CC}$ pin. $DRV_{CC}$ powers the gate drivers whereas $INTV_{CC}$ powers much of the LTC3899's internal circuitry. The $V_{BIAS}$ LDO and the $EXTV_{CC}$ LDO regulate $DRV_{CC}$ between 5V to 10V, depending on how the DRVSET pin is set. Each of these LDOs can supply a peak current of at least 50mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels. The $INTV_{CC}$ supply must be bypassed with a 0.1µF ceramic capacitor.

The DRVSET pin programs the $DRV_{CC}$ supply voltage as well as the $DRV_{CC}$ UVLO and $EXTV_{CC}$ switchover threshold voltages. Table 1 summarizes the different DRVSET pin configurations along with the voltage settings that go with each configuration. Tying the DRVSET pin to $INTV_{CC}$ programs $DRV_{CC}$ to 10V and chooses the higher UVLO/$EXTV_{CC}$ thresholds. Tying the DRVSET pin to GND programs $DRV_{CC}$ to 6V and chooses the lower UVLO/$EXTV_{CC}$ thresholds. By placing a 50k to 100k resistor between DRVSET and GND the $DRV_{CC}$ voltage can be programmed between 5V to 10V, as shown in Figure 9. With a resistor on DRVSET, the lower UVLO/$EXTV_{CC}$ thresholds are chosen.

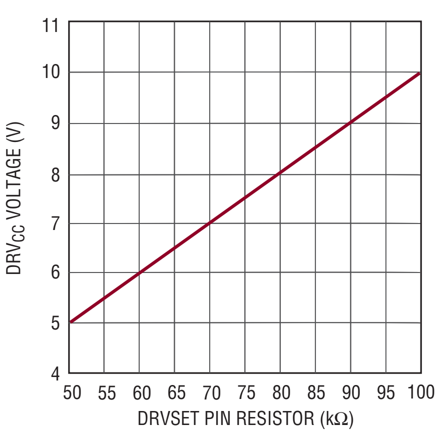


**Figure 9. Relationship Between $DRV_{CC}$ Voltage and Resistor Value at DRVSET Pin**

**Table 1.**

| DRVSET PIN | $DRV_{CC}$ VOLTAGE | $DRV_{CC}$ UVLO RISING/FALLING THRESHOLDS | $EXTV_{CC}$ SWITCHOVER THRESHOLD |
|---|---|---|---|
| 0V | 6V | 4.0V/3.8V | 4.7V |
| $INTV_{CC}$ | 10V | 7.5V/6.7V | 7.7V |
| Resistor to GND 50k to 100k | 5V to 10V | 4.0V/3.8V | 4.7V |

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3899 to be exceeded. The $DRV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the $V_{BIAS}$ LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.7V or 7.7V as determined by the DRVSET pin described above), the $V_{BIAS}$ LDO is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{BIAS} \bullet I_{DRVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, using the LTC3899 in the QFN package, the $DRV_{CC}$ current is limited to less than 40mA from a 40V supply when not using the $EXTV_{CC}$ supply at a 70°C ambient temperature:

$$T_J = 70°C + (40mA)(40V)(34°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the $V_{BIAS}$ supply current must be checked while operating in forced continuous mode (PLLIN/MODE = $INTV_{CC}$) at maximum $V_{BIAS}$.

When the voltage applied to $EXTV_{CC}$ rises above its switchover threshold, the $V_{BIAS}$ LDO is turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above the switchover threshold minus the comparator hysteresis. The $EXTV_{CC}$ LDO attempts to regulate the $DRV_{CC}$ voltage to the voltage as programmed by the DRVSET pin, so while $EXTV_{CC}$ is less than this voltage, the LDO is in dropout and the $DRV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than the programmed voltage, up to an absolute maximum of 14V, $DRV_{CC}$ is regulated to the programmed voltage.

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Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from one of the LTC3899's switching regulator outputs (4.7V/7.7V ≤ $V_{OUT}$ ≤ 14V) during normal operation and from the $V_{BIAS}$ LDO when the output is out of regulation (e.g., start-up, short circuit). If more current is required through the $EXTV_{CC}$ LDO than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $DRV_{CC}$ pins. In this case, do not apply more than 10V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC} \le V_{BIAS}$.

Significant efficiency and thermal gains can be realized by powering $DRV_{CC}$ from the output, since the $V_{IN}$ current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

For 5V to 14V regulator outputs, this means connecting the $EXTV_{CC}$ pin directly to $V_{OUT}$. Tying the $EXTV_{CC}$ pin to an 8.5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + (40mA)(8.5V)(34°C/W) = 82°C$$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive $DRV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This will cause $DRV_{CC}$ to be powered from the internal $V_{BIAS}$ regulator resulting in increased power dissipation in the LTC3899 at high input voltages.
2. $EXTV_{CC}$ connected directly to the output of one of the buck regulators. This is the normal connection for a 5V to 14V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 14V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. Ensure that $EXTV_{CC} < V_{BIAS}$.
4. $EXTV_{CC}$ connected to an output-derived boost network off one of the buck regulators. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V/7.7V.

**Topside MOSFET Driver Supply ($C_B$)**

External bootstrap capacitors, $C_B$, connected to the BOOST pins supply the gate drive voltage for the topside MOSFET. The LTC3899 features an internal switch between $DRV_{CC}$ and the BOOST pin for each controller. These internal switches eliminate the need for external bootstrap diodes between $DRV_{CC}$ and BOOST. Capacitor $C_B$ in the Functional Diagram is charged through this internal switch from $DRV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the $C_B$ voltage across the gate-source of the MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, SW, rises to $V_{IN}$ and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{DRVCC}$ ($V_{BOOST} = V_{OUT} + V_{DRVCC}$ for the boost controller). The value of the boost capacitor, $C_B$, needs to be 100 times that of the total input capacitance of the topside MOSFET(s).

**Fault Conditions: Buck Current Limit and Current Foldback**

The LTC3899 includes current foldback for the buck channels to help limit load current when the output is shorted to ground. If the buck output voltage falls below 70% of its nominal output level, then the maximum sense voltage is progressively lowered from 100% to 40% of its maximum selected value. Under short-circuit conditions with very low duty cycles, the buck channel will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of the LTC3899 (≈80ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)}\left(\frac{V_{IN}}{L}\right)$$

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The resulting average short-circuit current is:

$$I_{SC} = 40\% \bullet I_{LIM(MAX)} - \frac{1}{2}\Delta I_{L(SC)}$$

### Fault Conditions: Buck Overvoltage Protection (Crowbar)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of one of the buck regulators rises much higher than nominal levels. The crowbar causes huge currents to flow, that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

A comparator monitors the buck output for overvoltage conditions. The comparator detects faults greater than 10% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the overvoltage condition persists; if $V_{OUT}$ returns to a safe level, normal operation automatically resumes.

A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

### Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self heating on chip (such as $DRV_{CC}$ short to ground), the overtemperature shutdown circuitry will shut down the LTC3899. When the junction temperature exceeds approximately 175°C, the overtemperature circuitry disables the $DRV_{CC}$ LDO, causing the $DRV_{CC}$ supply to collapse and effectively shutting down the entire LTC3899 chip. Once the junction temperature drops back to the approximately 155°C, the $DRV_{CC}$ LDO turns back on. Long-term overstress ($T_J$ > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

### Phase-Locked Loop and Frequency Synchronization

The LTC3899 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter, and a voltage-controlled oscillator (VCO). This allows the turn-on of the top MOSFET of controller 1 to be locked to the rising edge of an external clock signal applied to the PLLIN/MODE pin. The turn-on of controller 2's top MOSFET is thus 180° out of phase with the external clock. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

If the external clock frequency is greater than the internal oscillator's frequency, $f_{OSC}$, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than $f_{OSC}$, current is sunk continuously, pulling down the VCO input.

If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the internal filter capacitor, CLP, holds the voltage at the VCO input.

Note that the LTC3899 can only be synchronized to an external clock whose frequency is within range of the LTC3899's internal VCO, which is nominally 55kHz to 1MHz. This is guaranteed to be between 75kHz and 850kHz. Typically, the external clock (on the PLLIN/MODE pin) input high threshold is 1.6V, while the input low threshold is 1.1V. The LTC3899 is guaranteed to synchronize to an external clock that swings up to at least 2.5V and down to 0.5V or less.

Rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. The VCO's input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase lock and synchronization. Although it is not required that the free-running frequency be near the external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

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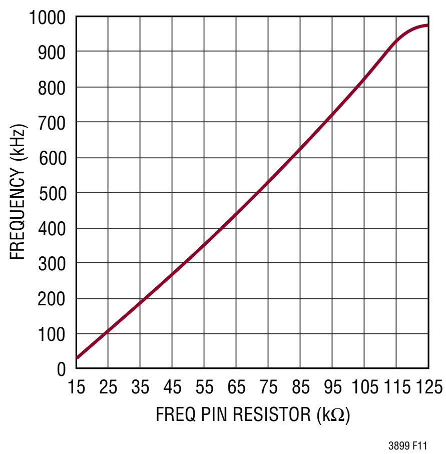


**Figure 10. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin**

Table 2 summarizes the different states in which the FREQ pin can be used.

**Table 2.**

| FREQ PIN | PLLIN/MODE PIN | FREQUENCY |
|---|---|---|
| 0V | DC Voltage | 350kHz |
| $INTV_{CC}$ | DC Voltage | 535kHz |
| Resistor to GND | DC Voltage | 50kHz to 900kHz |
| Any of the Above | External Clock 75kHz to 850kHz | Phase Locked to External Clock |

### Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3899 is capable of turning on the top MOSFET (bottom MOSFET for the boost controller). It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)\_BUCK} < \frac{V_{OUT}}{V_{IN}(f)}$$

$$t_{ON(MIN)\_BOOST} < \frac{V_{OUT} - V_{IN}}{V_{OUT}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC3899 is approximately 80ns for the bucks and 120ns for the boost. However, for the buck channels as the peak sense voltage decreases the minimum on-time gradually increases up to about 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

### Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% – (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3899 circuits: 1) IC $V_{BIAS}$ current, 2) $DRV_{CC}$ regulator current, 3) $I^2R$ losses, 4) Topside MOSFET transition losses.

1. The $V_{BIAS}$ current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. $V_{BIAS}$ current typically results in a small (<0.1%) loss.
2. $DRV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from $DRV_{CC}$ to ground. The resulting dQ/dt is a current out of $DRV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where $Q_T$ and $Q_B$ are the gate charges of the topside and bottom side MOSFETs.

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Supplying $DRV_{CC}$ from an output-derived source power through $EXTV_{CC}$ will scale the $V_{IN}$ current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of $DRV_{CC}$ current results in approximately 2.5mA of $V_{IN}$ current. This reduces the midcurrent loss from 10% or more (if the driver was powered directly from $V_{IN}$) to only a few percent.

3. $I^2R$ losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor and input and output capacitor ESR. In continuous mode the average output current flows through L and $R_{SENSE}$, but is chopped between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, $R_{SENSE}$ and ESR to obtain $I^2R$ losses. For example, if each $R_{DS(ON)} = 30m\Omega$, $R_L = 50m\Omega$, $R_{SENSE} = 10m\Omega$ and $R_{ESR} = 40m\Omega$ (sum of both input and output capacitance losses), then the total resistance is $130m\Omega$. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of $V_{OUT}$ for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the top MOSFET(s) (bottom MOSFET for the boost), and become significant only when operating at high input (output for the boost) voltages (typically 20V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7) \bullet V_{IN}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$$

Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that $C_{IN}$ has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of $20m\Omega$ to $50m\Omega$ of ESR. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

### Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, $V_{OUT}$ shifts by an amount equal to $\Delta I_{LOAD(ESR)}$, where ESR is the effective series resistance of $C_{OUT}$. $\Delta I_{LOAD}$ also begins to charge or discharge $C_{OUT}$ generating the feedback error signal that forces the regulator to adapt to the current change and return $V_{OUT}$ to its steady-state value. During this recovery time $V_{OUT}$ can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in Figure 12 circuit will provide an adequate starting point for most applications.

The ITH series $R_C$-$C_C$ filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

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Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing $R_C$ and the bandwidth of the loop will be increased by decreasing $C_C$. If $R_C$ is increased by the same factor that $C_C$ is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with $C_{OUT}$, causing a rapid drop in $V_{OUT}$. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of $C_{LOAD}$ to $C_{OUT}$ is greater than 1:50, the switch rise-time should be controlled so that the load rise-time is limited to approximately 25 • $C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

### Buck Design Example

As a design example for one channel, assume $V_{IN}$ = 12V (nominal), $V_{IN}$ = 22V (maximum), $V_{OUT}$ = 3.3V, $I_{MAX}$ = 5A, $V_{SENSE(MAX)}$ = 75mV and f = 350kHz. The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the FREQ pin to GND, generating 350kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN(NOM)}}\right)$$

A 4.7µH inductor will produce 29% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 5.73A. Increasing the ripple current will also help ensure that the minimum on-time of 80ns is not violated. The minimum on-time occurs at maximum $V_{IN}$:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f)} = \frac{3.3V}{22V(350kHz)} = 429ns$$

The equivalent $R_{SENSE}$ resistor value can be calculated by using the minimum value for the maximum current sense threshold (65mV):

$$R_{SENSE} \le \frac{65mV}{5.73A} \approx 0.01\Omega$$

Choosing 1% resistors: $R_A$ = 25k and $R_B$ = 78.7k yields an output voltage of 3.32V.

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Fairchild FDS6982S dual MOSFET results in: $R_{DS(ON)}$ = 0.035Ω/0.022Ω, $C_{MILLER}$ = 215pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{3.3V}{22V}(5A)^2\left[1+(0.005)(50°C-25°C)\right] (0.035\Omega)+(22V)^2\frac{5A}{2}(2.5\Omega)(215pF)\bullet \left(\frac{1}{6V-2.3V}+\frac{1}{2.3V}\right)(350kHz) = 308mW$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{34mV}{0.01\Omega} - \frac{1}{2}\left(\frac{80ns(22V)}{4.7\mu H}\right) = 3.21A$$

with a typical value of $R_{DS(ON)}$ and δ = (0.005/°C)(25°C) = 0.125. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = (3.21A)^2\ (1.125)\ (0.022\Omega) = 255mW$$

which is less than under full-load conditions.

## APPLICATIONS INFORMATION

$C_{IN}$ is chosen for an RMS current rating of at least 3A at temperature assuming only this channel is on. $C_{OUT}$ is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{O(RIPPLE)} = R_{ESR} (\Delta I_L) = 0.02\Omega\ (1.45A) = 29mV_{P-P}$$

### PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. Figure 11 illustrates the current waveforms present in the various branches of the 2-phase synchronous buck regulators operating in the continuous mode. Check the following in your layout:

1. Are the top N-channel MOSFETs MTOP1 and MTOP2 located within 1cm of each other with a common drain connection at $C_{IN}$? Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.
2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of $C_{DRVCC}$ must return to the combined $C_{OUT}$ (–) terminals. The path formed by the top N-channel MOSFET, Schottky diode and the $C_{IN}$ capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.
3. Does the LTC3899 $V_{FB}$ pins' resistive divider connect to the (+) terminal of $C_{OUT}$? The resistive divider must be connected between the (+) terminal of $C_{OUT}$ and signal ground. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).

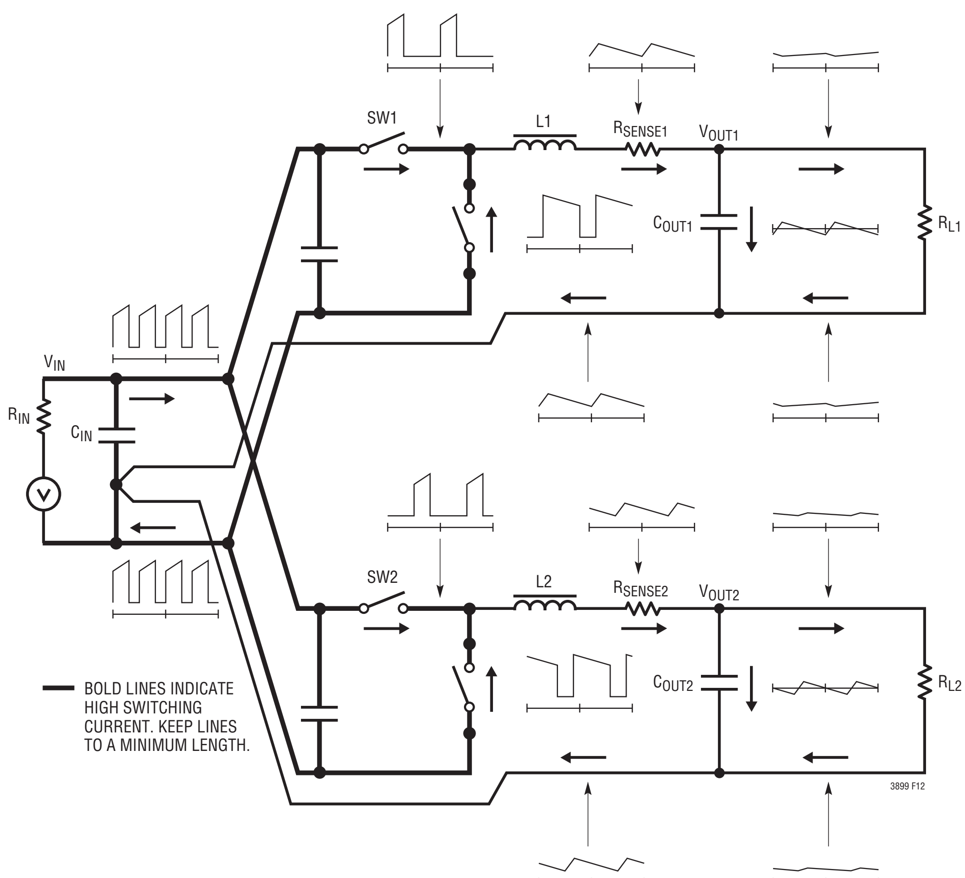


**Figure 11. Branch Current Waveforms for Bucks**

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## APPLICATIONS INFORMATION

4. Are the $SENSE^–$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^–$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
5. Is the $DRV_{CC}$ and decoupling capacitor connected close to the IC, between the $DRV_{CC}$ and the ground pin? This capacitor carries the MOSFET drivers' current peaks.
6. Keep the switching nodes (SW1, SW2, SW3), top gate (TG1, TG2, TG3), and boost nodes (BOOST1, BOOST2, BOOST3) away from sensitive small-signal nodes, especially from the opposites channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the LTC3899 and occupy minimum PC trace area.
7. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $DRV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC.

**PC Board Layout Debugging**

Start with one controller at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 25% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both should multiple controllers be turned on at the same time. A particularly difficult region of operation is when one buck channel is nearing its current comparator trip point when the other buck channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce $V_{IN}$ from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering $V_{IN}$ while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between $C_{IN}$, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

# TYPICAL APPLICATIONS

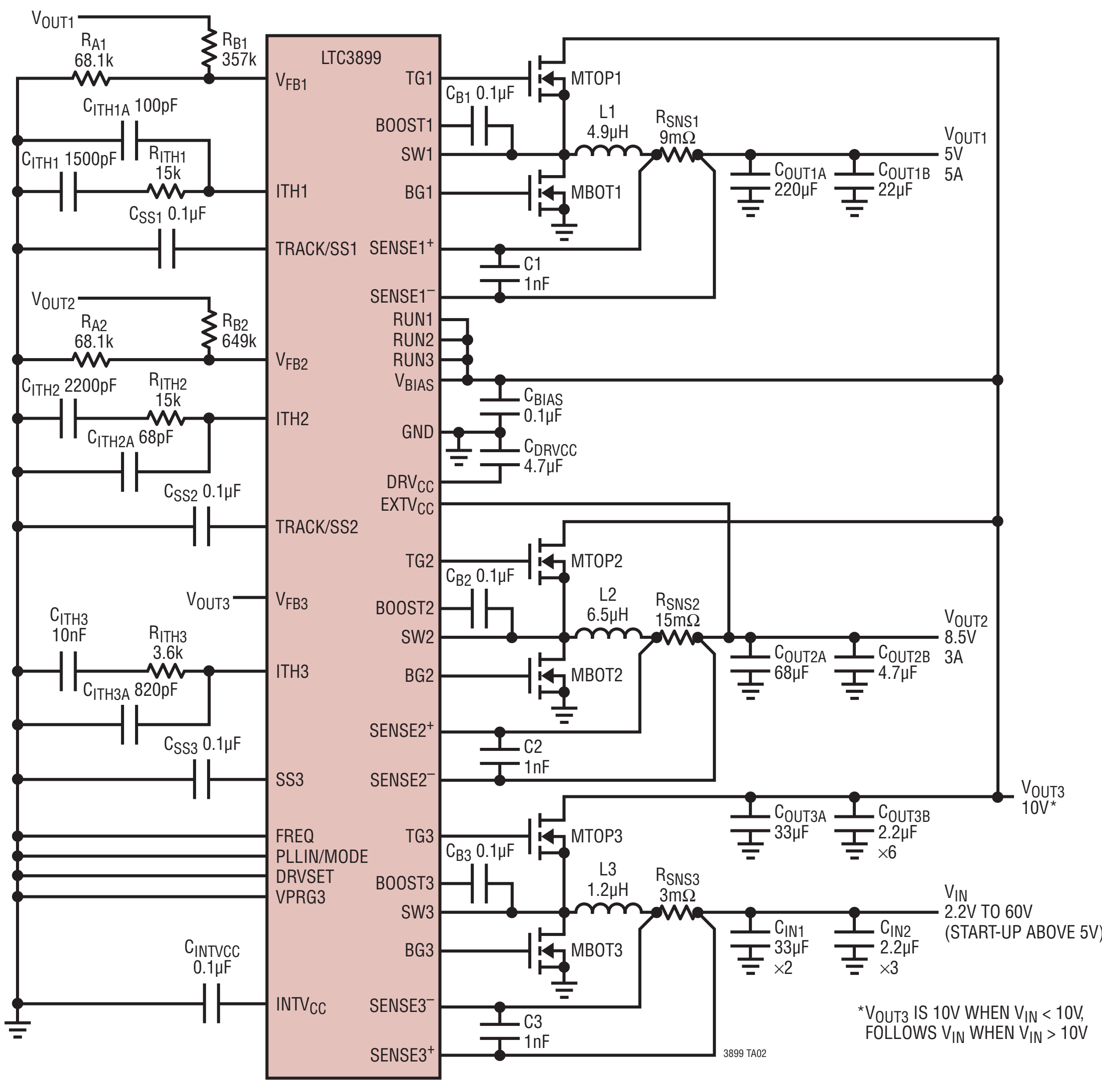
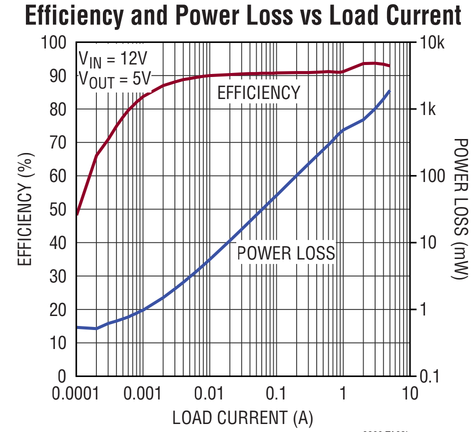



**Figure 12. High Efficiency Wide Input Range Dual 5V/8.5V Converter**

MTOP1, MBOT1: BSZ123N08NS3
MTOP2, MBOT2: BSZ123N08NS3
MTOP3, MBOT3: BSC042NE7NS3
L1: WURTH 744314490
L2: WURTH 744314650
L3: WURTH 744325120
$C_{OUT1A}$: SANYO 6TPB220ML
$C_{OUT2A}$: SANYO 10TPC68M
$C_{IN1}$, $C_{OUT3A}$: SUNCON 63HVP33M

**Efficiency and Power Loss vs Load Current**

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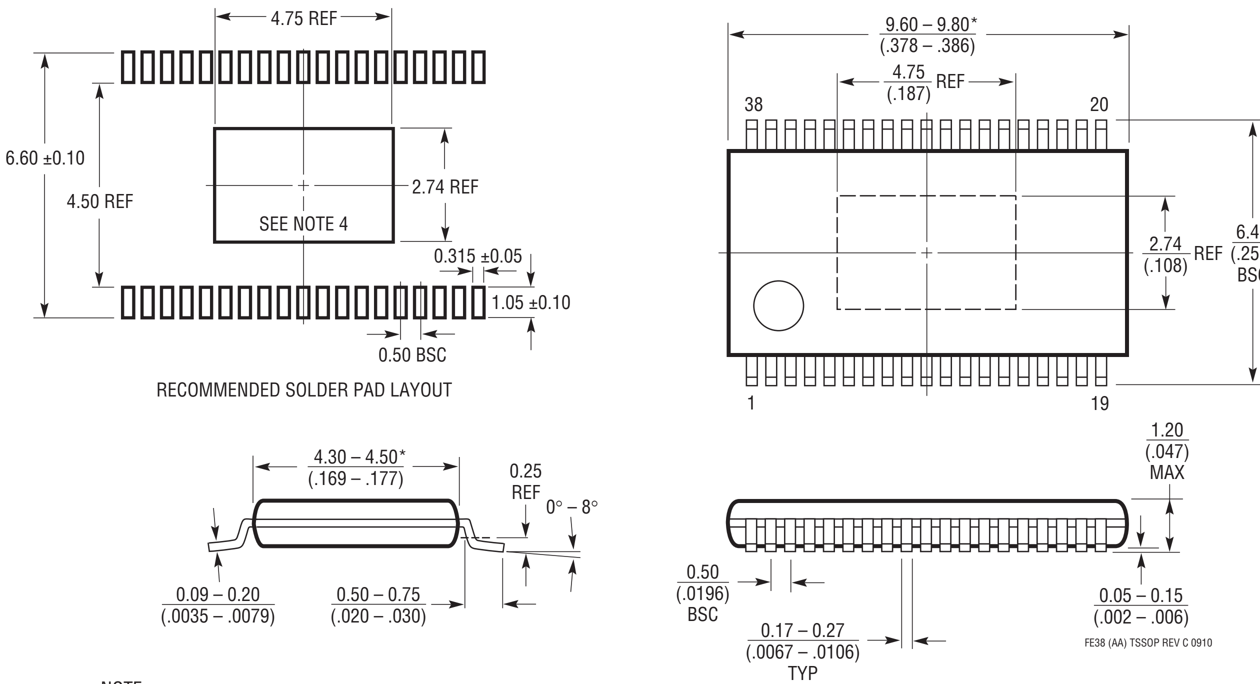
# PACKAGE DESCRIPTION

**FE Package**
**38-Lead Plastic TSSOP (4.4mm)**
(Reference LTC DWG # 05-08-1772 Rev C)
**Exposed Pad Variation AA**

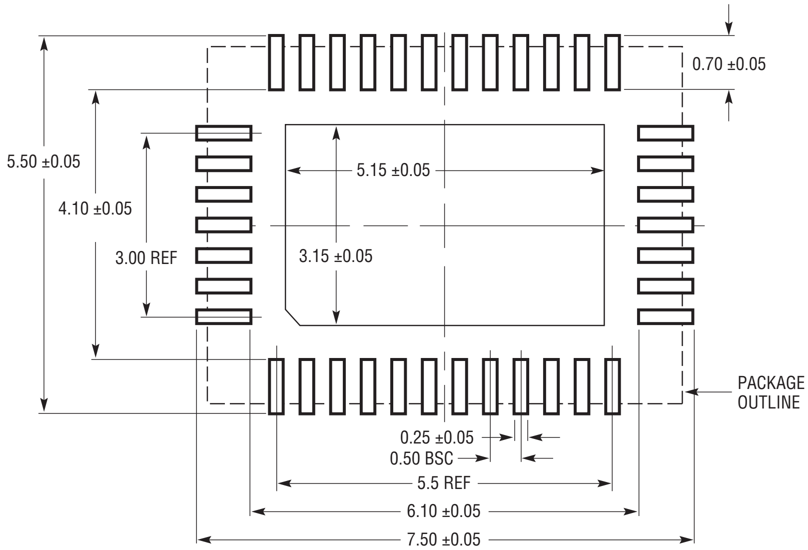



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

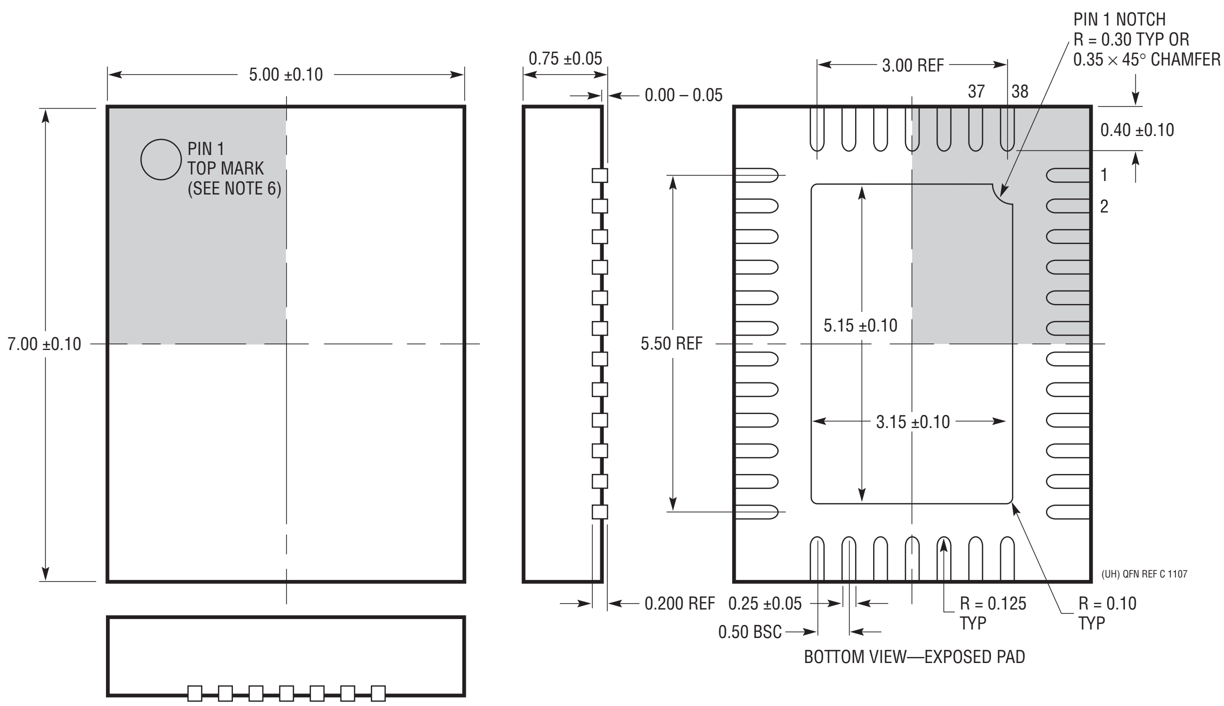
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

# PACKAGE DESCRIPTION

**UHF Package**
**38-Lead Plastic QFN (5mm × 7mm)**
(Reference LTC DWG # 05-08-1701 Rev C)




RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 09/15 | Clarified $INTV_{CC}$ Pin Functions. | 11 |
| | | SW1, SW2, SW3 pin callouts corrected. | 11 |
| | | Functional Diagrams modified. | 13, 14 |
| B | 11/22 | Added automotive products. | 1, 3 |

# TYPICAL APPLICATION

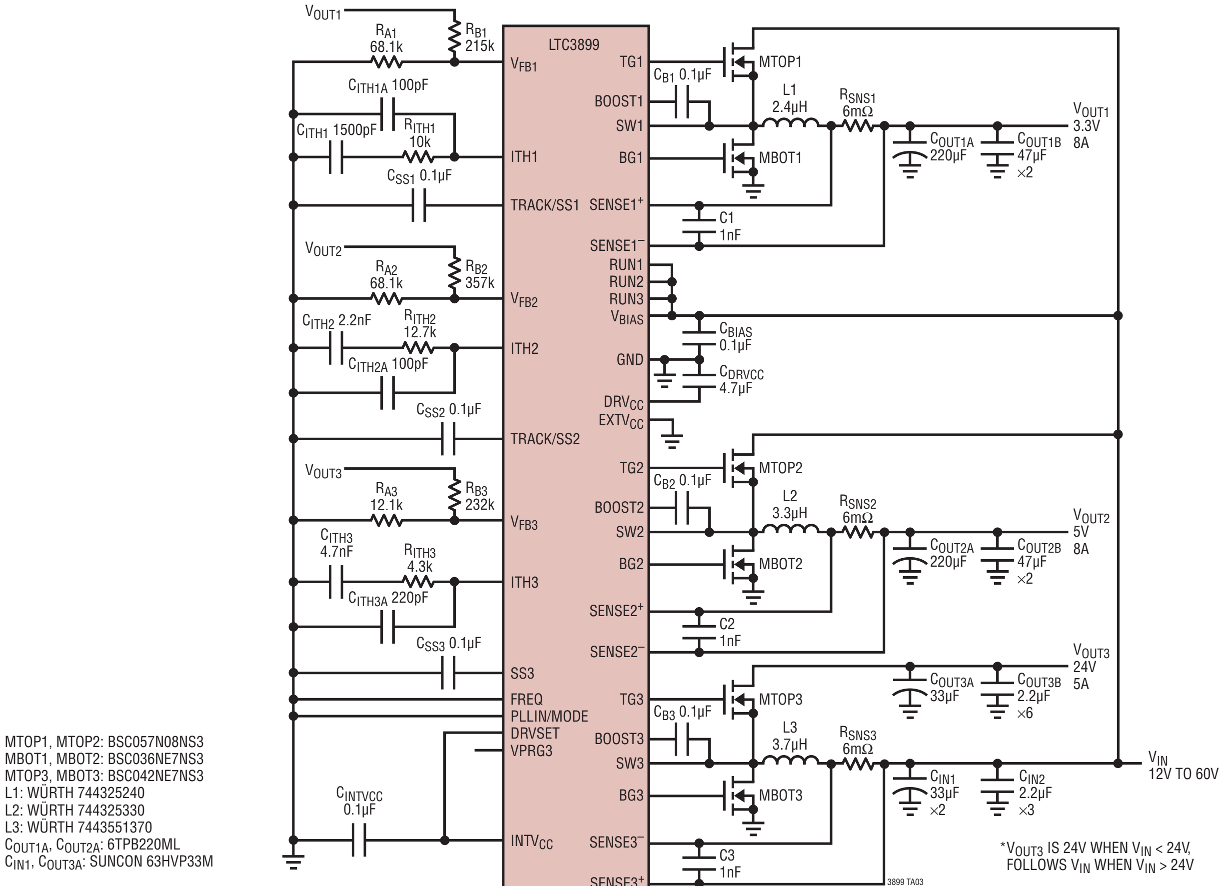



**Figure 13. High Efficiency Triple 24V/3.3V/5V Converter with 10V Gate Drive**

# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC3859AL | Triple Output, Buck/Buck/Boost Synchronous Controller with 28µA Burst Mode $I_Q$ | 4.5V (Down to 2.5V After Start-Up) ≤ $V_{IN}$ ≤ 38V, $V_{OUT}$ Up to 60V, $I_Q$ = 28µA, Buck $V_{OUT}$ Range: 0.8V to 24V, Boost $V_{OUT}$ Up to 60V |
| LTC3892/LTC3892-1 | 60V, Low $I_Q$, Dual 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle | PLL Fixed Frequency 50kHz to 900kHz, 4.5V ≤ $V_{IN}$ ≤ 60V, 0.8V ≤ $V_{OUT}$ ≤ 0.99$V_{IN}$, $I_Q$ = 29µA |
| LTC3769 | Low $I_Q$ Synchronous Step-Up DC/DC Controller | 4.5V (Down to 2.5V After Start-Up) ≤ $V_{IN}$ ≤ 60V, $V_{OUT}$ Up to 60V, $I_Q$ = 28µA, PLL Fixed Frequency 50kHz to 900kHz, 4mm × 4mm QFN-24, TSSOP-20E |
| LTC3784 | Low $I_Q$, Multiphase, Dual Channel Single Output Synchronous Step-Up DC/DC Controller | 4.5V (Down to 2.5V After Start-Up) ≤ $V_{IN}$ ≤ 60V, $V_{OUT}$ Up to 60V, PLL Fixed Frequency 50kHz to 900kHz , $I_Q$ = 28µA |
| LTC3890/LTC3890-1 LTC3890-2/LTC3890-3 | 60V, Low $I_Q$, Dual 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle | PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ $V_{IN}$ ≤ 60V, 0.8V ≤ $V_{OUT}$ ≤ 24V, $I_Q$ = 50µA |
| LTC3891 | 60V, Low $I_Q$, Synchronous Step-Down DC/DC Controller with 99% Duty Cycle | PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ $V_{IN}$ ≤ 60V, 0.8V ≤ $V_{OUT}$ ≤ 24V, $I_Q$ = 50µA |
| LTC3857/LTC3857-1 LTC3858/LTC3858-1 | Low $I_Q$, Dual Output 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle | Phase-Lockable Fixed Operating Frequency 50kHz to 900kHz, 4V ≤ $V_{IN}$ ≤ 38V, 0.8V ≤ $V_{OUT}$ ≤ 24V, $I_Q$ = 50µA/170µA |
| LTC3864 | 60V, Low $I_Q$, High Voltage DC/DC Controller with 100% Duty Cycle | Fixed Frequency 50kHz to 850kHz, 3.5V ≤ $V_{IN}$ ≤ 60V, 0.8V ≤ $V_{OUT}$ ≤ $V_{IN}$, $I_Q$ = 40µA, MSOP-12E, 3mm × 4mm DFN-12 |
| LT®8705 | 80V $V_{IN}$ and $V_{OUT}$ Synchronous 4-Switch Buck-Boost DC/DC Controller | $V_{IN}$ Range: 2.8V (Need $EXTV_{CC}$ > 6.4V) to 80V, $V_{OUT}$ Range: 1.3V to 80V; 4 Regulation Loops |

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