Hot Swappable Supercapacitor Charger, Backup Controller and System Monitor

FEATURES

- **Integrated Hot Swap Controller with Circuit Breaker**
- **High Efficiency Synchronous Step-Down CC/CV Charging of One to Four Series Supercapacitors**
- **Step-Up Mode in Backup Provides Greater Utilization of Stored Energy in Supercapacitors**
- **16-Bit ADC for Monitoring System Voltages/ Currents, Capacitance and ESR**
- **Programmable Undervoltage and Overvoltage Thresholds to 35V**
- V_{IN}: 4.5V to 35V, $V_{CAP(n)}$: Up to 5V per Capacitor, Charge/Backup Current: >10A
- Programmable Input Current Limit Prioritizes System Load Over Capacitor Charge Current
- All N-FET Charger Controller and PowerPath™ Controller
- Compact 44-Lead 4mm × 7mm QFN Package

APPLICATIONS

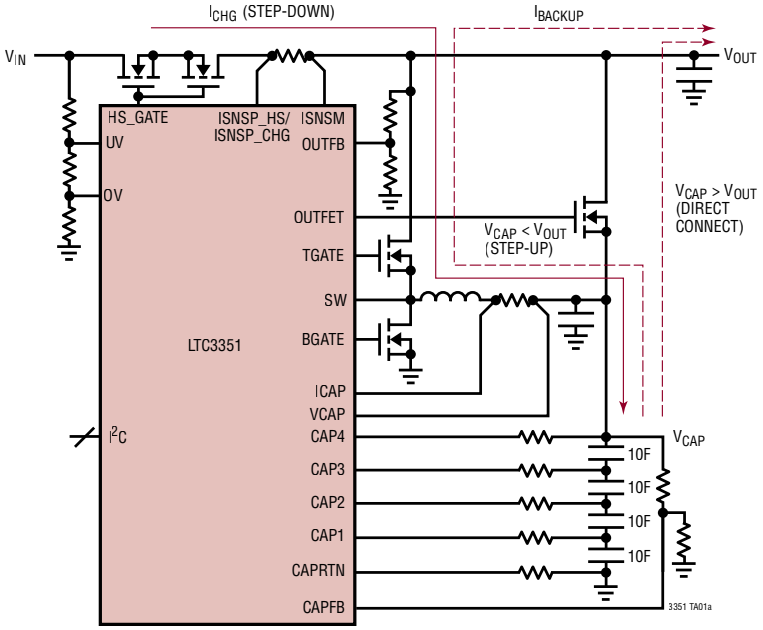
- Swappable PCIE Cards with NVM
- High Current 12V Ride-Through UPS
- Servers/Mass Storage/High Availability Systems

DESCRIPTION

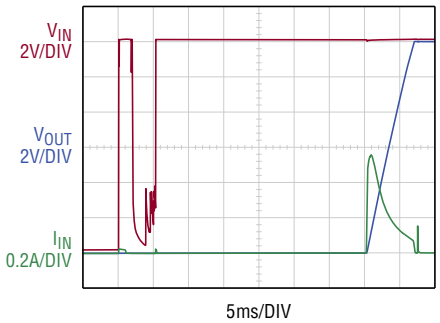
The LTC®3351 is a backup power controller that charges and monitors a series stack of one to four supercapacitors. The LTC3351's synchronous step-down controller drives N-channel MOSFETs for constant current/constant voltage charging with programmable input current limit. In addition, the step-down converter runs in reverse as a step-up converter to deliver power from the supercapacitor stack to the backup supply rail. Internal balancers eliminate the need for external balance resistors and each capacitor has a shunt regulator for overvoltage protection.

The LTC3351 monitors system voltages, currents, stack capacitance and ESR which can all be read over the I²C/SMBus port. The hot swap controller uses N-channel MOSFETs for inrush control and a low loss path from the input to the output. The ideal diode controller uses an N-channel MOSFET for a low loss power path from the supercapacitors to the output. The LTC3351 is available in a thermally enhanced low profile 44-lead 4mm × 7mm × 0.75mm QFN surface mount package.

TYPICAL APPLICATION



Example Hot Swap from 12V

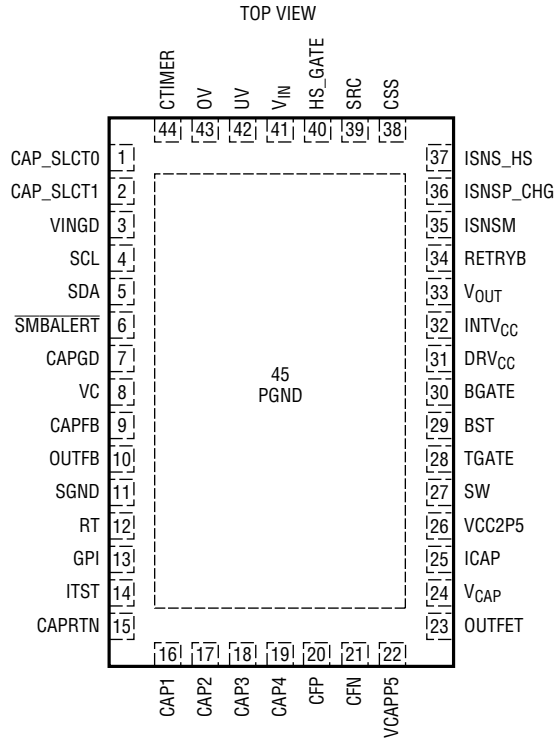


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_{OUT}, ISNSP_HS, ISNSP_CHG, ISNSM, UV, OV, RETRYB, OUTFB ..... –0.3V to 40V
VCAP ..... –0.3V to 22V
CAP4-CAP3, CAP3-CAP2, CAP2-CAP1, CAP1-CAPRTN ..... –0.3V to 5.5V
DRV_{CC}, CAPFB, $\overline{SMBALERT}$, CAPGD, VINGD, GPI, SDA, SCL ..... –0.3V to $INTV_{CC}$ + 0.3V
BST ..... –0.3V to 45.5V
CAP_SLCT0, CAP_SLCT1 ..... –0.3V to VCC2P5 + 0.3V
BST to SW ..... –0.3V to 5.5V
ISNSP_HS to ISNSM, ISNSP_CHG to ISNSM, ICAP to VCAP ... –0.3V to 0.3V
I_{INTVCC} 100mA
$I_{CAP(1,2,3,4)}$, I_{CAPRTN} 600mA
I_{CAPGD}, I_{VINGD} , $I_{\overline{SMBALERT}}$ 10mA
Operating Junction Temperature Range (Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFF PACKAGE
44-LEAD (4mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 36.4°C/W, θ_{JC} = 2.6°C/W
EXPOSED PAD (PIN 45) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3351EUFF#PBF	LTC3351EUFF#TRPBF	3351	44-Lead (4mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3351IUFF#PBF	LTC3351IUFF#TRPBF	3351	44-Lead (4mm × 7mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, $VDRV_{CC}$ = $VINTV_{CC}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator							
V_{IN}	Input Supply Voltage		●	4.5		35	V
I_Q	Input Quiescent Current, I_{VOUT} (Note 4)				2.25		mA
$V_{CAPFBHI}$	Maximum Regulated V_{CAP} Feedback Voltage	Full Scale (1111b)	●	1.188	1.2	1.212	V
V_{CAPFB_DEF}	Default V_{CAPFB_DAC} Setting	(1010b)	●	0.997	1.0125	1.028	V
$V_{CAPFBLO}$	Minimum Regulated V_{CAP} Feedback Voltage	Zero Scale (0000b)	●	0.625	0.6375	0.650	V
I_{CAPFB}	CAPFB Input Leakage Current	V_{CAPFB} = 1.2V	●	–50		50	nA
V_{OUTFB}	Regulated V_{OUT} Feedback Voltage		●	1.182	1.2	1.218	V
$V_{OUTFB(TH)}$	OUTFET Turn-Off Threshold	Falling Threshold		1.27	1.3	1.33	V
I_{OUTFB}	OUTFB Input Leakage Current	V_{OUTFB} = 1.2V	●	–50		50	nA
V_{OUTBST}	V_{OUT} Voltage in Step-Up Mode	V_{IN} = 0V	●	4.5		35	V
V_{UVLO}	$INTV_{CC}$ Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	 3.85	4.3 4	4.45	V V
$V_{DRVUVLO}$	DRV_{CC} Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	 3.75	4.2 3.9	4.35	V V
V_{DUVLO}	V_{OUT} – V_{CAP} Differential Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	160 55	200 90	240 125	mV mV
V_{OVLO}	Switcher V_{IN} Overvoltage Lockout	Rising Threshold Falling Threshold	● ●	37.7 36.3	38.6 37.2	39.5 38.1	V V
V_{VCAPP5}	Charge Pump Output Voltage	Relative to VCAP, 0V < V_{CAP} < 20V			5		V
Input Current Sense Amplifier							
V_{SNSI}	Regulated Input Current Sense Voltage (ISNSP_CHG – ISNSM)		●	31.04	32	32.96	mV
Charge Current Sense Amplifier							
V_{SNSC}	Regulated Charge Current Sense Voltage (I_{CAP} – V_{CAP})	V_{CAP} = 10V, Charge Mode	●	31.04	32	32.96	mV
V_{CMC}	Common Mode Range (ICAP, VCAP)			0		20	V
V_{PEAK}	Peak Inductor Current Sense Voltage	Active in Both Step-Up/Step-Down Modes	●	51	58	65	mV
I_{ICAP}	ICAP Pin Current	Step-Down Mode, VSNSC = 32mV Step-Up Mode, VSNSC = 32mV			27 100		µA µA
Error Amplifier							
g_{MV}	V_{CAP} Voltage Loop Transconductance				1		mmho
g_{MC}	Charge Current Loop Transconductance				64		µmho
g_{MI}	Input Current Loop Transconductance				64		µmho
g_{MO}	V_{OUT} Voltage Loop Transconductance				350		µmho
Oscillator							
f_{SW}	Switching Frequency	RT = 107k	 ●	495 490	500 500	505 510	kHz kHz
	Maximum Programmable Frequency	RT = 53.6k			1		MHz
	Minimum Programmable Frequency	RT = 267k			200		kHz
DCMAX	Maximum Duty Cycle	Step-Down Mode, 53.6k < R_T < 267k Step-Up Mode, 53.6k < R_T < 267k		97 87	98 93	99.5	% %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, $VDRV_{CC}$ = $VINTV_{CC}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Drivers							
R_{UP-TG}	TGATE Pull-Up On-Resistance				2		Ω
$R_{DOWN-TG}$	TGATE Pull-Down On-Resistance				0.6		Ω
R_{UP-BG}	BGATE Pull-Up On-Resistance				2		Ω
$R_{DOWN-BG}$	BGATE Pull-Down On-Resistance				0.6		Ω
t_{NO}	Non-Overlap Time				50		ns
$t_{ON(MIN)}$					85		ns
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	5.2V < V_{IN} < 35V			5		V
DV_{INTVCC}	Load Regulation	I_{INTVCC} = 50mA			–1.5	–2.5	%
Ideal Diode							
V_{FTO}	Fast On Threshold Voltage				65		mV
V_{FR}	Forward Regulation Voltage				30		mV
V_{RTO}	Reverse Turn Off Threshold Voltage				–30		mV
UV/OV Comparator							
$V_{UV/OVI(TH)}$	UV/OV Input Threshold (Rising Edge)		●	1.182	1.2	1.218	V
$V_{UV/OVI(HYS)}$	UV/OV Hysteresis				60		mV
$I_{UV/OV}$	UV/OV Input Leakage Current	$V_{UV/OV}$ = 0.5V	●	–50		50	nA
V_{VINGD}	VINGD Output Low Voltage	I_{SINK} = 5mA			300		mV
I_{VINGD}	VINGD High-Z Leakage Current	VINGD = 5V	●			1	µA
	UV Falling to VINGD Low Delay				1		µs
CAPGD							
$V_{CAPFB(TH)}$	CAPGD Rising Threshold as % of Regulated V_{CAP} Feedback Voltage	vcapfb_dac = Full Scale (1111b)	●	90	92	94	%
$V_{CAPFB(HYS)}$	CAPGD Hysteresis at CAPFB as a % of Regulated V_{CAP} Feedback Voltage	vcapfb_dac = Full Scale (1111b)			2.5		%
V_{CAPGD}	CAPGD Output Low Voltage	I_{SINK} = 5mA			200		mV
I_{CAPGD}	CAPGD High-Z Leakage Current	V_{CAPGD} = 5V	●			1	µA
Analog-to-Digital Converter							
V_{RES}	Measurement Resolution				16		Bits
V_{GPI}	General Purpose Input Voltage Range	Unbuffered Buffered		0 0		5 3.5	V V
I_{GPI}	General Purpose Input Pin Leakage Current	Buffered Input				1	µA
R_{GPI}	GPI Pin Resistance	Buffer Disabled			1.25		MΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, $VDRV_{CC}$ = $VINTV_{CC}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Measurement System Error							
V_{ERR}	Measurement Error (Note 5)	V_{IN} = 0V V_{IN} = 30V				100 1.5	mV %
		V_{OUT} = 5V V_{OUT} = 30V				100 1.5	mV %
		V_{CAP} = 0V V_{CAP} = 10V				100 1.5	mV %
		V_{GPI} = 0V, Unbuffered V_{GPI} = 5V, Unbuffered				2 1	mV %
		V_{CAP1} = 0V V_{CAP1} = 2V				2 1	mV %
		V_{CAP2} = 0V V_{CAP2} = 2V				2 1	mV %
		V_{CAP3} = 0V V_{CAP3} = 2V				2 1	mV %
		V_{CAP4} = 0V V_{CAP4} = 2V				2 1	mV %
		V_{SNSI} = 0mV V_{SNSI} = 32mV				200 2	µV %
		V_{SNSC} = 0mV V_{SNSC} = 32mV				200 2	µV %
CAP1 to CAP4							
R_{SHNT}	Shunt Resistance				0.5		Ω
DVCAPMAX	Maximum Shunt Operating Voltage					3.6	V
Programming Pins							
V_{ITST}	ITST Voltage	R_{TST} = 20Ω	●	1.182	1.2	1.209	V
I^2C/SMBus – SDA, SCL, SMBALERT							
$I_{IL,SDA,SCL}$	Input Leakage Low			–1		1	µA
$I_{IH,SDA,SCL}$	Input Leakage High			–1		1	µA
V_{IH}	Input High Threshold			1.5			V
V_{IL}	Input Low Threshold					0.8	V
f_{SCL}	SCL Clock Frequency					400	kHz
t_{LOW}	Low Period of SCL Clock			1.3			µs
t_{HIGH}	High Period of SCL Clock			0.6			µs
t_{BUF}	Bus Free Time Between Start and Stop Conditions			1.3			µs
$t_{HD,STA}$	Hold Time, After (Repeated) Start Condition			0.6			µs
$t_{SU,STA}$	Setup Time After a Repeated Start Condition			0.6			µs
$t_{SU,STO}$	Stop Condition Set-Up Time			0.6			µs
$t_{HD,DATO}$	Output Data Hold Time			0		900	ns
$t_{HD,DATI}$	Input Data Hold Time			0			ns
$t_{SU,DAT}$	Data Set-Up Time			100			ns
t_{SP}	Input Spike Suppression Pulse Width					50	ns
$V_{SMBALERT}$	SMBALERT Output Low Voltage	I_{SINK} = 5mA			200		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, $VDRV_{CC}$ = $VINTV_{CC}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{SMBALERT}$	SMBALERT High-Z Leakage Current	$V_{SMBALERT}$ = 5V	●			1	µA
Hot Swap Controller							
$V_{IN(UVLO\_HS)}$	Hot Swap Input Supply Undervoltage Lockout	V_{IN} rising, Hot Swap operation	●	3.7	3.85	4	V
$V_{ILIM(TH)}$	Current Limit Threshold (ISNS_HS-ISNSM)	V_{OUT} < V_{IN} – 11V V_{OUT} = V_{IN}	● ●	7 46	10 48	13 50	mV mV
$I_{(OV,UV,RETRYB)}$	OV, UV, RETRYB Pin Input Current		●	–50	0	50	nA
$V_{TH(RETRYB)}$	RETRYB Threshold		●	185	200	215	mV
$V_{TIMER(TH)}$	CTIMER Pin Threshold	Rising Falling	●	1.188	1.2 0.3	1.212	mV mV
$I_{TIMER(DN)}$	CTIMER Pull-Down Current		●	1.4	2	2.6	µA
$I_{TIMER(UP)}$	CTIMER Pull-Up Current		●	320	400	480	µA
$I_{TIMER(RATIO)}$	CTIMER Pull-Down/Pull-Up Current		●		0.5	0.6	%
$I_{HS\_GATE(UP)}$	HS_GATE Pull-Up Current		●	16	24	30	µA
$I_{HS\_GATE(FST)}$	HS_GATE Fast Pull-Down Resistance	V_{HS_GATE} = V_{OUT}			25		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3351 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3351E is guaranteed to meet specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3351I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} = 36.4°C/W for the UFF package.

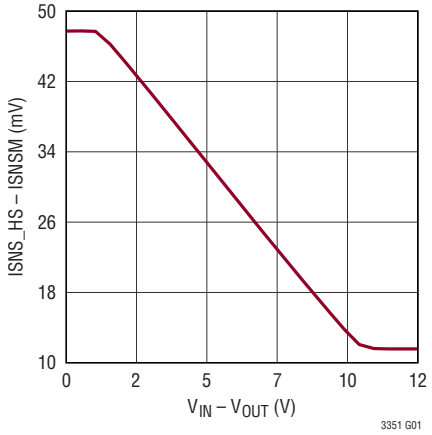
Note 3: The LTC3351 includes over temperature protection that is intended to protect the device during momentary overload conditions. When over temperature protection is active the switcher is shutdown. Junction temperature will exceed 125°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

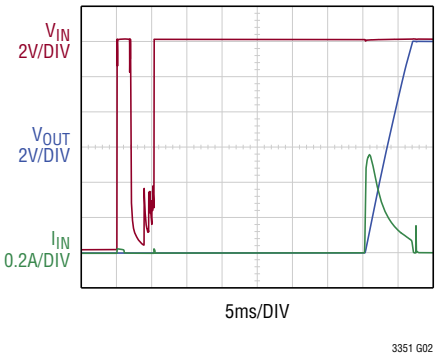
Note 5: Measurement error is the magnitude of the difference between the actual measured value and the ideal value. V_{SNSI} is the voltage between I_{SNS_CHG} and I_{SNSM}, representing input current. V_{SNSC} is the voltage between I_{CAP} and V_{CAP}, representing charge current. Error for V_{SNSI} and V_{SNSC} is expressed in µV, a conversion to an equivalent current may be made by dividing by the sense resistors, R_{SNSI} and R_{SNSC}, respectively.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

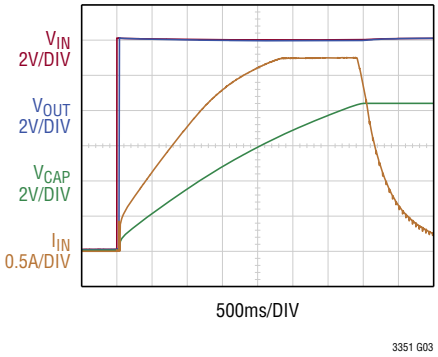
Hot Swap Current Limit Fold-Back Curve



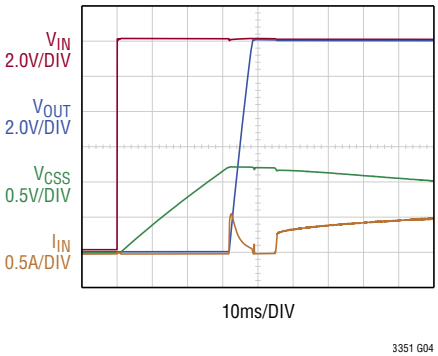
Example Hot Swap, 12V



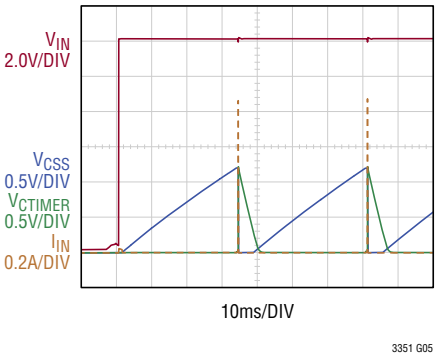
Hot Swap and Full Charge Cycle



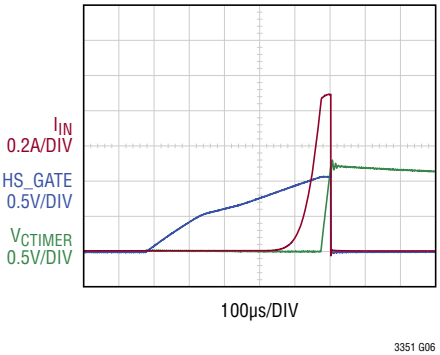
Hot Swap and Begin Charge



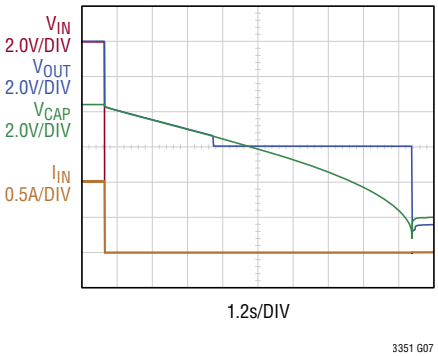
Hot Swap Startup into Shorted Output



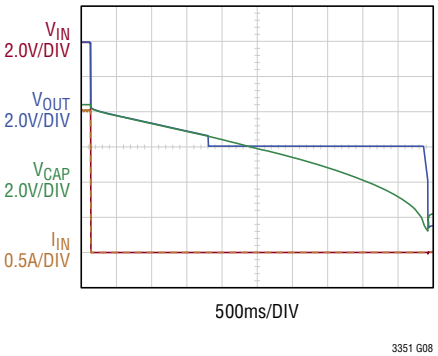
Hot Swap Short Detailed



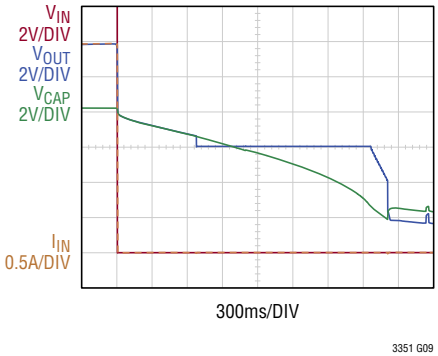
Backup Operation, 1A



Backup Operation, 2A

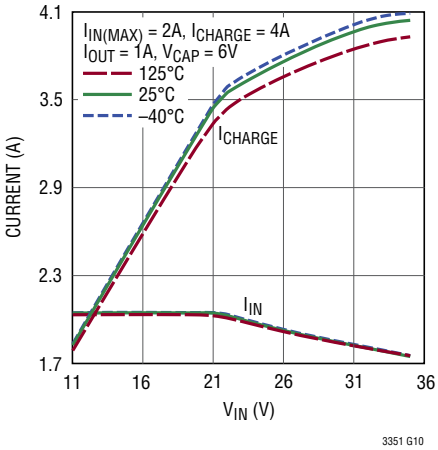


Backup Operation, 3.5A

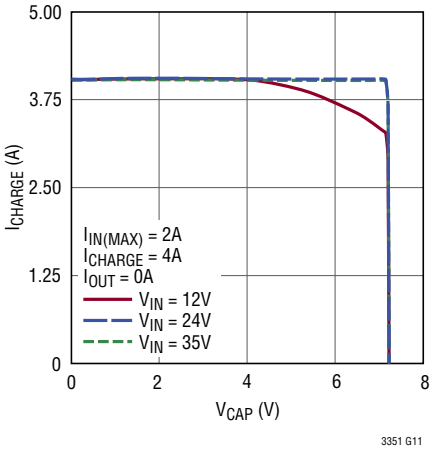


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

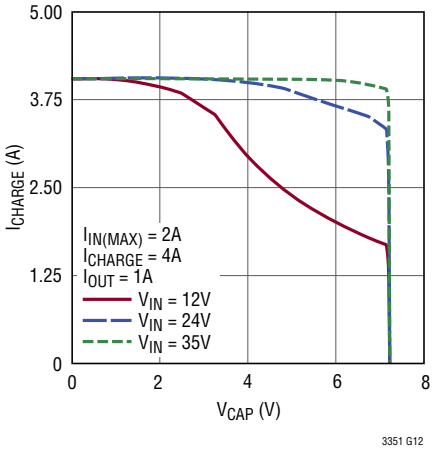
I_{IN} and I_{CHARGE} vs V_{IN}



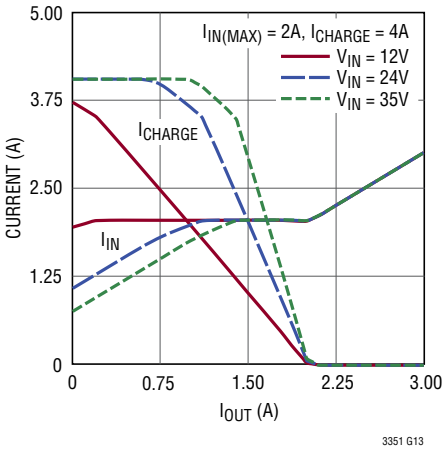
I_{CHARGE} vs V_{CAP}



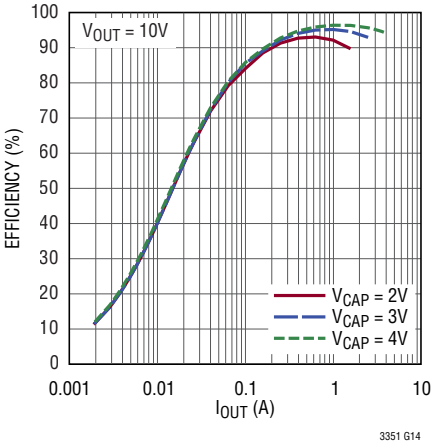
I_{CHARGE} vs V_{CAP}



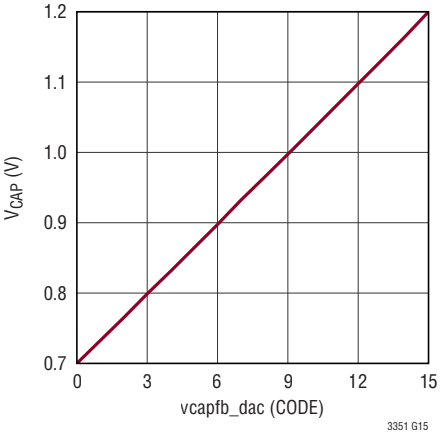
I_{IN} and I_{CHARGE} vs I_{OUT}



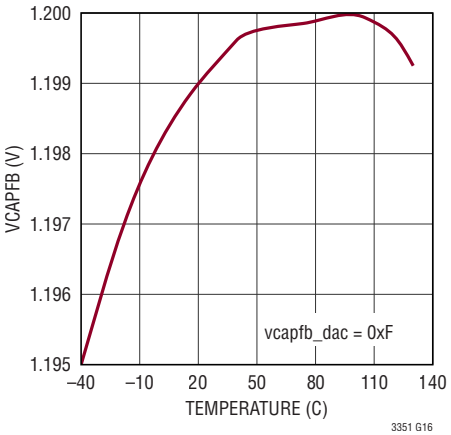
Efficiency in Boost Mode



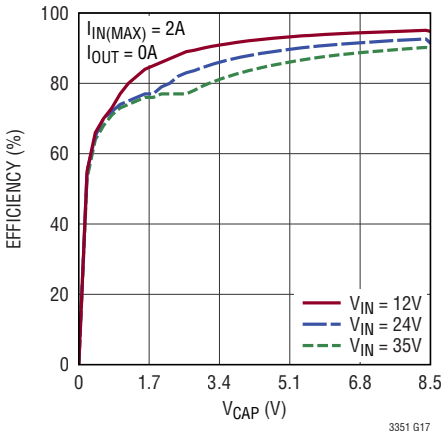
V_{CAP} vs vcapfb_dac



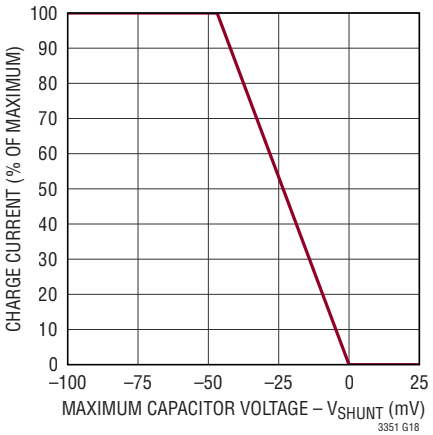
V_{CAP} vs Temperature



Charger Efficiency vs V_{CAP}



Charge Current vs Shunt Voltage



PIN FUNCTIONS

CAP_SLCT0, CAP_SLCT1 (Pins 1, 2): CAP_SLCT0 and CAP_SLCT1 set the number of super-capacitors used. Refer to Table 1 in the Applications Information section.

VINGD (Pin 3): Power-Fail Status Output. This open-drain output is pulled low when V_{OUT} is not powered from V_{IN}.

SCL (Pin 4): Clock Pin for the I^2C/SMBus Serial Port.

SDA (Pin 5): Bidirectional Data Pin for the I^2C/SMBus Serial Port.

SMBALERT (Pin 6): Interrupt Output. This open-drain output is pulled low when an alarm threshold is exceeded and will remain low until the acknowledgement of the part's response to an SMBus ARA.

CAPGD (Pin 7): Capacitor Power Good. This open-drain output is pulled low when CAPFB is below $V_{CAPFB(TH)}$.

VC (PIN 8): Control Voltage Pin. This is the compensation node for the charge current, input current, supercapacitor stack voltage and output voltage control loops. An RC network is needed between VC and SGND. There is an internal compensation resistor in series with this pin. It is 1kΩ in buck mode and 2kΩ in boost mode. Nominal voltage range for this pin is 1V to 3V.

CAPFB (Pin 9): Capacitor Stack Feedback Pin. This pin closes the feedback loop for constant voltage regulation. An external resistor divider between V_{CAP} and SGND with the center tap connected to CAPFB programs the final supercapacitor stack voltage. This pin is nominally equal to the output of the V_{CAP} DAC when the synchronous controller is charging in constant voltage mode.

OUTFB (Pin 10): Step-Up Mode Feedback Pin. This pin closes the feedback loop for voltage regulation of V_{OUT} during input power failure using the synchronous controller in step-up mode. An external resistor divider between V_{OUT} and SGND with the center tap connected to OUTFB programs the minimum backup supply rail voltage when input power is unavailable. This pin is nominally 1.2V when in backup and the synchronous controller is not in current limit. To disable step-up mode tie OUTFB to $INTV_{CC}$.

SGND (Pin 11): Signal Ground. All small-signal and compensation components should be connected to this pin, which in turn connects to PGND. SGND should connect to PGND on top metal under the LTC3351. PGND should be connected to the ground plane with vias under the exposed pad (pin 45). This should be the only connection between SGND and the ground plane.

RT (Pin 12): Timing Resistor. The switching frequency of the synchronous controller is set by placing a resistor, RT, from this pin to SGND. This resistor is always required. If not present the synchronous controller will not start.

GPI (Pin 13): General Purpose Input. The voltage on this pin is digitized directly by the ADC. For high impedance inputs an internal buffer can be selected and used to drive the ADC. The GPI pin can be connected to a negative temperature coefficient (NTC) thermistor to monitor the temperature of the supercapacitor stack. A low drift bias resistor is required from $INTV_{CC}$ to GPI and a thermistor is required from GPI to ground. Connect GPI to SGND if not used. Read the digitized voltage on this pin in the meas_gpi register.

ITST (Pin 14): Programming Pin for Capacitance Test Current. This current partially discharges the capacitor stack at a precise rate for capacitance measurement. This pin servos to 1.2V during a capacitor measurement. A resistor, RTST, from this pin to SGND programs the test current. The resistor on this pin must be at least 20Ω. Current flows from VCAP4 to this pin during this test and must not dissipate more than 300mW in the IC.

CAPRTN (Pin 15): Capacitor Stack Shunt Return Pin. Connect this pin to the grounded bottom plate of the first supercapacitor in the stack through a shunt resistor.

CAP1 (Pin 16): First Supercapacitor Pin. The top plate of the first supercapacitor and the bottom plate of the second supercapacitor are connected to this pin through a shunt resistor. CAP1 and CAPRTN are used to measure the voltage across the first supercapacitor and shunt current around the capacitor to provide balancing and prevent overvoltage. The voltage between this pin and CAPRTN is digitized and is read in the meas_vcap1 register.

PIN FUNCTIONS

CAP2 (Pin 17): Second Supercapacitor Pin. The top plate of the second supercapacitor and the bottom plate of the third supercapacitor are connected to this pin through a shunt resistor. CAP2 and CAP1 are used to measure the voltage across the second supercapacitor and to shunt current around the capacitor to provide balancing and prevent overvoltage. If not used, this pin should be shorted to CAP1. The voltage between this pin and CAP1 is digitized and is read in the meas_vcap2 register.

CAP3 (Pin 18): Third Supercapacitor Pin. The top plate of the third supercapacitor and the bottom plate of the fourth supercapacitor are connected to this pin through a shunt resistor. CAP3 and CAP2 are used to measure the voltage across the third supercapacitor and shunt current around the capacitor to provide balancing and prevent overvoltage. If not used, this pin should be shorted to CAP2. The voltage between this pin and CAP2 is digitized and is read in the meas_vcap3 register.

CAP4 (Pin 19): Fourth Supercapacitor Pin. The top plate of the fourth supercapacitor is connected to this pin through a shunt resistor. CAP4 and CAP3 are used to measure the voltage on the capacitor and shunt current around the supercapacitor to provide balancing and prevent overvoltage. If not used, this pin should be shorted to CAP3. The voltage between this pin and CAP3 is digitized and is read in the meas_vcap4 register. The capacitance test current set by the ITST pin is pulled from this pin.

CFP (Pin 20): VCAPP5 Charge Pump Flying Capacitor Positive Terminal. Place a 6.3V 0.1µF between CFP and CFN.

CFN (Pin 21): VCAPP5 Charge Pump Flying Capacitor Negative Terminal. Place a 6.3V 0.1µF between CFP and CFN.

VCAPP5 (Pin 22): Charge Pump Output. The internal charge pump drives this pin to V_{CAP} + $INTV_{CC}$. It is used as the high side rail for the OUTFET gate drive and charge current sense amplifier. Connect a 6.3V 0.1µF capacitor from VCAPP5 to V_{CAP}.

OUTFET (Pin 23): Output Ideal Diode Gate Drive Output. This pin controls the gate of an external N-channel MOSFET used as an ideal diode between V_{OUT} and V_{CAP}. The gate drive receives power from the internal charge pump output VCAPP5. Connect the source of the N-channel MOSFET to V_{CAP} and the drain to V_{OUT}. If the output ideal diode MOSFET is not used, OUTFET should be left floating.

V_{CAP} (Pin 24): Supercapacitor Stack Voltage and Charge Current Sense Amplifier Negative Input. Connect this pin to the top of the supercapacitor stack. The voltage at this pin is digitized and is read in the meas_vcap register.

ICAP (Pin 25): Charge Current Sense Amplifier Positive Input. The ICAP and V_{CAP} pins measure the voltage across the sense resistor, R_{SNSC}, to provide instantaneous current signals for the control loops and ESR measurement system. The maximum charge current is $32mV/R_{SNSC}$. The voltage between this pin and V_{CAP} is the charging/discharge current as read in the meas_ichg register.

VCC2P5 (Pin 26): Internal 2.5V Regulator Output. This regulator provides power to the internal logic circuitry only. Decouple this pin to SGND with a minimum 1µF low ESR ceramic capacitor.

SW (Pin 27): Switch Node Connection to the Inductor. The negative terminal of the boot-strap capacitor, CB, is connected to this pin. The voltage on this pin is also used as the source reference for the top side N-channel MOSFET gate drive. In step-down mode, the voltage swing on this pin is from a diode (external) forward voltage below ground to V_{OUT}. In step-up mode, the voltage swing is from ground to a diode forward voltage above V_{OUT}.

TGATE (Pin 28): Top Gate Driver Output. This pin is the output of a floating gate driver for the top external N-channel MOSFET. The voltage swing at this pin is ground to V_{OUT} + DRV_{CC}.

BST (Pin 29): TGATE Driver Supply Input. The positive terminal of the boot-strap capacitor, CB, is connected to this pin. This pin swings from a diode voltage drop below DRV_{CC} up to V_{OUT} + DRV_{CC}.

BGATE (Pin 30): Bottom Gate Driver Output. This pin drives the bottom external N-channel MOSFET between PGND and DRV_{CC}.

DRV_{CC} (Pin 31): Power Rail for the Bottom Gate Driver. Connect to $INTV_{CC}$ or to an external supply. Decouple this pin to ground with a minimum 6.3V 2.2µF low ESR ceramic capacitor. Do not exceed 5.5V on this pin.

PIN FUNCTIONS

$INTV_{CC}$ (Pin 32): Internal 5V Regulator Output. The control circuits and gate drivers (when connected to DRV_{CC}) are powered from this supply. If not connected to DRV_{CC}, decouple this pin to ground with a minimum 4.7µF low ESR ceramic capacitor.

V_{OUT} (Pin 33): Output Voltage Supply. This pin supplies power to the LTC3351 after the hot swap start-up has finished. The switching controller charges the capacitor stack from the voltage at this pin and the LTC3351 backs up the voltage at this pin if the input voltage goes outside the OV/UV range or an input current fault occurs.

RETRYB (Pin 34): Retry Comparator Input. The hot swap controller will not attempt to connect V_{IN} and V_{OUT} unless this pin is below 200mV. This high voltage capable pin may be connected to V_{OUT} if the system needs to be fully powered down before repowering after a power loss and backup.

ISNSM (Pin 35): Input Current Sense Pin. This is the negative input for both the hot swap current sense amplifier and the switching charger input current sense amplifier.

ISNSP_CHG (Pin 36): Input Current Sense Pin. This is the positive input for the switching charger input current sense amplifier. The switching charger will reduce charge current to keep the voltage between this pin and ISNSM to 32mV. The current is measured using the sense resistor between this pin and ISNSM and is measured by the ADC and reported in the meas_iin register.

ISNSP_HS (Pin 37): Input Current Sense Pin. This is the positive input for the hot swap input current sense amplifier. The hot swap controller will limit the voltage between this pin and ISNSM to 48mV. This pin is also the input current sense for the circuit breaker function.

CSS (Pin 38): Soft Start and Delay Capacitor Pin. A capacitor from this pin to V_{OUT} determines both the maximum dV/dt of V_{OUT} during the power up and the debounce delay from OV and UV becoming good before attempting to reconnect V_{IN} and V_{OUT}.

SRC (Pin 39): Hot Swap/Input FETs Source Pin. This pin senses the source voltage of the hot swap and input FETs.

HS_GATE (Pin 40): Hot Swap/Input FETs Gate Pin. This pin controls the external hot swap/input FETs. This pin is pulled up to, at most, V_{INTVCC} above the V_{OUT} pin.

V_{IN} (Pin 41): External DC Power Source Input and Sense Pin. For V_{IN} voltages greater than 8V, a 100Ω resistor in series with this pin is required. The voltage at this pin is digitized and is reported in the meas_vin register.

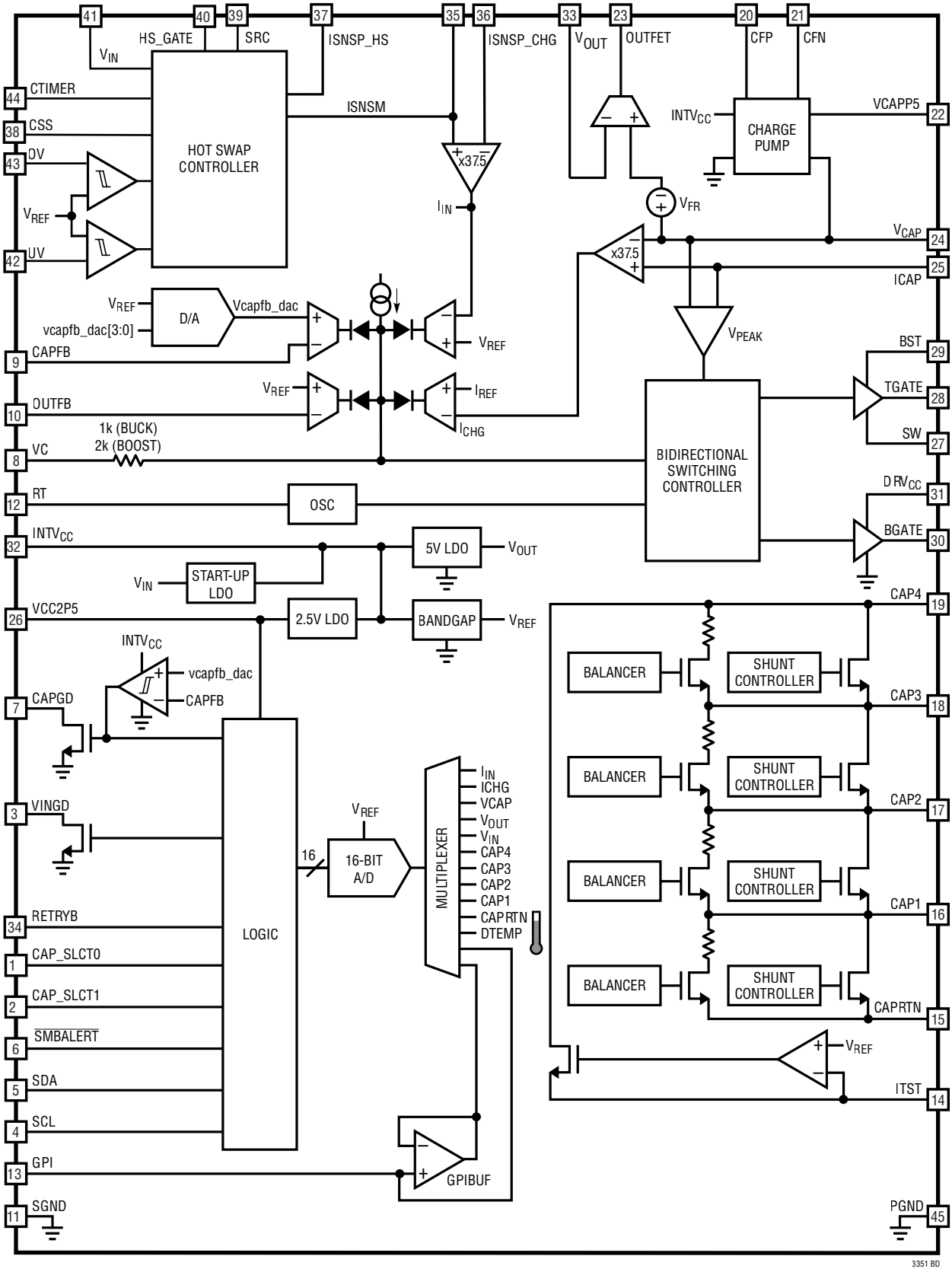
UV (Pin 42): Power-Fail Comparator Input. When the voltage at this pin drops below $V_{UV(TH)}$, the hot swap controller is disconnected, the part enters backup mode and VINGD is pulled low.

OV (Pin 43): Power-Fail Comparator Input. When the voltage at this pin exceeds $V_{OV(TH)}$, the hot swap controller is disconnected, the part enters backup mode and VINGD is pulled low.

CTIMER (Pin 44): Fault and Retry Timing Capacitor. A capacitor from this pin to SGND programs the fault and retry timing. During an over current fault condition this capacitor is charged with $I_{TIMER(UP)}$ (400µA). Once this pin voltage exceeds $V_{TIMER(TH)}$ (1.2V) a fault is declared and V_{OUT} is disconnected from V_{IN}. This pin is continuously discharged with $I_{TIMER(DN)}$ (2µA), and once it discharges to 300mV, and RETRYB is low, the hot swap controller will again attempt to reconnect V_{IN} and V_{OUT}.

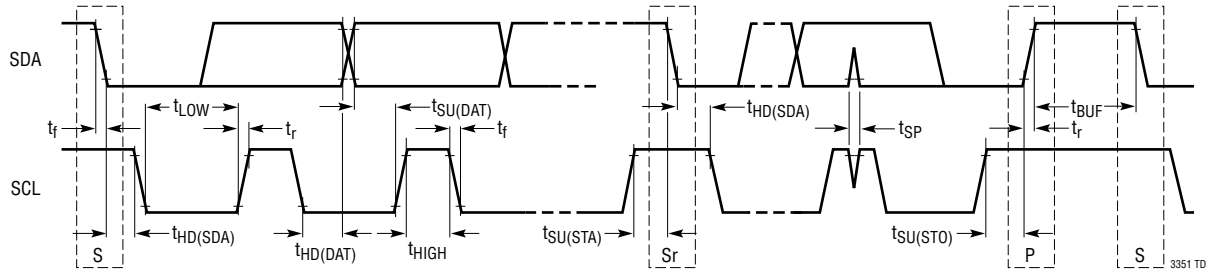
PGND (Exposed Pad Pin 45): Power Ground. For rated thermal performance connect the exposed pad to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3351. Connect the exposed pad to the SGND pin on top copper.

BLOCK DIAGRAM



TIMING DIAGRAM

Definition of Timing for F/S Mode Devices on the I²C Bus



S = START, Sr = REPEATED START, P = STOP

I²C/SMBus Legend

S	START CONDITION
Sr	REPEATED START CONDITION
Rd	READ (BIT VALUE OF 1)
Wr	WRITE (BIT VALUE OF 0)
A	ACKNOWLEDGE
N	NACK
P	STOP CONDITION
PEC*	PACKET ERROR CODE
	MASTER TO SLAVE
	SLAVE TO MASTER

SMBus WRITE WORD PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	P

SMBus WRITE WORD WITH PEC PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	PEC*	A	P

SMBus READ WORD PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	DATA BYTE LOW	A	DATA BYTE HIGH	N	P

SMBus READ WORD WITH PEC PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	PEC*	N	P

SMBus ALERT RESPONSE ADDRESS PROTOCOL

S	ALERT RESPONSE ADDRESS	Rd	A	DEVICE ADDRESS	Rd	N	P

SMBus ALERT RESPONSE ADDRESS PROTOCOL WITH PEC

S	ALERT RESPONSE ADDRESS	Rd	A	DEVICE ADDRESS	Rd	A	PEC*	N	P

*USE OF PACKET ERROR CHECKING IS OPTIONAL

OPERATION

Introduction

The LTC3351 is a highly integrated backup power controller and system monitor. It features a bidirectional switching controller, hot swap controller, output ideal diode, supercapacitor shunts/balancers, under and over voltage comparators, a 16-bit ADC, and I^2C/SMBus programmability with status reporting.

If V_{IN} is within externally programmable UV/OV threshold voltages, the hot swap controller connects V_{IN} to V_{OUT} and the synchronous switching controller operates in step-down mode charging a stack of supercapacitors. A programmable input current limit ensures that the supercapacitors will automatically be charged at the highest possible charge current that the input can support. If V_{IN} goes outside the UV/OV thresholds, or if the hot swap controller's circuit breaker trips, or if a simulated failure is requested, then the hot swap controller will disconnect V_{OUT} from V_{IN} and the synchronous controller will run in reverse as a step-up converter to deliver power from the supercapacitor stack to V_{OUT}.

An ideal diode controller drives an external MOSFET to provide a low loss power path from V_{CAP} to V_{OUT}. This ideal diode works seamlessly with the bidirectional controller to provide power from the supercapacitors to V_{OUT}. The hot swap controller utilizes two back-to-back MOSFETs to control inrush, provide a short circuit breaker function and prevent back driving V_{IN} while in backup mode.

The LTC3351 provides balancing and overvoltage protection to a series stack of one to four supercapacitors. The internal capacitor voltage balancers eliminate the need for external balance resistors. Overvoltage protection is provided by shunt regulators that use an internal switch and an external resistor across each supercapacitor.

The LTC3351 monitors system voltages, currents, and its own die temperature. A general purpose input (GPI) pin is provided to measure an additional system parameter or implement a thermistor measurement. In addition, the LTC3351 can measure the capacitance and equivalent series resistance of the supercapacitor stack. This provides indication of the health of the supercapacitors and, along with the V_{CAP} voltage measurement, provides information on the total energy stored and the maximum power that can be delivered.

Operations Example

The LTC3351 is a highly integrated circuit with many features and operating modes. To better explain the operations of the LTC3351, a simplified example will be used. This example is graphically shown in Figure 1 and will be referred to throughout. Due to the widely varying time scales of the events with which the LTC3351 operates, the time axis of Figure 1 is not to scale.

The example begins with V_{IN} and V_{CAP} at 0V. V_{IN} is applied suddenly at the point labeled "hot plug". There is a very small inrush current into the drain capacitance of the hot swap FET connected to V_{IN}, this is shown as a small "spike" on the I_{IN} waveform. This "spike" is very small in either duration or amplitude, depending on the rise rate of V_{IN}. During the time labeled "debounce", the LTC3351 qualifies the input as good using the UV and OV comparators and expires an input debounce timer using the C_{SS} pin. Once this debounce time has passed, the LTC3351 begins turning on the hot swap FETs to charge the capacitance on V_{OUT} in a controlled way, during which time both the input current and rise rate of V_{OUT} are controlled. This results in a low constant I_{IN} current while the V_{OUT} capacitance is charged.

Once V_{OUT} has been charged to V_{IN}, the charger is allowed to start charging the supercapacitors. For this example; at the beginning of the charge cycle the supercapacitors are fully discharged. The charger will begin with constant current charging of the supercapacitors. Since the capacitor voltage is very low, the power delivered is very low. This low power delivery results in a low input current despite high charge current. As the voltage on the supercapacitors rises, the delivered power also rises and thus the input current also rises. This constant current phase of charging is labeled "CC Charging."

In this example I_{OUT}, the downstream system load, turns on during the constant current phase of charging. When this happens is outside the control of the LTC3351 and its timing in this example is arbitrary. Since output current

OPERATION

is supplied from V_{IN} via the hot swap FETs this step in load current directly causes a step in input current. The charge current is unaffected by this load step because the LTC3351 is not in input current limit.

As the supercapacitors charge, their voltage increases and the input current increases due to the increasing power being delivered to the supercapacitors. In this example the increasing input current reaches the input current limit at the beginning of the time labeled “CP charging.” With a constant input voltage, input current limit causes the LTC3351 to effectively have an input power limit. Depending on the settings of the input current limit, charge current limit, charge voltage, system load current and input voltage the charging phase of operation may or may not reach the input current limit.

During the constant power phase of charging, the charge current decreases as the charge voltage increases to maintain constant input power. This results in a slowing rate of charge as the charger approaches constant voltage charging. Once V_{CAP} reaches the programmed charge voltage, the constant voltage phase of charging begins. This is labeled “CV charging.”

During constant voltage charging, current is being delivered to the supercapacitors and there is a voltage drop across their internal ESR (equivalent series resistance). The LTC3351 holds the V_{CAP} voltage constant during this phase. Holding the V_{CAP} voltage constant allows the voltage across this ESR to fall towards zero as the internal capacitance is charged to V_{CAP}. During this time the charge current decays toward the leakage current of the capacitors.

The LTC3351 CV charges forever, waiting for a power failure, while keeping the capacitors charged, balanced and ready for backup. While fully charged and standing by for backup, the LTC3351 can also measure the ESR and capacitance of the batteries if requested (not shown in Figure 1). This is the condition the LTC3351 is likely to spend most time in, assuming input power loss is infrequent as is typically the case.

When power does fail, as labeled “power failure” in Figure 1, the OV or UV comparators detect the power failure at the input. The hot swap FET is turned off to isolate V_{OUT} from V_{IN}. Once the FET is off, V_{OUT} immediately falls to V_{CAP} (or the programmed boost voltage if

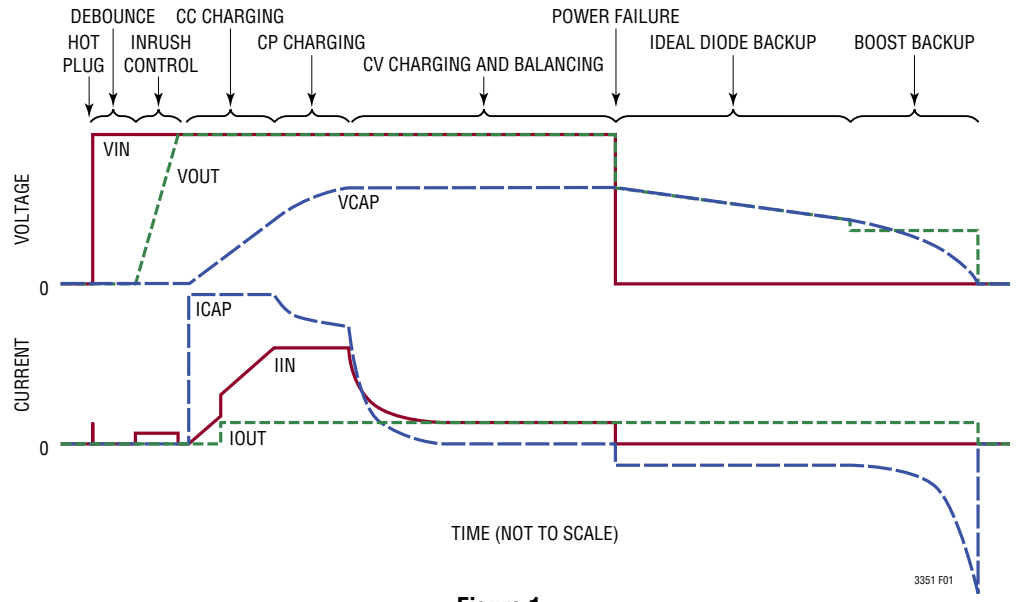


Figure 1.

OPERATION

it is higher, however in this example it is not). The ideal diode FET between V_{CAP} and V_{OUT} is turned on during the time labeled “ideal diode backup.” While operating in ideal diode backup, power is supplied directly from the capacitors without conversion. V_{CAP} is discharged during this time and V_{OUT} falls along with V_{CAP}.

Once the V_{OUT} voltage approaches the programmed boost voltage, the boost converter is turned on and the ideal diode turned off. The boost converter then supplies the output at constant voltage. As the capacitor voltage falls, the capacitor current must increase to supply the constant power load at V_{OUT}. This continues until either the boost reaches its current limit or exhausts the available energy in the capacitors. This time is labeled “boost backup.”

Bidirectional Switching Controller—Step-Down Mode

The bidirectional switching controller is designed to charge a series stack of supercapacitors (Figure 2). Charging proceeds at a constant current until the supercapacitors reach their maximum charge voltage determined by the CAPFB servo voltage and the resistor divider between V_{CAP} and CAPFB. The maximum charge current is determined by the value of the sense resistor, R_{SNSC}, connected in series with the inductor. The charge current loop servos the voltage across the sense resistor to 32mV. When charging begins, an internal soft-start ramp gradually increases the charge current. The V_{CAP} voltage and charge current are read from the meas_vcap and meas_ichg registers, respectively.

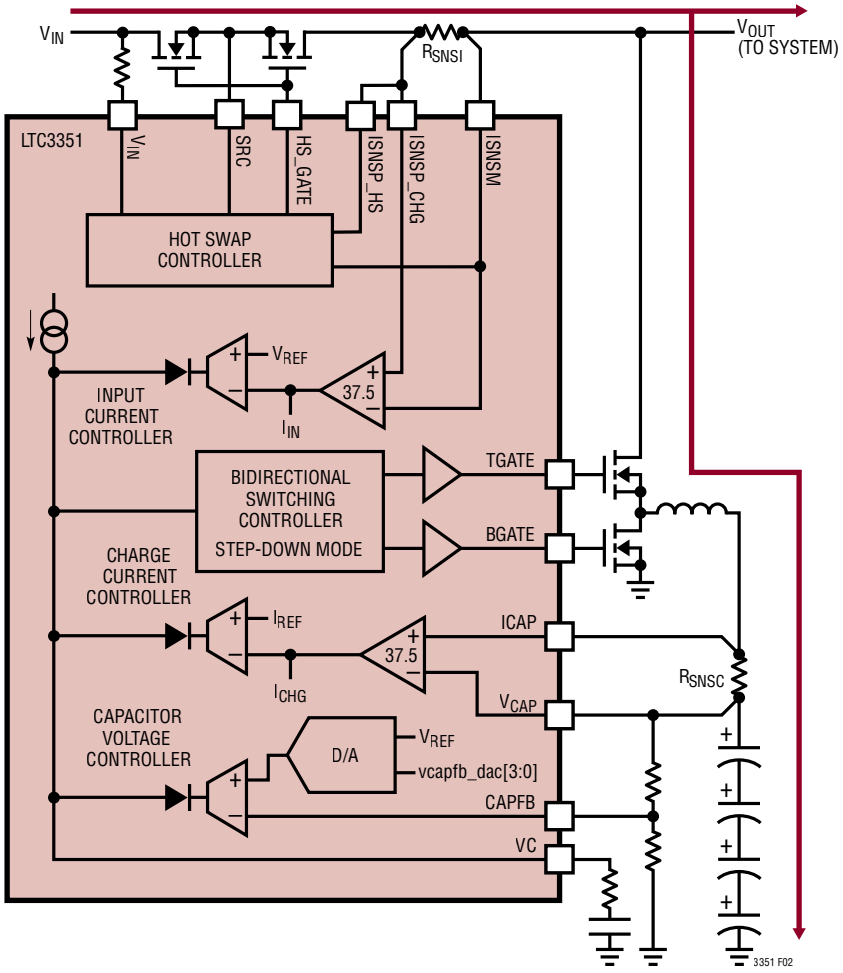


Figure 2. Power Path Block Diagram - Power Available from V_{IN}

OPERATION

The LTC3351 provides constant power charging (for a fixed V_{IN}) by limiting the input current drawn by the switching controller in step-down mode. The charger input current limit will reduce charge current to limit the voltage between ISNSP_CHG and ISNSM, typically across R_{SNSI}, to 32mV. If the combined system load plus supercapacitor charge current is large enough to cause the switching controller to reach the programmed input current limit, the input current limit loop will reduce the charge current by precisely the amount necessary to enable the external load to be satisfied. Even if the charge current is programmed to exceed the allowable input current, the input current limit will not be violated; the supercapacitor charger will reduce its current as needed. The input current is read from the meas_iin register.

Bidirectional Switching Controller—Step-Up Mode

The bidirectional switching controller acts as a step-up converter to provide power from the supercapacitors to V_{OUT} when input power is unavailable (Figure 3). VINGD low enables step-up mode. V_{OUT} regulation is set by a resistor divider between V_{OUT} and OUTFB. To disable step-up mode tie OUTFB to $INTV_{CC}$.

Step-up mode is often used with the output ideal diode. If the V_{OUT} regulation voltage is set below the capacitor stack voltage, upon removal of input power, power to V_{OUT} is provided from the supercapacitor stack via the output ideal diode. V_{CAP} and V_{OUT} will decrease as the load current discharges the supercapacitor stack. The output ideal diode will shut off and V_{OUT} will fall a PN diode (~700mV) below V_{CAP} when the voltage on OUTFB falls below 1.3V ($V_{OUTFB(TH)}$). If OUTFB falls below 1.2V when the output ideal diode shuts off, the synchronous step-up controller will turn on immediately to regulate OUTFB to 1.2V by providing power from the supercapacitor stack. If OUTFB is above 1.2V when the output ideal diode shuts off, the load current will flow through the body diode of the output ideal diode N-channel MOSFET for a period of time until OUTFB falls to 1.2V.

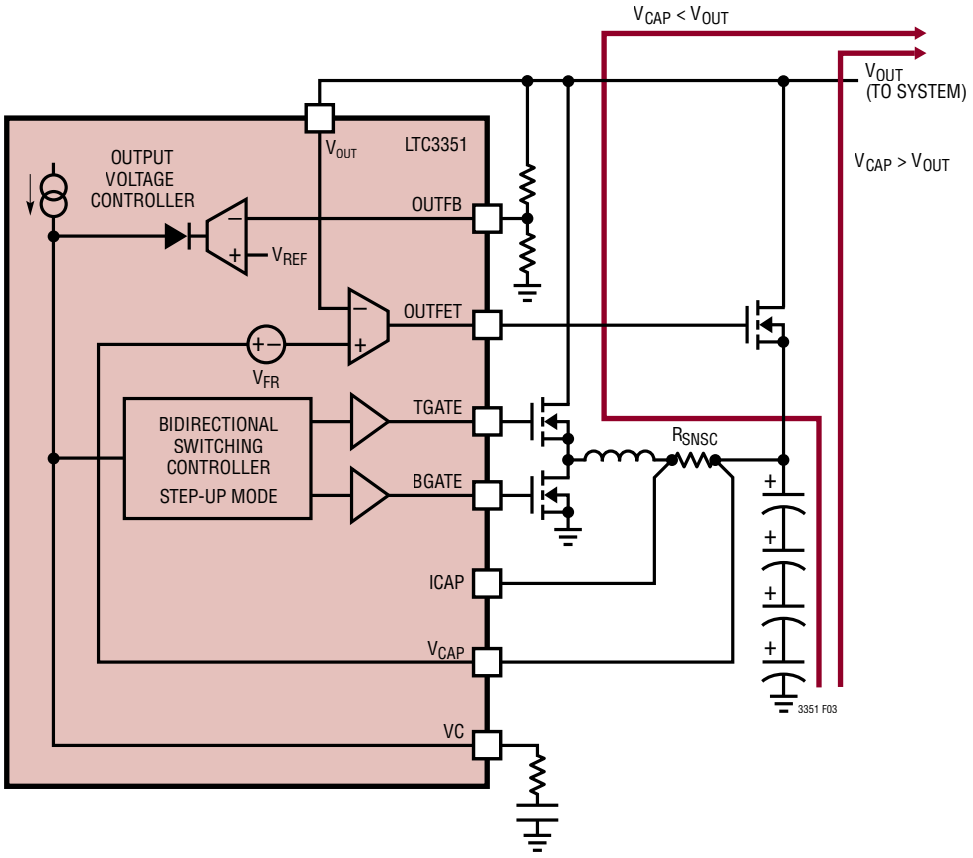


Figure 3. Power Path Block Diagram - Power Backup

OPERATION

The synchronous controller in step-up mode will run non-synchronously when V_{CAP} is less than 90mV (V_{DUVLO} falling) below V_{OUT}. It will run synchronously when V_{CAP} falls 200mV (V_{DUVLO} rising) below V_{OUT}.

Hot Swap Controller

Upon applying power to V_{IN}, the LTC3351 will immediately turn on a strong pull-down on the HS_GATE pin to prevent the external FETs from conducting current from V_{IN} to V_{OUT}. During the initial V_{IN} rise the LTC3351 may limit the rise rate of the voltage at the V_{IN} pin by drawing current through the 100Ω resistor in series with the pin. The LTC3351 will then drive the $INTV_{CC}$ pin to 3.6V using current from the V_{IN} pin. Once the $INTV_{CC}$ voltage is greater than 3.3V the hot swap turn-on sequence will begin.

If both the under voltage (UV) and (OV) comparators are in range, the CSS pin will begin to source 1µA of current, charging the C_{SS} capacitor. Once the CSS pin reaches 1.2V and the RETRYB pin is below 200mV ($V_{TH(RETRYB)}$) the LTC3351 will begin the process of connecting V_{IN} and V_{OUT} using the external FETs. The LTC3351 will begin pulling up on the HS_GATE pin using 24µA ($I_{HS\_GATE(UP)}$) of current. As V_{OUT} begins to rise, the capacitor from V_{OUT} to the CSS pin provides feedback to the LTC3351 about the rise rate of the output. Therefore, the sizing of the C_{SS} capacitor determines the maximum slew rate of V_{OUT} and the inrush current.

During the ramp up of HS_GATE and V_{OUT}, both the current limit and the circuit breaker are active. V_{IN} to V_{OUT} differential foldback reduces both the current limit and circuit breaker threshold while charging the output capacitor; this reduces the required SOA of the hot swap FETs.

If, at any time, the under voltage (UV) or overvoltage (OV) comparators go out of range, or if the CTIMER pin reaches 1.2V ($V_{TIMER(TH)}$), the LTC3351 will declare a fault and quickly turn off the external FET by grounding HS_GATE. The FET sources will be kept within a safe voltage of the gate by the SRC pin. Once a fault is declared the LTC3351's backup controller will begin supplying power to V_{OUT} from the energy stored in the capacitor stack. This will continue until either a new turn-on sequence occurs, the supercapacitor stored energy is depleted, or the boost is disabled via I^2C/SMBus.

The LTC3351 will limit the current from V_{IN} to V_{OUT} through the external FETs using the voltage across the current sense resistor(s) sensed using the ISNSP_HS and ISNSM pins. When V_{OUT} is within 1V of V_{IN} the LTC3351 will limit the voltage across the ISNSP_HS and ISNSM pins to 48mV ($V_{ILIM(TH)}$). To limit power in the external FET this limit is folded back to 10mV as the voltage from V_{IN} to V_{OUT} increases from 1V to 10V. Above 10V the limit remains at 10mV. This current limit is separate from the switching charger's input current limit. The switching charger's input current limit is unaffected by the above described fold back.

The LTC3351's CTIMER pin will source current when the input current is within 1.66% of the input current limit. As with the input current limit, this threshold is folded back as the voltage from V_{IN} to V_{OUT} increases. The current sourced from the CTIMER pin to the C_{TIMER} capacitor is about 400µA ($I_{TIMER(UP)}$). Once the voltage at the CTIMER pin exceeds 1.2V ($V_{TIMER(TH)}$ rising) a fault is declared and the turn-off sequence is initiated. The CTIMER pin has a static 2µA ($I_{TIMER(DN)}$) load that discharges the C_{TIMER} capacitor. Once a fault is declared the CTIMER pin must fall below 300mV before the turn-on sequence is re-attempted.

RETRYB Pin

The LTC3351's RETRYB pin determines if the LTC3351 tries to connect V_{IN} and V_{OUT} after a fault. The faults are UV, OV, circuit breaker (CTIMER), or a simulated fault programmed via the I^2C/SMBus port by setting ctl_hotswap_disable. If the RETRYB pin is low ($V_{TH(RETRYB)}$ below 200mV) the LTC3351 will try to connect V_{IN} and V_{OUT} using the hot swap controller. The RETRYB pin is high voltage tolerant and high impedance. A divider from V_{OUT} to RETRYB allows a precise threshold to be set. This can be used to ensure the system completely powers down following a failure before re-powering.

VINGD Pin

The VINGD pin indicates that the input voltage is within the OV/UV range and the system is powered from V_{IN}. For VINGD to be high, the voltage at UV must be above 1.2V (V_{OV} rising) the voltage at OV must be below 1.17V (V_{UV} falling), the circuit breaker must not be tripped, the hot

OPERATION

swap must not be disabled via I²C/SMBus, and the hot swap controller must have completed connecting V_{IN} and V_{OUT}. The state of the VINGD pull-down is read from the vingd bit in the sys_status register.

If UV is set to a level near or less than the charge voltage of the capacitors, V_{IN} becomes high impedance and the V_{OUT} load is very low, it is possible for a small amount of current to flow from V_{CAP} to V_{IN} through V_{OUT} due to the maximum duty cycle operation. In this condition, the high duty cycle buck is effectively a reverse low duty cycle boost. The boost has a small amount of output current that holds V_{IN} above V_{CAP} and possibly UV, causing the part to falsely indicate VINGD. Eventually V_{CAP} will be discharged below the programmed UV threshold and VINGD will indicate correctly. This situation can be avoided by programming the UV threshold at least 3% above the capacitor charge voltage.

Ideal Diode

The LTC3351 has an ideal diode controller that drives an external N-channel MOSFET between V_{CAP} and V_{OUT}. The ideal diode consists of a precision amplifier that drives the gates of N-channel MOSFETs whenever the voltage at V_{OUT} is approximately 30mV (V_{FR}) below the voltage at V_{CAP}. Within the amplifier's linear range, the small-signal resistance of the ideal diode will be quite low, keeping the forward drop near 30mV. At higher current levels, the MOSFETs will be in full conduction.

The ideal diode provides a path for the supercapacitors to power V_{OUT} when V_{IN} is unavailable or the hot swap controller is disconnected. In addition to a Fast-Off comparator, the ideal diode also has a Fast-On comparator that turns on the external MOSFET when V_{OUT} drops 65mV (V_{FTO}) below V_{CAP}. The ideal diode will shut off when OUTFB is just above regulation allowing the synchronous controller to power V_{OUT} in step-up mode.

Gate Drive Supply (DRV_{CC})

The bottom gate driver is powered from the DRV_{CC} pin, which is normally connected to the $INTV_{CC}$ pin. An external LDO can also be used to power the gate drivers to minimize power dissipation inside the LTC3351. See the Applications Information section for details.

Switcher/Charger Undervoltage Lockout (UVLO)

Internal undervoltage lockout circuits monitor both the $INTV_{CC}$ and DRV_{CC} pins. The switching controller is kept off until $INTV_{CC}$ rises above V_{UVLO} (4.3V) and DRV_{CC} rises above $V_{DRVUVLO}$ (4.2V). The controller is disabled if either $INTV_{CC}$ falls below 4V or DRV_{CC} falls below 3.9V.

Charging is disabled until V_{OUT} is V_{DUVLO} (200mV) above the supercapacitor voltage and VINGD is high. Charging is disabled when V_{OUT} falls to within 90mV of the supercapacitor voltage or when VINGD is low.

R_T Oscillator and Switching Frequency

The R_T pin is used to program the switching frequency. A resistor, R_T, from this pin to ground sets the switching frequency according to:

$$f_{SW}(MHz) = \frac{53.5}{R_T(k\Omega)}$$

R_T also sets the scale factor for the capacitor measurement value reported in the meas_cap register, described in the ESR and Capacitance Measurement section of this data sheet.

Switching Controller Input Overvoltage Protection

Input overvoltage protection turns off both switching controller switches if V_{IN} exceeds V_{OVLO} (38.6V). The controller will resume switching if V_{IN} falls below 37.2V. The hot swap controller is unaffected by this and uses its own programmable OV threshold.

V_{CAP} DAC

The feedback reference for the CAPFB servo point is programmed using an internal 4-bit digital-to-analog converter (DAC). The reference voltage is programmable from 0.6375V ($V_{CAPFBLO}$) to 1.2V ($V_{CAPFBHI}$) in 37.5mV increments. The DAC defaults to 0xA (V_{CAPFB_DEF} 1.0125V) and is programmed via the vcapfb_dac register.

Supercapacitors lose capacitance as they age. By initially setting the V_{CAP} DAC to a low setting, the final charge voltage on the supercapacitors can be increased as they age to maintain a constant level of stored backup energy throughout the lifetime of the supercapacitors. The

OPERATION

capacitance and ESR measurement system may temporarily increase this DAC to a value as much as full scale (1.2V) during the ESR test.

If using the capacitance and ESR test, the highest usable DAC setting will be determined by the voltage increase between that setting and 1.2V at the CAPFB pin, wherein the capacitor stack's voltage increases by 1.25 times the voltage specified in cap_delta_v_setting.

Charge Status Indication

The LTC3351 includes a comparator to report the status of the supercapacitors via an open-drain NMOS transistor on the CAPGD pin. This pin pulls to ground until the CAPFB pin voltage rises to within nominally 8% of the V_{CAP} DAC setting. Once the CAPFB pin is above this threshold, the CAPGD pin goes high impedance. The output of this comparator may also be read from the cappg bit in the sys_status register.

Capacitor Voltage Balancer

The LTC3351 has an integrated active stack balancer. This balancer slowly balances all of the capacitor voltages to within approximately 10mV of each other. This maximizes the life of the supercapacitors by keeping the voltage on each as low as possible to achieve the needed total stack voltage. When the difference between any two capacitor voltages exceeds approximately 10mV, the capacitor with the largest voltage is discharged with a resistive balancer (approximately 75Ω until all capacitor voltages are within 10mV). The balancers can be disabled by setting the ctl_disable_balancer bit.

Capacitor Shunt Regulators

During charging, the capacitors are protected from overvoltage. The capacitors in the stack will not have exactly the same capacitance due to manufacturing tolerances or uneven aging. This will cause the capacitor voltages to increase at different rates with the same charge current. If this mismatch is severe enough or if the capacitors are being charged to near their maximum voltage, it becomes necessary to limit the voltage increase on some capacitors while still charging the other capacitors. Up to 500mA of current may be shunted around a capacitor whose voltage is approaching the programmable shunt voltage. This shunt current reduces the charge rate of that capacitor relative to the other capacitors. If a capacitor continues to approach its shunt voltage, the stack charge current is reduced. This protects the capacitor from overvoltage while still charging the other capacitors, although at a reduced rate of charge. When shunting, the internal switch may be on more than 96% duty cycle. The shunts are disabled by setting the ctl_disable_shunt bit. The shunt voltage is programmable in the vshunt register. Shunt voltages may be programmed in 183.5µV increments. If a voltage greater than 3.6V is programmed, the charge current will be reduced as that voltage is approached but the shunt will not turn on. The default value is 0x3999, resulting in a shunt voltage of approximately 2.7V. See Register Map for more information.

I²C/SMBus and $\overline{\text{SMBALERT}}$

The LTC3351 contains an I²C/SMBus compatible port. This port allows communication with the LTC3351 for configuration and reading back telemetry data. The port supports two SMBus formats, read word and write word. These may be used with or without the packet error code (PEC) feature. Refer to the SMBus specification for details of these formats and PEC. The registers accessible via this port are organized on an 8-bit address bus and each register is 16 bits wide. The "command code" (or subaddress) of the SMBus read/write word formats is the 8-bit address of each of these registers. The address of the LTC3351 is 0b0001001.

The $\overline{\text{SMBALERT}}$ pin is asserted (pulled low) whenever an enabled limit is exceeded or when an enabled status event happens (see the Limit Checking and Alarms and the Monitor Status Register sections of this data sheet). The LTC3351 will de-assert the $\overline{\text{SMBALERT}}$ pin only after responding to a SMBus alert response address (ARA), an SMBus protocol used to respond to a $\overline{\text{SMBALERT}}$. The host will read from the ARA (0b0001100) and each part asserting $\overline{\text{SMBALERT}}$ will begin to respond with its address. The responding parts arbitrate in such a way that only the part with the lowest address responds completely. Only when a part has responded with its entire address does it release the $\overline{\text{SMBALERT}}$ signal. If multiple parts are asserting the $\overline{\text{SMBALERT}}$ signal then multiple

OPERATION

reads from the ARA are needed. For more information refer to the SMBus specification.

Details on the registers accessible through this interface are available in the Register Map section of this data sheet.

For I^2C masters unable to create the repeated start needed for the read and write word protocols, a stop followed by a start may be substituted.

Analog-to-Digital Converter

The LTC3351 has an integrated 16-bit sigma-delta analog-to-digital converter (ADC). This converter is automatically multiplexed between the measured channels. Its results are stored in registers accessible via the I^2C/SMBus port. There are 11 channels measured by the ADC, each of which takes approximately 800µs to measure. In addition to providing status information about the system voltages and currents, some of these measurements are used by the LTC3351 to balance, protect (shunt), and measure the capacitors in the stack.

The result of each analog-to-digital conversion is stored in a 16-bit register as a signed, two's complement number.

To reduce average quiescent current, the effective duty cycle of the ADC can be reduced by programming adc_wait_vin and/or adc_wait_backup. Each register inserts a delay in the ADC's measurement cycle during its respective mode of operation. Each LSB of these registers has a weight of approximately 400µs. At some times, such as when shunting or making capacitance and ESR measurement, these settings may be temporarily ignored. Measurements of individual channels may be enabled or disabled by setting the appropriate bit in adc_backup_ch_en_reg and adc_vin_ch_en_reg.

The measurements from the ADC are stored to meas_vcap1, meas_vcap2, meas_vcap3, meas_vcap4, meas_gpi, meas_vin, meas_vcap, meas_vout, meas_iin, meas_ichg and meas_dtemp.

ESR and Capacitance Measurement

The LTC3351 monitors the health of a supercapacitor stack by measuring the capacitance and the ESR. Both the capacitance and ESR are measured in a single test. The LTC3351 measures ESR by applying and measuring a current step with the high efficiency charger and measuring the change in voltage. The capacitance is measured by discharging a fixed voltage with a known current and measuring time.

The ESR and capacitance measurement sequence, initiated by setting ctl_start_cap_esr_meas, is:

1. The mon_meas_active and mon_esr_meas_active bits become high if the capacitors are charged, otherwise, mon_capesr_pending becomes high.
2. The charger is configured to charge at a pre-set current up to a full vcapfb_dac setting, this current is set using an 8 bit DAC controlled either by:
   a. An internal algorithm that selects the optimal current based on the previous capacitor measurement (assuming the LTC3351 is not in input current limit)
   b. An override setting, programmed in esr_i_override, is used if non-zero. If it is likely the LTC3351 will operate in input current limit while charging, then this should be set low enough to avoid input current limit.
3. The measurement system waits esr_i_on_settling for the current and capacitor effects to stabilize. Each LSB of esr_i_on_settling is 1024 switcher periods.
4. A series of measurements of capacitor voltages and charge currents are made. The charger is then temporarily shut off.
5. The measurement system waits esr_i_off_settling for the current and capacitor effects to stabilize. Each LSB of esr_i_off_settling is 1024 switcher periods.
6. A series of measurements of capacitor voltages and charger currents are made. From these measurements, and the previous measurements, the ESR is calculated and stored in meas_esr.
7. The capacitors will be charged to at least 1.25 • cap_delta_v_setting above their initial voltage (as measured at step 1).

   If the capacitor voltage reaches the maximum charge voltage (V_{CAPFB} = 1.2V), then the test will stop trying to charge and continue without fully charging. The test may fail later due to this. If the charger is unable to reach 1.25 • cap_delta_v_setting above the initial

OPERATION

voltage with capfb less than 1.2V, it will continue trying to charge indefinitely. This may occur if the charger is limited by the input voltage and maximum duty cycle of the buck charger. This may also occur if there is no charge current available due to system load exceeding the input current limit. If either of these conditions occurs, the test will remain in this condition indefinitely.

8. The charger is temporarily disabled. The mon_cap_meas_active bit becomes high, the mon_esr_meas_active bit becomes low and the ITST current is enabled. After a time set by cap_i_on_settling, a series of voltage measurements is made.
9. The capacitor stack is discharged a fixed voltage (set by cap_delta_v_setting) from the voltage measured in the previous step using the ITST current (1.2V/RTST, up to 60mA or 300mW). This voltage is measured using the CAP1-4 pins.
10. The time required to discharge by this fixed voltage is measured. It is then scaled for cap_delta_v_setting and stored as meas_cap.
11. The charger stays off and the ITST current stays on until the stack voltage returns to the voltage set by vcapfb_dac.
12. The charger is turned back on and the ITST current is turned off. The mon_meas_active bit goes low.

Figure 4 shows this sequence graphically.

This measurement is only initiated when the ctl_start_cap_esr_meas bit is set. The results of the measurement can be checked against limits and issue a $\overline{\text{SMBALERT}}$ if limits are exceeded, see the Limit Checking and Alarms section of this data sheet.

The measurement of Capacitance and ESR can fail if power fails during the test or if the capacitor stack is discharged below the CAPGD threshold. The test will also fail if ctl_stop_cap_esr_meas is set. If it does fail, mon_meas_failed will be set.

Monitor Status Register

The LTC3351 has a monitor status register (monitor_status_reg) containing status bits to indicate the state of the capacitance and ESR monitoring system. These bits are set and cleared by the capacitor monitor upon certain events during a capacitor and ESR measurement, as described in the ESR and Capacitance Measurement section.

There is a corresponding monitor status mask register (monitor_status_mask_reg). Writing a one to any of these bits will cause the $\overline{\text{SMBALERT}}$ pin to pull low when the corresponding bit in monitor_status_reg has a rising edge. This allows reduced polling of the LTC3351 when waiting for a capacitance or ESR measurement to complete.

Details of monitor_status_reg and monitor_status_mask_reg can be found in the Register Map section of this data sheet.

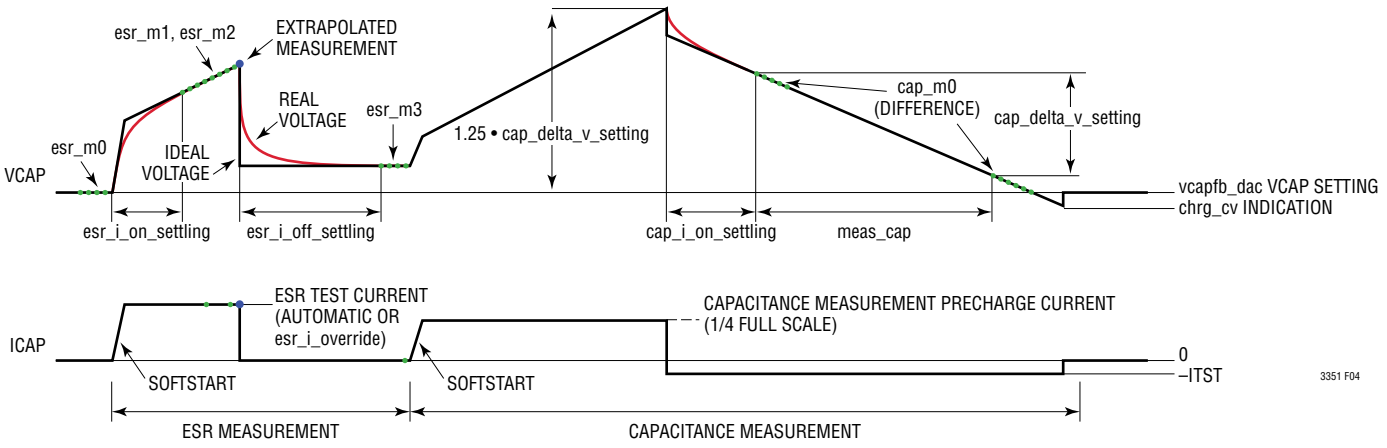


Figure 4.

OPERATION

System Status Register

The sys_status register contains data about the state of the charger, switcher and comparators. Details of this register may be found in the Register Map section of this data sheet.

Limit Checking and Alarms

The LTC3351 has a limit checking function that will check each measured value against I²C/SMBus programmable limits. This feature is optional and all of the limits are disabled by default. The limit checking is designed to simplify system monitoring, eliminating the need to continuously poll the LTC3351 for measurement data.

If a measured parameter goes outside of the programmed level of an enabled limit, the associated bit in the alarm_reg register is set high and the $\overline{\text{SMBALERT}}$ pin is pulled low. This informs the I²C/SMBus host that a limit has been exceeded. The alarm_reg may then be read to determine exactly which programmed limits have been exceeded.

A single ADC is shared between the 11 channels with about 9ms between consecutive measurements of the same channel. In a transient condition, it is possible for these parameters to exceed their programmed levels in between consecutive ADC measurements without setting the alarm.

Once the LTC3351 has responded to an SMBus ARA the $\overline{\text{SMBALERT}}$ pin is released. The LTC3351 will not pull the pin low again until another limit is exceeded. To reset a limit that has been exceeded write a zero to the respective bit in the alarm_reg register. When writing alarm_reg, zeros will clear their respective bits in the register, ones will be ignored.

A number of the LTC3351's registers are used for limit checking. Individual limits are enabled or disabled in alarm_mask_reg. Once an enabled alarm's measured value exceeds the programmed level for that alarm the alarm is set. That alarm may only be cleared by writing a zero to the appropriate bit of alarm_reg. All alarms that have been set and have not yet been cleared may be read in the alarm_reg.

All of the individual measured voltages have a corresponding undervoltage (UV) and overvoltage (OV) alarm level. All of the individual capacitor voltages are compared to the same alarm levels, set in cap_ov_lvl and cap_uv_lvl. The input current measurement has an overcurrent (OC) alarm programmed in iin_oc_lvl. The charge current has an undercurrent alarm programmed in ichg_uc_lvl.

Die Temperature Sensor

The LTC3351 has an integrated die temperature sensor monitored by the ADC and digitized to meas_dtemp. An alarm is configured on die temperature by setting dtemp_cold_lvl and/or dtemp_hot_lvl and enabling their respective alarms in alarm_mask_reg. To convert the code in the meas_dtemp register to degrees Celsius use the following:

$$T_{DIE}\ (°C) = 0.0295 \bullet \text{meas\_dtemp} - 274°C$$

General Purpose Input

The general purpose input (GPI) pin is used to measure an additional system parameter where the voltage on this pin is digitized by the ADC. For high impedance inputs, an internal buffer may be selected and used to drive the ADC. This buffer is enabled by setting the ctl_gpi_buffer_en bit in the ctl_reg register. With this buffer, the input range is limited from 0V to 3.5V. If this buffer is not used, the range is from 0V to 5V, however, the input stage of the ADC will draw about 0.8µA per volt from this pin. The ADC input is a switched capacitor amplifier running at about 2MHz, so this current draw will be at that frequency. The pin current can be eliminated at the cost of reduced range and increased offset by enabling the buffer.

Alarms are available for this pin voltage with levels programmed using gpi_uv_lvl and gpi_ov_lvl. These alarms are enabled using the mask_alarm_gpi_uv and mask_alarm_gpi_ov bits in alarm_mask_reg.

To monitor the temperature of the supercapacitor stack, the GPI pin can be connected to a negative temperature coefficient (NTC) thermistor. A low drift bias resistor is required from $INTV_{CC}$ to GPI and a thermistor is required from GPI to ground. Connect GPI to SGND if not used.

OPERATION

Internal Diodes

The LTC3351 has numerous internal diodes as part of its circuits and ESD protection structures. In normal operation, these diodes are reverse biased. Figure 5 shows all the diodes except the substrate diodes. These substrate diodes have their anode connect to ground and their cathodes connect to every pin except SW.

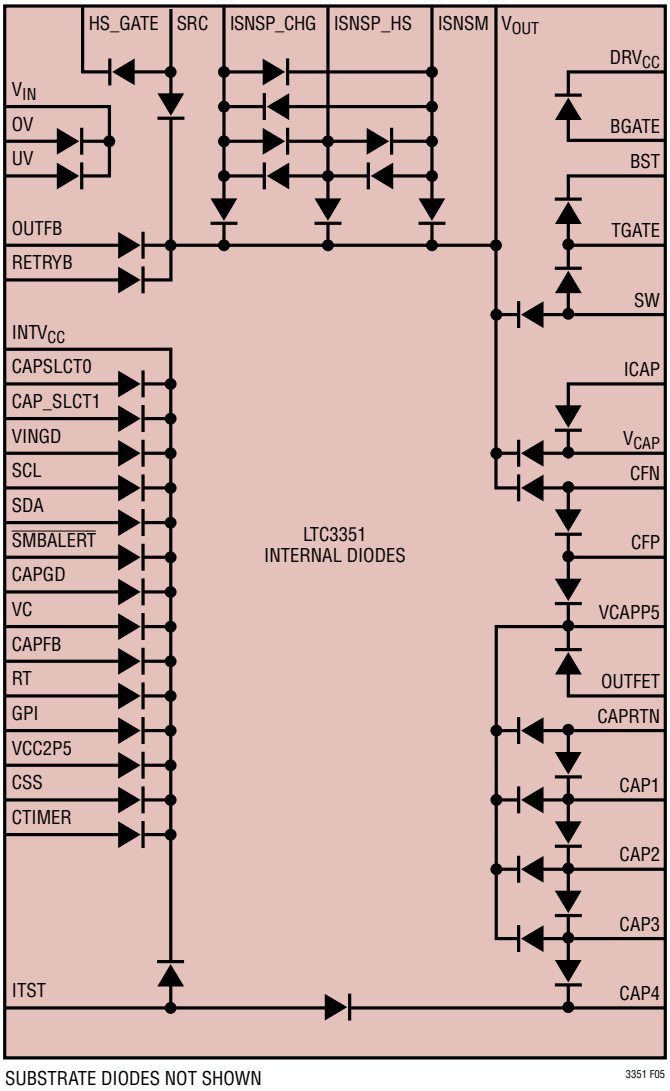


Figure 5.

APPLICATIONS INFORMATION

Digital Configuration

Although the LTC3351 has extensive digital features, none are mandatory for basic use. The shunt voltage is programmed via vshunt, which has a default value of 2.7V. The capacitor voltage feedback reference defaults to 1.0125V (V_{CAPFB_DEF}) and is set using vcapfb_dac. If these values are acceptable, no software is required for basic use.

All other digital features are optional, most for system monitoring. The ADC automatically runs and stores conversions to registers (e.g., meas_vcap). Capacitance and ESR measurements only run if requested. Each measured parameter has programmable limits (e.g., vcap_uv_lvl and vcap_ov_lvl) which may trigger an alarm and $\overline{\text{SMBALERT}}$ when enabled. All alarms are disabled by default.

Capacitor Configuration

The LTC3351 is used with one to four supercapacitors. If fewer than four capacitors are used, the capacitors must be populated from CAPRTN to CAP4, and the unused CAP pins must be tied to the highest used CAP pin. For example, if three capacitors are used, tie CAP4 to CAP3. If only two capacitors are used, tie both CAP4 and CAP3 to CAP2. The number of capacitors used must be programmed on the CAP_SLCT0 and CAP_SLCT1 pins by tying the pins to VCC2P5 for a one and ground for a zero as shown in Table 1. The value programmed on these pins is read back from num_caps via I^2C/SMBus.

Table 1.

Number of Capacitors	num_caps register	CAP_SLCT1	CAP_SLCT0
1	0	0	0
2	1	0	1
3	2	1	0
4	3	1	1

Capacitor Shunt Regulator Programming

V_{SHUNT} is programmed via the vshunt register and defaults to 2.7V at initial power-up. V_{SHUNT} serves to limit the voltage on any individual capacitor by turning on a shunt around that capacitor as the voltage approaches V_{SHUNT}. CAPRTN, CAP1, CAP2, CAP3 and CAP4 are connected to the supercapacitors through resistors which serve as ballasts for the internal shunts. The shunt current is approximately V_{SHUNT} divided by twice the shunt resistance value. For a V_{SHUNT} of 2.7V, 2.7Ω resistors should be used for 500mA of shunt current. If the shunts are disabled, the shunt resistors must be populated with 100Ω.

Since the shunt current is less than what the switcher can supply, the on-chip logic will automatically reduce the charging current to allow the shunt to protect the capacitor. This greatly reduces the charge rate once any shunt is activated. For this reason, program V_{SHUNT} as high as possible to reduce the likelihood of it activating during a charge cycle. Ideally, V_{SHUNT} is set high enough so that any likely capacitor mismatches would not cause the shunts to turn on. This keeps the charger operating at the highest possible charge current and reduces the charge time. If the shunts never turn on, the charge cycle completes quickly and the balancers eventually equalize the voltage on the capacitors. The shunt setting may also be used to discharge the capacitors for testing, storage or other purposes.

Simulated Power Failure

The LTC3351 has the ability to simulate a power failure by setting ctl_hotswap_disable. This causes the hot swap controller to disconnect V_{OUT} from V_{IN} and indicate power has failed exactly as if it would had power actually failed. In this configuration all power consumption downstream will be supplied by the supercapacitors either through the ideal diode or the boost converter. If, during this test, the stored energy is exhausted, then V_{OUT} will collapse, just as in a real power failure. At the end of the simulated failure test, the ctl_hotswap_disable bit must be cleared to allow the hot swap to reconnect V_{IN} to V_{OUT}. The min_vout_hs_disable register may be used to automatically clear ctl_hotswap_disable if V_{OUT} falls below the programmed voltage. Clearing the ctl_hotswap_disable does not force the hot swap to reconnect, it only allows it to reconnect if its usual conditions are met, mainly that OV, UV and RETRYB voltages are correct. If the hot swap is re-enabled while there is system load current, it is considered a hot reconnect and is discussed in the Hot Reconnects section of this data sheet.

APPLICATIONS INFORMATION

Hot Swap Component Selection

The hot swap controller will servo the HS_GATE pin to regulate the voltage across the sense resistor(s) between ISNSP_HS and ISNSM to be, at most, 48mV ($V_{ILIM(TH)}$) . This current limit is folded back as the voltage between V_{IN} and V_{OUT} increases to 12V, at which point the regulation voltage drops to 12mV and no further.

The CSS capacitor is used both to set an input qualification delay (debounce) and to limit the V_{OUT} dV/dt rate to limit the inrush current.

$$dV_{OUT}/dt = 48\mu A/C_{SS}$$

$$t_{DELAY} = \frac{1.2V \bullet C_{SS}}{1\mu A}$$

The primary concern when selecting a CSS capacitor value is to select a value large enough to slow the V_{OUT} rise rate such that the input current stays below the minimum hot swap current limit due to foldback. The following equations are for input voltages above 10V and assume a 12mV minimum current limit voltage. The minimum C_{SS} capacitor could be reduced further for lower voltage inputs due to the minimum current limit voltage being higher due to less foldback. The following equations assume any V_{OUT} load remain off until after the hot swap completes, if loads are present on VOUT the CSS capacitor must be further increased to set a V_{OUT} rise rate such that the dV/dt • C_{OUT} current and the load current do not exceed the folded back current limit at any point.

The maximum dV/dt of the output without reaching current limit is

$$\frac{dV_{OUT}}{dt} = \frac{12mV}{R_{SNS} \bullet C_{OUT}}$$

$$\text{Minimum } C_{SS} = \frac{48\mu A}{12mV} \bullet R_{SNS} \bullet C_{OUT}$$

$$= 4mmho \bullet R_{SNS} \bullet C_{OUT}$$

The C_{SS} capacitance may be increased to any value to achieve a longer delay, however it must be larger than the minimum C_{SS} computed above to avoid current limit and tripping the circuit breaker.

The switcher and hot swap controller both share the negative terminal for their current sense amplifiers. The switcher reduces charger current so that there is at most 32mV between ISNSP_CHG and ISNSM and the hot swap controller will limit the input current to at most 48mV between ISNSP_HS and ISNSM. This allows a single sense resistor to be used in many applications, resulting in a hot swap circuit breaker that is 50% higher than the switcher's input current limit. Any two values may be selected by using two current sense resistors, see the Input Sense Resistors Selection section of this data sheet for more information.

Setting Switcher Input and Charge Currents

The maximum switcher input current is determined by the resistance across the ISNSP_CHG and ISNSM pins, typically R_{SNSI}. The maximum charge current is determined by the value of the sense resistor, R_{SNSC}, connected in series with the inductor. The input and charge current loops servo the voltage across their respective sense resistor to 32mV. Therefore, the maximum input and charge currents are:

$$I_{IN(MAX)} = \frac{32mV}{R_{SNSI}}$$

$$I_{CHG(MAX)} = \frac{32mV}{R_{SNSC}}$$

The peak inductor current limit for both buck and boost modes, I_{PEAK}, is 80% higher than the maximum charge current and is equal to:

$$I_{PEAK} = \frac{58mV}{R_{SNSC}}$$

This current limit is active in both charging and backup modes. In backup mode, it is the only control limitation on inductor and output current.

Low Current Charging and High Current Backup

The LTC3351 accommodates applications requiring low charge currents and high backup currents. In these applications, program the desired charge current using R_{SNSI}. The higher current needed during backup is set using

APPLICATIONS INFORMATION

R_{SNSC}. The input current limit will override the charge current limit when the supercapacitors are charging while the charge current limit provides sufficient current capability for backup operation.

The charge current will be limited to $I_{CHG(MAX)}$ at low V_{CAP} (i.e., low duty cycles). As V_{CAP} rises, the switching controller's input current will increase until it reaches $I_{IN(MAX)}$. The input current will be maintained at $I_{IN(MAX)}$ and the charge current will decrease as V_{CAP} rises further.

Some applications may want to use only a portion of the input current limit to charge the supercapacitors. Two input current sense resistors placed in series can be used to accomplish this as shown in Figure 6. ISNSP_CHG is kelvin connected to the positive terminal of R_{SNSI1} and ISNSM is kelvin connected to the negative terminal of R_{SNSI2}. The load current is pulled through R_{SNSI1} while the input current to the charger is pulled through R_{SNSI1} and R_{SNSI2}. The input current limit is:

$$32mV = R_{SNSI1} \bullet I_{LOAD} + (R_{SNSI1} + R_{SNSI2}) \bullet I_{INCHG}$$

For example, suppose that only 2A of input current is desired to charge the supercapacitors but the system load and charger combined can pull a total of up to 4A from the supply. Setting $R_{SNSI1} = R_{SNSI2} = 8m\Omega$ will set a 4A current limit for the load and charger, while setting a 2A limit for the charger. With no system load, the charger can pull up to 2A of input current. As the load pulls 0A to 4A of current, the charger's input will drop from 2A to 0A. The following equation can be used to determine charging input current as a function of system load current:

$$I_{INCHG} = \frac{32mV}{R_{SNSI1}+R_{SNSI2}} - \frac{R_{SNSI1}}{R_{SNSI1}+R_{SNSI2}} \bullet I_{LOAD}$$

The contact resistance of the negative terminal of R_{SNSI1} and the positive terminal of R_{SNSI2} as well as the resistance of the trace connecting them will contribute error to the input current limit. To minimize the error, place both input current sense resistors close together with a large PCB pad area between them as the system load current is pulled from the trace connecting the two sense resistors.

Note that the backup current will flow through R_{SNSI2}. Size the R_{SNSI2} resistor package to handle the power dissipation.

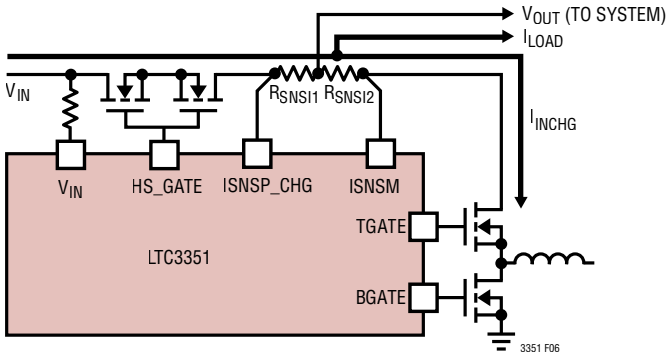


Figure 6.

Input Sense Resistors Selection

Any combination of hot swap current limit and switching charger input current limit can be achieved with two resistors. In Figure 7 below, three resistors are shown, however, in all configurations at least one will be replaced with a short.

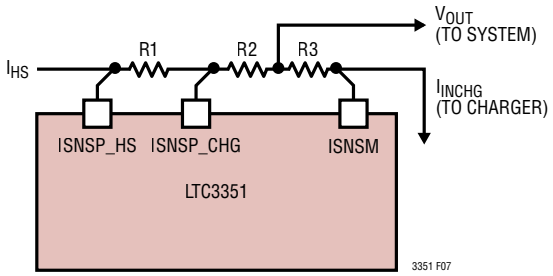


Figure 7.

If the desired hot swap current limit is 1.5 time the charger input current limit, then only R2 is needed and R1 and R3 are replaced with shorts.

$$R2 = 48mV/I_{HS}$$

If the desired hot swap current limit is greater than 1.5 times the charger input current limit, then R1 is replaced with a short. This will typically be the case when a higher backup current than charge current is needed.

$$R2 = 48mV/I_{HS}$$

APPLICATIONS INFORMATION

$R3 = 32mV/I_{INCHG} – R2$

In this configuration, R3 adds to the output impedance of the boost. Alternatively, the resistors may be reconfigured as shown in Figure 8.

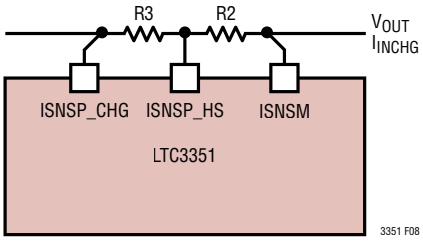


Figure 8.

If the desired charger input current limit is more than 2/3 of the hot swap input current limit R3 is replaced with a short.

$R2 = 32mV/I_{INCHG}$

$R1 = 48mV/I_{HS} – R2$

Note that the circuit breaker timer (the CTIMER pin) may run as low as 2% below the current limit, setting the charger's input current limit too close to the hot swap current limit will trip the circuit breaker. Operation with the charger's input current set close to the hot swap current limit requires careful attention to the LTC3351's tolerance for both $V_{ILIM(HS)}$ and V_{SNSI}, the tolerance of both current sense resistors, the layout, the worst case switching charger's input current ripple, and how quickly the switching charger can reduce its current due to the fastest increase in downstream V_{OUT} current.

Setting V_{CAP} Voltage

The LTC3351 V_{CAP} voltage is set by an external feedback resistor divider, as shown in Figure 9. The regulated output voltage is determined by:

$$V_{CAP} = \left(1 + \frac{R_{FBC1}}{R_{FBC2}}\right) CAPFBREF$$

where CAPFBREF is the output of the V_{CAP} DAC, programmed via vcapfb_dac. Take great care to route the CAPFB line away from noise sources, such as the SW line, BST, TGATE or BGATE.

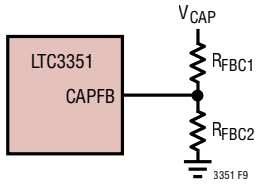


Figure 9.

Setting V_{OUT} Voltage in Backup Mode

The output voltage for the switching controller in step-up mode is set by an external feedback resistor divider, as shown in Figure 10. The regulated output voltage is determined by:

$$V_{OUT} = \left(1 + \frac{R_{FBO1}}{R_{FBO2}}\right) 1.2V$$

Take great care to route the OUTFB line away from noise sources, such as the SW line, BST or TGATE.

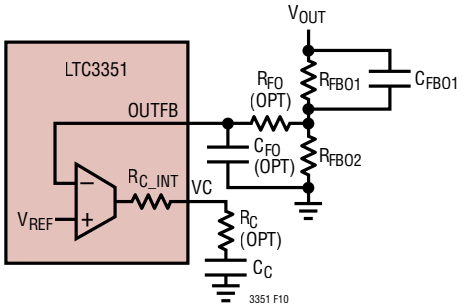


Figure 10. V_{OUT} Voltage Divider and Compensation Network

R_{C_INT} in Figure 10 is 1kΩ in buck mode and 2kΩ in boost mode.

Compensation

The input current, charge current, V_{CAP} voltage, and V_{OUT} voltage loops all require a 1nF to 10nF capacitor from the VC node to ground. When using the output ideal diode and backing up to low voltages (<8V), use 8.2nF to 10nF on VC. When not using the output ideal diode, 4.7nF to 10nF on VC is recommended. For very high backup voltages (>15V), 1nF to 4.7nF is recommended.

In addition to the VC node capacitor, the V_{OUT} voltage loop requires a phase-lead capacitor, C_{FBO1}, for stability and improved transient response during input power

APPLICATIONS INFORMATION

failure (Figure 10). The product of the top divider resistor and the phase-lead capacitor is used to create a zero at approximately 2kHz:

$$R_{FBO1} \bullet C_{FBO1} \approx \frac{1}{2\pi(2kHz)}$$

Choose R_{FBO1}, such that $C_{FBO1} \geq 100pF$, to minimize the effects of parasitic pin capacitance. Because the phase-lead capacitor introduces a larger ripple at the input of the V_{OUT} transconductance amplifier, an additional R_C low-pass filter from the V_{OUT} divider to the OUTFB pin may be needed to eliminate voltage ripple spikes. The filter time constant should be located at the switching frequency of the switching controller:

$$R_{FO} \bullet C_{FO} = \frac{1}{2\pi f_{SW}}$$

with $C_{FO} > 10pF$ to minimize the effects of parasitic pin capacitance. For backup applications, where the V_{OUT} regulation voltage is low (~5V to 6V), an additional 1k to 3k resistor, R_C, in series with the VC capacitor improves stability and transient response.

Minimum V_{CAP} Voltage in Backup Mode

In backup mode, power is provided to the output from the supercapacitors either through the output ideal diode or the switching controller operating in step-up mode.

The output ideal diode provides a low loss power path from the supercapacitors to V_{OUT}. The minimum internal (open-circuit) supercapacitor voltage will be equal to the minimum V_{OUT} necessary for the system to operate plus the voltage drops due to the output ideal diode and equivalent series resistance, R_{SC}, of each supercapacitor in the stack.

Example: System needs 5V to run and draws 1A during backup. There are four supercapacitors in the stack, each with an R_{SC} of 45mΩ. The output ideal diode forward regulation voltage is 30mV (OUTFET $R_{DS(ON)} < 30m\Omega$). The minimum open-circuit supercapacitor voltage is:

$$V_{CAP(MIN)} = 5V + 0.030V + (1A \bullet 4 \bullet 45m\Omega) = 5.21V$$

Using the switching controller in step-up mode allows the supercapacitors to be discharged to a voltage much lower than the minimum V_{OUT} needed to run the system. The amount of power that the supercapacitor stack can deliver at its minimum internal (open-circuit) voltage should be greater than what is needed to power the output and the step-up converter.

According to the maximum power transfer rule:

$$P_{CAP(MIN)} = \frac{V_{CAP(MIN)}^2}{4 \bullet n \bullet R_{SC}} > \frac{P_{BACKUP}}{\eta}$$

In the equation above η is the efficiency of the switching controller in step-up mode and n is the number of supercapacitors in the stack.

Example: System needs 5V to run and draws 1A during backup. There are four supercapacitors in the stack (n = 4), each with an R_{SC} of 45mΩ. The converter efficiency is 90%. The minimum open-circuit supercapacitor voltage is:

$$V_{CAP(MIN)} = \sqrt{\frac{4 \bullet 4 \bullet 45m\Omega \bullet 5V \bullet 1A}{0.9}} = 2.0V$$

In this case, the voltage seen at the terminals of the capacitor stack is half this voltage, or 1V, according to the maximum power transfer rule.

Note the minimum V_{CAP} voltage can also be limited by the peak inductor current limit (180% of maximum charge current) and the maximum duty cycle in step-up mode (~90%).

Optimizing Supercapacitor Energy Storage Capacity

In most systems the supercapacitors will provide backup power to one or more DC/DC converters. A DC/DC converter presents a constant power load to the supercapacitor stack. When the supercapacitors are near their maximum voltage, the loads will draw little current. As the capacitors discharge, the current drawn from supercapacitors will increase to maintain constant power to the load. The amount of energy required in back up mode is the product of this constant backup power, P_{BACKUP}, and the backup time, t_{BACKUP}.

APPLICATIONS INFORMATION

The energy stored in a stack of n supercapacitors available for backup is:

$$\frac{1}{2}nC_{SC}\left(V_{CELL(MAX)}^2 - V_{CELL(MIN)}^2\right)$$

where C_{SC}, $V_{CELL(MAX)}$ and $V_{CELL(MIN)}$ are the capacitance, maximum voltage and minimum voltage of a single capacitor in the stack, respectively. The maximum voltage on the stack is $V_{CAP(MAX)} = n \bullet V_{CELL(MAX)}$. The minimum voltage on the stack is $V_{CAP(MIN)} = n \bullet V_{CELL(MIN)}$.

Some of this energy will be dissipated as conduction loss in the ESR of the supercapacitor stack. A higher backup power requirement leads to a higher conduction loss for a given stack ESR.

The amount of capacitance needed is found by solving the following equation for C_{SC}:

where:

$$\gamma_{MAX} = 1 + \sqrt{1 - \frac{4R_{SC} \bullet P_{BACKUP}}{nV_{CELL(MAX)}^2}} \text{ and,}$$

$$\gamma_{Min} = 1 + \sqrt{1 - \frac{4R_{SC} \bullet P_{BACKUP}}{nV_{CELL(MIN)}^2}}$$

R_{SC} is the equivalent series resistance (ESR) of a single supercapacitor in the stack. Note that the maximum power transfer rule limits the minimum cell voltage to:

$$V_{CELL(MIN)} = \frac{V_{CAP(MIN)}}{n} \geq \sqrt{\frac{4R_{SC} \bullet P_{BACKUP}}{n}}$$

A calculator for this is available on the LTC3350 website.

$$P_{BACKUP} \bullet t_{BACKUP} = \frac{1}{4}nC_{SC}\left[\gamma_{MAX} \bullet V_{CELL(MAX)}^2 - \gamma_{MIN} \bullet V_{CELL(MIN)}^2 - \frac{4R_{SC} \bullet P_{BACKUP}}{n} \ln\left(\frac{\gamma_{MAX} \bullet V_{CELL(MAX)}}{\gamma_{MIN} \bullet V_{CELL(MIN)}}\right)\right]$$

APPLICATIONS INFORMATION

To minimize the size of the capacitance for a given amount of backup energy, increase the maximum voltage on the stack, $V_{CELL(MAX)}$. However, the voltage is limited to a maximum of 2.7V and higher than this may lead to an unacceptably low capacitor lifetime.

An alternative option is to keep $V_{CELL(MAX)}$ at a voltage that leads to reasonably long lifetime and increase the capacitor utilization ratio of the supercapacitor stack. The capacitor utilization ratio, α_B, can be defined as:

$$\alpha_B = \frac{V_{CELL(MAX)}^2 - V_{CELL(MIN)}^2}{V_{CELL(MAX)}^2}$$

If the synchronous controller is used in step-up mode, then the supercapacitors can be run down to a voltage set by the maximum power transfer rule to maximize the utilization ratio. The minimum voltage in this case is:

$$V_{CELL(MIN)} = \sqrt{\frac{4R_{SC} \bullet P_{BACKUP}}{n\eta}}$$

where η is the efficiency of the boost converter (~90% to 96%). For the backup equation, γ_{MAX} and γ_{MIN}, substitute P_{BACKUP}/η for P_{BACKUP}. In this case the energy needed for backup is governed by the following equation:

$$\frac{P_{BACKUP}}{\eta} t_{BACKUP} \le \frac{1}{2} nC_{SC} \bullet V_{CELL(MAX)}^2 \bullet \left[\frac{\alpha_B + \sqrt{\alpha_B}}{2} - \frac{1-\alpha_B}{2} \ln\left(\frac{1+\sqrt{\alpha_B}}{\sqrt{1-\alpha_B}} \right) \right]$$

Once a capacitance is found using the above equation the maximum ESR allowed needs to be checked:

$$R_{SC} \le \frac{\eta(1-\alpha_B) n V_{CELL(MAX)}^2}{4P_{BACKUP}}$$

Capacitor Selection Procedure

1. Determine backup requirements P_{BACKUP} and t_{BACKUP}.
2. Determine maximum cell voltage that provides acceptable capacitor lifetime.
3. Choose number of capacitors in the stack.
4. Choose a desired utilization ratio, α_B, for the supercapacitor (e.g., 80%).
5. Solve for capacitance, C_{SC}:

$$C_{SC} \ge \frac{2P_{BACKUP} \bullet t_{BACKUP}}{n\eta V_{CELL(MAX)}^2} \bullet \left[\frac{\alpha_B + \sqrt{\alpha_B}}{2} - \frac{1-\alpha_B}{2} \ln\left(\frac{\left(1+\sqrt{\alpha_B}\right)}{\sqrt{1-\alpha_B}} \right) \right]^{-1}$$

6. Find supercapacitor with sufficient capacitance C_{SC} and minimum R_{SC}:

$$R_{SC} \le \frac{\eta(1-\alpha_B) n V_{CELL(MAX)}^2}{4P_{BACKUP}}$$

7. If a suitable capacitor is not available, iterate by choosing more capacitance, a higher cell voltage, more capacitors in the stack and/or a lower utilization ratio.
8. Make sure to take into account the lifetime degradation of ESR and capacitance, as well as the maximum discharge current rating of the supercapacitor. A list of supercapacitor suppliers is provided in Table 2.

Table 2. Supercapacitor Suppliers

AVX	www.avx.com
Bussmann	www.cooperbussmann.com
CAP-XX	www.cap-xx.com
Illinois Capacitor	www.illcap.com
Kemet Corp.	www.kemet.com
Maxwell	www.maxwell.com
Murata	www.murata.com
NESS CAP	www.nesscap.com
Tecate Group	www.tecategroup.com

APPLICATIONS INFORMATION

Inductor Selection

The switching frequency and inductor selection are interrelated. Higher switching frequencies allow the use of smaller inductor and capacitor values, but generally results in lower efficiency due to MOSFET switching and gate charge losses. In addition, the effect of inductor value on ripple current must also be considered. The inductor ripple current decreases with higher inductance or higher frequency and increases with higher V_{IN}. Accepting larger values of ripple current allows the use of low inductances but results in higher output voltage ripple and greater core losses.

For the LTC3351, the best overall performance will be attained if the inductor is chosen to be:

$$L = \frac{V_{IN(MAX)}}{I_{CHG(MAX)} \bullet f_{SW}}$$

for $V_{IN(MAX)} \leq 2VCAP$ and:

$$L = \left(1 - \frac{V_{CAP}}{V_{IN(MAX)}}\right) \frac{V_{CAP}}{0.25 \bullet I_{CHG(MAX)} \bullet f_{SW}}$$

for $V_{IN(MAX)} \geq 2VCAP$, where V_{CAP} is the final supercapacitor stack voltage, $V_{IN(MAX)}$ is the maximum input voltage, $I_{CHG(MAX)}$ is the maximum regulated charge current, and f_{SW} is the switching frequency. Using these equations, the inductor ripple will be at most 25% of $I_{CHG(MAX)}$.

Using the above equation, the inductor may be too large to provide a fast enough transient response to hold up V_{OUT} when input power goes away. This occurs in cases where the maximum V_{IN} is high (e.g. 25V) and the backup voltage low (e.g. 6V). In these situations it would be best to choose an inductor that is smaller resulting in maximum peak-to-peak ripple as high as 40% of $I_{CHG(MAX)}$.

Once the value for L is known, the type of inductor core is selected. Ferrite cores are recommended for their very low core loss. Selection criteria should concentrate on minimizing copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This causes an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate. The saturation current for the inductor should be at least 80% higher than the maximum regulated current, $I_{CHG(MAX)}$. A list of inductor suppliers is provided in Table 3.

Table 3. Inductor Vendors

VENDOR	URL
Coilcraft	www.coilcraft.com
Murata	www.murata.com
Sumida	www.sumida.com
TDK	www.tdk.com
Toko	www.toko.com
Vishay	www.vishay.com
Würth Electronic	www.we-online.com

C_{OUT} and C_{CAP} Capacitance

V_{OUT} serves as the input to the synchronous controller in step-down mode and as the output in step-up (backup) mode. If step-up mode is used, place 100µF of bulk (aluminum electrolytic, OS-CON, POSCAP) capacitance for every 2A of backup current desired. For 5V system applications, 100µF per 1A of backup current is recommended. In addition, a certain amount of high frequency bypass capacitance is needed to minimize voltage ripple. The voltage ripple in step-up mode is:

$$\Delta V_{OUT} =$$

$$\left[\left(1 - \frac{V_{CAP}}{V_{OUT}}\right) \frac{1}{C_{OUT} \bullet f_{SW}} + \frac{V_{OUT}}{V_{CAP}} \bullet R_{ESR}\right] I_{OUT(BACKUP)}$$

Maximum ripple occurs at the lowest V_{CAP} that can supply $I_{OUT(BACKUP)}$. Multilayer ceramics are recommended for high frequency filtering.

If step-up mode is unused, then the specification for C_{OUT} will be determined by the desired ripple voltage in step-down mode:

$$\Delta V_{OUT} =$$

$$\frac{V_{CAP}}{V_{OUT}}\left(1 - \frac{V_{CAP}}{V_{OUT}}\right) \frac{I_{CHG(MAX)}}{C_{OUT} \bullet f_{SW}} + I_{CHG(MAX)} \bullet R_{ESR}$$

APPLICATIONS INFORMATION

In continuous conduction mode, the source current of the top MOSFET is a square wave of duty cycle V_{CAP}/V_{OUT}. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{CHG(MAX)} \frac{V_{CAP}}{V_{OUT}} \sqrt{\frac{V_{OUT}}{V_{CAP}} - 1}$$

This formula has a maximum at $V_{OUT} = 2VCAP$, where $I_{RMS} = I_{CHG(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Medium voltage (20V to 35V) ceramic, tantalum, OS-CON and switcher-rated electrolytic capacitors can be used as input capacitors. Sanyo OS-CON SVP, SVPD series, Sanyo POSCAP TQC series, or aluminum electrolytic capacitors from Panasonic WA series or Cornell Dubilier SPV series in parallel with a couple of high performance ceramic capacitors can be used as an effective means of achieving low ESR and high bulk capacitance.

V_{CAP} serves as the input to the switching controller in step-up mode and as the output in step-down mode. The purpose of the V_{CAP} capacitor is to filter the inductor current ripple. The V_{CAP} ripple (ΔV_{CAP}) is approximated by:

$$\Delta V_{CAP} \approx \Delta I_{PP} \left(\frac{1}{8C_{CAP} \bullet f_{SW}} + R_{ESR} \right)$$

where f_{SW} is the switching frequency, C_{CAP} is the capacitance on V_{CAP} and ΔI_{PP} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_{PP} increases with input voltage.

Because supercapacitors have low series resistance, it is important that C_{CAP} be sized properly so that the bulk of the inductor current ripple flows through the filter capacitor and not the supercapacitor. It is recommended that:

$$\left(\frac{1}{8C_{CAP} \bullet f_{SW}} + R_{ESR} \right) \leq \frac{n \bullet R_{SC}}{5}$$

where n is the number of supercapacitors in the stack and R_{SC} is the ESR of each supercapacitor. The capacitance on V_{CAP} can be a combination of bulk and high frequency capacitors. Aluminum electrolytic, OS-CON and POSCAP capacitors are suitable for bulk capacitance while multilayer ceramics are recommended for high frequency filtering.

Power MOSFET Selection

Two external power MOSFETs are selected for the LTC3351's synchronous controller: one N-channel MOSFET for the top switch and one N-channel MOSFET for the bottom switch. The selection criteria of the external N-channel power MOSFETs include maximum drain-source voltage (V_{DSS}), threshold voltage, on-resistance ($R_{DS(ON)}$), reverse transfer capacitance (C_{RSS}), total gate charge (Q_G), and maximum continuous drain current.

Select V_{DSS} of both MOSFETs to be higher than the maximum input supply voltage (including transient). The peak-to-peak drive levels are set by the DRV_{CC} voltage. Logic-level threshold MOSFETs should be used because DRV_{CC} is powered from either $INTV_{CC}$ (5V) or an external LDO whose output voltage must be less than 5.5V.

MOSFET power losses are determined by $R_{DS(ON)}$, C_{RSS} and Q_G. The conduction loss at maximum charge current for the top and bottom MOSFET switches are:

$$P_{COND(TOP)} = \frac{V_{CAP}}{V_{OUT}} I_{CHG(MAX)}{}^2 \bullet R_{DS(ON)} (1 + \delta\Delta T)$$

$$P_{COND(BOT)} = \left(1 - \frac{V_{CAP}}{V_{OUT}} \right) I_{CHG(MAX)}{}^2 \bullet R_{DS(ON)} (1 + \delta\Delta T)$$

The term $(1 + \delta\Delta T)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

Both MOSFET switches have conduction loss. However, transition loss occurs only in the top MOSFET in step-down mode and only in the bottom MOSFET in step-up mode. These losses are proportional to $V_{OUT}{}^2$ and can be considerably large in high voltage applications (V_{OUT} > 20V). The maximum transition loss is:

$$P_{TRAN} \approx \frac{k}{2} V_{OUT}{}^2 \bullet I_{CHG(MAX)} \bullet C_{RSS} \bullet f_{SW}$$

APPLICATIONS INFORMATION

where k is related to the drive current during the Miller plateau and is approximately equal to one.

The synchronous controller can operate in both step-down and step-up mode with different voltages on V_{OUT} in each mode. If V_{OUT} is 12V in step-down mode (input power available) and 10V in step-up mode (backup mode) then both MOSFETs can be sized to minimize conduction loss. If V_{OUT} can be as high as 25V while charging and V_{OUT} is held to 6V in backup mode, then the MOSFETs should be sized to minimize losses during backup mode. This may lead to choosing a high side MOSFET with significant transition loss which may be tolerable when input power is available so long as thermal issues do not become a limiting factor. The bottom MOSFET can be chosen to minimize conduction loss. If step-up mode is unused, then choosing a high side MOSFET that that has a higher $R_{DS(ON)}$ device and lower C_{RSS} would minimize overall losses.

Another power loss related to switching MOSFET selection is the power lost to driving the gates. The total gate charge, QG, must be charged and discharged each switching cycle. The power is lost to the internal LDO and gate drivers within the LTC3351. The power lost due to charging the gates is:

$$P_G \approx (Q_{GTOP} + Q_{GBOT}) \bullet f_{SW} \bullet V_{OUT}$$

where Q_{GTOP} is the top MOSFET gate charge and Q_{GBOT} is the bottom MOSFET gate charge. Whenever possible, utilize MOSFET switches that minimize the total gate charge to limit the internal power dissipation of the LTC3351.

Schottky Diode Selection

Optional Schottky diodes can be placed in parallel with the top and bottom MOSFET switches. These diodes clamp SW during the non-overlap times between conduction of the top and bottom MOSFET switches. This prevents the body diodes of the MOSFET switches from turning on, storing charge during the non-overlap time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. One or both diodes can be omitted if the efficiency loss can be tolerated. Rate the diode for about one-third to one-fifth of the full load current since it is on for only a fraction of the duty cycle. Larger diodes result in additional switching losses due to their larger junction capacitance. In order for the diodes to be effective, the inductance between them and the top and bottom MOSFETs must be as small as possible. Place these components next to each other on the same layer of the PC board.

Top MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor, C_B, connected to the BST pin supplies the gate drive voltage for the top MOSFET. Capacitor C_B, in Figure 11, is charged though an external diode, D_B, from DRV_{CC} when the SW pin is low. The value of the bootstrap capacitor, C_B, needs to be 20 times that of the total input capacitance of the top MOSFET.

The bottom MOSFET, MN2 in Figure 11, turning on ensures that the SW pin goes low. If the bottom MOSFET is on for less than 50µS for eight consecutive switching cycles, the bottom MOSFET will turn on for 100nS to 250nS at the end of the eighth switching cycle to refresh the voltage on C_B.

With the top MOSFET on, the BST voltage is above the system supply rail:

$$V_{BST} = V_{OUT} + V_{DRVCC}$$

The reverse break down of the external diode, D_B, must be greater than $V_{OUT(MAX)} + V_{DRVCC(MAX)}$.

The step-up converter briefly runs non-synchronously when used with the output ideal diode. During this time the BST to SW voltage can pump up to voltages exceeding 5.5V if D_B is a Schottky diode. Fast switching PN diodes are recommended due to their low leakage and junction capacitance. A Schottky diode can be used if the step-up converter runs synchronous throughout backup mode.

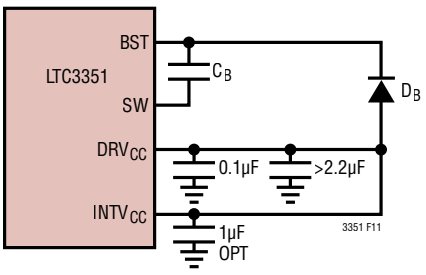


Figure 11.

APPLICATIONS INFORMATION

$INTV_{CC}/DRV_{CC}$ and IC Power Dissipation

The LTC3351 features a low dropout linear regulator (LDO) that supplies power to $INTV_{CC}$ from the V_{OUT} supply. $INTV_{CC}$ powers the gate drivers (when connected to DRV_{CC}) and much of the LTC3351's internal circuitry. The LDO regulates the voltage at the $INTV_{CC}$ pin to 5V. The LDO can supply a maximum current of 50mA and must be bypassed to ground with a minimum of 1µF when not connected to DRV_{CC}. DRV_{CC} should have at least a 2.2µF ceramic or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used on DRV_{CC}, an additional 0.1µF ceramic capacitor placed directly adjacent to the DRV_{CC} pin is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3351 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, is supplied by the 5V LDO.

Power dissipation for the IC in this case is highest and is approximately equal to $(V_{OUT}) \bullet (I_Q + I_G)$, where I_Q is the non-switching quiescent current of ~4mA and I_G is gate charge current. The junction temperature is estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the I_G supplied by the $INTV_{CC}$ LDO is limited to less than 42mA from a 35V supply in the QFN package at a 70°C ambient temperature:

$T_J = 70°C + (35V)(4mA + 42mA)(36.4°C/W) = 125°C$

To prevent the maximum junction temperature from being exceeded, the $INTV_{CC}$ LDO current must be checked while operating in continuous conduction mode at maximum V_{OUT}.

The power dissipation in the IC is drastically reduced if DRV_{CC} is powered from an external LDO. In this case the power dissipation in the IC is equal to power dissipation due to I_Q and the power dissipated in the gate drivers, $(V_{DRVCC}) \bullet (I_G)$. Assuming the external DRV_{CC} LDO output is 5V and is supplying 42mA to the gate drivers, at 70°C ambient the junction temperature rises to only 80.5°C:

$T_J = 70°C + [(35V)(2.25mA)+(5V)(42mA)](36.4°C/W) = 80.5°C$

Power the external LDO from V_{OUT}. It must be enabled after the $INTV_{CC}$ LDO has powered up and its output must be less than 5.5V. $INTV_{CC}$ should no longer be tied to DRV_{CC}.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3351 is capable of turning on the top MOSFET in step-down mode. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. The minimum on-time for the LTC3351 is approximately 85ns. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{CAP}}{V_{OUT} \bullet f_{SW}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the switching controller will begin to skip cycles. The charge current and V_{CAP} voltage will continue to be regulated, but the ripple voltage and current will increase.

Ideal Diode MOSFET Selection

An external N-channel MOSFET is required for the output ideal diode. Important parameters for the selection of this MOSFET is the maximum drain-source voltage, V_{DSS}, gate threshold voltage and on-resistance ($R_{DS(ON)}$).

When the supercapacitors are at 0V, the input voltage is applied across the output ideal diode MOSFET. Therefore, the V_{DSS} of the output ideal diode MOSFET must withstand the highest voltage on V_{IN}.

The gate drive for the ideal diode is 5V. Use logic-level threshold N-channel MOSFET.

As a general rule, select a MOSFET with a low enough $R_{DS(ON)}$ to obtain the desired V_{DS} while operating at full load current. The LTC3351 will regulate the forward voltage drop across the output ideal diode MOSFET to 30mV

APPLICATIONS INFORMATION

if $R_{DS(ON)}$ is low enough. The required $R_{DS(ON)}$ can be calculated by dividing 0.030V by the load current in amps.

Achieving forward regulation will minimize power loss and heat dissipation, but it is not a necessity. If a forward voltage drop of more than 30mV is acceptable, then a smaller MOSFET can be used but must be sized compatible with the higher power dissipation. Care should be taken to ensure that the power dissipated is never allowed to rise above the manufacturer's recommended maximum level.

During backup mode, the output ideal diode shuts off when the voltage on OUTFB falls below 1.3V. For high V_{OUT} backup voltages (>8.4V), the output ideal diode will shut off when V_{CAP} is more than a diode drop (~700mV) above the V_{OUT} regulation point (i.e., OUTFB > 1.2V). The body diode of the output ideal diode N-channel MOSFET will carry the load current until V_{CAP} drops to within a diode drop of the V_{OUT} regulation voltage at which point the switching controller takes over. During this period the power dissipation in the output ideal diode MOSFET increases significantly. Diode conduction time is small compared to the overall backup time but can be significant when discharging very large supercapacitors (>600F). Care should be taken to properly heat sink the MOSFET to limit the temperature rise.

Hot Swap Input FET Selection

In addition to $R_{DS(ON)}$ requirements, the hot swap input FET must be sized for safe operating area (SOA). This is done by sizing for both the start-up characteristic of the system and to handle a short circuit of the duration set by CTIMER. Typically, the FET should be sized for the worst case startup condition and CTIMER should be set such that a short circuit will require less SOA than the startup condition. Logic level gate FETs are required.

The foldback curve reduces the SOA requirement of the FET. The LTC3351's foldback curve reduces the effective current limit as the voltage across the FET (as measured from V_{IN} to V_{OUT}) increases. The current is linearly reduced from 100% at 1V to about 20% at 11V, voltages larger than 11V will remain at 20%.

Simplified SOA Requirement Calculation:

1. Determine the output slew rate (see page 26).
2. Using this slew rate and the output capacitance determine the inrush current.
3. Add any enabled downstream loads to this inrush current to determine the input current.
4. Using the slew rate and maximum input voltage, determine the output capacitor charge time.

Using the output capacitor charging time, the input current and the maximum input voltage, select a FET with an appropriate SOA. The CTIMER capacitor value should be set to not exceed the FETs SOA when the output is shorted with maximum input voltage.

Hot Reconnects

Return of input power when operating in backup mode must be considered. The RETRYB pin provides a mechanism to prevent returning to input power based on either the V_{OUT} voltage or digital signal, typically indicating the backup has completed. The RETRYB pin may also be grounded causing the LTC3351 to attempt to reconnect the system to the input once all other reconnect criteria are met. If the RETRYB pin is grounded, and a handover from backup operation back to V_{IN} operation is required, it is essential that the load line of the system remain below the foldback curve of the hot swap controller. If the system load exceeds the foldback curve of the hot swap controller, the controller will be unable to support the load and an over-current fault will occur. After the CTIMER cool down time has passed, the cycle will repeat indefinitely until the energy storage is depleted and the load shuts down, returning the system to conditions resembling an initial power-up. This may be prevented by keeping the foldback curve above the systems load line. Boosting to a voltage near V_{IN} will allow the hot swap to start at a high current point on the foldback curve and may allow the hot swap controller to reconnect V_{IN} without running into current limit.

APPLICATIONS INFORMATION

Alternate Hot Swap Controller Configuration

Typically, the CSS capacitor sets both the debounce time and the maximum rise rate of V_{OUT}. If the fixed relationship between the debounce time and the maximum rise rate is not satisfactory the hot swap controller has an alternate configuration to decouple these two parameters, however this comes at the expense of reduced current limit speed.

In this alternate configuration, the CSS capacitor is connected from the CSS pin to ground. In this configuration, the CSS capacitor will only function as a debounce timer. The rise rate of the output is controlled by $I_{HS\_GATE(UP)}$ into the capacitance of the HS_GATE node. Adding a capacitor from the HS_GATE pin to ground allows the output rise rate to be programmed independently of all other parameters. However, this capacitance represents a large load that the current limit amplifier must drive, resulting in a slower current limit. A 1kΩ resistor should be placed in series with this capacitor. This resistor will limit current into the HS_GATE when the HS_GATE pin is pulled to ground due to a fault being detected.

Increased Capacitance Test Current

The LTC3351 can sink up to 60mA of capacitance test current dissipating up to 300mW. This constant current sink is capable of testing large capacitors, however the test time may become unreasonably long. To increase the test current, a simple circuit using a low V_t (<1.2V V_{GS}) NMOS and a resistor may be used. The gate of the NMOS is connected to the ITST pin such that when the ITST circuit is turned on the NMOS is also turned on. This circuit allows much higher capacitance test current than the LTC3351 alone.

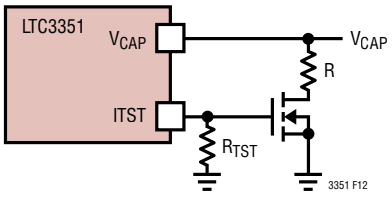


Figure 12. Increased Capacitance Test Current

When using this circuit, the test current will be the original ITST circuit current plus an additional current due to the capacitor stack voltage across the resistor. This requires a modified equation for converting meas_cap to capacitance. This equation is:

$$C = \frac{-56 \bullet 10^{-9} \bullet R_t \bullet meas\_cap}{R \bullet \ln\left[1 - \frac{\Delta V_{CAP}}{1.2V \bullet \frac{R}{R_{TST}} + V_{CAP}}\right]}$$

Where R is the resistance in the added ITST circuit, V_{CAP} is the charge voltage at the beginning of the test and ΔV_{CAP} is the voltage set using the cap_delta_v_setting register. R, R_{TST} and R_t are in Ohms, C is in Farads, and V_{CAP} and ΔV_{CAP} are in volts. The above equation is valid when ctl_cap_scale is 1 (the small setting); if the large setting is used, the above equation should be multiplied by 100.

Increased Shunt Current

The LTC3351 can shunt up to 500mA around an individual cell that has reached V_{SHUNT} as set by the vshunt register. This limits the charge rate of the other capacitors because the charge current is reduced to near the shunt current while shunting to prevent each cap from exceeding V_{SHUNT}. To enable faster charging while shunting, higher shunt current is needed.

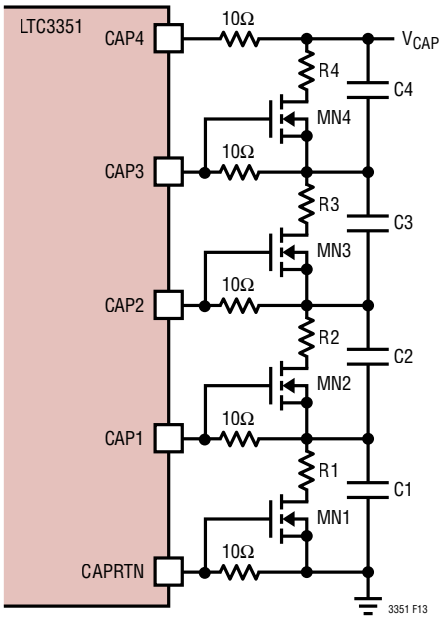


Figure 13. Increased Shunt Current Circuit Addition

APPLICATIONS INFORMATION

Higher shunt current may be accommodated with an external NMOS and resistor across each capacitor as shown in Figure 13. The shunt current will be V_{SHUNT} divided by R_X (assuming the $R_{DS(ON)}$ of MNx is small compared to R_X). The logic level NMOS must be selected so that its V_{GS} at the desired shunt current is less than one half the V_{SHUNT} voltage. When using this circuit the shunt resistors should be increased to 10Ω to minimize the drop across the LTC3351's internal shunt FET and thus maximize the V_{GS} for MN_X. Using 10Ω resistors will also reduce the power dissipation allowing a smaller package size compared to the typical application's 2.7Ω. When using 10Ω resistors the internal shunt FET will turn on the external NMOS, however the internal balancer's current will not create enough voltage across the 10Ω resistors to turn on the external NMOS. Additionally, increasing the 10Ω resistors to 500Ω will allow the internal balancers to turn on the external FETs, thus also increasing balance current.

Input Short Protection

The LTC3351's input current sense amplifier, ISNSP_HS to ISNSM and ISNSP_CHG to can have at most 0.3V between them. This is not typically an issue since the LTC3351 regulates input current to 48mV (hot swap current limit) or 32mV (charger input current limit) using these pins. The LTC3351 hot swap does not regulate reverse input current. If the input voltage is rapidly reduced (the input directly shorted to ground for instance) large currents will flow from the V_{OUT} capacitance to the V_{IN} short. Unless external protection is used, these large currents can quickly produce many volts of drop across the input sense resistor(s), overstressing the input current sense pins. If the input is shorted after it has fallen below the UV threshold, this is not an issue since the hot swap FETs have already been turned off. However, if the input supply can be shorted to ground while the LTC3351 is connected, the input protection circuit in Figure 14 is recommended. Also if the system load is so low that the LTC3351 circuit can be disconnected from the input and then shorted to ground before the input falls below UV, then the same circuit is also recommended.

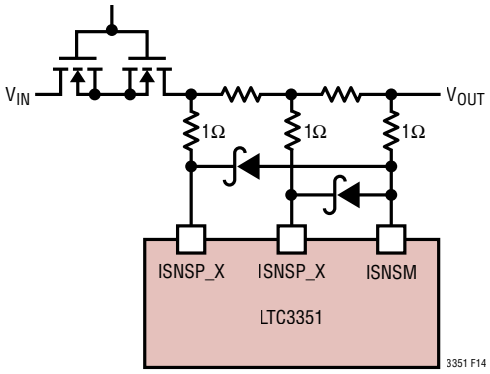


Figure 14. Input Short Protection Circuit

Since there are several possible configurations for the input current sense resistors, not all possible protection circuits are shown. To construct a circuit for another configuration of input current sense resistors, there should be one Schottky diode for each current sense amplifier (ISNSP_HS-ISNSM and ISNSP_CHG-ISNSM). There should be 1Ω between the current sense resistor and the current sense pins, and the diode should be connected such that it can conduct current in the direction from V_{OUT} to V_{IN}, this means the anodes will be connected to ISNSM. In this circuit, the Schottky diode is a simple clamp to limit the voltage across the pins. The 1Ω resistors are needed to limit the current in each Schottky diode. Clearly, if only one sense resistor is used, only one protection diode is needed.

Supercapacitor Settling

The ESR-only supercapacitor model using a capacitor in series with an equivalent series resistance (ESR) is over-simplified. Real supercapacitors have an additional settling time due to their internal physics

To explain the implications of this settling, assume a super capacitor of infinite capacitance such that any voltage change due to charging or discharging can be ignored. In the simple ESR-only model, a pulse of current would simply result in a step in voltage at its rising edge and a step back to its initial voltage at its falling edge. A real supercapacitor's response to the same pulse of current's rising edge will be an instantaneous step in voltage due to the high frequency ESR, followed by a settling to a higher voltage due to the "DC" ESR. On the falling edge there will be an

APPLICATIONS INFORMATION

instantaneous drop in voltage due to the high frequency ESR and a slower settling back to the original voltage due to the "DC" ESR. The following figure illustrates this.

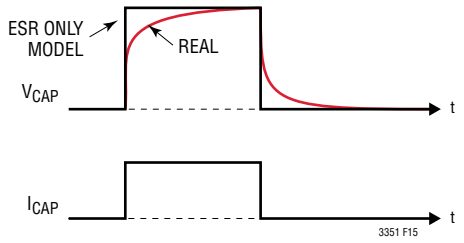


Figure 15.

This results in an ESR measurement dependent on the frequency at which it is measured. There is a high frequency ESR and a larger "DC" ESR. In energy storage applications where the capacitors will supply a sustained load, the "DC" ESR limits the deliverable power. Supercapacitor manufacturers have various methods for measuring ESR. Even when specifying a "DC" ESR, the measurement is often done at a frequency significantly higher than "DC", often near 100Hz, thereby reporting an intermediate frequency ESR.

ESR Measurement Timing Adjustments

The LTC3351 default ESR measurement timing is set to measure between the DC and high frequency ESR, closer to the high frequency ESR for a wide variety of supercapacitors. The timing can be adjusted to measure closer to the DC ESR, however this must done empirically based on the exact switching controller configuration and capacitors used. Values appropriate for some capacitors would result in failed measurements for others and there are no meaningful defaults preprogrammed in the LTC3351.

Using an DC coupled oscilloscope with a precision offset, observe the supercapacitor stack voltage (V_{CAP}) during the ESR test. AC coupling will not work as the signal time scales are too long to cross the oscilloscope's AC coupling high pass filter without distortion. Set the oscilloscope to trigger on $\overline{\text{SMBALERT}}$ falling and enabling the mon_meas_active alert using the mask_mon_meas_active bit. Then set the ctl_start_cap_esr_meas to start the ESR measurement. The SMBAlert will need to be cleared each time to re-trigger the oscilloscope. Alternatively, a current probe can be used to trigger on input current, since the input current will be high during the ESR test.

The esr_i_override setting is available to prevent the automatic adjustment of the ESR test current. The automatically selected ESR test current is available in the next_esr_i register. After several measurements have been completed, next_esr_i may be used as a starting point to manually set esr_i_override. While adjusting the timing of the ESR measurement, either set esr_i_override so the test current won't change between successive measurements or do each measurement twice for each setting and ignore the first result.

Referring to Figure 4, using the oscilloscope you can now see the effects of esr_i_on_settling and esr_i_off_settling on the captured waveform. Begin by adjusting esr_i_off_settling so that V_{CAP} is no longer decreasing significantly after esr_i_off_settling time. This time will likely be significantly longer than the default time.

The esr_i_on_settling time is a little more complicated to adjust as the capacitors are being charged during this time. If the esr_i_on_settling time is too short, the internal chemistry of the supercapacitor will not have settled and the ESR measured will be closer to the high frequency ESR than the DC ESR. If esr_i_on_settling is too long and esr_i_override is not set, then charge current will be automatically adjusted downward, resulting in reduced signal for the ESR measurement. If esr_i_on_settling is too long while esr_i_override is set, the capacitors will charge to constant voltage and charge current will fall, corrupting the measurement. This can be observed in the input current waveform. During an ESR test, it should not decrease, it should turn off cleanly. The charge current can also be observed by comparing esr_m1_i and esr_m2_i. They should be about the same, esr_m2_i should not be significantly less than esr_m1_i. If it is, esr_i_on_settling is too long.

If esr_i_override is set, monitor the increase in stack voltage during the ESR test. Ideally it should be about the same as the Δv in the capacitance test (as set by cap_delta_v_setting). If the change in voltage during the ESR test is less than in the capacitance test, esr_i_override can be increased to maximize the signal available for

APPLICATIONS INFORMATION

ESR test. If the voltage increase during the ESR test is more than the voltage set by cap_delta_v_setting, cap_delta_v_setting can be increased for more resolution in the capacitance test.

When configuring the test, there must be enough voltage between the vcapfb_dac setting and 1.2V to perform the test.

If configuring the ESR test to measure the high frequency ESR, the only adjustment necessary is to reduce the esr_i_off_settling to 0. The default setting for esr_i_on_settling is set to fully allow the switcher to settle under all normal conditions and should not be further reduced when measuring the high frequency ESR.

Individual Capacitor ESR and Capacitance Calculation

The LTC3351 reports total stack capacitance and ESR. From the stored voltage and current measurements, it is possible to calculate each individual capacitor's ESR and capacitance. For the calculation algorithm contact the factory.

Capacitance Measurement Timing Adjustments

Like the ESR measurement, the capacitance measurement is subject to non-ideal effects of the supercapacitors. The LTC3351 measures capacitance by pre-charging the capacitor stack by 1.25 • cap_delta_v_setting (the ESR test contributes to this charging), turning on a test discharge current, waiting the time specified by cap_i_on_settling, measuring a first voltage, then waiting for the stack to discharge cap_delta_v_setting from the first measurement. In this test the capacitors are discharged by a known voltage with a known current and the time is proportional to capacitance.

Since the capacitors are charged by 1.25 times the change in voltage during the capacitance test, there is an "extra" 25 percent of the measurement time. Some of this time can be used to allow the capacitors to settle into a constant rate of voltage decrease. A starting point would be to use 15 percent of the expected discharge time as cap_i_on_settling. In the equation below, C should be the minimum expected stack capacitance due to aging and tolerance and Δv is change in voltage.

$$t_{DISCHARGE} = \frac{\Delta v \bullet C \bullet R_{TST}}{1.2V}$$

Combining the above equation, the equation for switcher frequency and cap_i_on_settling LSB weight results in:

$$cap\_i\_on\_settling = \frac{\Delta v \bullet C \bullet 6.5 \bullet 10^6 \bullet R_{TST}}{R_t}$$

The above equation is only a starting point. Adequate settling can be confirmed by triggering an oscilloscope on the rising edge of ITST (or alternately on SMBALERT using the mon_esr_done alarm). Observe the response of the discharging capacitors. They should have clearly settled into a linear discharge by the time specified in cap_i_on_settling after the trigger. If they have not settled in time, cap_i_on_settling needs to be increased. cap_i_on_settling cannot be increased beyond 25 percent of the expected minimum measurement time. If 25 percent of the expected measurement time is inadequate to settle, the expected measurement time may be increased by increasing Δv via cap_delta_v_setting.

PCB Layout Considerations

When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the IC. Check the following in your layout:

1. The VCC2P5 bypass capacitor must return to SGND or the ground plane. If returning to the ground plane keep away from the switcher's high di/dt loop.
2. Referring to Figure 16, keep MN1, MN2 and C_{OUT} close together. The high di/dt loop formed by the MOSFETs, Schottky diodes and the V_{OUT} capacitance should have short, wide traces to minimize high frequency noise and voltage stress from inductive ringing. Surface mount components are preferred to reduce parasitic inductances from component leads. Connect the drain of the top MOSFET directly to the positive terminal of C_{OUT}. Connect the source of the bottom MOSFET directly to the negative terminal of C_{OUT}. This capacitor provides the AC current to the MOSFETs.

APPLICATIONS INFORMATION

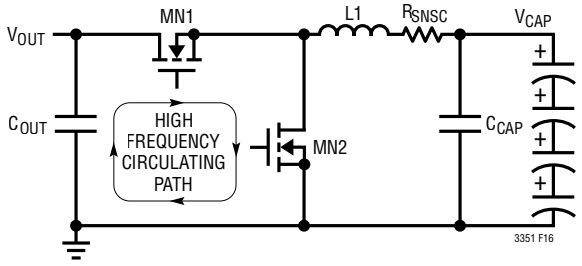


Figure 16.

3. Ground is referenced to the negative terminal of the V_{CAP} decoupling capacitor in step-down mode and to the negative terminal of the V_{OUT} decoupling capacitor in step-up mode. The combined IC SGND pin/PGND paddle and the ground returns of C_{INTVCC} and C_{DRVCC} must return to the combined negative terminal of C_{OUT} and C_{CAP}.

4. Effective grounding techniques are critical for successful DC/DC converter layouts. Orient power components such that switching current paths in the ground plane do not cross through the SGND pin and exposed pad on the backside of the LTC3351. Switching path currents can be controlled by orienting the MOSFET switches, the inductor, and V_{OUT} and V_{CAP} decoupling capacitors in close proximity to each other.

   It is important to keep SGND and the components connected to SGND away from interference due to switching currents. To do this, an island of SGND is formed on top metal. This SGND island should only connect to PGND on top metal under the LTC3351, between the SGND pin and the exposed pad of the LTC3351. This should be the only connection between SGND and PGND. This area of top metal is where the LTC3351's small signal components such as R_T, V_C, feedback dividers and VCC2P5 bypass capacitor should be connected. Power components and all other bypass capacitors should not connect to SGND.

5. Locate V_{CAP} and V_{OUT} dividers near the LTC3351 and away from switching components. Kelvin the top of resistor dividers to the positive terminals of C_{CAP} and C_{OUT}, respectively. The bottom of the resistive dividers should return directly to the SGND pin. The feedback resistor connections should not be run along the high current feeds from the C_{OUT} capacitor.

6. Route I_{CAP} and V_{CAP} sense lines together, keep them short. Apply this rule to ISNSP_HS, ISNSP_CHG and ISNSM as well. Filter components should be placed near the part and not near the sense resistors. Ensure accurate current sensing with Kelvin connections at the sense resistors. See Figure 17.

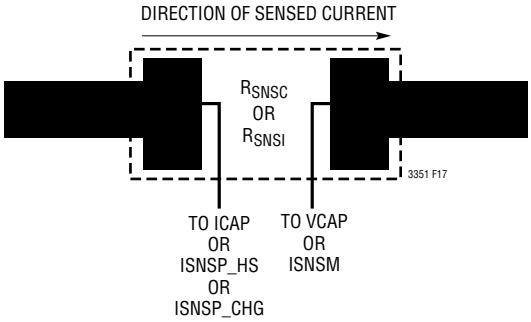


Figure 17.

7. Locate the DRV_{CC} and BST decoupling capacitors in close proximity to the LTC3351. These capacitors carry the MOSFET drivers' high peak currents. An additional 0.1µF ceramic capacitor placed immediately next to the DRV_{CC} pin can help improve noise performance substantially.

8. Locate the small-signal components away from high frequency switching nodes (BST, SW, TG, and BG). All of these nodes have very large and fast moving signals and should be kept on the output side of the LTC3351.

9. The output ideal diode senses the voltage between V_{OUT} and V_{CAP}. V_{CAP} is used for Kelvin sensing the charge current. Place the output ideal diode MOSFET near the charge current sense resistor, R_{SNSC}, with a short, wide trace to minimize resistance between the source of the ideal diode MOSFET and R_{SNSC}.

10. The OUTFET pin for the external ideal diode controller has extremely limited drive current. Care must be taken to minimize leakage to adjacent PC board traces. 100nA of leakage from this pin will introduce an additional ideal diode offset of approximately 10mV.

REGISTER MAP

Symbol Name	Command Code	Access	Bit Range	Default	Description
ctl_reg	0	R/W	[10:0]	0	Control Register: Several independent control bits are grouped into this register.
ctl_start_cap_esr_meas			[0]	0	Begin a capacitance and ESR measurement when possible; this bit clears itself once a measurement cycle begins or becomes pending. Enum: start_measurement = 1
ctl_gpi_buffer_en			[1]	0	A one in this bit location enables the input buffer on the GPI pin. With a zero in this location the GPI pin is measured without the buffer.
ctl_stop_cap_esr_meas			[2]	0	Stops an active capacitance/ESR measurement; this bit clears itself once a measurement cycle has been stopped. Enum: stop_measurement = 1
ctl_cap_scale			[3]	0	Increases capacitor measurement resolution 100 times, this is used when measuring smaller capacitors. Enums: large_cap = 0, small_cap = 1
ctl_disable_shunt			[4]	0	Disables the shunt feature.
ctl_hotswap_disable			[5]	0	Disables the HotSwap controller. The gate of the hotswap FET is forced low, disconnecting VIN and VOUT and forcing the switcher into backup mode. This can be used to simulate a power failure for testing.
ctl_force_boost_off			[6]	0	This bit disables the boost.
ctl_force_charger_off			[7]	0	This bit disables the charger.
ctl_force_itst_on			[8]	0	This bit forces the ITST current on. This can be used to discharge the capacitor stack or manually measure capacitance. Note that this only enables the test current, it does not disable the charger. Set ctl_force_charger_off to disable the charger.
ctl_disable_balancer			[10]	0	Disables the balancer.
alarm_mask_reg	1	R/W	[15:0]	0	Mask Alarms Register: Writing a one to any bit in this register enables a rising edge of its respective bit in alarm_reg to trigger an SMBALERT.
mask_alarm_gpi_uv			[0]	0	GPI Under Voltage alarm mask
mask_alarm_gpi_ov			[1]	0	GPI Over Voltage alarm mask
mask_alarm_vin_uv			[2]	0	VIN Under Voltage alarm mask
mask_alarm_vin_ov			[3]	0	VIN Over Voltage alarm mask
mask_alarm_vcap_uv			[4]	0	VCAP Under Voltage alarm mask
mask_alarm_vcap_ov			[5]	0	VCAP Over Voltage alarm mask
mask_alarm_vout_uv			[6]	0	VOUT Under Voltage alarm mask
mask_alarm_vout_ov			[7]	0	VOUT Over Voltage alarm mask
mask_alarm_dtemp_cold			[8]	0	Die temperature cold alarm mask
mask_alarm_dtemp_hot			[9]	0	Die temperature hot alarm mask
mask_alarm_ichg_uc			[10]	0	Charge undercurrent alarm mask
mask_alarm_iin_oc			[11]	0	Input overcurrent alarm mask
mask_alarm_cap_uv			[12]	0	Capacitor Under Voltage alarm mask
mask_alarm_cap_ov			[13]	0	Capacitor Over Voltage alarm mask
mask_alarm_cap_lo			[14]	0	Capacitance low alarm mask
mask_alarm_esr_hi			[15]	0	ESR high alarm mask

REGISTER MAP

Symbol Name	Command Code	Access	Bit Range	Default	Description
monitor_status_ mask_reg	2	R/W	[14:0]	0	Mask Monitor Status Register: Writing a one to any bit in this register enables a rising edge of its respective bit in monitor_status_reg to trigger an SMBALERT.
mask_mon_meas_ active			[0]	0	Set the SMBALERT when there is a rising edge on mon_meas_active
mask_mon_capesr_ pending			[2]	0	Set the SMBALERT when there is a rising edge on mon_capesr_pending
mask_mon_cap_done			[3]	0	Set the SMBALERT when there is a rising edge on mon_cap_done
mask_mon_esr_done			[4]	0	Set the SMBALERT when there is a rising edge on mon_esr_done
mask_mon_meas_ failed			[5]	0	Set the SMBALERT when there is a rising edge on mon_meas_failed
mask_mon_disable_ charger			[7]	0	Set the SMBALERT when there is a rising edge on mon_disable_charger
mask_mon_cap_ meas_active			[8]	0	Set the SMBALERT when there is a rising edge on mon_cap_meas_active
mask_mon_esr_meas_ active			[9]	0	Set the SMBALERT when there is a rising edge on mon_esr_meas_active
mask_mon_power_ failed			[10]	0	Set the SMBALERT when there is a rising edge on mon_power_failed
mask_mon_power_ returned			[11]	0	Set the SMBALERT when there is a rising edge on mon_power_returned
mask_mon_balancing			[12]	0	Set the SMBALERT when there is a rising edge on mon_balancing
mask_mon_shunting			[13]	0	Set the SMBALERT when there is a rising edge on mon_shunting
mask_mon_cap_ precharge			[14]	0	Set the SMBALERT when there is a rising edge on mon_cap_precharge
vcapfb_dac	3	R/W	[3:0]	10	VCAP Regulation Reference: This register is used to program the capacitor voltage feedback loop's reference voltage. Only bits 3:0 are active. VCAPFB_DAC = 37.5mV * vcapfb_dac + 637.5mV
vshunt	5	R/W	[15:0]	14744	Shunt Voltage Register: This register programs the shunt voltage for each capacitor in the stack. When set below 3.6V, the charger will limit current and the active shunts will shunt current to prevent this voltage from being exceeded. As a capacitor voltage nears this level, the charge current will be reduced. Current will be shunted when the capacitor voltage is within 25mV of vshunt. Vshunt should be programmed at least 50mV higher than the intended final balanced individual capacitor voltage. When programmed above 3.6V no current will be shunted, however the charge current will be reduced as described. 182.8µV per LSB.
adc_vin_ch_en_reg	6	R/W	[11:1]	3842	
adc_vin_ichg_en			[1]	1	Enables ADC measurement of charge current while in charging mode.
adc_vin_dtemp_en			[2]	0	Enables ADC measurement of die temperature while in charging mode.
adc_vin_gpi_en			[3]	0	Enables ADC measurement of GPI (general purpose input) while in charging mode.
adc_vin_iin_en			[4]	0	Enables ADC measurement of input current while in charging mode.
adc_vin_vout_en			[5]	0	Enables ADC measurement of vout while in charging mode.
adc_vin_vcap_en			[6]	0	Enables ADC measurement of vcap while in charging mode.
adc_vin_vin_en			[7]	0	Enables ADC measurement of vin while in charging mode.
adc_vin_vcap1_en			[8]	1	Enables ADC measurement of vcap1 while in charging mode. This bit must be set for capacitance and ESR measurement.

REGISTER MAP

Symbol Name	Command Code	Access	Bit Range	Default	Description
adc_vin_vcap2_en			[9]	1	Enables ADC measurement of vcap2 while in charging mode. This bit must be set for capacitance and ESR measurement if there are two or more capacitors in the stack.
adc_vin_vcap3_en			[10]	1	Enables ADC measurement of vcap3 while in charging mode. This bit must be set for capacitance and ESR measurement if there are three or more capacitors in the stack
adc_vin_vcap4_en			[11]	1	Enables ADC measurement of vcap4 while in charging mode. This bit must be set for capacitance and ESR measurement if there are four capacitors in the stack
adc_backup_ch_en_reg	7	R/W	[11:1]	0	
adc_backup_ichg_en			[1]	0	Enables ADC measurement of charge current while in backup mode.
adc_backup_dtemp_en			[2]	0	Enables ADC measurement of die temperature while in backup mode.
adc_backup_gpi_en			[3]	0	Enables ADC measurement of GPI (general purpose input) while in backup mode.
adc_backup_iin_en			[4]	0	Enables ADC measurement of input current while in backup mode.
adc_backup_vout_en			[5]	0	Enables ADC measurement of vout while in backup mode.
adc_backup_vcap_en			[6]	0	Enables ADC measurement of vcap while in backup mode.
adc_backup_vin_en			[7]	0	Enables ADC measurement of vin while in backup mode.
adc_backup_vcap1_en			[8]	0	Enables ADC measurement of vcap1 while in backup mode.
adc_backup_vcap2_en			[9]	0	Enables ADC measurement of vcap2 while in backup mode.
adc_backup_vcap3_en			[10]	0	Enables ADC measurement of vcap3 while in backup mode.
adc_backup_vcap4_en			[11]	0	Enables ADC measurement of vcap4 while in backup mode.
adc_wait_vin	8	R/W	[15:0]	100	Sets the wait time between ADC measurement groups while in charging mode. The LSB of this register has a weight of 400uS. The ADC measures all enabled channels then waits this time before measuring all channels again. The ADC data is used for balancing and shunting, increasing this time reduces the shunt and balancer update rate and is not typically recommended if shunting or balancing is enabled. If shunting or measuring capacitance/ESR this time may be ignored by the ADC. 400uS per LSB
adc_wait_backup	9	R/W	[15:0]	100	Sets the wait time between ADC measurement groups while in backup mode. The LSB of this register has a weight of 400uS. The ADC measures all enabled channels then waits this time before measuring all channels again. 400uS per LSB
gpi_uv_lvl	10	R/W	[15:0]	0	General Purpose Input Under Voltage Level: This is an alarm threshold for the GPI pin. If enabled, the GPI pin voltage falling below this level will trigger an alarm and an SMBALERT. 182.8µV per LSB
gpi_ov_lvl	11	R/W	[15:0]	0	General Purpose Input Over Voltage Level: This is an alarm threshold for the GPI pin. If enabled, the GPI pin voltage rising above this level will trigger an alarm and an SMBALERT. 182.8µV per LSB
vin_uv_lvl	12	R/W	[15:0]	0	VIN Under Voltage Level: This is an alarm threshold for the input voltage. If enabled, the input pin voltage falling below this level will trigger an alarm and an SMBALERT. 2.19mV per LSB
vin_ov_lvl	13	R/W	[15:0]	0	VIN Over Voltage Level: This is an alarm threshold for the input voltage. If enabled, the input pin voltage rising above this level will trigger an alarm and an SMBALERT. 2.19mV per LSB
vcap_uv_lvl	14	R/W	[15:0]	0	VCAP Under Voltage Level: This is an alarm threshold for the capacitor stack voltage. If enabled, the VCAP pin voltage falling below this level will trigger an alarm and an SMBALERT. 1.46mV per LSB
vcap_ov_lvl	15	R/W	[15:0]	0	VCAP Over Voltage Level: This is an alarm threshold for the capacitor stack voltage. If enabled, the VCAP pin voltage rising above this level will trigger an alarm and an SMBALERT. 1.46mV per LSB

REGISTER MAP

Symbol Name	Command Code	Access	Bit Range	Default	Description
vout_uv_lvl	16	R/W	[15:0]	0	VOUT Under Voltage Level: This is an alarm threshold for the output voltage. If enabled, the VOUT pin voltage falling below this level will trigger an alarm and an SMBALERT. 2.19mV per LSB
vout_ov_lvl	17	R/W	[15:0]	0	VOUT Over Voltage Level: This is an alarm threshold for the output voltage. If enabled, the VOUT pin voltage rising above this level will trigger an alarm and an SMBALERT. 2.19mV per LSB
dtemp_cold_lvl	18	R/W	[15:0]	0	Die Temperature Cold Level: This is an alarm threshold for the die temperature. If enabled, the die temperature falling below this level will trigger an alarm and an SMBALERT. Temperature = 0.0295C per LSB - 274C
dtemp_hot_lvl	19	R/W	[15:0]	0	Die Temperature Hot Level: This is an alarm threshold for the die temperature. If enabled, the die temperature rising above this level will trigger an alarm and an SMBALERT. Temperature = 0.0295C per LSB - 274C
ichg_uc_lvl	20	R/W	[15:0]	0	Charge Undercurrent Level: This is an alarm threshold for the charge current. If enabled, the charge current falling below this level will trigger an alarm and an SMBALERT. 1.955µV/Rsnsc per LSB
iin_oc_lvl	21	R/W	[15:0]	0	Input Overcurrent Level: This is an alarm threshold for the input current. If enabled, the input current rising above this level will trigger an alarm and an SMBALERT. 1.955µV/Rsnsi per LSB
cap_uv_lvl	22	R/W	[15:0]	0	Capacitor Under Voltage Level: This is an alarm threshold for each individual capacitor voltage in the stack. If enabled, any capacitor voltage falling below this level will trigger an alarm and an SMBALERT. 182.8µV per LSB.
cap_ov_lvl	23	R/W	[15:0]	0	Capacitor Over Voltage Level: This is an alarm threshold for each individual capacitor in the stack. If enabled, any capacitor voltage rising above this level will trigger an alarm and an SMBALERT. 182.8µV per LSB
cap_lo_lvl	24	R/W	[15:0]	0	Capacitance Low Level: This is an alarm threshold for the measured stack capacitance. If the measured stack capacitance is less than this level it will trigger an alarm and an SMBALERT, if enabled. When ctl_cap_scale is set to 1, capacitance is 3.36µF * RT/RTST per LSB. When ctl_cap_scale is set to 0 it is 336µF * RT/RTST per LSB.
esr_hi_lvl	25	R/W	[15:0]	0	ESR High Level: This is an alarm threshold for the measured stack ESR. If enabled, a measurement of stack ESR exceeding this level will trigger an alarm and an SMBALERT. Rsnsc/64 per LSB.
esr_i_on_settling	26	R/W	[15:0]	2	Time to allow the charging current to settle before measuring the charge voltage and current for ESR. Each LSB is 1024 switcher periods.
esr_i_off_settling	27	R/W	[15:0]	8	Time to wait after turning the charge current off before measuring the charge voltage and current for ESR. Each LSB is 1024 switcher periods.
esr_i_override	28	R/W	[15:0]	0	This value overrides the LTC3351's adaptive test current selection for the ESR test. If this register is non-zero, the lower 8 bits will be used as an 8 bit DAC value to set the charge current during the ESR test. Typically this register will not need to be set. ITEST = 32mV * (esr_i_override[7:0] + 1) / 256 / Rsnsc
cap_i_on_settling	29	R/W	[15:0]	8	Time to wait after turning the test current on before measuring the first voltage of the capacitance measurement. Each LSB is 1024 switcher periods.
cap_delta_v_setting	30	R/W	[15:0]	550	The target delta V for the capacitance test. The scale is 182.8µV per LSB. The default is approximately 100mV.

REGISTER MAP

Symbol Name	Command Code	Access	Bit Range	Default	Description
min_boost_cap_ voltage	31	R/W	[15:0]	0	If this register is non-zero, it sets the minimum capacitor voltage the boost will operate at. If any capacitor voltage falls below this value in boost mode the boost will be forced off, the boost will not turn back on even if the capacitor voltage rises above this voltage. Only after input power returns will the boost be re-enabled. This prevents the boost from cycling on and off many times once the capacitors' voltage has discharged to the point it can no longer support the system load through the boost. To use this feature vcap[1:num_caps+1] measurements must be enabled in backup mode, see adc_backup_ch_en_reg. Also the capacitor voltages are only measured as often as set by adc_wait_backup.
min_vout_hs_disable	32	R/W	[15:0]	0	If this register is non-zero, it sets the minimum voltage VOUT is allowed to reach while the HotSwap is disabled. If the voltage falls below this level the ctl_hotswap_disable bit will be cleared, re-enabling the HotSwap controller. To use this feature the VOUT measurement must be enabled in boost mode, see adc_backup_ch_en_reg. Also the VOUT voltage is only measured as often as set by adc_wait_backup.
alarm_reg	35	R/W	[15:0]	0	Alarms Register: A one in any bit in the register indicates its respective alarm has triggered. All bits are active high. Alarms are cleared by clearing (writing 0) the appropriate bit in this register. Setting (writing 1) bits has no effect. For example to clear the alarm_gpi_uv alarm, write 0xFFFD.
alarm_gpi_uv			[0]	0	GPI Under Voltage alarm
alarm_gpi_ov			[1]	0	GPI Over Voltage alarm
alarm_vin_uv			[2]	0	VIN Under Voltage alarm
alarm_vin_ov			[3]	0	VIN Over Voltage alarm
alarm_vcap_uv			[4]	0	VCAP Under Voltage alarm
alarm_vcap_ov			[5]	0	VCAP Over Voltage alarm
alarm_vout_uv			[6]	0	VOUT Under Voltage alarm
alarm_vout_ov			[7]	0	VOUT Over Voltage alarm
alarm_dtemp_cold			[8]	0	Die temperature cold alarm
alarm_dtemp_hot			[9]	0	Die temperature hot alarm
alarm_ichg_uc			[10]	0	Charge undercurrent alarm
alarm_iin_oc			[11]	0	Input overcurrent alarm
alarm_cap_uv			[12]	0	Capacitor Under Voltage alarm
alarm_cap_ov			[13]	0	Capacitor Over Voltage alarm
alarm_cap_lo			[14]	0	Capacitance low alarm
alarm_esr_hi			[15]	0	ESR high alarm
monitor_status_reg	36	R	[15:0]	N/A	Monitor Status: This register provides real time status information about the state of the monitoring system. Each bit is active high.
mon_meas_active			[0]	N/A	Capacitance/ESR measurement is active. This bit becomes one at the begining of a capacitance/ESR measurement and remains 1 after the measurement has completed until the capacitors have been discharged back to their regualtion voltage.
mon_capesr_scheduled			[1]	N/A	Indicates that the LTC3351 is waiting programmed time to begin a capacitance/ ESR measurement
mon_capesr_pending			[2]	N/A	Indicates that the LTC3351 is waiting for satisfactory conditions to begin a capacitance/ESR measurement
mon_cap_done			[3]	N/A	Indicates that the capacitance measurement has completed
mon_esr_done			[4]	N/A	Indicates that the ESR Measurement has completed

REGISTER MAP

Symbol Name	Command Code	Access	Bit Range	Default	Description
mon_meas_failed			[5]	N/A	Indicates the last attempted capacitance and ESR measurement was unable to complete
mon_boost_shutdown			[6]	N/A	This bit is set in boost mode when any capacitor falls below min_boost_cap_voltage_reg. It is cleared when power returns.
mon_disable_charger			[7]	N/A	Indicates the capacitance and ESR measurement system has temporarily disabled the charger.
mon_cap_meas_active			[8]	N/A	Indicates the capacitance and ESR measurement system is measuring capacitance.
mon_esr_meas_active			[9]	N/A	Indicates the capacitance and ESR measurement system is measuring ESR.
mon_power_failed			[10]	N/A	This bit is set when VIN is outside the UV/OV range or the HotSwap controller is disabled by setting the ctl_hotswap_disable. It is cleared only when mon_power_returned is set.
mon_power_returned			[11]	N/A	This bit is set when the output is powered by the input and the charger is able to charge. It is cleared only when mon_power_failed is set.
mon_balancing			[12]	N/A	Indicates the LTC3351 is balancing the capacitor voltage.
mon_shunting			[13]	N/A	Indicates a capacitor voltage is approaching vshunt and a shunt is turned on.
mon_cap_precharge			[14]	N/A	Indicates the capacitor stack is being precharged for a capacitance measurement.
mon_reset			[15]	N/A	This bit is set during a power on reset. It is cleared on any I2C/SMBus write. It can be used to determine if the chip has reset during a power loss followed by a power return.
meas_gpi	37	R	[15:0]	N/A	Measurement of GPI pin voltage. 182.8µV per LSB
meas_vin	38	R	[15:0]	N/A	Measured Input Voltage. 2.19mV per LSB
meas_vcap	39	R	[15:0]	N/A	Measured Capacitor Stack Voltage. 1.46mV per LSB.
meas_vout	40	R	[15:0]	N/A	Measured Output Voltage. 2.19mV per LSB.
meas_dtemp	41	R	[15:0]	N/A	Measured die temperature. Temperature = 0.0295C per LSB - 274C
meas_ichg	42	R	[15:0]	N/A	Measured Charge Current. 1.955µV/Rsnsc per LSB
meas_iin	43	R	[15:0]	N/A	Measured Input Current. 1.955µV/Rsnsi per LSB
lo_vcap	44	R	[15:0]	N/A	The lowest measured capacitor voltage from the last measurement set.
hi_vcap	45	R	[15:0]	N/A	The highest measured capacitor voltage from the last measurement set.
meas_cap	46	R	[15:0]	N/A	Measured capacitor stack capacitance value. When ctl_cap_scale is set to 1, capacitance is 3.36µF * RT/RTST per LSB. When ctl_cap_scale is set to 0 it is 336µF * RT/RTST per LSB.
meas_esr	47	R	[15:0]	N/A	Measured capacitor stack equivalent series resistance (ESR) value. Rsnsc/64 per LSB
meas_vcap1	48	R	[15:0]	N/A	Measured voltage between the CAP1 and CAPRTN pins. 182.8µV per LSB
meas_vcap2	49	R	[15:0]	N/A	Measured voltage between the CAP2 and CAP1 pins. 182.8µV per LSB
meas_vcap3	50	R	[15:0]	N/A	Measured voltage between the CAP3 and CAP2 pins. 182.8µV per LSB
meas_vcap4	51	R	[15:0]	N/A	Measured voltage between the CAP4 and CAP3 pins. 182.8µV per LSB. When the ITST current is on, either due to ctl_force_itst_on or during a capacitance measurement, this voltage measurement will temporarily be low due to the ITST current flowing in the shunt resistor.
cap_m0_vc1	52	R	[15:0]	N/A	The voltage change on cap1 due to the capacitance measurement. The relative voltage change on each capacitor during the capacitance measurement and the total capacitance can be used to calculate the capacitance of each individual capacitor.

REGISTER MAP

Symbol Name	Command Code	Access	Bit Range	Default	Description
cap_m0_vc2	53	R	[15:0]	N/A	The voltage change on cap2 due to the capacitance measurement. The relative voltage change on each capacitor during the capacitance measurement and the total capacitance can be used to calculate the capacitance of each individual capacitor.
cap_m0_vc3	54	R	[15:0]	N/A	The voltage change on cap3 due to the capacitance measurement. The relative voltage change on each capacitor during the capacitance measurement and the total capacitance can be used to calculate the capacitance of each individual capacitor.
cap_m0_vc4	55	R	[15:0]	N/A	The voltage change on cap4 due to the capacitance measurement. The relative voltage change on each capacitor during the capacitance measurement and the total capacitance can be used to calculate the capacitance of each individual capacitor.
esr_m0_vc1	56	R	[15:0]	N/A	A measurement of VCAP1 just before turning current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m0_vc2	57	R	[15:0]	N/A	A measurement of VCAP2 just before turning current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m0_vc3	58	R	[15:0]	N/A	A measurement of VCAP3 just before turning current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m0_vc4	59	R	[15:0]	N/A	A measurement of VCAP4 just before turning current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m1_vc1	60	R	[15:0]	N/A	The first VCAP1 voltage measurement with charge current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m1_vc2	61	R	[15:0]	N/A	The first VCAP2 voltage measurement with charge current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m1_vc3	62	R	[15:0]	N/A	The first VCAP3 voltage measurement with charge current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m1_vc4	63	R	[15:0]	N/A	The first VCAP4 voltage measurement with charge current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m1_i	64	R	[15:0]	N/A	The first charge current measurement with charge current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m2_vc1	65	R	[15:0]	N/A	The second VCAP1 voltage measurement with the charge current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m2_vc2	66	R	[15:0]	N/A	The second VCAP2 voltage measurement with the charge current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m2_vc3	67	R	[15:0]	N/A	The second VCAP3 voltage measurement with the charge current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m2_vc4	68	R	[15:0]	N/A	The second VCAP4 voltage measurement with the charge current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m2_i	69	R	[15:0]	N/A	The second charge current measurement with charge current on for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m3_vc1	70	R	[15:0]	N/A	The VCAP1 voltage measurement with charge current off for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m3_vc2	71	R	[15:0]	N/A	The VCAP2 voltage measurement with charge current off for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m3_vc3	72	R	[15:0]	N/A	The VCAP3 voltage measurement with charge current off for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m3_vc4	73	R	[15:0]	N/A	The VCAP4 voltage measurement with charge current off for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.
esr_m3_i	74	R	[15:0]	N/A	The charge current measurement with charge current off for the ESR measurement. This value is used by the LTC3351 in the calculation of meas_esr.

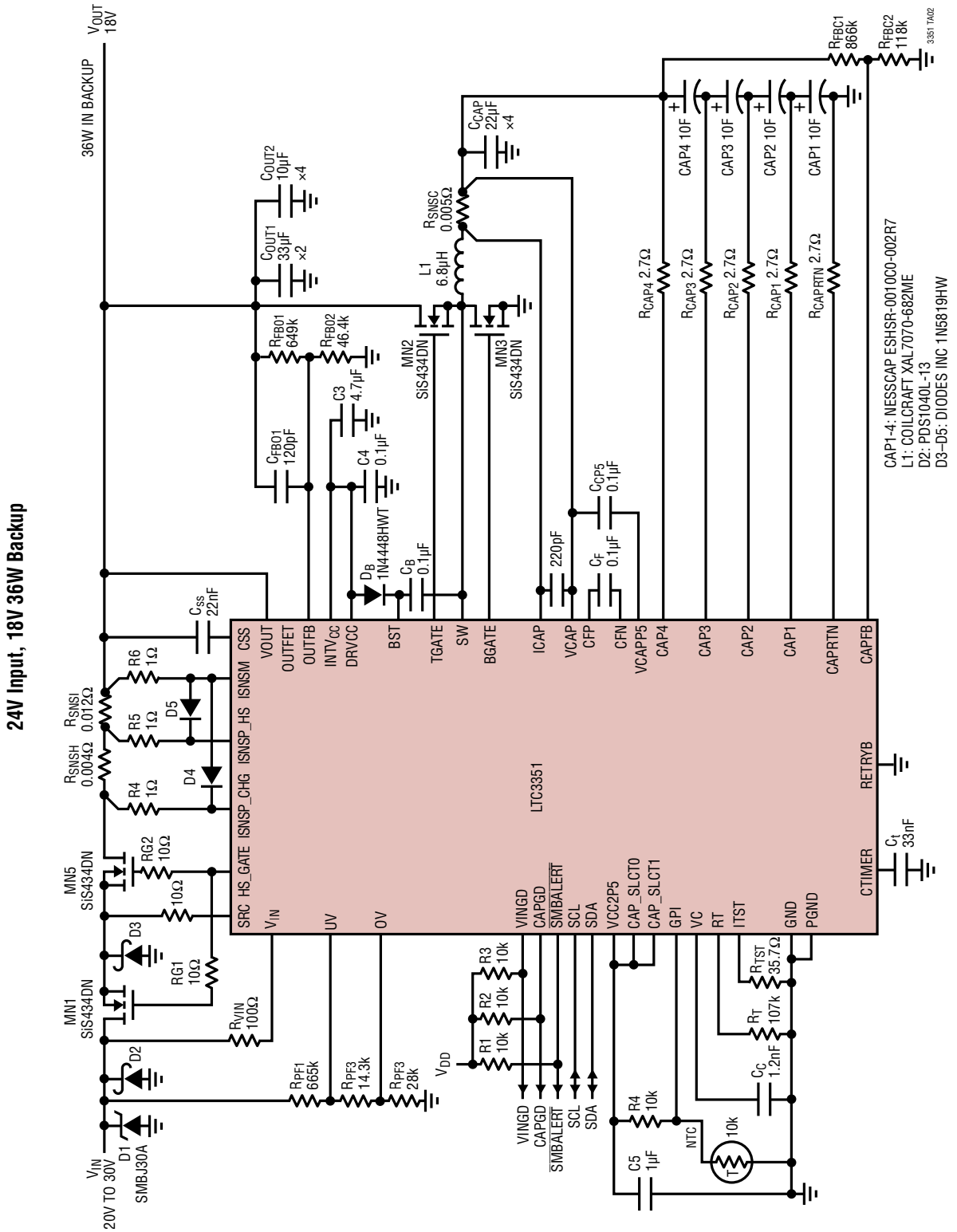
REGISTER MAP

Symbol Name	Command Code	Access	Bit Range	Default	Description
rev_code	80	R	[15:0]	6	The LTC3351 revision code.
next_esr_i	84	R	[7:0]	32	The 8 bit DAC setting for the charge current that the LTC3351 has calculated for the next ESR measurement based on the previous ESR measurement. The first ESR measurement will use a setting of 32. If esr_i_override is non-zero, this register will be calculated but esr_i_override will be used instead. If non-zero ITEST = 32mV * (next_esr_i[7:0] + 1) / 256 / Rsnsc
num_caps	237	R	[1:0]	0	Number of Capacitors. This register shows the state of the CAP_SLCT1, CAP_SLCT0 pins. The value read in this register is the number of capacitors programmed minus one.
sys_status	238	R	[11:0]	N/A	System Status Register: This register provides real time status information about the instantaneous state of the system. Each bit is active high.
stepdown_mode			[0]	N/A	The synchronous controller is in step-down mode (charging)
stepup_mode			[1]	N/A	The synchronous controller is in step-up mode (backup)
chrg_cv			[2]	N/A	The charger is in constant voltage mode
chrg_uvlo			[3]	N/A	The charger is in under-voltage lockout or has been disabled by ctl_force_charger_off.
chrg_input_ilim			[4]	N/A	The charger is in input current limit
cappg			[5]	N/A	The capacitor voltage is above power good threshold
boost_en			[7]	N/A	Indicates the boost is enabled
buck_en			[8]	N/A	Indicates the charger is enabled
chrg_ci			[9]	N/A	Indicates the charger is in constant current mode
vingd			[11]	N/A	Indicates the input voltage is inside the UV/OV range.

Revision: 149 Date: 2017-08-18 15:51:04 -0400 (Fri, 18 Aug 2017)

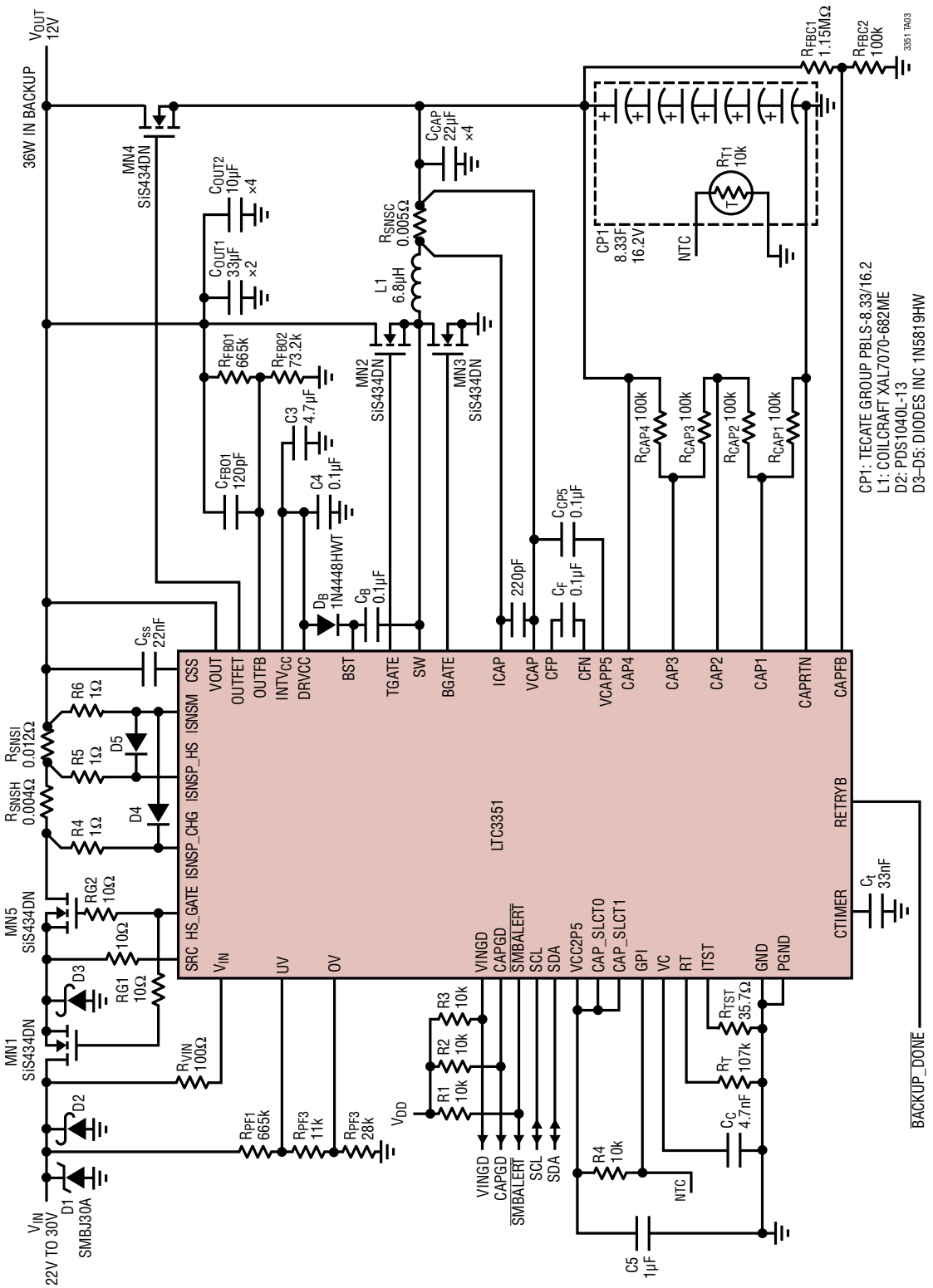
Note: All registers are 16 bits. Unused bits not shown above should be written as 0 and ignored when reading

TYPICAL APPLICATIONS



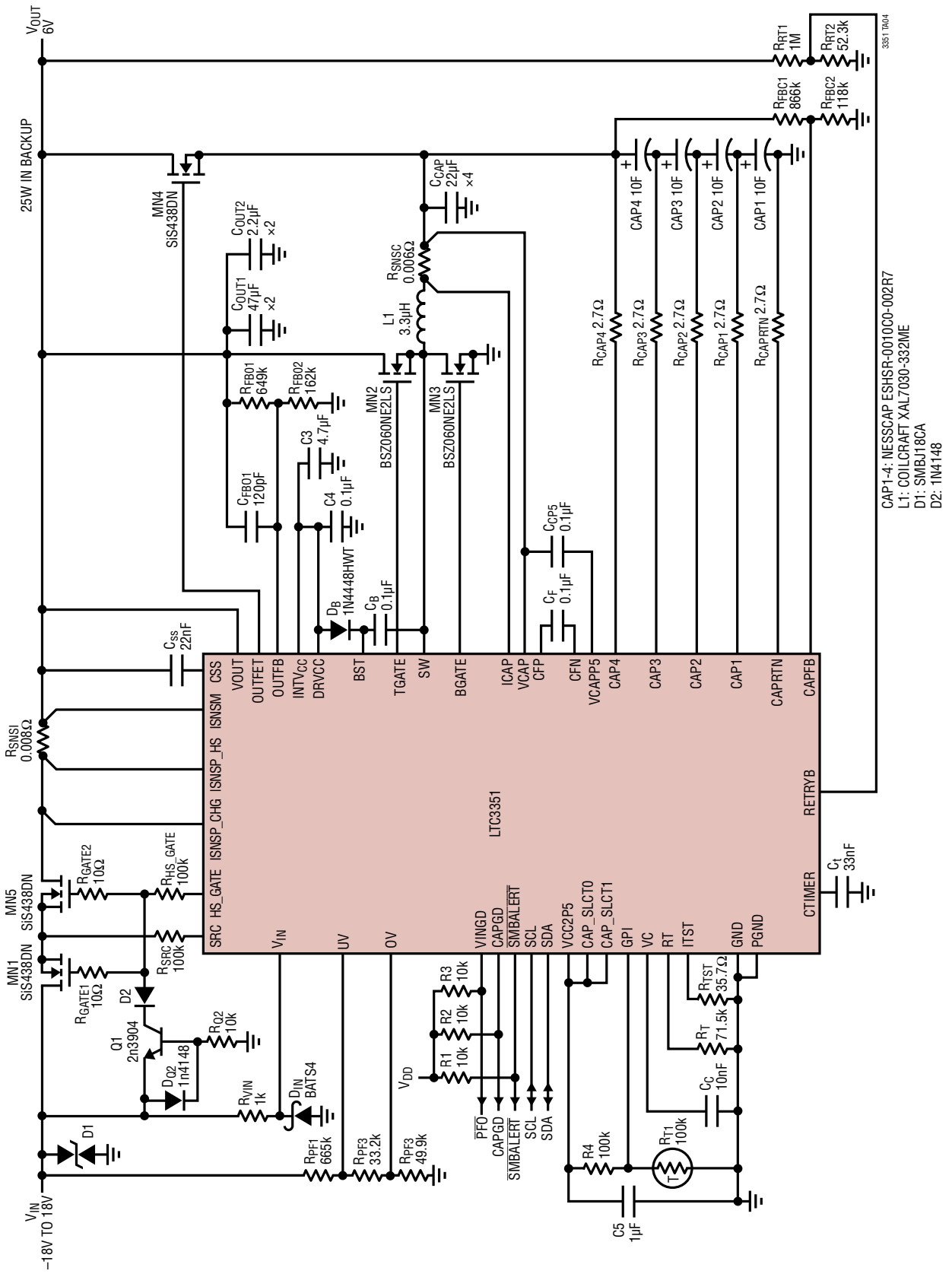
TYPICAL APPLICATIONS

24V Input, 12V 36W Backup, 6 Capacitor Stack



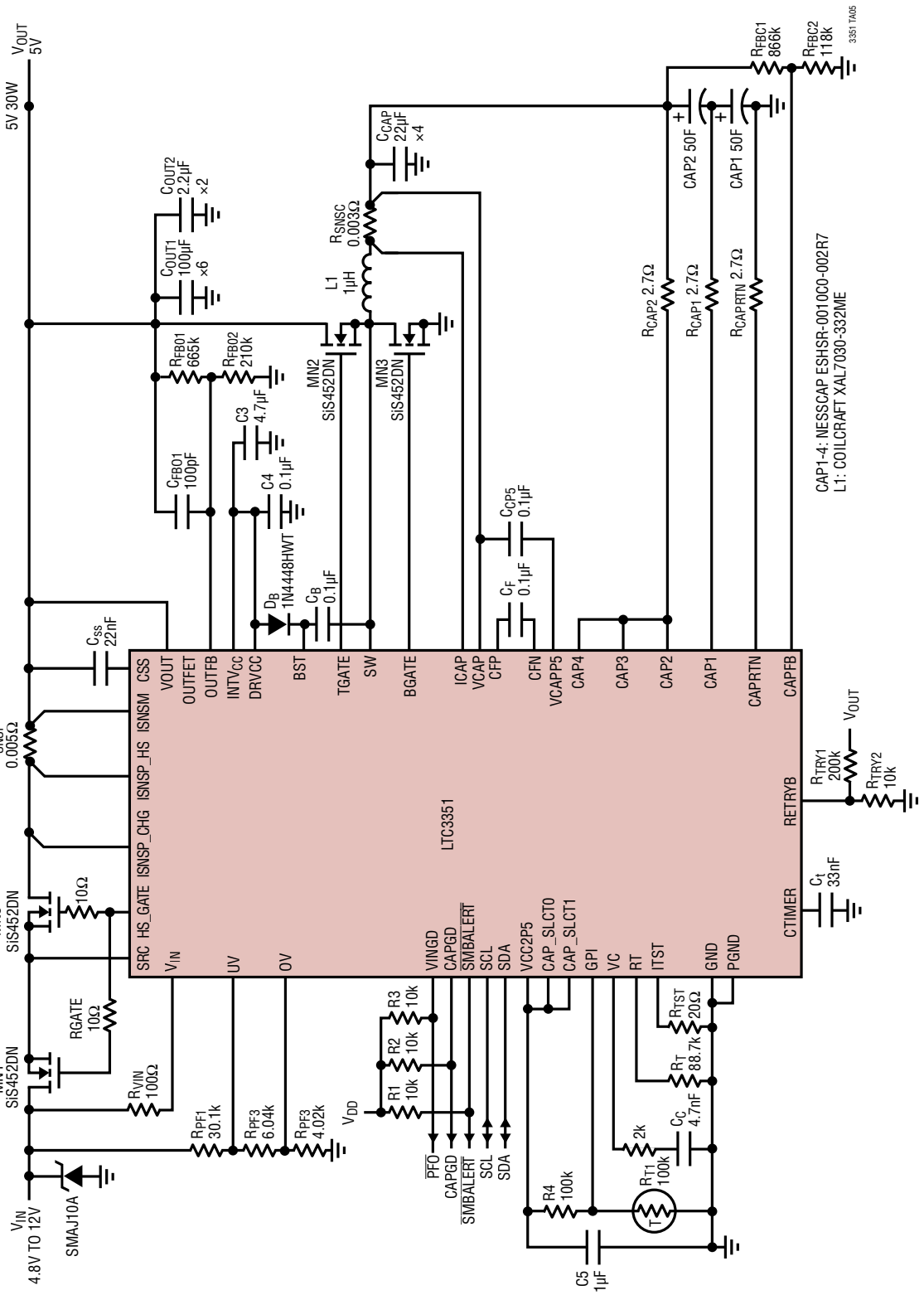
TYPICAL APPLICATIONS

12V Backup Controller with Reverse Input Protection



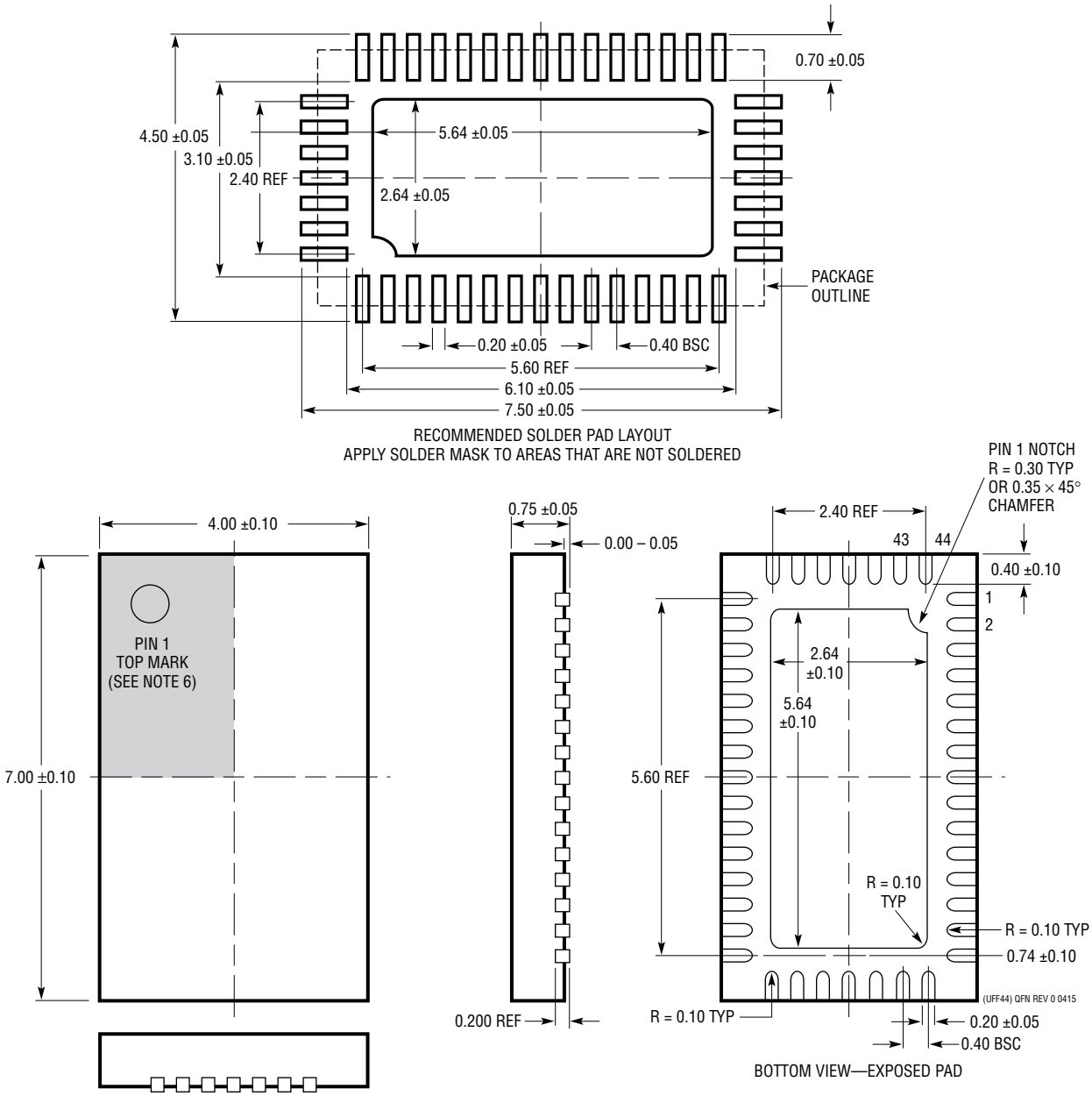
TYPICAL APPLICATIONS

4.8V to 12V 10A Supercap Charger with 5V 30W Backup Mode



PACKAGE DESCRIPTION

UFF Package
44-Lead Plastic QFN (4mm × 7mm)
(Reference LTC DWG # 05-08-1500 Rev Ø)



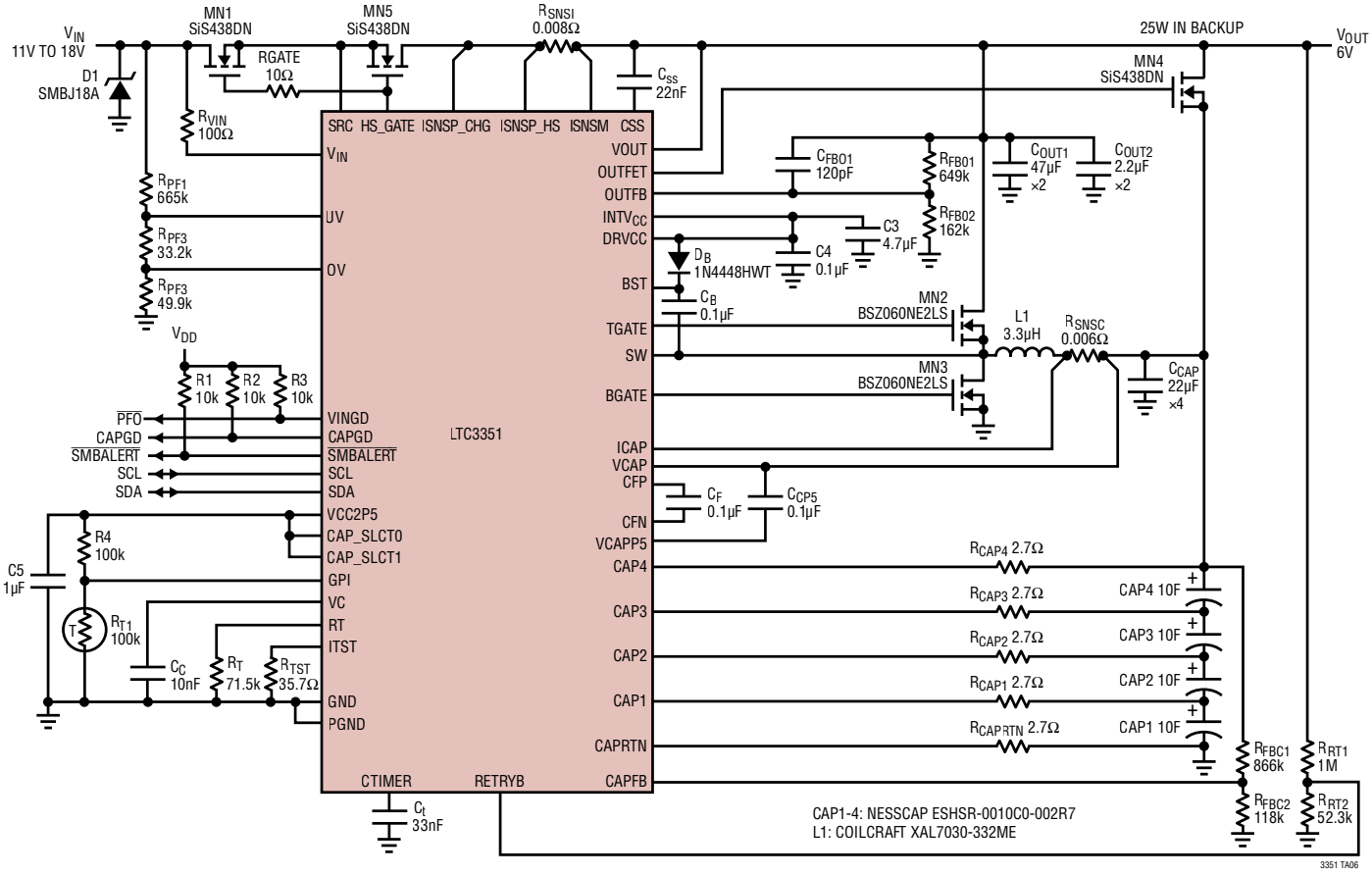
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/19	Split F_{SW} specification into room temperature and overtemperature and changed limits. Hot Swap Component Selection: Changed verbiage from “reduced” to “increased”.	3 26
B	04/21	Changed rev_code register from 5 to 6 in the Register Map table.	49

TYPICAL APPLICATION

12V PCLE Backup Controller



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Power Management		
LTC3350	Bidirectional Controller, Monitor and PowerPath for Supercapacitors	I_{CHARGE} = 10A+, V_{IN}: 4.5V to 35V, V_{OUT}: 4V to 35V
LTC3225	Boost Charge Pump Supercapacitor Charger	I_{CHARGE} = 0.15A, V_{IN}: 2.8V to 5.5V, V_{OUT}: 4.8V to 5.3V
LTC3226	Boost Charge Pump and PowerPath Manager for Supercapacitors	I_{CHARGE} = 0.33A, V_{IN}: 2.5V to 5.5V, V_{OUT}: 2.5V to 5.5V
LTC3625	Buck and Boost Supercapacitor Charger	I_{CHARGE} = 1A, V_{IN}: 2.7V to 5.5V, V_{OUT}: 4V to 5.3V
LTC3355	Buck Supercapacitor Charger and Boost Backup	I_{CHARGE} = 1A, V_{IN}: 3V to 20V, V_{OUT}: 2.7V to 5.5V
LTC3110	Bidirectional Buck-Boost and PowerPath Manager for Supercapacitors	I_{CHARGE} = 2A, V_{IN}: 0.1V to 5.5V, V_{OUT}: 1.8V to 5.5V
LTC3643	Bidirectional Boost Charger/Buck Backup, Electrolytic Capacitors	I_{CHARGE} = 2A, V_{IN}: 3V to 17V, V_{OUT}: Up to 40V
LTC4040	Buck Battery Charger and Boost Backup for Li Batteries	I_{CHARGE} = 2.5A, V_{IN}: 2.5V to 5.5V, V_{OUT}: 3.5V to 5V
LTC3128	Buck-Boost Supercapacitor Charger	I_{CHARGE} = 3A, V_{IN}: 1.7V to 5.5V, V_{OUT}: 1.8V to 5.5V
LTC4425	Linear/Ideal Diode Supercapacitor Charger	I_{CHARGE} = 3A, V_{IN}: 1.7V to 5.5V, V_{OUT}: 2.7V to 5.5V
LTC4110	Bidirectional Buck-Boost Flyback Controller	I_{CHARGE} = 3A, V_{IN}: 4.5V to 19V, V_{OUT}: 2.7V to 19V