Five-Channel, Low Dropout, 300 mA, Current Source Output, 12-/16-Bit SoftSpan DAC

FEATURES

- Per channel programmable output current ranges: 300 mA, 200 mA, 100 mA, 50 mA, 25 mA, 12.5 mA, 6.25 mA, and 3.125 mA
- Flexible 2.1 V to V_{CC} output supply voltages
- Flexible single- or dual-supply operation
- 0.6 V maximum dropout voltage guaranteed
- Separate voltage supply per output channel
- Internal switches to optional negative supply
- Full 12-bit and 16-bit resolution at all ranges
- Guaranteed operation −40°C to 125°C (H-grade)
- Precision internal reference or external reference
  - Internal V_{REF} temperature coefficient of 10 ppm/°C maximum (LFCSP) or 2.4 ppm/°C nominal (WLCSP)
- Analog multiplexer monitors voltages and currents
- A/B toggle via SPI or dedicated pin
- 1.71 V to V_{CC} digital input and output supply voltage
- 32-lead lead frame chip scale package (LFCSP)
- 36-ball wafer level chip scale package (WLCSP)

APPLICATIONS

- Tunable lasers
- Semiconductor optical amplifier biasing
- Resistive heaters
- Current mode biasing

GENERAL DESCRIPTION

The LTC2672 is a family of five-channel, 12-/16-bit current source, digital-to-analog converters (DACs) that provide five high compliance, current source outputs with guaranteed 0.6 V dropout at 200 mA. There are eight current ranges that are programmable per channel with full-scale outputs of up to 300 mA. The channels can be paralleled to allow either ultrafine adjustments of large currents or combined outputs of up to 1.5 A. A dedicated supply pin is provided for each output channel. Each channel can be operated from 2.1 V to V_{CC}, and internal switches allow any output to be pulled to the optional negative supply. The LTC2672 includes a precision integrated 1.25 V reference (10 ppm/°C maximum (LFCSP) or 2.4 ppm/°C nominal (WLCSP)), with the option to use an external reference. The serial peripheral interface (SPI)-compatible, 3-wire serial interface operates on logic levels as low as 1.71 V and at clock rates as high as 50 MHz.

Note that throughout this data sheet, multifunction pins, such as $\overline{CS}$/LD, are referred to by the entire pin name or by a single function of the pin.

FUNCTIONAL BLOCK DIAGRAM

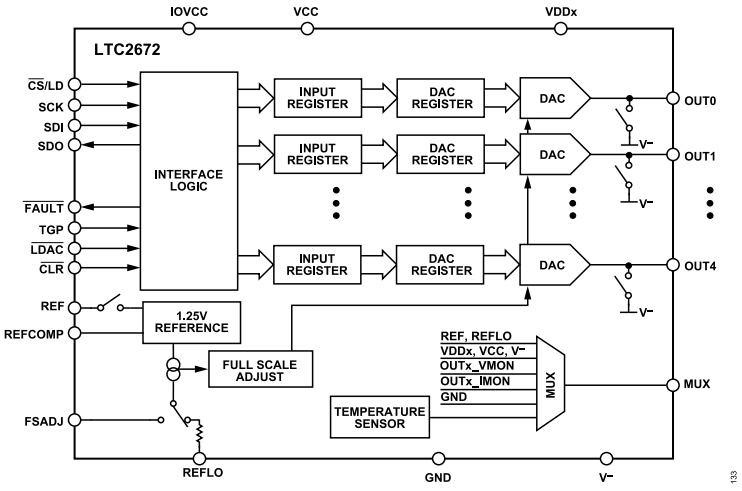


Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

10/2024—Rev. B to Rev. C

Added Figure 19; Renumbered Sequentially ... 14
Changes to Ordering Guide ... 27

1/2024—Rev. A to Rev. B

Added 36-Ball WLCSP (Universal) ... 1
Reorganized Layout (Universal) ... 1
Changes to Features Section ... 1
Changes to General Description Section ... 1
Changes to Figure 1 ... 1
Changes to Table 1 ... 4
Changes to Thermal Resistance Section and Table 5 ... 9
Added Electrostatic Discharge (ESD) Ratings Section and Table 6; Renumbered Sequentially ... 9
Change to Figure 5 Caption ... 10
Added Figure 6; Renumbered Sequentially ... 10
Changes to Table 7 ... 10
Changes to Toggle Operations Section ... 19
Changes to Figure 30 ... 20
Moved Figure 31 and Table 11 ... 21
Changed Fault Indicator Pin ($\overline{\text{FAULT}}$, Pin 30) Section to Fault Indicator Pin ($\overline{\text{FAULT}}$) Section ... 23
Changes to Safe Supply Ranges Section ... 24
Change to Reference Modes Section ... 25
Changes to Board Layout Section ... 25
Updated Outline Dimensions ... 26
Changes to Ordering Guide ... 27

4/2021—Rev. 0 to Rev. A

TABLE OF CONTENTS

12/2020—Revision 0: Initial Version

SPECIFICATIONS

All specifications apply over the full operating T_J range, unless otherwise noted. Typical values are at T_J = 25°C, V_{CC} = IO_{VCC} = 5 V, V^- = –3.3 V, V_{DDx} = 5 V, FSADJ = V_{CC}, and reference output voltage (V_{REF}) = 1.25 V external, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC PERFORMANCE, LTC2672-16						
Resolution			16			Bits
Monotonicity		All ranges[1]	16			Bits
Differential Nonlinearity	DNL	All ranges[1]	−1	+0.45	+1	LSB
Integral Nonlinearity	INL	All ranges[1]	−64	+12	+64	LSB
Current Offset Error	I_{OS}	All current ranges[1]	−0.4	+0.1	+0.4	%FSR
I_{OS} Temperature Coefficient		All current ranges		10		ppm/°C
Gain Error	GE[2]	300 mA and 200 mA output current ranges	−0.9	+0.3	+0.9	%FSR
		100 mA, 50 mA, and 25 mA output current ranges, LFCSP model	−1.2	+0.4	+1.2	%FSR
		100 mA, 50 mA, and 25 mA output current ranges, WLCSP model	−1.4	+0.4	+1.4	%FSR
		12.5 mA, 6.25 mA, and 3.125 mA output current ranges LFCSP model	−1.5	+0.7	+1.5	%FSR
		12.5 mA, 6.25 mA, and 3.125 mA output current ranges, WLCSP model	−2.0	+0.7	+2.0	%FSR
Gain Temperature Coefficient		FSADJ = V_{CC}		30		ppm/°C
Total Unadjusted Error	TUE [2]	300 mA and 200 mA output current ranges	−1.4	+0.4	+1.4	%FSR
		100 mA, 50 mA, and 25 mA output current ranges, LFCSP model	−1.7	+0.5	+1.7	%FSR
		100 mA, 50 mA, and 25 mA output current ranges, WLCSP model	−1.9	+0.5	+1.9	%FSR
		12.5 mA, 6.25 mA, and 3.125 mA output current ranges, LFCSP model	−2	+0.8	+2	%FSR
		12.5 mA, 6.25 mA, and 3.125 mA output current ranges, WLCSP model	−2.5	+0.8	+2.5	%FSR
Power Supply Rejection	PSR	Range = 100 mA, OUTx current (I_{OUTx}) = 50 mA				
		V_{CC} = 4.75 V to 5.25 V		0.5		LSB
		V_{DDx} = 2.85 V to 3.15 V		0.4		LSB
		V_{DDx} = 4.75 V to 5.25 V		0.7		LSB
		V^- = −3.25 V to −2.75 V		0.6		LSB
DC Crosstalk[3]		Result of a 200 mW change in dissipated power		0.1		%FSR
Dropout Voltage (V_{DDx} − V_{OUTx}[4])	$V_{DROPOUT}$	200 mA range, (V_{DDx} − V^-) = 4.75 V		0.45	0.6	V
		200 mA range, (V_{DDx} – V^-) = 2.85 V		0.5	0.65	V
		300 mA range, (V_{DDx} – V^-) = 4.75 V		0.75		V
		300 mA range, (V_{DDx} – V^-) = 2.85 V		0.85	1.15	V
Off Mode Output Leakage Current[5]		800 Ω load to GND	−1	+0.1	+1	µA
OUTx Switch to V^- Resistance	$R_{PULLDOWN}$	Span code = 1000b, sinking 80 mA		8	12	Ω
DC PERFORMANCE, LTC2672-12						
Resolution			12			Bits
Monotonicity		All ranges[1]	12			Bits
Differential Nonlinearity	DNL	All ranges[1]	−0.5	+0.03	+0.5	LSB
Integral Nonlinearity	INL	All ranges[1]	−4	+0.8	+4	LSB
Current Offset Error	I_{OS}	All current ranges[1]	−0.4	+0.1	+0.4	%FSR
I_{OS} Temperature Coefficient		All current ranges		10		ppm/°C
Gain Error	GE[2]	300 mA and 200 mA output current ranges	−0.9	+0.3	+0.9	%FSR
		100 mA, 50 mA, and 25 mA output current ranges	−1.2	+0.4	+1.2	%FSR

SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
		12.5 mA, 6.25 mA, and 3.125 mA output current ranges	−1.5	+0.7	+1.5	%FSR
Gain Temperature Coefficient		FSADJ = V_{CC}		30		ppm/°C
Total Unadjusted Error	TUE[2]	300 mA and 200 mA output current ranges	−1.4	+0.4	+1.4	%FSR
		100 mA, 50 mA, and 25 mA output current ranges	−1.7	+0.5	+1.7	%FSR
		12.5 mA, 6.25 mA, and 3.125 mA output current ranges	−2	+0.8	+2	%FSR
Power Supply Rejection	PSR	Range = 100 mA, I_{OUTx} = 50 mA				
		V_{CC} = 4.75 V to 5.25 V		0.04		LSB
		V_{DDx} = 2.85 V to 3.15 V		0.03		LSB
		V_{DDx} = 4.75 V to 5.25 V		0.05		LSB
		V^- = −3.25 V to −2.75 V		0.04		LSB
DC Crosstalk[3]		Result of a 200 mW change in dissipated power		0.1		%FSR
Dropout Voltage (V_{DDx} − V_{OUTx}[4])	$V_{DROPOUT}$	200 mA range; (V_{DDx} − V^-) = 4.75 V		0.45	0.6	V
		200 mA range; (V_{DDx} – V^-) = 2.85 V		0.5	0.65	V
		300 mA range; (V_{DDx} – V^-) = 4.75 V		0.75		V
		300 mA range; (V_{DDx} – V^-) = 2.85 V		0.85	1.15	V
Off Mode Output Leakage Current[5]		800 Ω load to GND	−1	+0.1	+1	µA
OUTx Switch to V^- Resistance	$R_{PULLDOWN}$	Span code = 1000b, sinking 80 mA		8	12	Ω
AC PERFORMANCE		T_A = 25°C for all ac performance specifications				
Settling Time[6, 7]	t_{SET}					
Full-Scale Step 3.125 mA Range		±0.0015% (±1 LSB at 16b)		21.1		µs
		±0.024% (±1 LSB at 12b)		3.8		µs
145 mA to 155 mA Step 200 mA Range		±0.0015% (±1 LSB at 16b)		7.2		µs
		±0.024% (±1 LSB at 12b)		3.6		µs
Full-Scale Step 200 mA Range		±0.0015% (±1 LSB at 16b)		200		µs
		±0.024% (±1 LSB at 12b)		3.5		µs
Glitch Impulse		At midscale transition, 200 mA range, resistive load that connects the DAC output to GND (R_{LOAD}) = 4 Ω		1.0		nA × s
DAC to DAC Crosstalk[8]		100 mA to 200 mA step, R_{LOAD} = 15 Ω		230		pA × s
i_{NOISE}		Output current noise density internal reference, I_{OUTx} = 150 mA, R_{LOAD} = 4 Ω, load capacitance (C_{LOAD}) = 10 µF				
Frequency (f) = 1 kHz				12		nA/√Hz
f = 10 kHz				5		nA/√Hz
f = 100 kHz				0.5		nA/√Hz
f = 1 MHz				0.05		nA/√Hz
REFERENCE						
Reference Output Voltage	V_{REF}		1.248	1.250	1.252	V
V_{REF} Temperature Coefficient[9]		LFCSP model	−10	+3	+10	ppm/°C
		WLCSP model		2.4		ppm/°C
V_{REF} Line Regulation		V_{CC} = 5 V ± 10%		50		µV/V
V_{REF} Short-Circuit Current		V_{CC} = 5.5 V, forcing output to GND		2.5		mA
REFCOMP Pin Short-Circuit Current		V_{CC} = 5.5 V, forcing output to GND		65		µA
V_{REF} Load Regulation		V_{CC} = 5 V, reference current (I_{REF}) = 100 µA sourcing		140		mV/mA
V_{REF} Output Voltage Noise Density		REFCOMP pin current ($C_{REFCOMP}$) = REFCOMP pin capacitance (C_{REF}) = 0.1 µF at f = 10 kHz		32		nV/√Hz
External Reference Input Current				0.001	1	µA
External Reference Input Capacitance[10]				40		pF
External Reference Input Voltage		REFCOMP pin is tied to GND	1.225		1.275	V
External Full-Scale Adjust Resistor	R_{FSADJ}	R_{FSADJ} to GND	19	20	41	kΩ

SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUT/OUPUT						
Digital Output High Voltage	V_{OH}	SDO pin, load current = −100 µA	IO_{VCC} − 0.2			V
Digital Output Low Voltage	V_{OL}	SDO pin, load current = 100 µA			0.2	V
		$\overline{FAULT}$ pin, load current = 100 µA			0.2	V
Digital High-Z Output Leakage Current		SDO pin leakage current ($\overline{CS}$/LD high)	−1		+1	µA
		$\overline{FAULT}$ pin leakage current (not asserted)			1	µA
Digital Input Current		Input voltage (V_{IN}) = GND to IO_{VCC}	−1		+1	µA
Digital Input Capacitance[10]	C_{IN}				8	pF
High Level Input Voltage	V_{IH}	2.85 ≤ IO_{VCC} ≤ V_{CC}	0.8 × IO_{VCC}			V
		1.71 ≤ IO_{VCC} ≤ 2.85	0.8 × IO_{VCC}			V
Low Level Input Voltage	V_{IL}	2.85 ≤ IO_{VCC} ≤ V_{CC}			0.3	V
		1.71 ≤ IO_{VCC} ≤ 2.85			0.3	V
POWER SUPPLY						
Analog Supply Voltage	V_{CC}		2.85		5.5	V
Digital Input and Output Supply Voltage	IO_{VCC}		1.71		V_{CC}	V
Negative Supply	V^-		−5.5		0	V
Output Supplies	V_{DDx}	200 mA range and lower (relative to GND)	2.1		V_{CC}	V
		300 mA range and lower (relative to GND)	2.4		V_{CC}	V
Output Supplies, Total Voltage[11]		Safe operating area (V_{DDx} relative to V^-)	2.85		9	V
V_{CC} Supply Current		All ranges (code = 0, all channels)		4	5.3	mA
IO_{VCC} Supply Current		All ranges (code = 0, all channels)		0.01	1	µA
V^- Supply Current		All ranges (code = 0, all channels)		7.5	11	mA
V_{DDX} Supply Current		All ranges (code = 0, per channel)		1.5	2.2	mA
		25 mA range (code = full-scale, per channel)[12]		28	32	mA
		200 mA range (code = full-scale, per channel)[12]		205	215	mA
V_{CC} Shutdown Current[13, 14]	I_{SLEEP}			50	500	µA
IO_{VCC} Shutdown Current[13, 14]				0.01	1	µA
V^- Shutdown Current[13, 14]				0.29	1.2	mA
V_{DDX} Shutdown Current[13, 14]				80	250	µA
MONITOR MULTIPLEXER						
MUX Pin DC Output Impedance				15		kΩ
MUX Pin Leakage Current		Monitor multiplexer disabled (high impedance)	−1	+0.1	+1	µA
MUX Pin Output Voltage Range		Monitor multiplexer selected to OUT0 pin voltage to OUT4 pin voltage	V^-		V_{CC}	V
MUX Pin Continuous Current[11]		T_A = 25°C (do not exceed)	−1		+1	mA

1 Offset current is measured at Code 384 for the LTC2672-16, and at code 24 for the LTC2672-12. Linearity is defined from Code 384 to Code 65535 for the LTC2672-16 and from Code 24 to Code 4095 for the LTC2672-12.

2 For the full-scale current (I_{FS}) = 300 mA, R_{LOAD} = 10 Ω. For I_{FS} = 200 mA, R_{LOAD} = 15 Ω. For I_{FS} = 100 mA, R_{LOAD} = 30 Ω. For I_{FS} = 50 mA, R_{LOAD} = 50 Ω. For I_{FS} = 25 mA, R_{LOAD} = 100 Ω. For I_{FS} = 12.5 mA, R_{LOAD} = 200 Ω. For I_{FS} = 6.25 mA, R_{LOAD} = 400 Ω. For I_{FS} = 3.125 mA, R_{LOAD} = 800 Ω.

3 I_{FS} = 200 mA and R_{LOAD} = 15 Ω. DC crosstalk is measured with a 100 mA to 200 mA current step on all four aggressor channels. Total power dissipation change is 4 × 50 mW = 200 mW. The monitor channel is held at 3/4 × I_{FS} or 150 mA.

4 V_{OUTx} is the channel output (OUTx) voltage.

5 The loads attached to the OUTx pins must be terminated to GND.

6 V_{DDx} = 5 V (3.125 mA range), V_{DDx} = 3.6 V (200 mA range), and V^- = −3.3 V for all ranges. For large current output steps, internal thermal effects result in a final settling tail. In most cases, the tail is too small to affect settling to ±0.024%, but several milliseconds can be needed for full settling to the ±0.0015% level. For optimal results,

SPECIFICATIONS

solder/via all GND and REFLO pins as well as the exposed pad (LFCSP package only) to a solid GND plane and set V_{DDx} as low as practicable for each channel to reduce power dissipation in the device.

[7] Internal reference mode. The load is 15 Ω (200 mA range) or 800 Ω (3.125 mA range) terminated to GND.

[8] DAC to DAC crosstalk is the glitch that appears at the output of one DAC because of a 100 mA to 200 mA step change in an adjacent DAC channel. The measured DAC is at midscale (100 mA output current) in the 200 mA span range, with the internal reference, V_{DDx} = 5 V, V^- = −3.3 V.

[9] The temperature coefficient is calculated by first computing the ratio of the maximum change in the output voltage to the nominal output voltage, and then dividing the ratio by the specified temperature range.

[10] Guaranteed by design and not production tested.

[11] Stresses beyond those listed for extended periods can cause permanent damage to the device or affect device reliability and lifetime.

[12] Single channel at a specified output.

[13] V_{CC} = IO_{VCC} = 5 V, V_{DDx} = 5 V, V^- = −3.3 V.

[14] Digital inputs are at 0 V or IO_{VCC}.

TIMING CHARACTERISTICS

All specifications apply over the full operating T_J range. Digital input low and high voltages are 0 V and IO_{VCC}, respectively.

Table 2. 2.85 V ≤ V_{CC} ≤ 5.5 V and 2.85 V ≤ IO_{VCC} ≤ V_{CC}

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
t_1	SDI valid to SCK setup	6			ns
t_2	SDI valid to SCK hold	6			ns
t_3	SCK high time	9			ns
t_4	SCK low time	9			ns
t_5	$\overline{CS}$/LD pulse width	10			ns
t_6	LSB SCK high to $\overline{CS}$/LD high	19			ns
t_7	$\overline{CS}$/LD low to SCK high	7			ns
t_8	SDO propagation delay from SCK falling edge, C_{LOAD} = 10 pF, 4.5 V < IO_{VCC} < V_{CC}			20	ns
	SDO propagation delay from SCK falling edge, C_{LOAD} = 10 pF, 2.85 V < IO_{VCC} < 4.5 V			30	ns
t_9	$\overline{CLR}$ pulse width	20			ns
t_{10}	$\overline{CS}$/LD high to SCK positive edge	7			ns
t_{11}	$\overline{LDAC}$ pulse width	15			ns
t_{12}	$\overline{CS}$/LD high to $\overline{LDAC}$ high or low transition	15			ns
f_{SCK}	SCK frequency			50	MHz
t_{13}	TGP high time[1]	1			µs
t_{14}	TGP low time[1]	1			µs

[1] Guaranteed by design and not production tested.

Table 3. 2.85 V ≤ V_{CC} ≤ 5.5 V and 1.71 V ≤ IO_{VCC} ≤ 2.85 V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
t_1	SDI valid to SCK setup	7			ns
t_2	SDI valid to SCK hold	7			ns
t_3	SCK high time	30			ns
t_4	SCK low time	30			ns
t_5	$\overline{CS}$/LD pulse width	15			ns
t_6	LSB SCK high to $\overline{CS}$/LD high	19			ns
t_7	$\overline{CS}$/LD low to SCK high	7			ns
t_8	SDO propagation delay from SCK falling edge, C_{LOAD} = 10 pF			60	ns
t_9	$\overline{CLR}$ pulse width	30			ns
t_{10}	$\overline{CS}$/LD high to SCK positive edge	7			ns
t_{11}	$\overline{LDAC}$ pulse width	15			ns
t_{12}	$\overline{CS}$/LD high to $\overline{LDAC}$ high or low transition	15			ns

SPECIFICATIONS

Table 3. 2.85 V ≤ V_{CC} ≤ 5.5 V and 1.71 V ≤ IO_{VCC} ≤ 2.85 V (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f_{SCK}	SCK frequency (50% duty cycle, excludes SDO operation)			15	MHz
t_{13}	TGP high time[1]	1			µs
t_{14}	TGP low time[1]	1			µs

[1] Guaranteed by design and not production tested.

Timing Diagrams

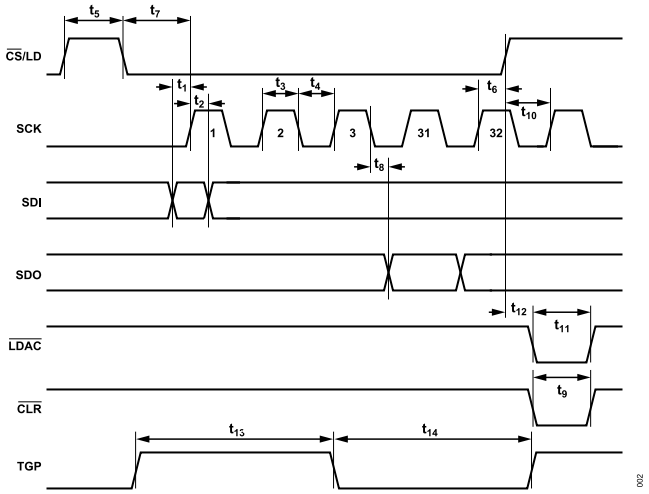


Figure 2. Timing Diagram for Serial Interface, LDAC, CLR, and Toggle Pins

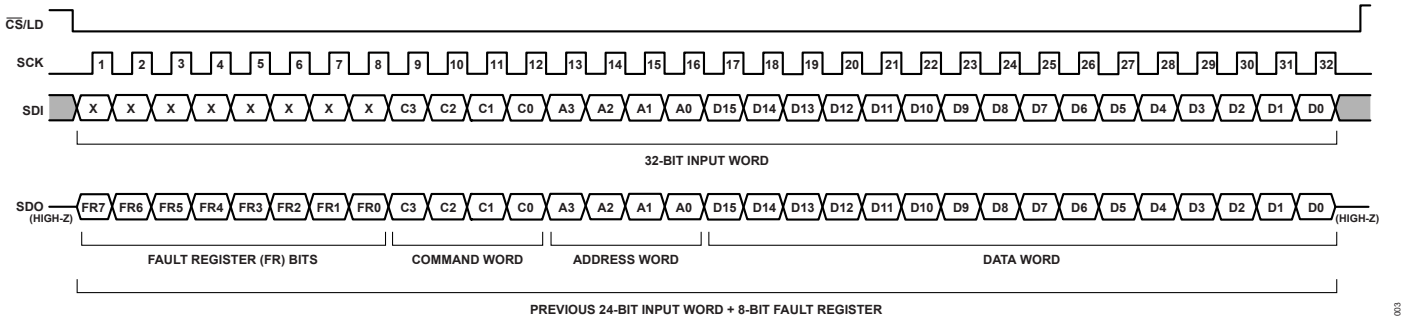


Figure 3. LTC2672 32-Bit Command Sequence

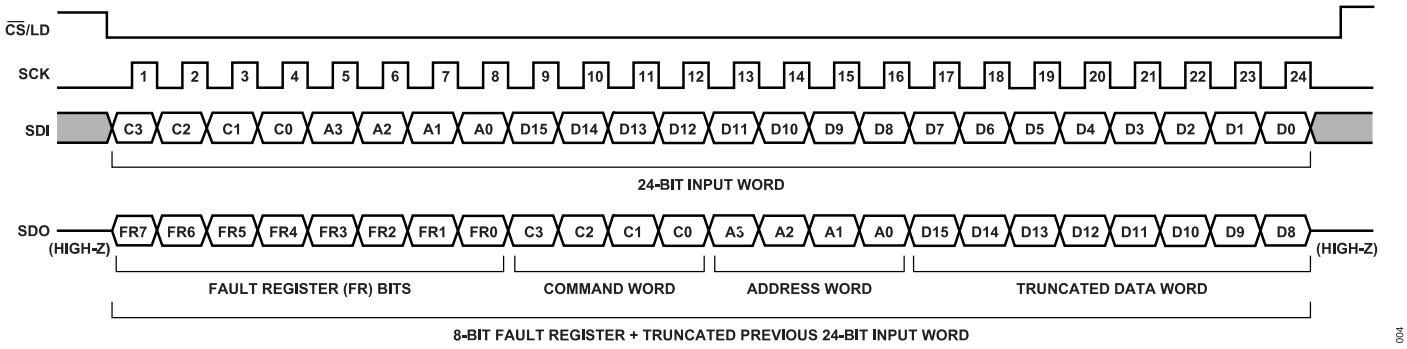


Figure 4. LTC2672 24-Bit Command Sequence

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{CC} to GND	−0.3 V to +6 V
IO_{VCC} to GND	−0.3 V to +6 V
V^- to GND	−6 V to +0.3 V
V_{DDx} to GND	−0.3 V to (V_{CC} + 0.3 V)
V_{DDx} to V^-	−0.3 V to +10 V
OUTx to GND	(V^- − 0.3 V) to (V_{DDx} + 0.3 V)
MUX	(V^- − 0.3 V) to (V_{CC} + 0.3 V)
REF, REFCOMP, FSADJ	−0.3 V to minimum (V_{CC} + 0.3 V, 6 V)
$\overline{CS}$/LD, SCK, SDI, $\overline{LDAC}$, $\overline{CLR}$, TGP to GND	−0.3 V to +6 V
$\overline{FAULT}$ to GND	−0.3 V to +6 V
SDO	–0.3 V to minimum (V_{CC} + 0.3 V, 6 V)
Temperature	
Operating Range (T_J)	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction, T_{JMAX}	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Thermal characteristics are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Thermal resistance values specified in Table 5 are simulated based on JEDEC specifications using a 2S2P thermal test board (see JEDEC JESD51), except for θ_{JC-TOP}, which uses a JEDEC 1S test board.

θ_{JA} is the junction to ambient thermal resistance, measured in a JEDEC natural convection environment.

θ_{JC} is the junction to case thermal resistance, measured at the center of the package top surface, with an infinite heat sink attached to the package surface.

θ_{JB} is the junction to board thermal resistance, measured at a point on the board 1 mm from the package edge, along the package center line, measured in a JEDEC θ_{JB} environment.

Ψ_{JB} is the junction to board thermal characterization parameter, measured in a JEDEC natural convection environment.

Ψ_{JT} is the junction to package top thermal characterization parameter, measured in a JEDEC natural convection environment.

Do not use θ_{JA}, θ_{JC}, and θ_{JB} thermal resistances to perform direct calculation/measurement of the die temperature because doing so results in incorrect values. The thermal resistances assume 100% of the power that is dissipated along the specified path between the measurement points. The thermal resistances are directly dependent on the PCB design and environment.

If direct measurement of the package is required, the Ψ_{JT} and Ψ_{JB} values must be used because they more accurately reflect the true thermal dissipation paths.

θ_{JC} must only be used where an external heat sink is attached directly to the package.

System level thermal simulation is highly recommended.

For more details about the thermal resistances, refer to *JEDEC51-12: Guidelines for Reporting and Using Electronic Package Thermal Information*.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC-TOP}	Ψ_{JT}	Ψ_{JB}	Unit
05-08-1693[1]	28.34	9.27	17.33	0.11	9.20	°C/W
CB-36-9[1]	29.56	3.85	0.18	0.36	3.62	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

Table 6. LTC2672, 36-Ball WLCSP and 32-lead LFCSP

Package Type	ESD Model	Withstand Voltage (V)	Class
36-Ball WLCSP	HBM	3000	2
	FICDM	1250	C3
32-lead LFCSP	HBM	3000	2
	FICDM	2000	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

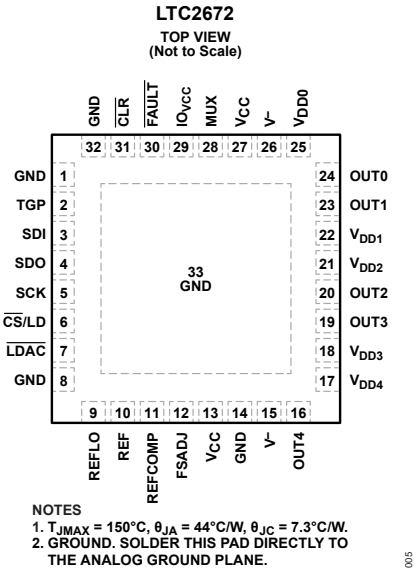


Figure 5. LFCSP Pin Configuration

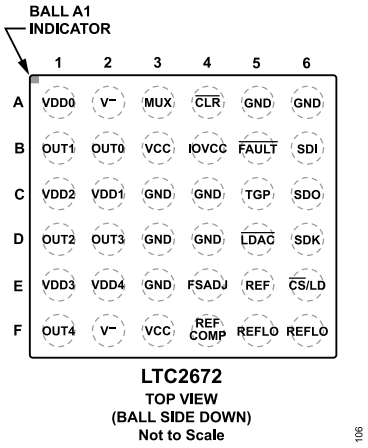


Figure 6. WLCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
LFCSP	**WLCSP**	**Mnemonic**	**Description**
1, 8, 14, 32	A5, A6, C3, C4, D3, D4, E3	GND	Analog Ground. Tie GND to an analog ground plane.
2	C5	TGP	Asynchronous Toggle Pin. A falling edge on TGP updates the DAC register with data from Input Register A. A rising edge on TGP updates the DAC register with data from Input Register B. Toggle operations only affect the DAC channels that have the toggle select bit (Tx) set to 1. Tie TGP to IO_{VCC} if the toggle operations are being done through software. Tie TGP to GND if the toggle operations are not used. Logic levels are determined by IO_{VCC}.
3	B6	SDI	Serial Data Input. Data on SDI is clocked into the DAC on the rising edge of SCK. The LTC2672 accepts input word lengths of 24 bits, 32 bits, or multiples of 32 bits. Logic levels are determined by IO_{VCC}.
4	C6	SDO	Serial Data Output. The serial output of the 32-bit shift register appears at SDO. The data transferred to the device via SDI is delayed 32 SCK rising edges before being output at the next falling edge. SDO can be used for data echo readback or daisy-chain operation. SDO becomes high impedance when $\overline{CS}$/LD is high. Logic levels are determined by IO_{VCC}.
5	D6	SCK	Serial Clock Input. Logic levels are determined by IO_{VCC}.
6	E6	$\overline{CS}$/LD	Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting SDI data into the register, and SDO is enabled. When $\overline{CS}$/LD is taken high, SDO and SCK are disabled, and the specified command (see Table 8) is executed. Logic levels are determined by IO_{VCC}.
7	D5	$\overline{LDAC}$	Active Low Asynchronous DAC Update Pin. $\overline{LDAC}$ allows updates independent of SPI timing. If $\overline{CS}$/LD is high, a falling edge on $\overline{LDAC}$ updates all DAC registers with the contents of the input registers. $\overline{LDAC}$ is gated by $\overline{CS}$/LD and has no effect if $\overline{CS}$/LD is low. Logic levels are determined by IO_{VCC}. If $\overline{LDAC}$ is not used, tie $\overline{LDAC}$ to IO_{VCC}.
9	F5, F6	REFLO	Reference Low. REFLO is the signal ground for the reference. Tie REFLO directly to GND.
10	E5	REF	Reference Input and Output. The voltage at REF proportionally scales the full-scale output current of each DAC output channel. By default, the internal 1.25 V reference is routed to REF. REF must be buffered when driving external dc load currents. If the reference is disabled (see the Reference Modes section), the reference output is disconnected, and REF becomes a high impedance input that accepts a precision external reference. For low noise and reference stability, tie a capacitor from REF to GND. The capacitor value must be less than $C_{REFCOMP}$, where $C_{REFCOMP}$ is the capacitance tied to REFCOMP. The allowable external reference input range is 1.225 V to 1.275 V.
11	F4	REFCOMP	Internal Reference Compensation Pin. For low noise and reference stability, tie a 0.1 µF capacitor from REFCOMP to GND. Tying REFCOMP to GND causes the device to power up with the internal reference disabled and allows the use of an external reference at start-up.
12	E4	FSADJ	Full-Scale Current Adjust Pin. FSADJ can be used in one of two ways to produce either nominal, internally calibrated output ranges, or incrementally tunable ranges. In either case, the reference voltage, V_{REF}, is forced across a resistor, R_{FSADJ}, to define a reference current that scales the outputs for all ranges and channels. Full-scale currents are

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 7. Pin Function Descriptions (Continued)

Pin No.			
LFCSP	WLCSP	Mnemonic	Description
			proportional to the voltage at REF and are inversely proportional to R_{FSADJ}. If FSADJ is tied to V_{CC}, an internal R_{FSADJ} (20 kΩ) is selected, which results in nominal output ranges. An external resistor of 19 kΩ to 41 kΩ can be used instead by connecting the resistor between FSADJ and GND. In this case, the external resistor controls the scaling of the ranges, and the internal resistor is automatically disconnected. See Table 10 for details. When using an external resistor, FSADJ is sensitive to stray capacitance and must be compensated with a snubber network that consists of a series combination of 1 kΩ and 1 µF connected in parallel to R_{FSADJ}. With the recommended compensation, FSADJ is stable while driving stray capacitance up to 50 pF.
13, 27	B3, F3	V_{CC}	Analog Supply Voltage. 2.85 V ≤ V_{CC} ≤ 5.5 V. All output supply voltages must be less than or equal to V_{CC}, (V_{DDx} ≤ V_{CC}). Bypass V_{CC} to GND with a 1 µF capacitor.
15, 26	A2, F2	V^-	Negative Supply Voltage. −5.5 V ≤ V^- ≤ GND. Bypass V^- to GND with a 1 µF capacitor unless V^- is connected to GND. See Figure 33 for safe operating voltages.
16, 19, 20, 23, 24	F1, D2, D1, B1, B2	OUT4 to OUT0	DAC Analog Current Outputs. Each current output pin has a dedicated analog supply pin, V_{DD0} to V_{DD4}. The load attached to OUTx must be terminated to GND. For information on combining outputs, see the Load Termination and Combining Channels section.
17, 18, 21, 22, 25	E2, E1, C1, C2, A1	V_{DD4} to V_{DD0}	Output Supplies. V_{DD0} to V_{DD4} operate at 2.1 V to V_{CC} with respect to GND, and at 2.85 V to 9 V with respect to V^-. These five positive supply inputs provide independent supplies for each of the five DAC current output pins, OUT0 to OUT4, respectively. Note that the highest output supply voltage must be less than or equal to V_{CC} (V_{DDx} ≤ V_{CC}). Bypass each supply input to GND separately with a 1 µF capacitor. Unused output supplies must be connected to a valid V_{CC} or V_{DDx} supply. Do not leave these pins floating. See Figure 33 for safe operating voltages.
28	A3	MUX	Analog Multiplexer Output. Pin voltages and currents can be monitored by measuring the voltage at MUX. When the multiplexer is disabled, MUX becomes high impedance. The available multiplexer selections are shown in Table 11.
29	B4	IO_{VCC}	Digital Input and Output Supply Voltage. 1.71 V ≤ IO_{VCC} ≤ V_{CC} + 0.3 V. Bypass IO_{VCC} to GND with a 0.1 µF capacitor.
30	B5	$\overline{FAULT}$	Active Low Fault Detection Pin. This open-drain, N-channel output pulls low when any valid fault condition is detected. $\overline{FAULT}$ is released on the next $\overline{CS}$/LD rising edge. A pull-up resistor is required (5 kΩ recommended).
31	A4	$\overline{CLR}$	Active Low Asynchronous Clear Input. A logic low at this level triggered input clears the device to the default reset code and output range, which is zero-scale with the outputs off. The control registers are cleared to zero. Logic levels are determined by IO_{VCC}.
33	N/A	GND	Ground. Solder this pad directly to the analog ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

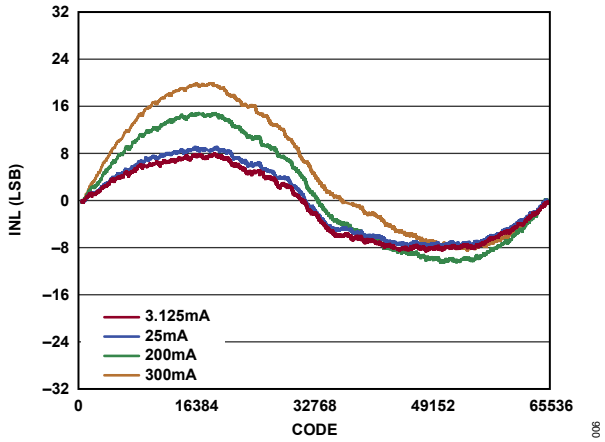


Figure 7. LTC2672-16 INL

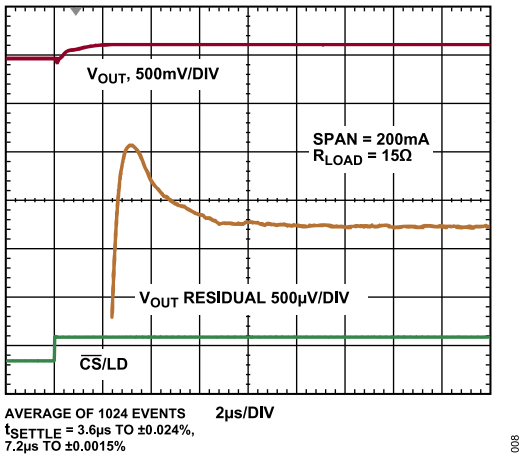


Figure 10. Settling 145 mA to 155 mA Step (VOUT Is the Output Voltage)

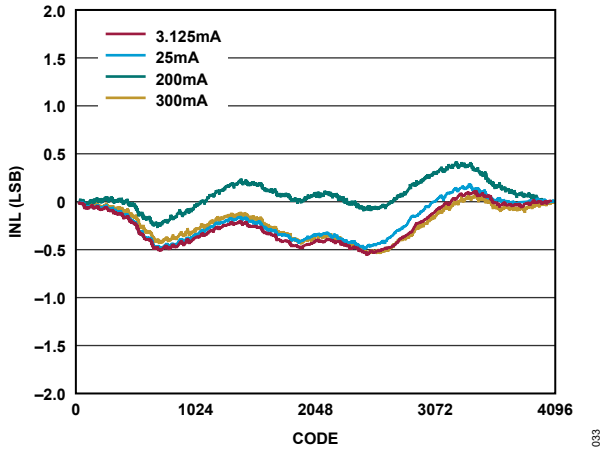


Figure 8. LTC2672-12 INL

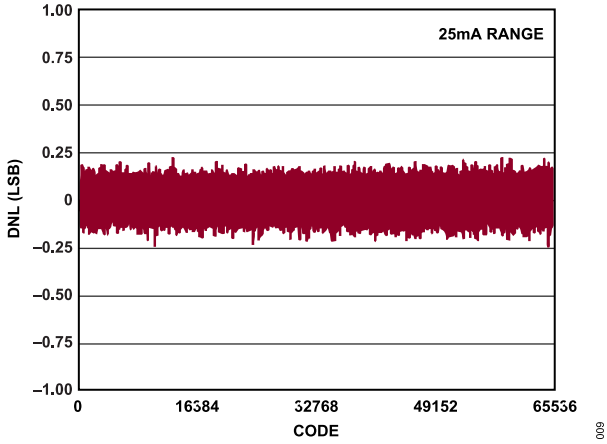


Figure 11. LTC2672-16 DNL

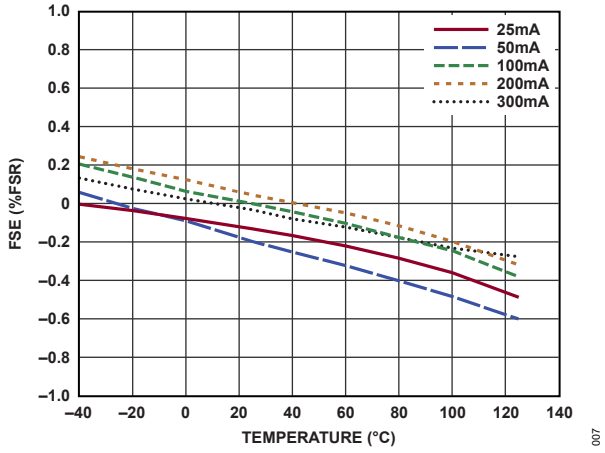


Figure 9. Full–Scale Current Error (FSE) vs Temperature

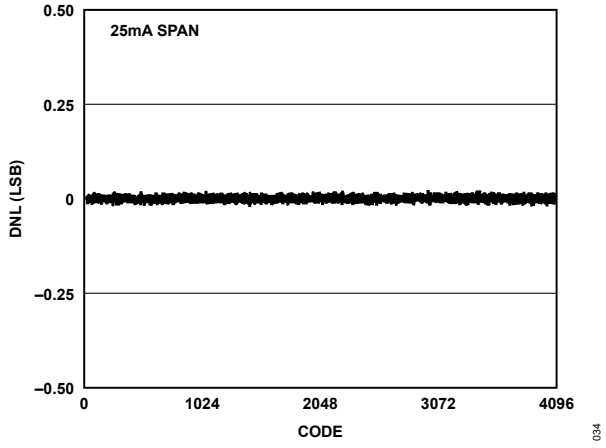


Figure 12. LTC2672-12 DNL

TYPICAL PERFORMANCE CHARACTERISTICS

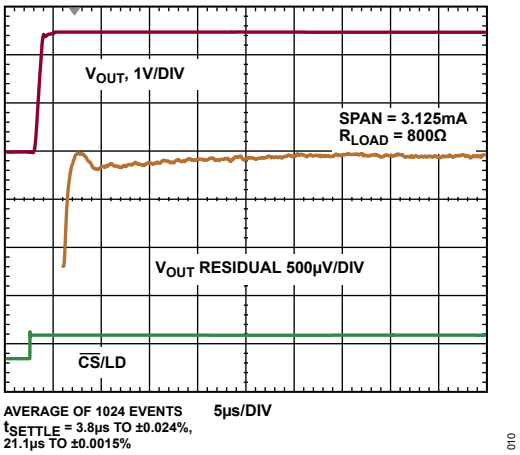


Figure 13. Settling 0 mA to 3.125 mA Step

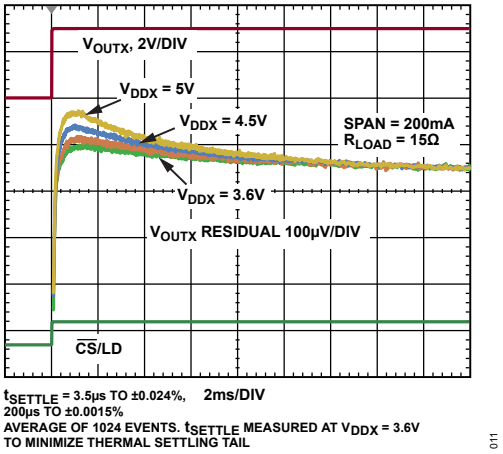


Figure 14. Settling 0 mA to 200 mA Step

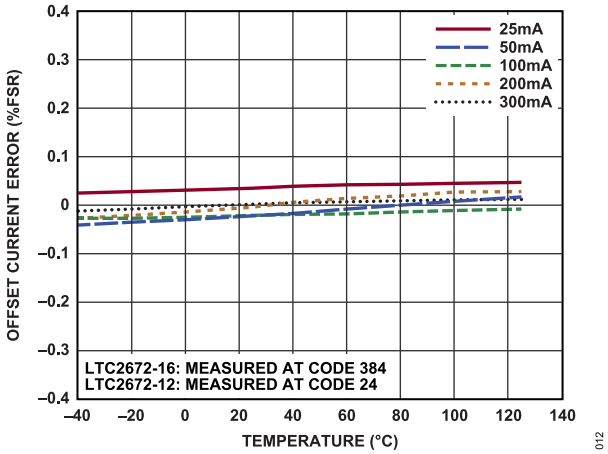


Figure 15. Offset Current Error vs. Temperature

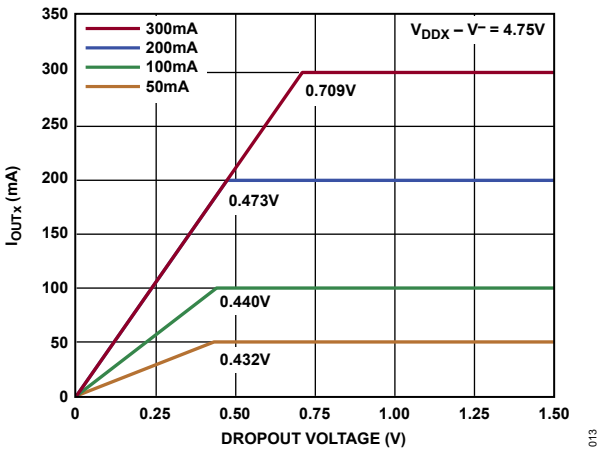


Figure 16. I_{OUTx} vs. Dropout Voltage for Multiple Current Ranges

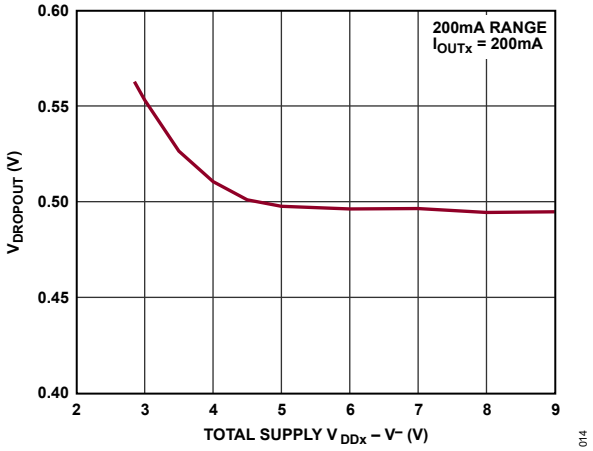


Figure 17. $V_{DROPOUT}$ vs. Total Supply $V_{DDx} - V^-$

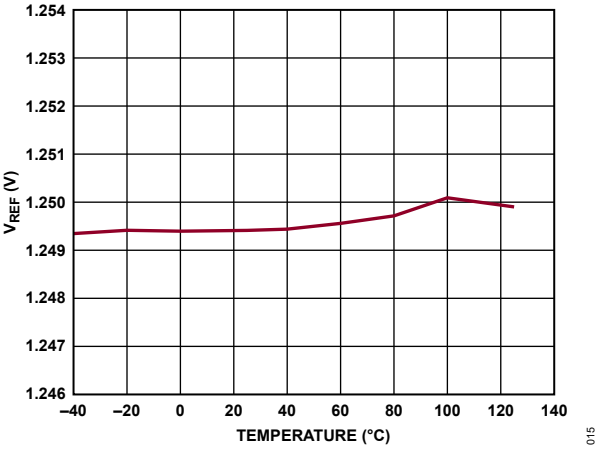


Figure 18. V_{REF} vs. Temperature (LFCSP)

TYPICAL PERFORMANCE CHARACTERISTICS

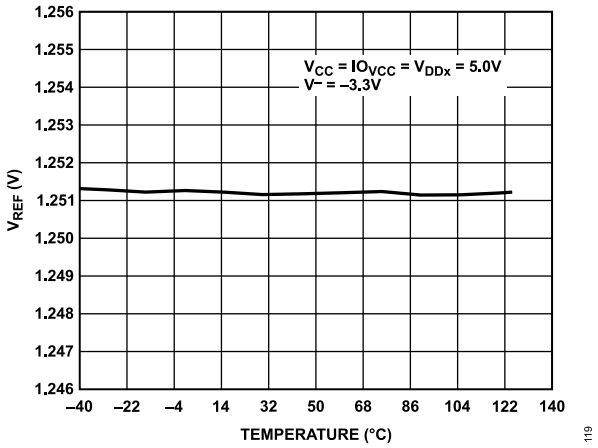


Figure 19. V_{REF} vs. Temperature (WLCSP)

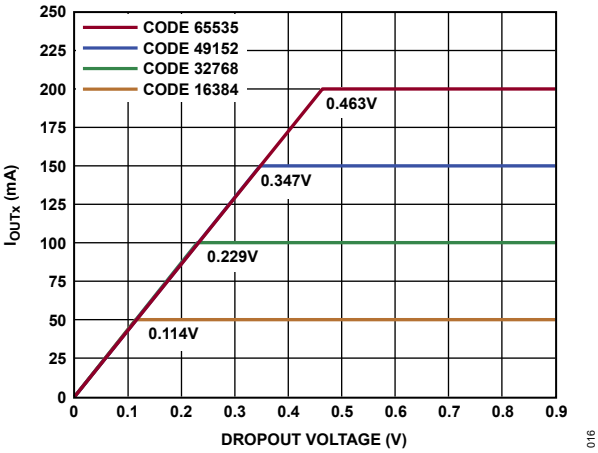


Figure 20. I_{OUTx} vs. Dropout Voltage for Multiple Codes (200 mA Span)

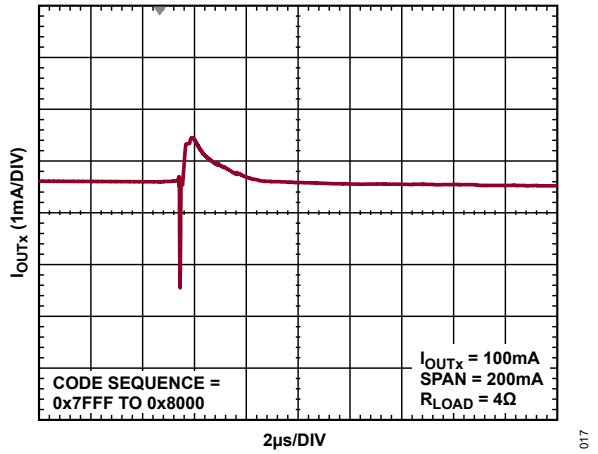


Figure 21. Midscale Glitch

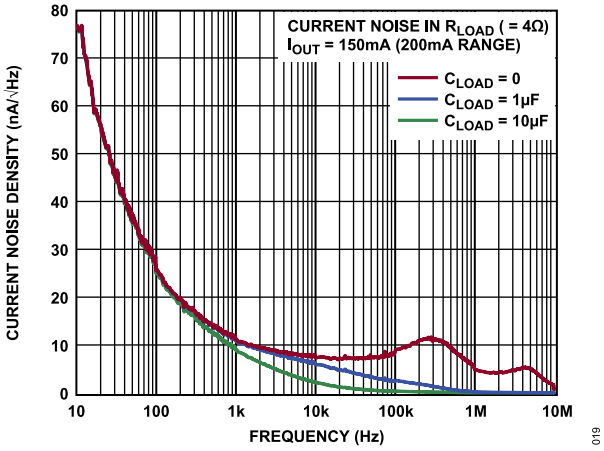


Figure 22. Current Noise Density vs. Frequency, Grounded C_{LOAD} = 0 µF, 1 µF, and 10 µF

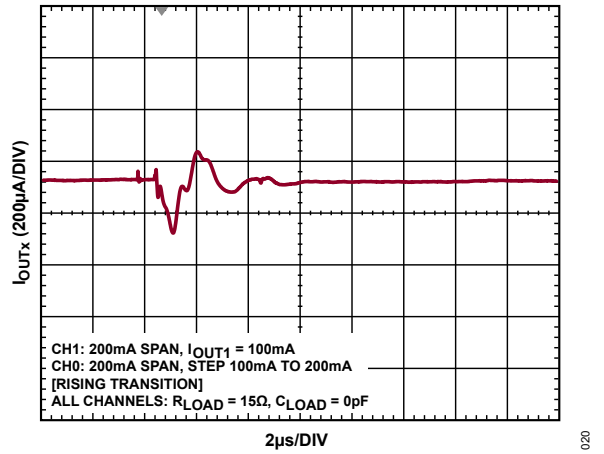


Figure 23. DAC to DAC Crosstalk (Rising)

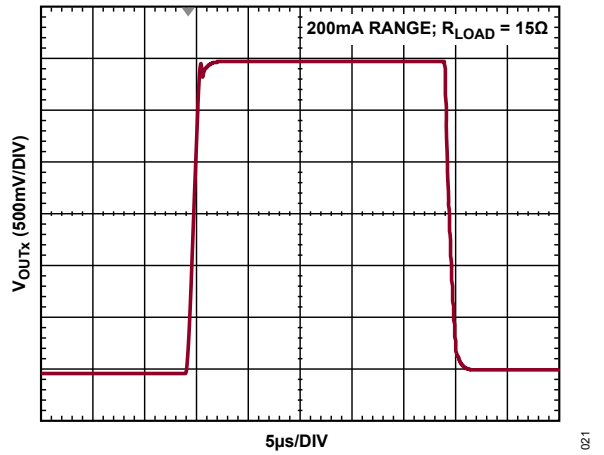


Figure 24. Large Signal Response

TERMINOLOGY

Integral Nonlinearity (INL)

INL is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. INL for this DAC is defined from Code 384 to Code 65535 for the LTC2672-16 and Code 24 to Code 4095 for the LTC2672-12.

Differential Nonlinearity (DNL)

DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Because the output must have a finite output current, DNL for this DAC is defined from Code 384 to Code 65,535 for the LTC2672-16 and Code 24 to Code 4095 for the LTC2672-12.

Current Offset Error (I_{OS})

Unipolar offset error is typically measured when zero code is loaded to the DAC register. Because offset can be either positive or negative polarity and the output current cannot go below zero, offset is defined at Code 384 for the LTC2672-16 and Code 24 for the LTC2672-12 and calculated based on the expected output at that code.

I_{OS} Temperature Coefficient

The I_{OS} temperature coefficient is a measure of the change in I_{OS} with a change in temperature and is expressed in ppm/°C.

Gain Error

Gain error is a measure of the span error of the DAC and is the deviation in slope of the DAC transfer characteristic from the ideal expressed as a percentage of full-scale range (%FSR).

Gain Error Temperature Coefficient

The gain error temperature coefficient is a measurement of the change in gain error with changes in temperature and is expressed in ppm/°C.

Power Supply Rejection (PSR)

PSR indicates how the output of the DAC is affected by changes in the supply voltage. PSR is the change in V_{OUTx} because of a specified change in V_{CC}, V^-, or V_{DDx} for a full-scale output of the DAC and is expressed in LSB.

Settling Time

Settling time is the amount of time it takes for the output of a DAC to settle to a specified error window for a full-scale input change and is measured from the rising edge of $\overline{CS}$/LD.

Glitch Impulse

Glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. Glitch impulse is normally specified as the area of the glitch in nA × sec and is measured when the digital input code is changed by 1 LSB at the midscale transition.

DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC in response to a 100 mA to 200 mA change in the outputs of all other DAC channels. The monitored channel is maintained at 150 mA (3/4 × I_{FS}). DC crosstalk is expressed in %FSR.

DAC to DAC Crosstalk

DAC to DAC crosstalk is the glitch that appears at the output of one DAC because of a step change from 100 mA to 200 mA in another DAC channel. The measured DAC is at midscale (100 mA output current) in the 200 mA range. The energy of the glitch is expressed in nA × sec.

Output Noise Spectral Density

Output noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nA/√Hz) and is measured by loading the DAC to 150 mA (3/4 × I_{FS}) and measuring noise at the output.

THEORY OF OPERATION

The LTC2672 is a family of five-channel, current source output DACs with selectable output ranges, a precision reference, and a multiplexer for surveying the channel output voltages and currents. Each output draws its current from a separate dedicated positive supply pin that accepts voltages of 2.1 V to V_{CC} to allow optimization of power dissipation and headroom for a wide range of loads. Internal 12 Ω switches allow any output pin to be connected to an optional negative V^- supply voltage and sink up to 80 mA.

LOAD TERMINATION AND COMBINING CHANNELS

The load attached to any OUTx pins must be terminated to ground. The OUTx pins that are not used in the system design must be left open (no connect).

Any combination of OUTx pins can be tied together if currents greater than 300 mA are needed or for finer control of large currents. The LTC2672 offers the following four span categories:

- Eight current ranges
- Off mode
- Switch to V^-
- Power-down

All channels tied together must be operated in the same span category.

Although the device is tolerant of mixing span categories, doing so must be avoided because mixing span categories can increase supply currents and/or compromise accuracy. When the combined channels are operated in the current range span category (3.125 mA to 300 mA), the ranges and DAC codes do not need to be the same for each channel.

POWER-ON RESET

The outputs reset to a current off state (off mode) on power-up, which makes system initialization consistent and repeatable. When power-on initialization is complete, select the output span via the SPI bus using Table 8, Table 9, and Table 10.

POWER SUPPLY SEQUENCING

The supplies (V_{CC}, IO_{VCC}, V^-, and V_{DD0} to V_{DD4}) can be powered up in any convenient order. If an external reference is used, do not allow the input voltage at REF to rise above V_{CC} + 0.3 V during supply turn on and turn off sequences (see the Absolute Maximum Ratings section). When startup is complete, ensure that no supply exceeds V_{CC}. DC reference voltages of 1.225 V to 1.275 V are acceptable.

Supply bypassing is critical to achieving the best possible performance. Use at least 1 µF of low equivalent series resistance (ESR) capacitance to ground on all supply pins and locate the capacitor as close to the device as possible. A 0.1 µF capacitor can be used for IO_{VCC}.

DATA TRANSFER FUNCTION

The DAC input to output transfer functions for all resolutions and output ranges ≥25 mA are shown in Figure 25 and Figure 26. The input code is in straight binary format for all ranges.

SERIAL INTERFACE

When the $\overline{CS}$/LD pin is taken low, the data on the SDI pin is bit loaded into the shift register on the rising edge of the clock (SCK pin). The 4-bit command, C3 to C0, is loaded first, followed by the 4-bit DAC address, A3 to A0, and then the 16-bit data word in straight binary format. For the LTC2672-16, the data word comprises the 16-bit input code ordered MSB to LSB. For the LTC2672-12, the data word comprises the 12-bit input code, ordered MSB to LSB, followed by four don't care bits. Data can only be transferred to the LTC2672 when the $\overline{CS}$/LD signal is low. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word.

Even though the minimum input word is 24 bits, it can be extended to 32 bits. To use the 32-bit word width, transfer eight don't care bits to the device first, followed by the 24-bit word. The 32-bit word is required for echo readback and daisy-chain operation. The 32-bit word also provides accommodation for processors that have a minimum word width of 16 bits or more.

The complete 24-bit and 32-bit sequences are shown in Figure 3 and Figure 4. Note that the fault register outputs appear on the SDO pin for either word width.

Table 8. SPI Commands

Command Number	Data
0000	Write code to DAC Channel x
1000	Write code to all DAC channels
0110	Write span to DAC Channel x
1110	Write span to all DAC channels
0001	Power up and update DAC Channel x
1001	Power up and update all DAC channels
0011	Write code to DAC Channel x, power up and update DAC Channel x
0010	Write code to DAC Channel x, power up, and update all DAC channels
1010	Power up, write code to and update all DAC channels
0100	Power down Channel x
0101	Power down chip
1011	Monitor multiplexer
1100	Toggle select
1101	Global toggle
0111	Configuration command
1111	No operation

THEORY OF OPERATION

Table 9. DAC Address Mapping

	Address			
DAC Number	A3	A2	A1	A0
DAC0	0	0	0	0
DAC1	0	0	0	1
DAC2	0	0	1	0
DAC3	0	0	1	1
DAC4	0	1	0	0

Note that any DAC address code used other than the codes given in Table 9 causes the command to be ignored.

Input and DAC Registers

The LTC2672 has five internal registers for each DAC, in addition to the main shift register. Each DAC channel has two sets of double-buffered registers, one set for the code data and one set for the span (output range) of the DAC. Double buffering provides the capability to simultaneously update the span and code, which allows smooth current transitions when changing output ranges. Double buffering also allows the simultaneous updating of multiple DACs. Each set of double-buffered registers comprises an input register and a DAC register.

Regarding the input register, the write operation shifts data from the SDI pin into a chosen register. The input registers are holding buffers. Write operations do not affect the DAC outputs.

In the code datapath, there are two input registers, Register A and Register B, for each DAC register. Register B is an alternate register used only in the toggle operation, and Register A is the default input register.

Regarding the DAC register, the update operation copies the contents of an input register to its associated DAC register. The content of a DAC register directly controls the DAC output current or range.

The update operation also powers up the selected DAC if the DAC had been in power-down mode. Note that updates always refresh both code and span data, but the values held in the DAC registers remain unchanged unless the associated input register values have been changed via a write operation. For example, if a new code is written and the channel is updated, the code is updated while the span is refreshed and unchanged. A channel update can come from a serial update command, an $\overline{LDAC}$ negative pulse, or a toggle operation.

OUTPUT RANGES AND SOFTSPAN OPERATION

The LTC2672 is a five-channel current DAC with selectable output ranges. The full set of current output ranges is only available through SPI programming.

Figure 28 shows a simplified diagram of a single channel of the LTC2672. The full-scale current range of the LTC2672 is selected via four control bits, Bits[S3:S0], on a per channel basis. The user can also provide an external reference at the REF pin or use an external resistor at the FSADJ pin to adjust the full-scale currents as needed.

The LTC2672 initializes at power-up with all channel outputs (OUT0 to OUT4) in off mode. The range and code of each channel are then fully programmable through SoftSpan™, as shown in Table 10, Figure 25, and Figure 26. Each channel has a set of double-buffered registers for range information. Program the span input register using the write span to DAC Channel x or write span all commands (0110b and 1110b, respectively, see Table 8). Figure 27 shows the syntax, and Table 10 shows the span codes and ranges. As with the double-buffered code registers, update operations copy the span input registers to the associated span DAC registers.

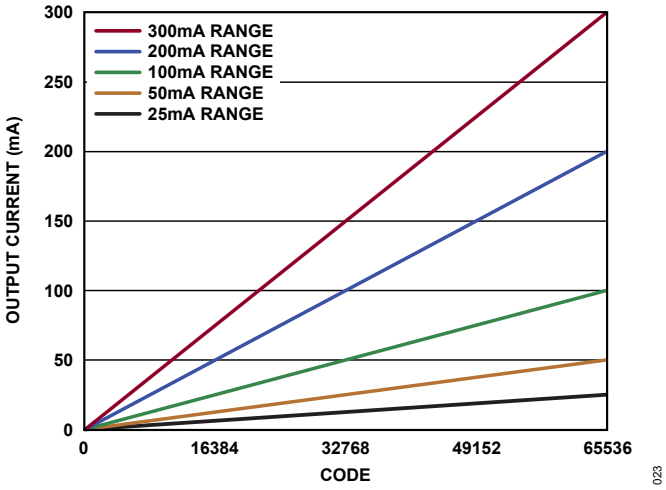


Figure 25. LTC2672-16 Transfer Function

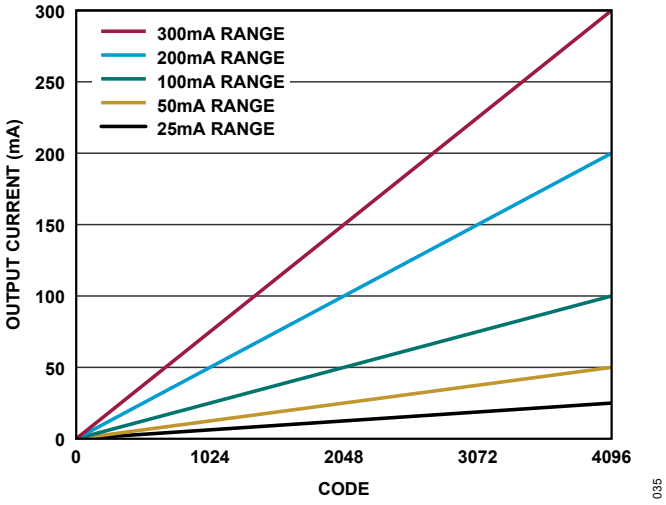


Figure 26. LTC2672-12 Transfer Function

As shown in Table 10 , there are two additional selections (Code 0000 and Code 1000) that place the output(s) in off mode or in a mode where a low on resistance (≤12 Ω) switch shunts the DAC output to the negative supply, V^-. When the switch is on, the OUTx

THEORY OF OPERATION

pin driver is disabled for that channel(s). Span codes not listed in Table 10 default to the off mode output range.

Table 10. Span Codes

				Output Range	
S3	S2	S1	S0	FSADJ = V_{CC}	External R_{FSADJ}
0	0	0	0	Off mode	Off mode
0	0	0	1	3.125 mA	50 × V_{REF}/R_{FSADJ}
0	0	1	0	6.25 mA	100 × V_{REF}/R_{FSADJ}
0	0	1	1	12.5 mA	200 × V_{REF}/R_{FSADJ}
0	1	0	0	25 mA	400 × V_{REF}/R_{FSADJ}
0	1	0	1	50 mA	800 × V_{REF}/R_{FSADJ}
0	1	1	0	100 mA	1600 × V_{REF}/R_{FSADJ}
0	1	1	1	200 mA	3200 × V_{REF}/R_{FSADJ}
1	1	1	1	300 mA	4800 × V_{REF}/R_{FSADJ}
1	0	0	0	Switch to V^-	Switch to V^-

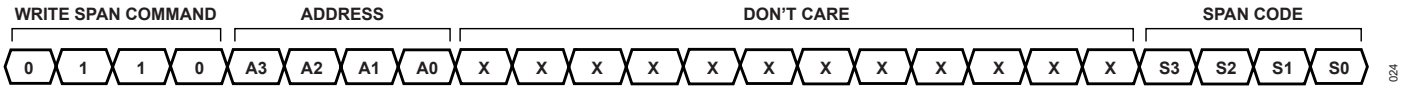


Figure 27. Write Span Syntax

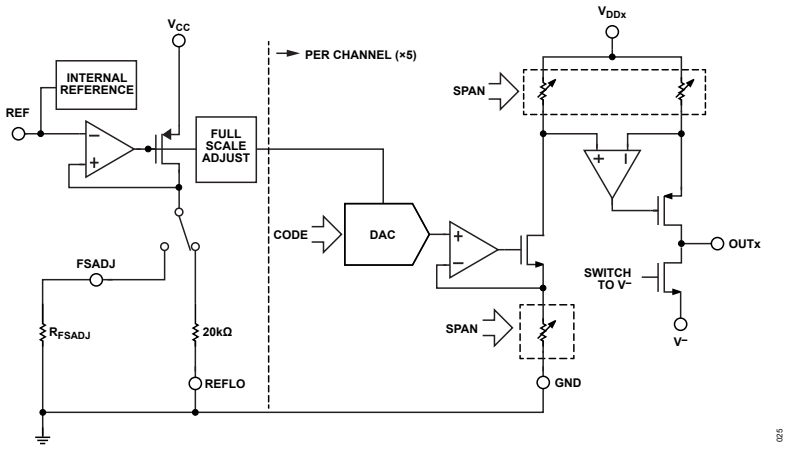


Figure 28. Single-Channel Simplified Diagram

THEORY OF OPERATION

TOGGLE OPERATIONS

Some systems require that the DAC outputs switch repetitively between two output levels (for example, switching between an on and off state). The LTC2672 toggle function facilitates these kinds of operations by providing two input registers (Register A and Register B) per DAC channel.

Toggling between Register A and Register B is controlled by three signals. The first signal is the toggle select command, which acts on the data field of 5 bits, each of which controls a single channel (see Figure 29). The second signal is the global toggle command, which controls all selected channels using the global toggle bit, TGB (see Figure 30). Lastly, the TGP pin allows the use of an external clock or logic signal to toggle the DAC outputs between Register A and Register B. The signals from these controls are combined as shown in Figure 31. If the toggle function is not needed, tie the TGP pin to ground and leave the toggle select register in its power-on reset state (cleared to zero). Input Register A then functions as the sole input register, and Register B is not used.

Toggle Select Register (TSR)

The toggle select command (1100b) syntax is shown in Figure 29. Each bit in the 5-bit TSR data field controls the corresponding DAC channel of the same name (T0 controls Channel 0, T1 controls Channel 1,..., and T4 controls Channel 4).

The toggle select bits (T0 to T4) have a dual function. First, each toggle select bit controls which input register (Register A or Register B) receives data from a write code operation. When the toggle select bit of a given channel is high, write code operations are directed to Register B of the addressed channel. When the bit is low, write code operations are directed to Register A. In addition, each toggle select bit enables the corresponding channel for a toggle operation.

Writing to Input Register A and Input Register B

When channels to toggle are chosen, write the desired codes to Input Register A for the chosen channels, then set the channel toggle select bits using the toggle select command and write the desired codes to Input Register B. When these steps are complete, the channels are ready to toggle. For example, to set up Channel 3 to toggle between Code 4096 and Code 4200, take the following steps:

1. Write Code Channel 3 (code = 4096) to Register A 00000011 00010000 00000000.
2. Toggle select (set Bit T3) 11000000 00000000 00001000.
3. Write Code Channel 3 (code = 4200) to Register B 00000011 00010000 01101000.

The write code of Step 3 is directed to Register B because in Step 2, Bit T3 was set to 1. Channel 3 now has Input Register A and Register B holding the two desired codes and is prepared for toggle operation.

Note that after writing to Register B, the code for Register A can still be changed. The state of the toggle select bit determines to which register (Register A or Register B) a write is directed.

For example, to change Register A while toggling Register B, take the following steps:

1. Reset the toggle select bit, Bit T3, to 0 (11000000 00000000 00000000).
2. Write the new Register A code. If the code used for this example is 4300, the instruction is 00000011 00010000 11001100.
3. Set the toggle select bit, Bit T3, back to 1 (see previous Step 2). It is not necessary to write to Register B again. Channel 3 is ready for the toggle operation.

Toggling Between Register A and Register B

When the input registers have been written to for all desired channels and the corresponding toggle select bits are set high, as in the previous example, the channels are ready for toggling.

The LTC2672 supports three types of toggle operations: one in which all selected channels are toggled together using the SPI port, another in which all selected channels are toggled together using an external clock or logic signal, and a third in which any combination of channels can be instructed to update from either input register.

The internal toggle update circuit is edge triggered, so only transitions (of TGB or TGP) trigger an update from the respective input register.

To toggle all selected channels together using the SPI port, ensure the TGP pin is high and that the bits in the toggle select register corresponding to the desired channels are also high. Use the global toggle command (1101b) to alternate codes and sequentially change the global toggle bit, TGB (see Figure 30). Changing TGB from 1 to 0 updates the DAC registers from the respective Input Register A. Changing TGB from 0 to 1 updates the DAC registers from the respective Input Register B. Note that in this way, up to five channels can be toggled with just one serial command.

To toggle all selected channels using an external logic signal, ensure that the TGB bit in the global toggle register is high, and that in the toggle select register, the bits corresponding to the desired channels are also high. Apply a clock or logic signal to the TGP pin to alternate codes. The TGP falling edges update the DAC registers from the associated Input Register A. The TGP rising edges update the DAC registers from the associated Input Register B. Note that after the input registers are set up, all toggling is triggered by the signal applied to the TGP pin with no further SPI instructions needed.

To cause any combination of channels to update from either Input Register A or Input Register B, ensure that the TGP pin is high

THEORY OF OPERATION

and that the TGB bit in the global toggle register is also high. Use the toggle select command to set the toggle select bits as needed to select the input register (Register A or Register B) with which each channel is to be updated. Then, update all channels either by using the serial command (1001b) or by applying a negative pulse to the $\overline{LDAC}$ pin. Any channels that have toggle select bits that are 0 update from Register A, and channels that have toggle select bits that are 1 update from Register B (see Figure 31). By alternating between toggle select and update operations, up to five channels can be simultaneously switched to Register A or Register B as needed.

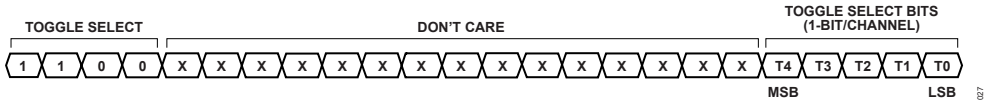


Figure 29. Toggle Select Syntax

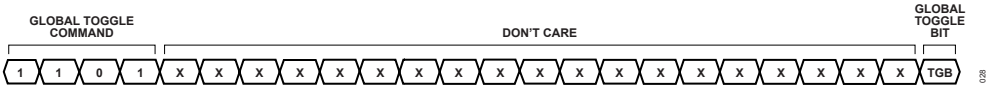


Figure 30. Global Toggle Syntax

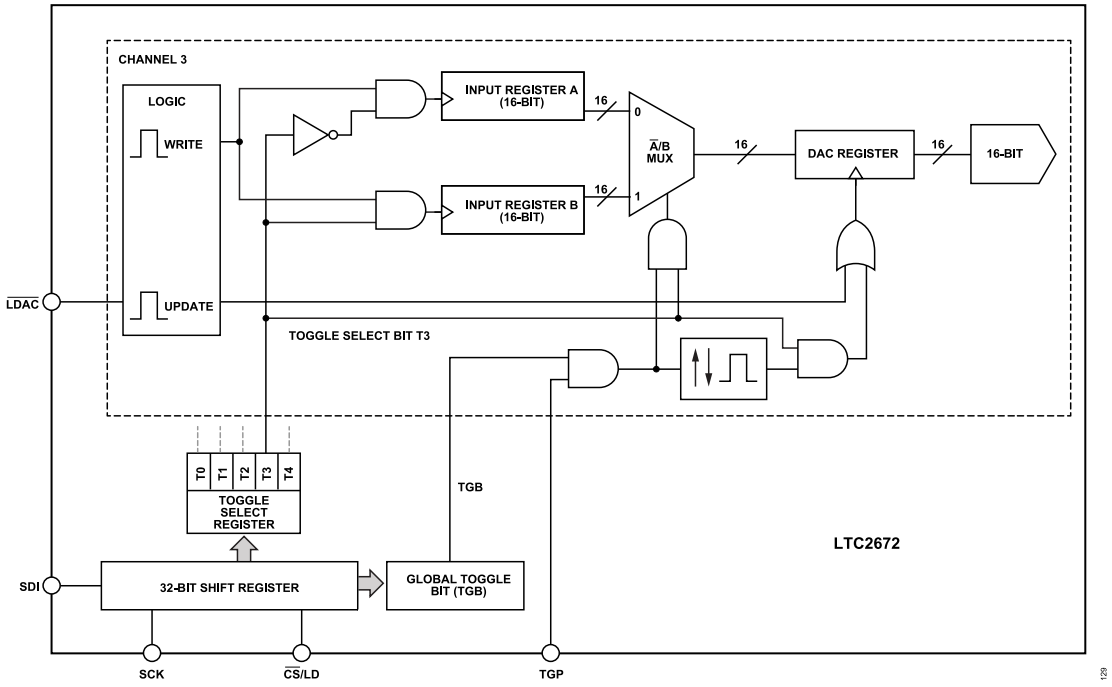


Figure 31. Conceptual Block Diagram, Toggle Functionality

THEORY OF OPERATION

DAISY-CHAIN OPERATION

The serial output of the shift register appears at the SDO pin. Data transferred to the device from the SDI input is delayed for 32 SCK rising edges before being output at the next SCK falling edge so that the data can be clocked into the microprocessor on the next 32 SCK rising edges.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (SCK, SDI, and $\overline{CS}$/LD). This kind of daisy-chain series is configured by connecting the SDO of each upstream device to the SDI of the next device in the chain. The shift registers of the devices are thus connected in series to effectively form a single input shift register that extends through the entire chain. Because of this connection, the devices can be addressed and controlled individually by concatenating their input words (the first instruction addresses the last device in the chain, and so on). The SCK and $\overline{CS}$/LD signals are common to all devices in the series.

When in use, $\overline{CS}$/LD is first taken low. Then, the concatenated input data is transferred to the chain using the SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, which completes the instruction sequence for all devices simultaneously. A single device can be controlled by using the no operation command (1111b) for all other devices in the chain. When $\overline{CS}$/LD is taken high, the SDO pin presents a high impedance output. Therefore, a pull-up resistor is required at the SDO of each device (except the last) for daisy-chain operation.

ECHO READBACK

The SDO pin can verify data transfers to the device. During each 32-bit instruction cycle, the SDO pin outputs the previous 32-bit instruction for verification. The 8-bit don't care prefix is replaced by eight fault register status bits, followed by the 4-bit command and address words and the full 16-bit data word (see Figure 3). The SDO sequence for a 24-bit instruction cycle is the same, except that the data word is truncated to 8 bits (see Figure 4). When $\overline{CS}$/LD is high, SDO presents a high impedance output and releases the bus for use by other SPI devices.

MONITOR MULTIPLEXER

The LTC2672 includes a multiplexer for monitoring both the voltages and currents at the five current output pins (OUTx). Additionally, V_{DDx}, V^-, V_{CC}, V_{REF}, and the die temperature can all be monitored.

The MUX pin is intended for use with high impedance inputs only. The impedance at the MUX pin is typically 15 kΩ. The continuous dc output current at the MUX pin must be limited to ±1 mA to avoid damaging internal circuitry.

The operating range of the multiplexer extends rail-to-rail from V^- to V_{CC}, and its output is disabled (high impedance) at power-up.

The syntax and codes for the multiplexer command are shown in Figure 32 and Table 11.

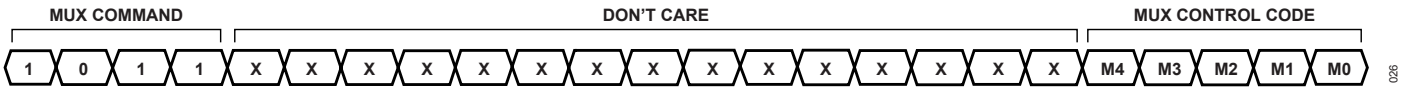


Figure 32. Multiplexer Command

Table 11. Analog Multiplexer Control Address Bits

M4	M3	M2	M1	M0	Multiplexer Signal Output	Notes[1]
0	0	0	0	0	Disabled (high-Z)	
0	0	0	0	1	OUT0 current measurement	I_{OUT0} = full-scale current (I_{FS}) × V_{MUX}/V_{REF}
0	0	0	1	0	OUT1 current measurement	$I_{OUT1} = I_{FS} \times V_{MUX}/V_{REF}$
0	0	0	1	1	OUT2 current measurement	$I_{OUT2} = I_{FS} \times V_{MUX}/V_{REF}$
0	0	1	0	0	OUT3 current measurement	$I_{OUT3} = I_{FS} \times V_{MUX}/V_{REF}$
0	0	1	0	1	OUT4 current measurement	$I_{OUT4} = I_{FS} \times V_{MUX}/V_{REF}$
0	0	1	1	0	V_{CC}	
0	1	0	0	0	V_{REF}	
0	1	0	0	1	V_{REFLO}	DAC ground (0 V) reference
0	1	0	1	0	Die temperature, T	$T = 25°C + (1.4\ V - V_{MUX})/(0.0037\ V/°C)$
1	0	0	0	0	V_{DD0}	
1	0	0	0	1	V_{DD1}	
1	0	0	1	0	V_{DD2}	
1	0	0	1	1	V_{DD3}	
1	0	1	0	0	V_{DD4}	
1	0	1	1	0	V^-	
1	0	1	1	1	GND	

THEORY OF OPERATION

Table 11. Analog Multiplexer Control Address Bits (Continued)

M4	M3	M2	M1	M0	Multiplexer Signal Output	Notes[1]
1	1	0	0	0	OUT0 pin voltage	
1	1	0	0	1	OUT1 pin voltage	
1	1	0	1	0	OUT2 pin voltage	
1	1	0	1	1	OUT3 pin voltage	
1	1	1	0	0	OUT4 pin voltage	

[1] I_{FS} is the full-scale current, and V_{MUX} is the output voltage of the multiplexer at the MUX pin.

THEORY OF OPERATION

Current Measurement Using the Multiplexer

Measure the current of any output pin by using the multiplexer command (1011b) with one of the multiplexer current measurement codes from Table 11. The multiplexer responds by outputting a voltage proportional to the actual output current. The proportionality factor is given by the following equation:

$$I_{OUTx} = I_{FS} \times V_{MUX}/V_{REF} \quad (1)$$

where:
I_{OUTx} is the output current the OUTx pin.

The current measurement function does not sense the current at the OUTx pins but instead uses the DAC settings to predict the output current. Therefore, the previous equation is invalid if the OUTx pin is open (or dropping out), or if the span is not set to one of the eight current ranges.

In the previous equation, note that V_{MUX} varies only with the DAC code (and reference voltage) and is the same for every span setting. I_{FS} must be given the value of the active span setting for the equation to evaluate correctly.

V_{MUX} has the same optimal linearity as the current outputs, but calibrating for slope error (±15% FSR) is necessary for accurate results. ±1% FSR accuracy is achievable with a one-point or two-point calibration.

Die Temperature Measurement Using the Multiplexer

Measure the die temperature by using the multiplexer command with the multiplexer Control Code 01010b. The voltage at the MUX pin (V_{MUX}) in this case is linearly related to the die temperature by a temperature coefficient of −3.7 mV/°C. The measured T_J is then

$$T_J = 25°C + (1.4\ V - V_{MUX})/(3.7\ mV/°C) \quad (2)$$

If needed, the temperature monitor can be calibrated by measuring the initial temperature and voltage, and then substituting these values for 25°C and 1.4 V, respectively, in the previous equation.

Monitor Multiplexer Precharge Considerations

The analog multiplexer in the LTC2672 is unbuffered, which obviates error terms from amplifier offsets. However, without buffers, the high impedance current outputs can be disturbed because of charge transfer at the moment when the MUX pin is connected. The LTC2672 contains circuitry that suppresses charging glitches on the output pins (OUTx) by precharging the mux pin before connecting it to the selected OUTx pin.

Because of the precharge behavior, the multiplexer output becomes valid approximately 7 µs after the multiplexer command is given ($\overline{CS}$/LD rising). Residual charging transients can be further reduced by adding capacitance to the OUTx pins, if needed.

Keep the total capacitance at the MUX pin (including board traces, buffer amplifier inputs, and any other parasitic capacitances) as small as feasible, and do not exceed 100 pF.

FAULT REGISTER

The LTC2672 provides notifications of operational fault conditions. The fault register (FR) status bits comprise the first data byte (8 bits) of each 24-bit or 32-bit SDO word outputted to the SDO pin during each SPI transaction. See Figure 3 and Figure 4 for the sequences.

An FR bit is set when its trigger condition is detected and clocked to SDO during the next SPI transaction. FR information is updated with each SPI transaction. Note that, if a fault condition is corrected by the action of an SPI instruction, the cleared FR flag for that condition is observable at SDO on the next SPI transaction.

Table 12 lists the FR bits and their associated trigger conditions.

FAULT INDICATOR PIN ($\overline{FAULT}$)

The $\overline{FAULT}$ pin is an open-drain, N-channel output that pulls low when a fault condition is detected. The $\overline{FAULT}$ pin is released on the next rising $\overline{CS}$/LD edge and is an open-drain output suitable for wired-OR connection to an interrupt bus. A pull-up resistor on the bus is required (5 kΩ is recommended).

Table 12. Fault Register (FR)

Bit	Fault Condition
FR0	Open-circuit condition detected on OUT0.
FR1	Open-circuit condition detected on OUT1.
FR2	Open-circuit condition detected on OUT2.
FR3	Open-circuit condition detected on OUT3.
FR4	Open-circuit condition detected on OUT4.
FR5	Overtemperature. If die temperature T_J > 175°C, FR5 is set, and thermal protection is activated. Can be disabled using the configuration command (0111b).
FR6	Unused.
FR7	Invalid SPI sequence length. Valid sequence lengths are 24, 32, and multiples of 32 bits. For all other lengths, FR7 is set, and the SPI instruction is ignored.

Fault Conditions and Thermal Overload Protection

There are three types of fault conditions that cause the $\overline{FAULT}$ pin to pull low. First, FR0 to FR4 flag an open-circuit (OC) condition on any of the output pins (OUT0 to OUT4, respectively) when an output channel enters dropout because of insufficient voltage from V_{DDx} to OUTx. An independent open-circuit detection circuit is provided for each of the five DAC current output pins.

FR5 provides a detection flag that is set when the die temperature exceeds 175°C. The overtemperature condition also forces all five DAC channels to power down and the open-drain $\overline{FAULT}$ pin to pull low. FR5 remains set, and the device stays in shutdown until

THEORY OF OPERATION

the die cools. Lower than approximately 150°C, the DAC channels can be returned to normal operation. Note that a $\overline{CS}$/LD rising edge releases the $\overline{FAULT}$ pin regardless of the die temperature.

Because any DAC channel can source up to 300 mA, the die heating potential of the system design must be evaluated carefully.

Finally, FR7 is provided to flag invalid SPI word lengths. Valid word lengths are 24 bits, 32 bits, and integer multiples of 32 bits. Any other length causes FR7 to set, the $\overline{FAULT}$ pin to assert, and the instruction itself to be ignored.

Note that FR6 is unused in this device.

CONFIGURATION COMMAND

The configuration command has three arguments: OC, TS, and RD (see Figure 35).

Setting the OC bit disables open-circuit detection (FR0 to FR4), while the TS bit disables thermal protection (FR5). Set TS with caution because thermal damage can easily occur and is the responsibility of the user.

The RD bit is used to select external reference operation. The REFCOMP pin must be grounded for external reference use.

POWER-DOWN MODE

For power constrained applications, power-down mode can be used to reduce the supply current whenever less than five DAC outputs are needed. When in power-down, the voltage-to-current output drivers and reference buffers are disabled. The current DAC outputs are set to off mode. Register contents are not disturbed during power-down.

Any channel or combination of channels can be put into power-down mode by using Command 0100b in combination with the appropriate DAC address. In addition, all DAC channels and the integrated reference together can be put into power-down using the power-down chip command, 0101b. The 16-bit data word is ignored for all power-down commands.

Active operation resumes by executing any command that includes a DAC update, either in software, as shown in Table 8, or by toggling (see the Toggle Operations section). The selected DAC channel is powered up as it is updated with the new code value. When updating a powered-down DAC, add wait time to accommodate for the extra power-up delay. If the channels are powered down (Command 0100b) before the update command, the power-up delay time is 30 µs. If, alternatively, the chip is powered down (Command 0101b), the power-up delay time is 35 µs.

SAFE SUPPLY RANGES

The five output supplies (V_{DD0} to V_{DD4}) can be independently set between 2.1 V (2.4 V for the 300 mA range) and V_{CC}. In addition, the negative supply, V^-, can be set to any voltage between −5.5 V and GND. However, keep the total output supply voltage (V_{DDx} with respect to V^-) in the 2.85 V to 9.0 V range, as specified in Table 1 and shown in Figure 33.

A minimum of 2.85 V is needed to establish drive for the output P-type metal-oxide semiconductor (PMOS), while the 9.0 V maximum provides a margin of voltage stress tolerance for the output circuit.

Dropout performance is sensitive to the total output supply voltage. $V_{DROPOUT}$ falls to its minimum as (V_{DDx} − V^-) rises from 2.85 V to 4.75 V, and then stays essentially constant as the voltage further increases to 9.0 V. See the $V_{DROPOUT}$ specifications in Table 1 and Figure 17.

V_{CC} must be in the 2.85 V ≤ V_{CC} ≤ 5.5 V range and be greater than or equal to the V_{DD0} to V_{DD4} output supplies.

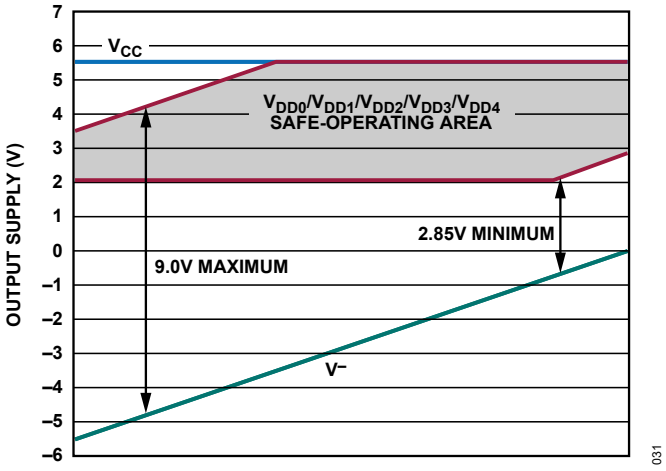


Figure 33. Output Supply Safe Operating Area

CURRENT OUTPUTS

The LTC2672 incorporates a high gain voltage to current converter at each current output pin. INL and DNL are guaranteed for all ranges from 3.125 mA to 300 mA if the minimum dropout voltage (V_{DDx} − V_{OUTx}) is met for all DAC codes.

If sufficient dropout voltage is maintained, the dc output impedances of the current outputs (OUT0 to OUT4) are high. Each current output has a dedicated positive supply pin, V_{DD0} to V_{DD4}, to allow the tailoring of the current compliance and power dissipation of each channel.

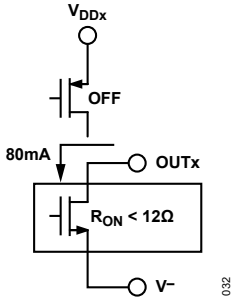


Figure 34. Switch to V⁻ Mode

THEORY OF OPERATION

Figure 35. Configuration Command Syntax, Open-Circuit (OC) Detection Disable, Thermal Shutdown (TS) Disable, and Reference Disable (RD)

SWITCH TO V⁻ MODE

Span Code 1000b can be used to pull outputs lower than GND. In switch to V^- mode, the output current is turned off for the addressed channel(s), and the channel voltage V_{OUTx} pulls to V^-. The pull-down switch can sink up to 80 mA at an effective resistance of 12 Ω maximum. Note that exceeding 80 mA can affect reliability and device lifetime. Switching to V^- mode can be invoked with a write span to all channels or a write span to the DAC Channel x command and the desired address. Span codes are shown in Table 10. A diagram of an output in switch to V^- mode is shown in Figure 34, where R_{ON} is the resistance when the NMOS transistor is conducting.

GAIN ADJUSTMENT USING THE FSADJ PIN

The full-scale output currents are proportional to the reference voltage and inversely proportional to the resistance associated with FSADJ, that is, $I_{OUTFS} \sim V_{REF}/R_{FSADJ}$.

If the FSADJ pin is tied to V_{CC}, the LTC2672 uses an internal $R_{FSADJ} \sim 20$ kΩ, trimmed to ensure optimal full-scale current error with no user intervention. Optionally, FSADJ can instead be connected to a grounded external resistor to tune the default current ranges to the application using an appropriately specified precision resistor. Values from 19 kΩ to 41 kΩ are supported. The new current ranges can be calculated using the external R_{FSADJ} column of Table 10. The internal resistor is automatically disconnected when using an external resistor.

When using an external resistor, the FSADJ pin is sensitive to stray capacitance. The FSADJ pin must be compensated with a snubber network consisting of a series combination of 1 kΩ and 1 µF connected in parallel to R_{FSADJ}. With the recommended compensation, the FSADJ pin is stable while driving stray capacitance of up to 50 pF.

OFFSET CURRENT AND CODE 0

The offset current error of the LTC2672 is guaranteed ±0.4 %FSR maximum. If the offset of a given channel is positive, some nonzero current flows at Code 0. If negative, the current is zero (leakage only) for a range of codes close to zero. Offset and linearity endpoints are measured at Code 384 for the LTC2672-16 and at Code 24 for the LTC2672-12, guaranteeing that the DAC operates with a measurable output current at the point of measurement.

A channel with a positive offset error may not completely turn off, even at Code 0. To turn an output completely off, set the span to off (Span Code 0000b from Table 10), and update the channel.

REFERENCE MODES

The LTC2672 can be used with either an internal or external reference. As with voltage DACs, the reference voltage scales the outputs so that the outputs reflect any errors in the reference. Full-scale output currents are limited to 300 mA maximum per channel, regardless of reference voltage.

The internal 1.25 V reference has a typical temperature drift of 3 ppm/°C (LFCSP) or 2.4 ppm/°C (WLCSP) and an initial output tolerance of ±2 mV maximum. The reference is trimmed, tested, and characterized independent of the DACs, and the DACs are tested and characterized with an ideal external reference.

To use the internal reference, leave the REFCOMP pin floating with no dc path to GND. In addition, the RD bit in the configuration register must have a value of 0. This value is reset to 0 at power-up and can be reset using the configuration command, 0111b. Figure 35 shows the command syntax.

For reference stability and low noise, tie a 0.1 µF capacitor between REFCOMP and GND. In this configuration, the internal reference can drive up to 0.1 µF with optimal stability. To ensure stable operation, the capacitive load on the REF pin must not exceed that on the REFCOMP pin. A buffer is needed if the internal reference will drive external circuitry.

To use an external reference, tie the REFCOMP pin to GND, which disables the output of the internal reference at startup so that the REF pin becomes a high impedance input. Apply the reference voltage at the REF pin after powering up. Set the RD bit to 1 using the configuration command, 0111b. The REF input voltage range is 1.225 V to 1.275 V.

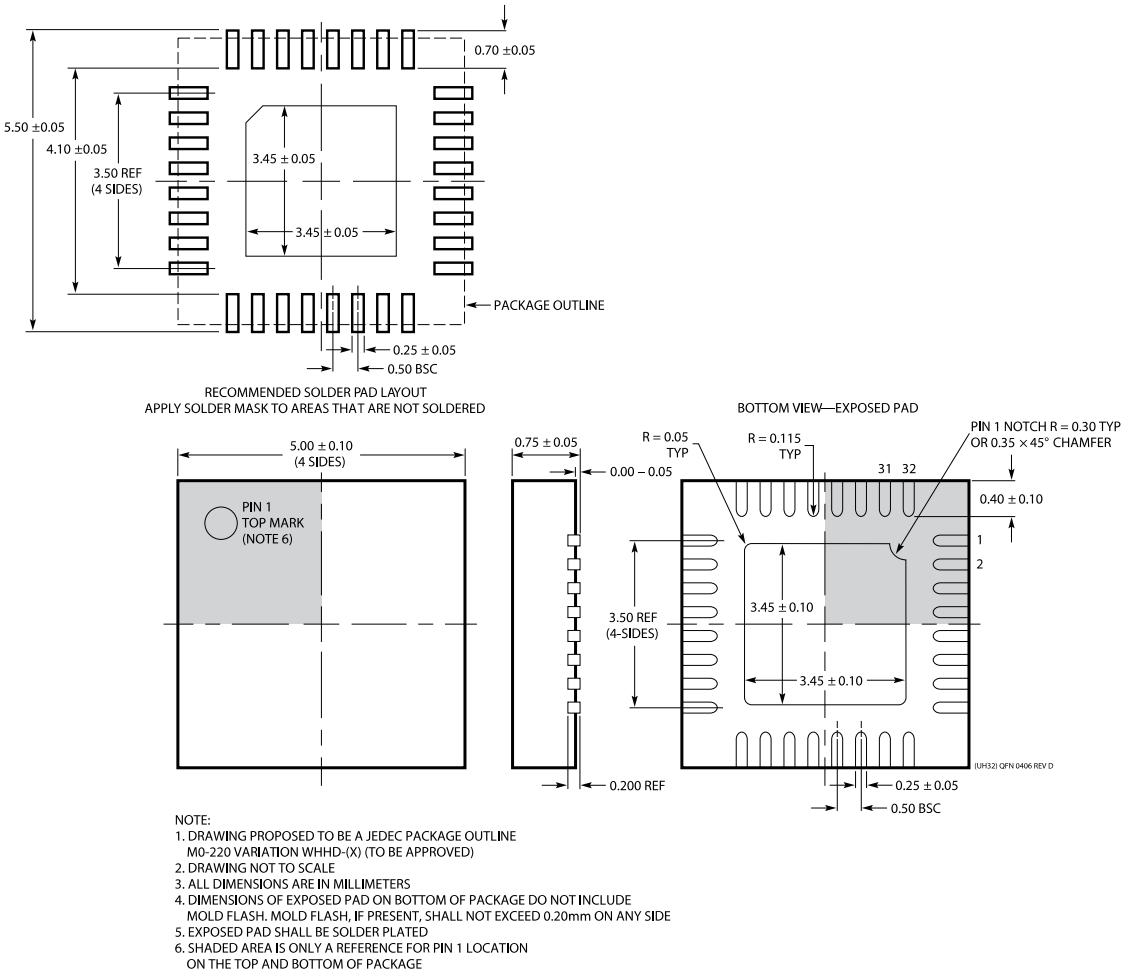
BOARD LAYOUT

The load regulation and dc crosstalk performance of the device is achieved in the device by minimizing the common-mode resistance of the signal and power grounds.

As with any high resolution converter, clean board grounding is important. A low impedance analog ground plane is necessary, as well as star grounding techniques. Keep the board layer used for star ground continuous to minimize ground resistances, that is, use the star ground concept without using separate star traces. Resistance from the REFLO pin to the star point must be as low as possible. The GND pin is recommended as the star ground point.

For optimal performance, stitch the ground plane with arrays of vias on 150 mil to 200 mil centers to connect the plane with the ground pours from the other board layers, which reduces the overall ground resistance and minimizes ground loop area.

OUTLINE DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

Figure 36. 32-Lead Plastic QFN
5 mm × 5 mm Body
(Reference LTC DWG # 05-08-1693 Rev. D)

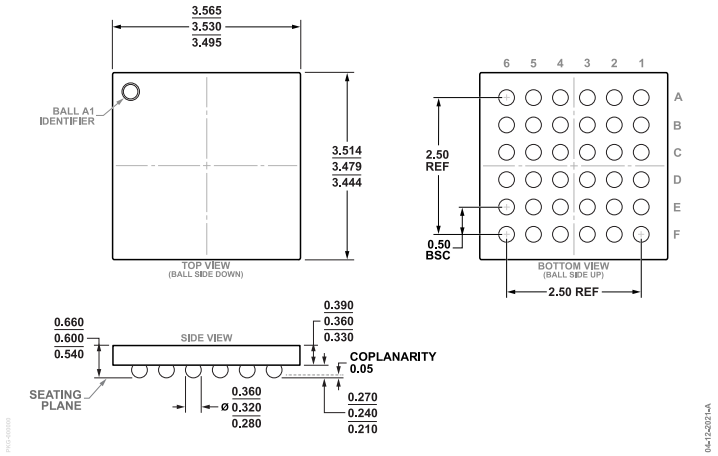


Figure 37. 36-Ball Wafer Level Chip Scale Package
[WLCSP]
(Dimensions shown in millimeters)

OUTLINE DIMENSIONS

Updated: January 11, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
LTC2672CUH-12#PBF	0°C to +70°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)		05-08-1693
LTC2672CUH-12#TRPBF	0°C to +70°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1693
LTC2672CUH-16#PBF	0°C to +70°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)		05-08-1693
LTC2672CUH-16#TRPBF	0°C to +70°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1693
LTC2672HCB-16#TRPBF	-40°C to +125°C	CHIPS W/SOLDER BUMPS/WLCSP	Reel, 1500	CB-36-9
LTC2672HUH-12#PBF	-40°C to +125°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)		05-08-1693
LTC2672HUH-12#TRPBF	-40°C to +125°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1693
LTC2672HUH-16#PBF	-40°C to +125°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)		05-08-1693
LTC2672HUH-16#TRPBF	-40°C to +125°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1693
LTC2672IUH-12#PBF	-40°C to +85°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)		05-08-1693
LTC2672IUH-12#TRPBF	-40°C to +85°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1693
LTC2672IUH-16#PBF	-40°C to +85°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)		05-08-1693
LTC2672IUH-16#TRPBF	-40°C to +85°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1693
LTC2672HCB-12#TRPBF	-40°C to +125°C	36-Ball CHIPS W/SOLDER BUMPS/WLCSP	Reel, 1500	CB-36-9

[1] All models are RoHS compliant.

EVALUATION BOARDS

Model	Description
DC2903A-A	LTC2672-16 LFCSP Evaluation Board
DC2903A-B	LTC2672-12 LFCSP Evaluation Board