2-Channel, 12-Bit ADCs with I²C Compatible Interface

FEATURES

- **12-Bit Resolution**
- **Low Power: 1.5mW at 1ksps, 35µW Sleep Mode**
- **14ksps Throughput Rate**
- **Internal Reference**
- **Low Noise: SNR = 73.5dB**
- Guaranteed No Missing Codes
- Single 5V Supply
- 2-wire I²C Compatible Serial Interface with 9 Addresses Plus One Global for Synchronization
- Fast Conversion Time: 1.3µs
- 1-Channel (LTC2301) and 2-Channel (LTC2305) Versions
- Unipolar or Bipolar Input Ranges (Software Selectable)
- Internal Conversion Clock
- Guaranteed Operation from –40°C to 125°C (MSOP Package)
- 12-Pin 4mm × 3mm DFN and 12-Pin MSOP Packages

APPLICATIONS

- Industrial Process Control
- Motor Control
- Accelerometer Measurements
- Battery Operated Instruments
- Isolated and/or Remote Data Acquisition
- Power Supply Monitoring

DESCRIPTION

The LTC®2301/LTC2305 are low noise, low power, 1-/2-channel, 12-bit successive approximation ADCs with an I²C compatible serial interface. These ADCs include an internal reference and a fully differential sample-and-hold circuit to reduce common mode noise. The LTC2301/LTC2305 operate from an internal clock to achieve a fast 1.3µs conversion time.

The LTC2301/LTC2305 operate from a single 5V supply and draw just 300µA at a throughput rate of 1ksps. The ADC enters nap mode when not converting, reducing the power dissipation.

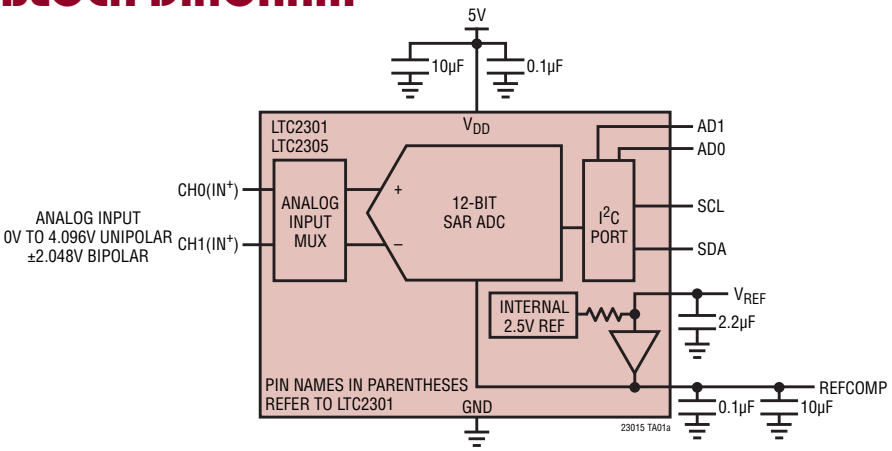
The LTC2301/LTC2305 are available in small 12-pin 4mm × 3mm DFN and 12-pin MSOP packages. The internal 2.5V reference further reduces PCB board space requirements.

The low power consumption and small size make the LTC2301/LTC2305 ideal for battery operated and portable applications, while the 2-wire I²C compatible serial interface makes these ADCs a good match for space-constrained systems.

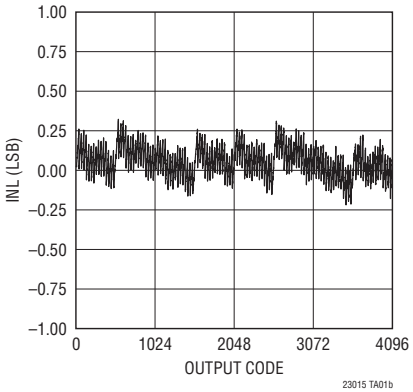
12-Bit I²C ADC Family

Input Channels	1	2	8
Part Number	LTC2301	LTC2305	LTC2309

BLOCK DIAGRAM



Integral Nonlinearity vs Output Code (LTC2305)

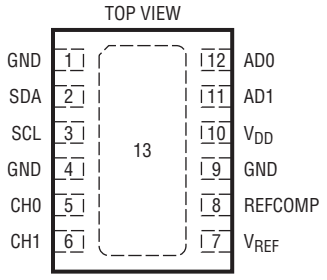


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{DD}) ..... –0.3V to 6.0V
Analog Input Voltage (Note 3)
CH0(IN^+), CH1(IN^-),
REF, REFCOMP .....(GND – 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage.....(GND – 0.3V) to (V_{DD} + 0.3V)
Digital Output Voltage .....(GND – 0.3V) to (V_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
LTC2301C/LTC2305C ..... 0°C to 70°C
LTC2301I/LTC2305I.....–40°C to 85°C
LTC2301H/LTC2305H (Note 13).....–40°C to 125°C
Storage Temperature Range..... –65°C to 150°C

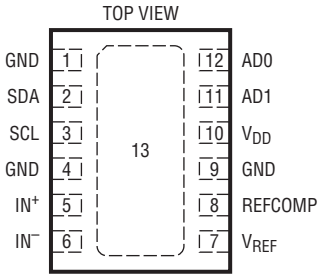
PIN CONFIGURATION

LTC2305



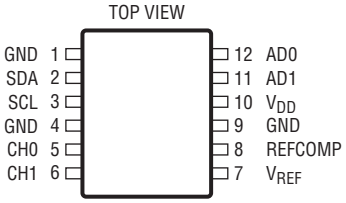
DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

LTC2301



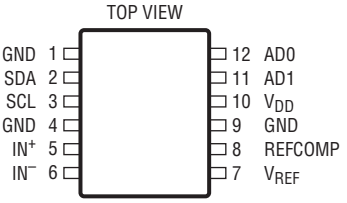
DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

LTC2305



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

LTC2301



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2301CDE#PBF	LTC2301CDE#TRPBF	2301	12-Lead (3mm × 4mm) Plastic DFN	0°C to 70°C
LTC2301IDE#PBF	LTC2301IDE#TRPBF	2301	12-Lead (3mm × 4mm) Plastic DFN	–40°C to 85°C
LTC2305CDE#PBF	LTC2305CDE#TRPBF	2305	12-Lead (3mm × 4mm) Plastic DFN	0°C to 70°C
LTC2305IDE#PBF	LTC2305IDE#TRPBF	2305	12-Lead (3mm × 4mm) Plastic DFN	–40°C to 85°C
LTC2301CMS#PBF	LTC2301CMS#TRPBF	2301	12-Lead Plastic MSOP	0°C to 70°C
LTC2301IMS#PBF	LTC2301IMS#TRPBF	2301	12-Lead Plastic MSOP	–40°C to 85°C
LTC2301HMS#PBF	LTC2301HMS#TRPBF	2301	12-Lead Plastic MSOP	–40°C to 125°C
LTC2305CMS#PBF	LTC2305CMS#TRPBF	2305	12-Lead Plastic MSOP	0°C to 70°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2305IMS#PBF	LTC2305IMS#TRPBF	2305	12-Lead Plastic MSOP	–40°C to 85°C
LTC2305HMS#PBF	LTC2305HMS#TRPBF	2305	12-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 5)	●		±0.4	±1	LSB
Differential Linearity Error		●		±0.3	±1	LSB
Bipolar Zero Error	(Note 6)	●		±0.5	±8	LSB
Bipolar Zero Error Drift				0.002		LSB/°C
Unipolar Zero Error	(Note 6)	●		±0.7	±6	LSB
Unipolar Zero Error Drift				0.002		LSB/°C
Unipolar Zero Error Match (LTC2305)				±0.1	±1	LSB
Bipolar Full-Scale Error	External Reference (Note 7) REFCOMP = 4.096V (Note 7)	● ●		±1 ±0.9	±10 ±9	LSB LSB
Bipolar Full-Scale Error Drift	External Reference			0.05		LSB/°C
Unipolar Full-Scale Error	External Reference (Note 7) REFCOMP = 4.096V (Note 7)	● ●		±0.5 ±0.7	±10 ±6	LSB LSB
Unipolar Full-Scale Error Drift	External Reference			0.05		LSB/°C
Unipolar Full-Scale Error Match (LTC2305)				±0.1	±2	LSB

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN}+$	Absolute Input Range (CH0, CH1, IN^+)	(Note 8)	●	–0.05		REFCOMP	V
$V_{IN}–$	Absolute Input Range (CH0, CH1, $IN^–$)	Unipolar (Note 8) Bipolar (Note 8)	●	–0.05 –0.05		0.25 • REFCOMP 0.75 • REFCOMP	V V
$V_{IN}+ – V_{IN}–$	Input Differential Voltage Range	$V_{IN} = V_{IN}+ – V_{IN}–$ (Unipolar) $V_{IN} = V_{IN}+ – V_{IN}–$ (Bipolar)	●		0 to REFCOMP ±REFCOMP/2		V V
I_{IN}	Analog Input Leakage Current		●			±1	µA
C_{IN}	Analog Input Capacitance	Sample Mode Hold Mode			55 5		pF pF
CMRR	Input Common Mode Rejection Ratio				70		dB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS. (Notes 4,9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 1kHz	●	71	73.4		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 1kHz	●	71	73.5		dB
THD	Total Harmonic Distortion	f_{IN} = 1kHz	●		–91	–77	dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 1kHz, First 5 Harmonics	●	79	92		dB
	Channel-to-Channel Isolation	f_{IN} = 1kHz			–109		dB
	Full Linear Bandwidth	f_{IN} = 1kHz			700		kHz
	–3dB Input Linear Bandwidth	(Note 10)			25		MHz
	Aperture Delay				13		ns
	Transient Response	Full-Scale Step			240		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0	●	2.46	2.50	2.54	V
V_{REF} Output Tempco	I_{OUT} = 0			±25		ppm/°C
V_{REF} Output Impedance	–0.1mA ≤ I_{OUT} ≤ 0.1mA			8		kΩ
$V_{REFCOMP}$ Output Voltage	I_{OUT} = 0			4.096		V
V_{REF} Line Regulation	V_{DD} = 4.75V to 5.25V			0.8		mV/V

I²C INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	2.85			V
V_{IL}	Low Level Input Voltage		●			1.5	V
V_{IHA}	High Level Input Voltage for Address Pins A1, A0		●	4.75			V
V_{ILA}	Low Level Input Voltage for Address Pins A1, A0		●			0.25	V
R_{INH}	Resistance from A1, A0 to V_{DD} to Set Chip Address Bit to 1		●			10	kΩ
R_{INL}	Resistance from A1, A0 to GND to Set Chip Address Bit to 0		●			10	kΩ
R_{INF}	Resistance from A1, A0 to GND or V_{DD} to Set Chip Address Bit to Float		●	2			MΩ
I_I	Digital Input Current	V_{IN} = V_{DD}	●	–10		10	µA
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	(Note 8)	●	0.25			V
V_{OL}	Low Level Output Voltage (SDA)	I = 3mA	●			0.4	V
t_{OF}	Output Fall Time $V_{IN(MIN)}$ to $V_{IL(MAX)}$	Bus Load C_B 10pF to 400pF (Note 11)	●	20 + 0.1C_B		250	ns
t_{SP}	Input Spike Suppression		●			50	ns
C_{CAX}	External Capacitance Load on Chip Address Pins (A1, A0) for Valid Float		●			10	pF

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	4.75	5	5.25	V
I_{DD}	Supply Current Nap Mode Sleep Mode	14ksps Sample Rate SLP Bit = 0, Conversion Done SLP Bit = 1, Conversion Done	● ● ●		2.3 225 7	3.5 400 15	mA µA µA
P_D	Power Dissipation Nap Mode Sleep Mode	14ksps Sample Rate SLP Bit = 0, Conversion Done SLP Bit = 1, Conversion Done	● ● ●		11.5 1.125 35	17.5 2 75	mW mW µW

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●			400	kHz
$t_{HD(SDA)}$	Hold Time (Repeated) START Condition		●	0.6			µs
t_{LOW}	LOW Period of the SCL Pin		●	1.3			µs
t_{HIGH}	HIGH Period of the SCL Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated START Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for SDA/SCL Signals	(Note 11)	●	$20 + 0.1C_B$		300	ns
t_f	Fall Time for SDA/SCL Signals	(Note 11)	●	$20 + 0.1C_B$		300	ns
$t_{SU(STO)}$	Set-Up Time for STOP Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a Second START Condition		●	1.3			µs

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Throughput Rate (Successive Reads)		●			14	ksps
t_{CONV}	Conversion Time		●		1.3	1.6	µs
t_{ACQ}	Acquisition Time	(Note 8)	●			240	ns
$t_{REFWAKE}$	REFCOMP Wakeup Time (Note 12)	$C_{REFCOMP}$ = 10µF, C_{REF} = 2.2µF			200		ms

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground or above V_{DD}, they will be clamped by internal diodes. These products can handle input currents greater than 100mA below ground or above V_{DD} without latchup.

Note 4: V_{DD} = 5V, f_{SMPL} = 14kHz, internal reference unless otherwise noted.

Note 5: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Bipolar zero error is the offset voltage measured from –0.5 LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111. Unipolar zero error is the offset voltage measured from 0.5 LSB when the output code flickers between 0000 0000 0000 and 0000 0000 0001.

Note 7: Full-scale bipolar error is the worst-case of –FS or FS untrimmed deviation from ideal first and last code transitions and includes the effect of offset error. Unipolar full-scale error is the deviation of the last code transition from ideal and includes the effect of offset error.

Note 8: Guaranteed by design, not subject to test.

Note 9: All specifications in dB are referred to a full-scale ±2.048V input with a 2.5V reference voltage.

Note 10: Full linear bandwidth is defined as the full-scale input frequency at which the SINAD degrades to 60dB or 10 bits of accuracy.

Note 11: C_B = capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF)

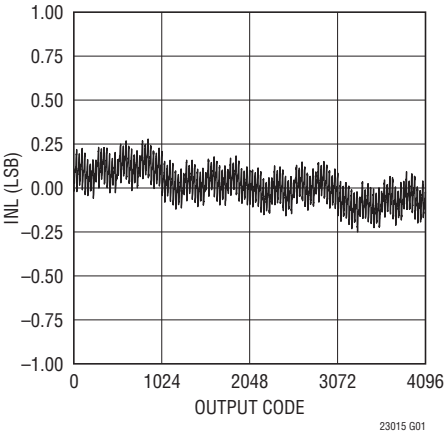
Note 12: REFCOMP wakeup time is the time required for the REFCOMP pin to settle within 0.5 LSB at 12-bit resolution of its final value after waking up from sleep mode.

Note 13: High temperatures degrade operating lifetimes. Operating lifetime is derated at temperatures greater than 105°C.

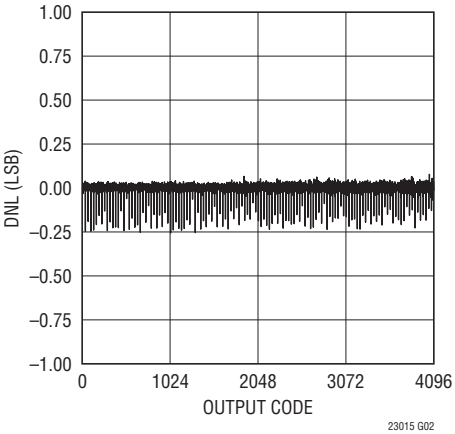
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC2301) T_A = 25°C, V_{DD} = 5V, f_{SMPL} = 14ksps, unless otherwise noted.

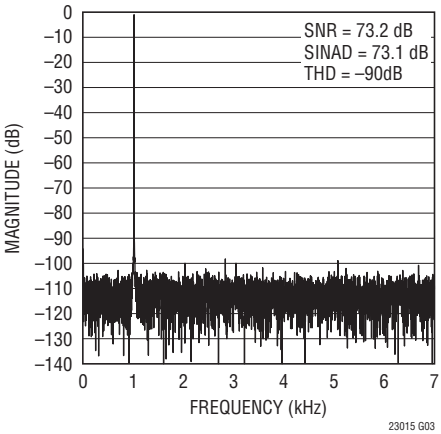
Integral Nonlinearity vs Output Code



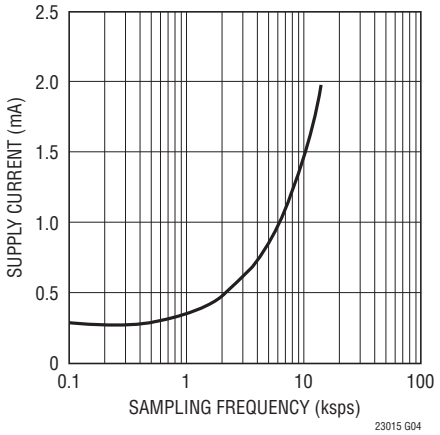
Differential Nonlinearity vs Output Code



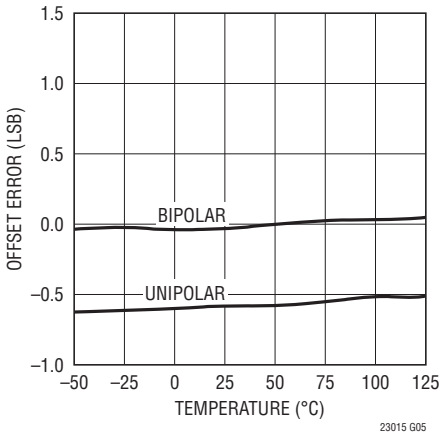
1kHz Sine Wave 8192 Point FFT Plot



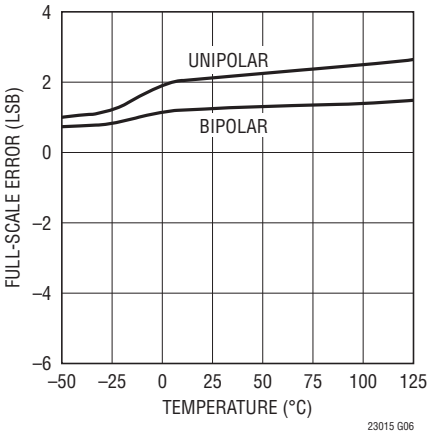
Supply Current vs Sampling Frequency



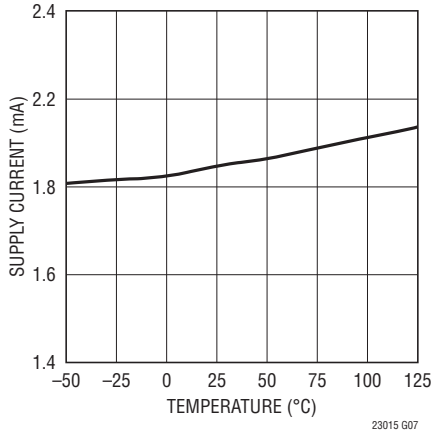
Offset Error vs Temperature



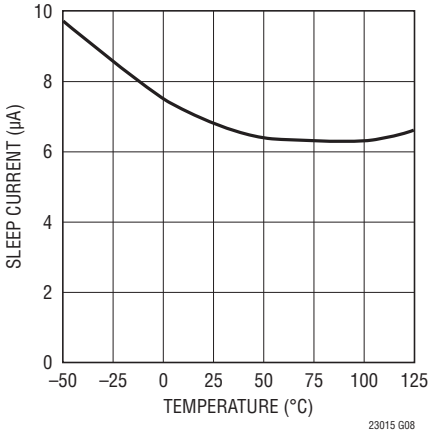
Full-Scale Error vs Temperature



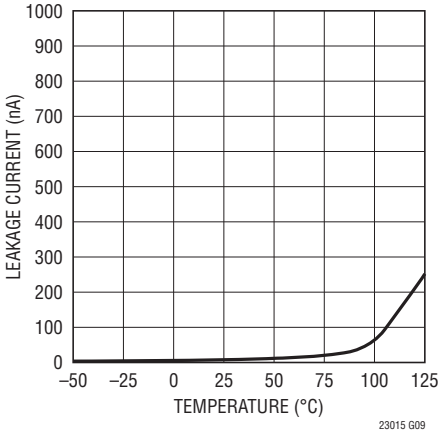
Supply Current vs Temperature



Sleep Current vs Temperature



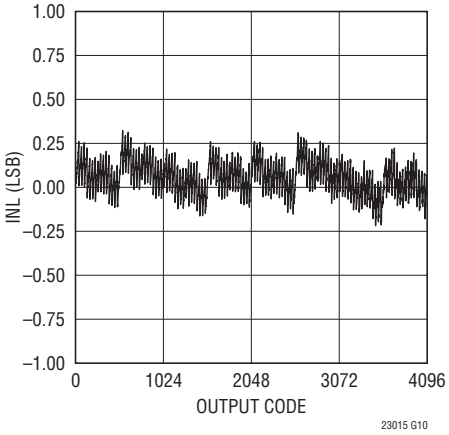
Analog Input Leakage Current vs Temperature



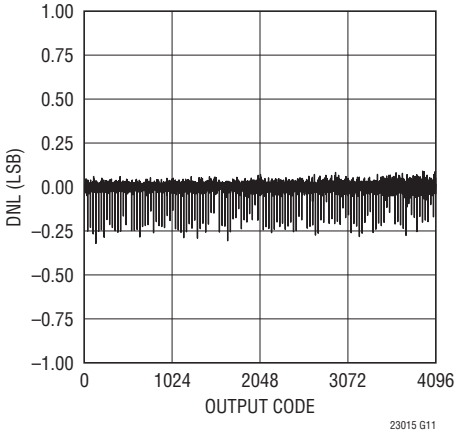
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC2305) T_A = 25°C, V_{DD} = 5V, f_{SMPL} = 14ksps, unless otherwise noted.

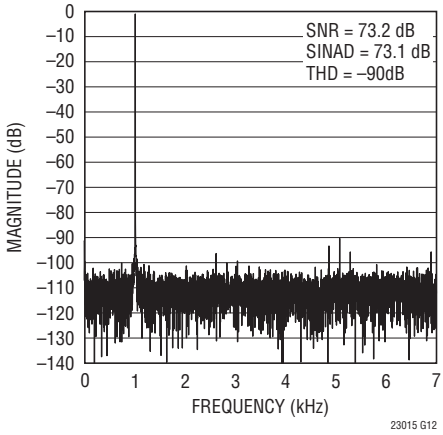
Integral Nonlinearity vs Output Code



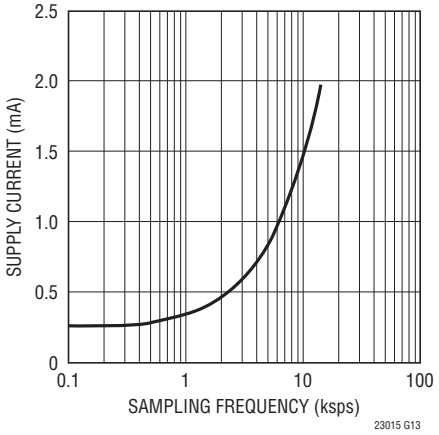
Differential Nonlinearity vs Output Code



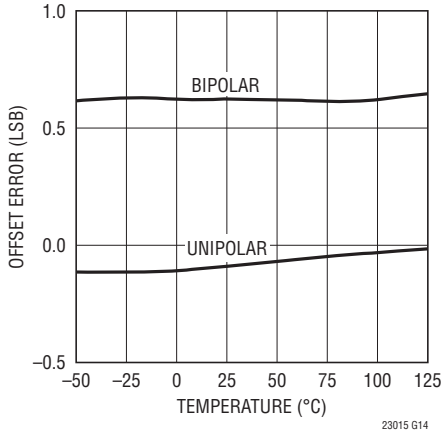
1kHz Sine Wave 8192 Point FFT Plot



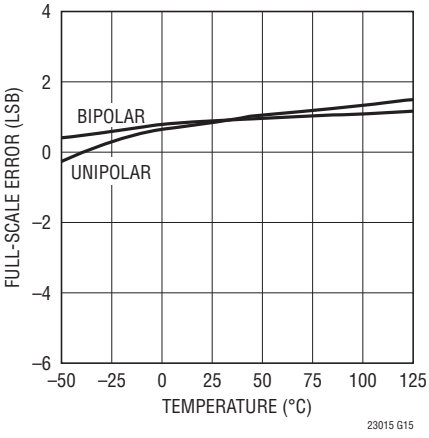
Supply Current vs Sampling Frequency



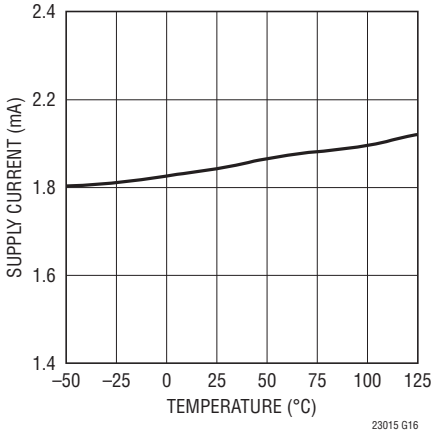
Offset Error vs Temperature



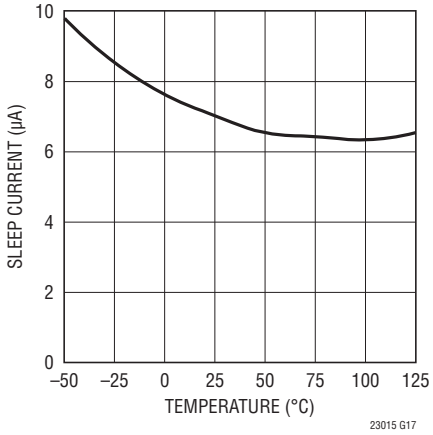
Full-Scale Error vs Temperature



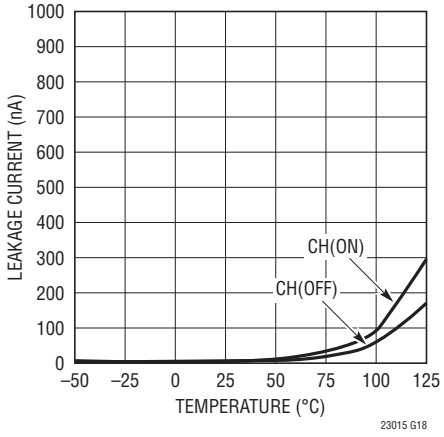
Supply Current vs Temperature



Sleep Current vs Temperature



Analog Input Leakage Current vs Temperature



PIN FUNCTIONS

(LTC2301)

GND (Pins 1, 4, 9): Ground. All GND pins must be connected to a solid ground plane.

SDA (Pin 2): Bidirectional Serial Data Line of the I^2C Interface. In transmitter mode (read), the conversion result is output at the SDA pin, while in receiver mode (write), the D_{IN} word is input at the SDA pin to configure the ADC. The pin is high impedance during the data input mode and is an open drain output (requires an appropriate pull-up device to V_{DD}) during the data output mode.

SCL (Pin 3): Serial Clock Pin of the I^2C Interface. The LTC2301 can only act as a slave and the SCL pin only accepts an external serial clock. Data is shifted into the SDA pin on the rising edges of the SCL clock and output through the SDA pin on the falling edges of the SCL clock.

IN^+, IN^- (Pins 5, 6): Positive (IN^+) and negative (IN^-) differential analog inputs.

V_{REF} (Pin 7): 2.5V Reference Output. Bypass to GND with a minimum 2.2µF ceramic capacitor. The internal reference may be overdriven by an external 2.5V reference at this pin.

REFCOMP (Pin 8): Reference Buffer Output. Bypass to GND with 10µF and 0.1µF ceramic capacitors in parallel. Nominal output voltage is 4.096V. The internal reference buffer driving this pin is disabled by grounding V_{REF}, allowing REFCOMP to be overdriven by an external source (see Figure 5c).

V_{DD} (Pin 10): 5V Analog Supply. The range of V_{DD} is 4.75V to 5.25V. Bypass V_{DD} to GND with 10µF and 0.1µF ceramic capacitors in parallel.

AD1 (Pin 11): Chip Address Control Pin. This pin is configured as a three-state (LOW, HIGH, floating) address control bit for the device I^2C address. See Table 2 for address selection.

AD0 (Pin 12): Chip Address Control Pin. This pin is configured as a three-state (LOW, HIGH, floating) address control bit for the device I^2C address. See Table 2 for address selection.

GND (Pin 13 – DFN Package Only): Exposed Pad Ground. Must be soldered directly to ground plane.

PIN FUNCTIONS

(LTC2305)

GND (Pins 1, 4, 9): Ground. All GND pins must be connected to a solid ground plane.

SDA (Pin 2): Bidirectional Serial Data Line of the I^2C Interface. In transmitter mode (read), the conversion result is output at the SDA pin, while in receiver mode (write), the D_{IN} word is input at the SDA pin to configure the ADC. The pin is high impedance during the data input mode and is an open drain output (requires an appropriate pull-up device to V_{DD}) during the data output mode.

SCL (Pin 3): Serial Clock Pin of the I^2C Interface. The LTC2305 can only act as a slave and the SCL pin only accepts an external serial clock. Data is shifted into the SDA pin on the rising edges of the SCL clock and output through the SDA pin on the falling edges of the SCL clock.

CH0-CH1 (Pins 5, 6): Channel 0 and Channel 1 Analog Inputs. CH0 and CH1 can be configured as single-ended or differential input channels. See the Analog Input Multiplexer section.

V_{REF} (Pin 7): 2.5V Reference Output. Bypass to GND with a minimum 2.2µF ceramic capacitor. The internal reference may be overdriven by an external 2.5V reference at this pin.

REFCOMP (Pin 8): Reference Buffer Output. Bypass to GND with 10µF and 0.1µF ceramic capacitors in parallel. Nominal output voltage is 4.096V. The internal reference buffer driving this pin is disabled by grounding V_{REF}, allowing REFCOMP to be overdriven by an external source (see Figure 5c).

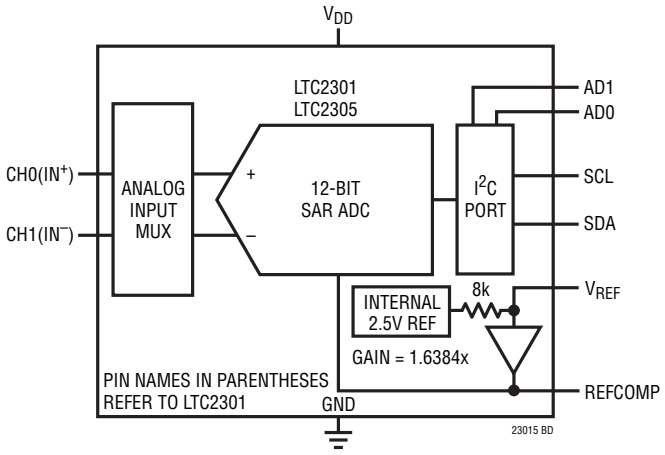
V_{DD} (Pin 10): 5V Analog Supply. The range of V_{DD} is 4.75V to 5.25V. Bypass V_{DD} to GND with 10µF and 0.1µF ceramic capacitors in parallel.

AD1 (Pin 11): Chip Address Control Pin. This pin is configured as a three-state (LOW, HIGH, floating) address control bit for the device I^2C address. See Table 2 for address selection.

AD0 (Pin 12): Chip Address Control Pin. This pin is configured as a three-state (LOW, HIGH, floating) address control bit for the device I^2C address. See Table 2 for address selection.

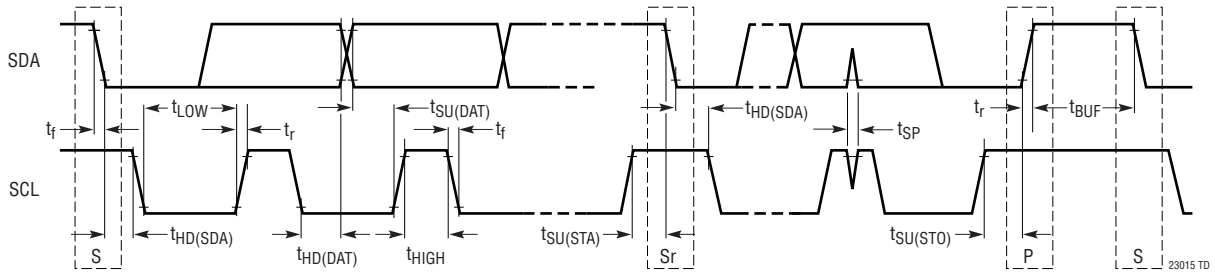
GND (Pin 13 – DFN Package Only): Exposed Pad Ground. Must be soldered directly to ground plane.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM

Definition of Timing for Fast/Standard Mode Devices on the I²C Bus



S = START, Sr = REPEATED START, P = STOP

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Overview

The LTC2301/LTC2305 are low noise, 1-/2-channel, 12-bit successive approximation register (SAR) A/D converters with an I^2C compatible serial interface. The LTC2301/LTC2305 both include a precision internal reference. The LTC2305 includes a 2-channel analog input multiplexer (MUX) while the LTC2301 includes an input MUX that allows the polarity of the differential input to be selected. These ADCs can operate in either unipolar or bipolar mode. Unipolar mode should be used for single-ended operation with the LTC2305, since single-ended input signals are always referenced to GND. A sleep mode option is also provided to further reduce power during inactive periods.

The LTC2301/LTC2305 communicate through a 2-wire I^2C compatible serial interface. Conversions are initiated by signaling a STOP condition after the part has been successfully addressed for a read/write operation. The device will not acknowledge an external request until the conversion is finished. After a conversion is finished, the device is ready to accept a read/write request. Once the LTC2301/LTC2305 is addressed for a read operation, the device begins outputting the conversion result under the control of the serial clock (SCL). There is no latency in the conversion result. There are 12 bits of output data followed by four trailing zeros. Data is updated on the falling edges of SCL, allowing the user to reliably latch data on the rising edge of SCL. A write operation may follow the read operation by using a repeat START or a STOP condition may be given to start a new conversion. By selecting a write operation, these ADCs can be programmed by a 6-bit D_{IN} word. The D_{IN} word configures the MUX and programs various modes of operation.

During a conversion, the internal 12-bit capacitive charge-redistribution DAC output is sequenced through a successive approximation algorithm by the SAR starting from the most significant bit (MSB) to the least significant bit (LSB). The sampled input is successively compared with binary weighted charges supplied by the capacitive DAC using a differential comparator. At the end of a conversion, the DAC output balances the analog input. The SAR contents (a 12-bit data word) that represent the sampled analog input are loaded into 12 output latches that allow the data to be shifted out via the I^2C interface.

Programming the LTC2301 and LTC2305

The software compatible LTC2301/LTC2305/LTC2309 family features a 6-bit D_{IN} word to program various modes of operation. Don't care bits (X) are ignored. The SDA data bits are loaded on the rising edge of SCL during a write operation, with the S/D bit loaded on the first rising edge and the SLP bit on the sixth rising edge (see Figure 7b in the I^2C Interface section). The input data word for the LTC2305 is defined as follows:

S/D	O/S	X	X	UNI	SLP

S/D = SINGLE-ENDED/$\overline{\text{DIFFERENTIAL}}$ BIT

O/S = ODD/$\overline{\text{SIGN}}$ BIT

UNI = UNIPOLAR/$\overline{\text{BIPOLAR}}$ BIT

SLP = SLEEP MODE BIT

For the LTC2301, the input word is defined as:

X	O/S	X	X	UNI	SLP

Analog Input Multiplexer

The analog input MUX is programmed by the S/D and O/S bits of the D_{IN} word for the LTC2305 and the O/S bit of the D_{IN} word for the LTC2301. Table 1 and Table 2 list the MUX configurations for all combinations of the configuration bits. Figure 1a shows several possible MUX configurations and Figure 1b shows how the MUX can be reconfigured from one conversion to the next.

Table 1. Channel Configuration for the LTC2305

S/D	O/S	CH0	CH1
0	0	+	–
0	1	–	+
1	0	+	
1	1		+

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Table 2. Channel Configuration for the LTC2301

O/S	IN+	IN–
0	+	–
1	–	+

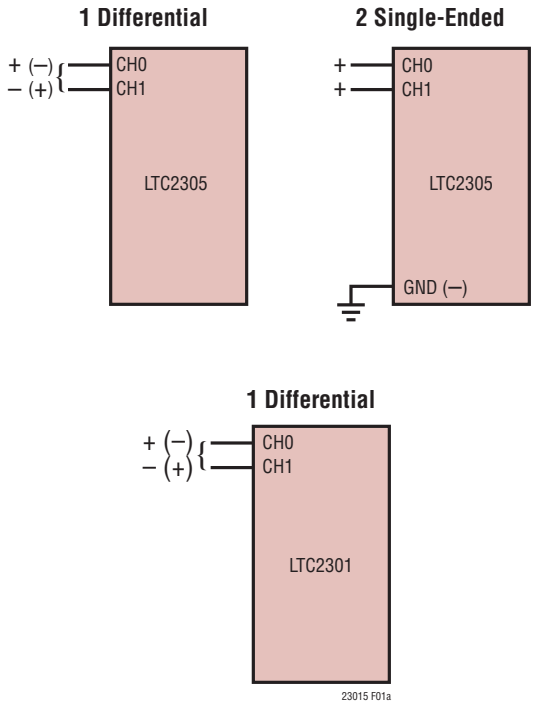

Figure 1a. Example MUX Configurations

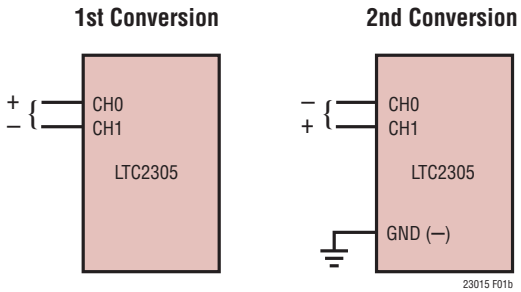

Figure 1b. Changing the MUX Assignment "On the Fly"

Driving the Analog Inputs

The analog inputs of the LTC2301/LTC2305 are easy to drive. Each of the analog inputs of the LTC2305 (CH0 and CH1) can be used as single-ended input relative to GND or as a differential pair. The analog inputs of the LTC2301 (IN^+, $IN^–$) are always configured as a differential pair. Regardless of the MUX configuration, the "+" and "–" inputs are sampled at the same instant. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors during the acquire mode. In conversion mode, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, the ADC inputs can be driven directly. Otherwise, more acquisition time should be allowed for a source with higher impedance.

Input Filtering

The noise and distortion of the input amplifier and other circuitry must be considered since they will add to the ADC noise and distortion. Therefore, noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications.

The analog inputs of the LTC2301/LTC2305 can be modeled as a 55pF capacitor (C_{IN}) in series with a 100Ω resistor (R_{ON}), as shown in Figure 2a. C_{IN} gets switched to the selected input once during each conversion. Large filter RC time constants will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle to 12-bit resolution within the acquisition time (t_{ACQ}) if DC accuracy is important.

When using a filter with a large C_{FILTER} value (e.g. 1µF), the inputs do not completely settle and the capacitive input switching currents are averaged into a net DC current (I_{DC}). In this case, the analog input can be modeled by an equivalent resistance ($R_{EQ} = 1/(f_{SMPL} \bullet C_{IN})$) in series with an ideal voltage source ($V_{REFCOMP}/2$), as shown in Figure 2b.

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The magnitude of the DC current is then approximately $I_{DC} = (V_{IN} - V_{REFCOMP}/2)/R_{EQ}$, which is roughly proportional to V_{IN}. To prevent large DC drops across the resistor R_{FILTER}, a filter with a small resistor and large capacitor should be chosen. When running at the maximum throughput rate of 14ksps, the input current equals 1.5µA at V_{IN} = 4.096V, which amounts to a full-scale error of 0.5 LSBs when using a filter resistor (R_{FILTER}) of 333Ω. Applications requiring lower sample rates can tolerate a larger filter resistor for the same amount of full-scale error.

Figures 3a and 3b show respective examples of input filtering for single-ended and differential inputs. For the single-ended case in Figure 4a, a 50Ω source resistor and a 2000pF capacitor to ground on the input will limit the input bandwidth to 1.6MHz. High quality capacitors and resistors should be used in the RC filter since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Dynamic Performance

Fast Fourier Transform (FFT) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band-limited to frequencies from above DC and below half the sampling

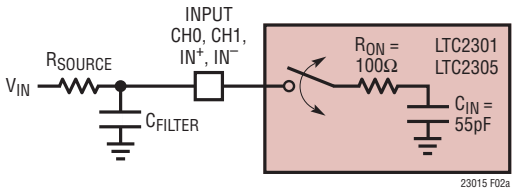

Figure 2a. Analog Input Equivalent Circuit

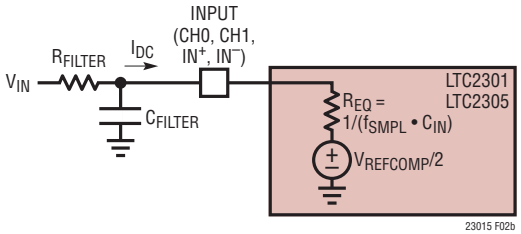

Figure 2b. Analog Input Equivalent Circuit for Large Filter Capacitances

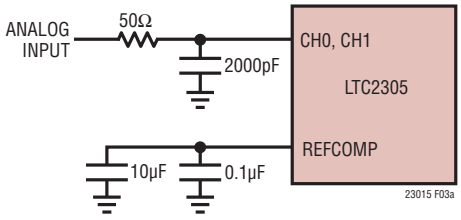

Figure 3a. Optional RC Input Filtering for Single-Ended Input

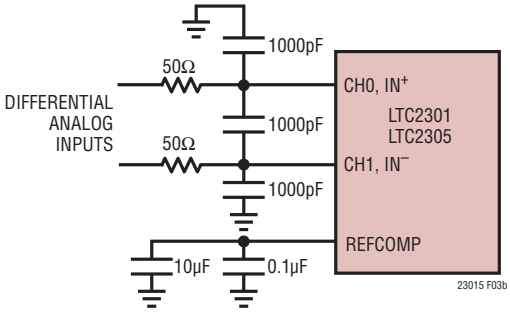

Figure 3b. Optional RC Input Filtering for Differential Inputs

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frequency. Figure 4 shows a typical SINAD of 73.2dB with a 14kHz sampling rate and a 1kHz input. A SNR of 73.3dB can be achieved with the LTC2301/LTC2305.

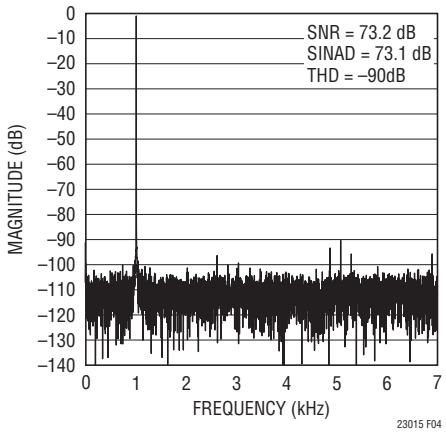

Figure 4. 1kHz Sine Wave 8192 Point FFT Plot

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\sqrt{\frac{V_2^2 + V_3^2 + V_4^2 ... + V_N^2}{V_1}}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through V_N are the amplitudes of the second through Nth harmonics.

Internal Reference

The LTC2301/LTC2305 have an on-chip, temperature compensated bandgap reference that is factory trimmed to 2.5V (Refer to Figure 5a). It is internally connected to a reference amplifier and is available at V_{REF} (Pin 7). V_{REF} should be bypassed to GND with a 2.2µF ceramic capacitor to minimize noise. An 8k resistor is in series with the output so that it can be easily overdriven by an external reference if more accuracy and/or lower drift are required, as shown in Figure 5b. The reference amplifier gains the V_{REF} voltage by 1.638 to 4.096V at REFCOMP. To compensate the reference amplifier, bypass REFCOMP with a 10µF ceramic capacitor in parallel with a 0.1µF ceramic capacitor for best noise performance. The internal reference buffer can also be overdriven from 1V to V_{DD} with an external reference at REFCOMP, as shown in Figure 5c. To do so, V_{REF} must be grounded to disable the reference buffer. This will result in an input range of 0V to $V_{REFCOMP}$ in unipolar mode and $\pm 0.5 \bullet V_{REFCOMP}$ in bipolar mode.

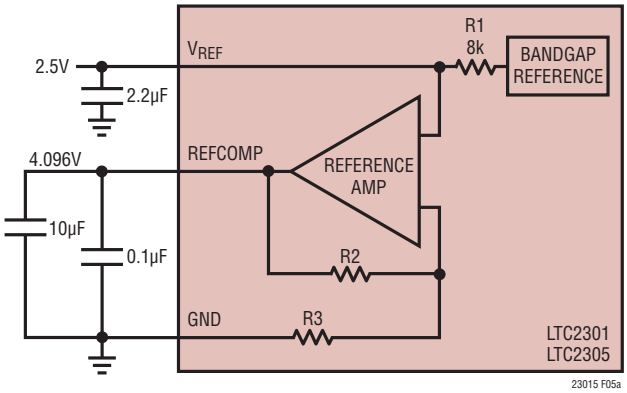

Figure 5a. LTC2301/LTC2305 Reference Circuit

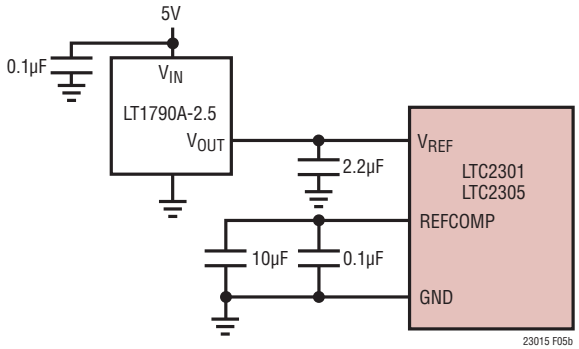

Figure 5b. Using the LT1790A-2.5 as an External Reference

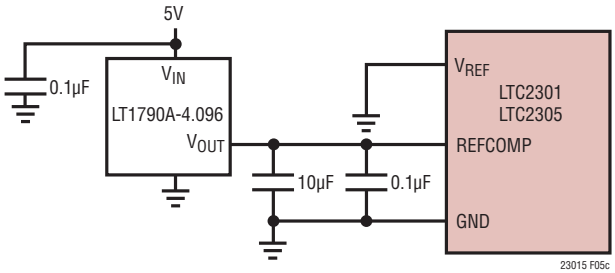

Figure 5c. Overdriving REFCOMP Using the LT1790A-4.096

APPLICATIONS INFORMATION

Internal Conversion Clock

The internal conversion clock is factory trimmed to achieve a typical conversion time (t_{CONV}) of 1.3µs and a maximum conversion time of 1.6µs over the full operating temperature range.

I²C Interface

The LTC2301/LTC2305 communicate through an I²C interface. The I²C interface is a 2-wire open-drain interface supporting multiple devices and multiple masters on a single bus. The connected devices can only pull the serial data line (SDA) LOW and can never drive it HIGH. SDA is required to be externally connected to the supply through a pull-up resistor. When the data line is not being driven low, it is HIGH. Data on the I²C bus can be transferred at rates up to 100kbits/s in the standard mode and up to 400kbits/s in the fast mode.

The V_{DD} power should not be removed from the LTC2301/LTC2305 when the I²C bus is active to avoid loading the I²C bus lines through the internal ESD protection diodes.

Each device on the I²C bus is recognized by a unique address stored in the device and can only operate either as a transmitter or receiver, depending on the function of the device. A device can also be considered as a master or a slave when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit the transfer. Devices addressed by the master are considered slaves.

The LTC2301/LTC2305 can only be addressed as slaves. Once addressed, they can receive configuration bits (D_{IN} word) or transmit the last conversion result. The serial clock line (SCL) is always an input to the LTC2301/LTC2305 and the serial data line (SDA) is bidirectional. These devices support the standard mode and the fast mode for data transfer speeds up to 400kbits/s (see Timing Diagram section for definition of the I²C timing).

The START and STOP Conditions

Referring to Figure 6, a START (S) condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The bus is considered to be busy after the START condition. When the data transfer is finished, a STOP (P) condition is generated by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is free after a STOP condition is generated. START and STOP conditions are always generated by the master.

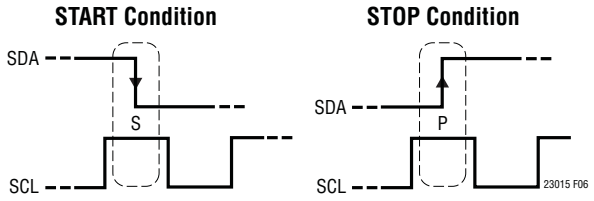

Figure 6. Timing Diagrams of START and STOP Conditions

When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START timing is functionally identical to the START and is used for writing and reading from the device before the initiation of a new conversion.

Data Transferring

After the START condition, the I²C bus is busy and data transfer can begin between the master and the addressed slave. Data is transferred over the bus in groups of nine bits, one byte followed by one acknowledge (ACK) bit. The master releases the SDA line during the ninth SCL clock cycle. The slave device can issue an ACK by pulling SDA LOW or issue a Not Acknowledge (NACK) by leaving the SDA line high impedance (the external pull-up resistor will hold the line HIGH). Change of data only occurs while the SCL line is LOW.

Data Format

After a START condition, the master sends a 7-bit address followed by a read/write (R/W) bit. The R/W bit is 1 for a read request and 0 for a write request. If the 7-bit address matches one of the LTC2301/LTC2305's 9 pin-selectable addresses (see Table 2), the ADC is selected. When the ADC is addressed during a conversion, it will not acknowledge R/W requests and will issue a NACK by leaving the SDA line HIGH. If the conversion is complete, the LTC2301/LTC2305 issues an ACK by pulling the SDA line LOW. The LTC2301/LTC2305 has two registers. The 12-bit wide output register contains the last conversion result. The 6-bit wide input register configures the input MUX and the operating mode of the ADC.

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Output Data Format

The output register contains the last conversion result. After each conversion is completed, the device automatically enters either nap or sleep mode depending on the setting of the SLP bit (see Nap Mode and Sleep Mode sections). When the LTC2301/LTC2305 is addressed for a read operation, it acknowledges by pulling SDA LOW and acts as a transmitter. The master/receiver can read up to two bytes from the LTC2301/LTC2305. After a complete read operation of 2 bytes, a STOP condition is needed to initiate a new conversion. The device will NACK subsequent read operations while a conversion is being performed.

The data output stream is 16 bits long and is shifted out on the falling edges of SCL (see Figure 7a). The first bit is the MSB and the 12th bit is the LSB of the conversion result. The remaining four bits are zero. Figures 13 and 14 are the transfer characteristics for the bipolar and unipolar modes. Data is output on the SDA line in 2's complement format for bipolar readings and in straight binary for unipolar readings.

Input Data Format

When the LTC2301/LTC2305 is addressed for a write operation, it acknowledges by pulling SDA LOW during the LOW period before the 9th cycle and acts as a receiver. The master/transmitter can then send 1 byte to program the device. The input byte consists of the 6-bit D_{IN} word followed by two bits that are ignored by the ADC and are considered don't cares (X) (see Figure 7b). The input bits are latched on the rising edge of SCL during the write operation.

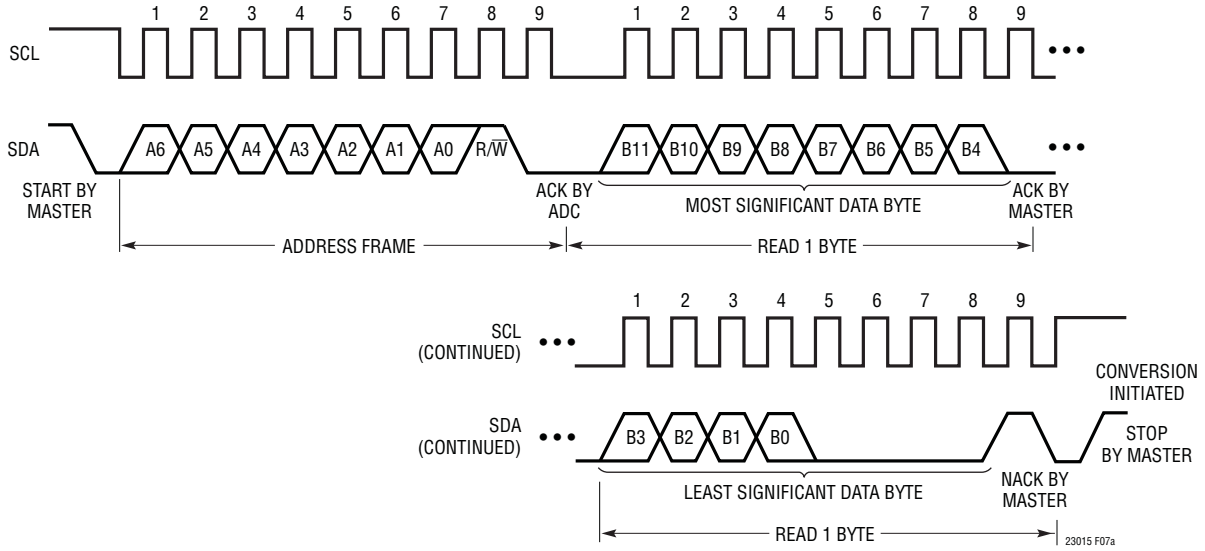

Figure 7a. Timing Diagram for Reading from the LTC2301/LTC2305

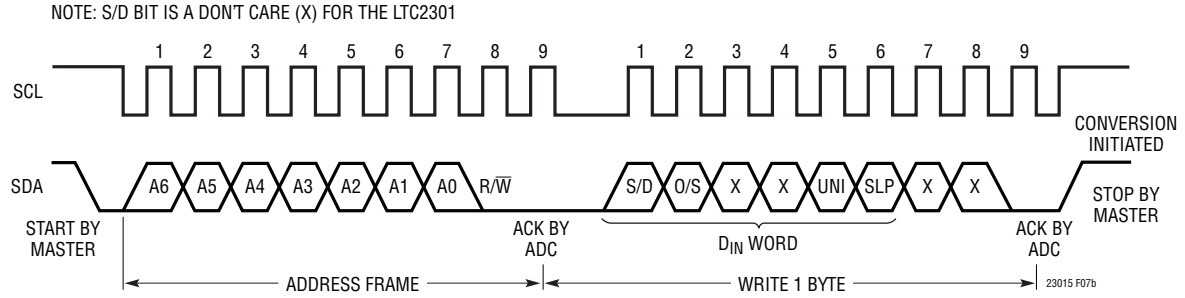

Figure 7b. Timing Diagram for Writing to the LTC2301/LTC2305

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After power-up, the ADC initiates an internal reset cycle which sets the D_{IN} word to all 0s (S/D=0/S=UNI=SLP=0). A write operation may be performed if the default state of the ADC's configuration is not desired. Otherwise, the ADC must be properly addressed and followed by a STOP condition to initiate a conversion.

Initiating a New Conversion

The LTC2301/LTC2305 awakens from either nap or sleep when properly addressed for a read/write operation. A STOP command may then be issued after performing the read/write operation to trigger a new conversion.

Issuing a STOP command after the 8th SCL clock pulse of the address frame and before the completion of a read/write operation will also initiate new conversion, but the output result may not be valid due to lack of adequate acquisition time (see Acquisition section).

LTC2301/LTC2305 Address

The LTC2301/LTC2305 have two address pins (AD0 and AD1) that may be tied high, low or left floating to enable one of the 9 possible addresses (see Table 2).

In addition to the configurable addresses listed in Table 2, the LTC2301/LTC2305 also contain a global address (1101011) which may be used for synchronizing multiple LTC2301/LTC2305s or other I^2C LTC230X SAR ADCs (see Synchronizing Multiple LTC2301/LTC2305s with Global Address Call section).

Table 2. Address Assignment

AD1	AD0	ADDRESS
LOW	LOW	0001000
LOW	Float	0001001
LOW	HIGH	0001010
Float	HIGH	0001011
Float	Float	0011000
Float	LOW	0011001
HIGH	LOW	0011010
HIGH	Float	0011011
HIGH	HIGH	0101000

Continuous Read

In applications where the same input channel is sampled each cycle, conversions can be continuously performed and read without a write cycle (see Figure 8). The D_{IN} word remains unchanged from the last value written into the device. If the device has not been written to since power-up, the D_{IN} word defaults to all 0s (S/D=0/S=UNI=SLP=0). At the end of a read operation, a STOP condition may be given to start a new conversion. At the conclusion of the conversion cycle, the next result may be read using the method described above. If the conversion cycle is not concluded and a valid address selects the device, the LTC2301/LTC2305 generates a NACK signal indicating the conversion cycle is in progress.

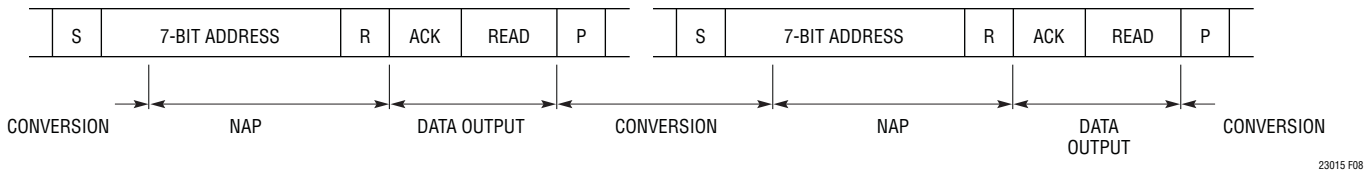

Figure 8. Consecutive Reading with the Same Configuration

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Continuous Read/Write

Once the conversion cycle is complete, the LTC2301/LTC2305 can be written to and then read from using the repeated START (Sr) command. Figure 9 shows a cycle which begins with a data write, a repeated START, followed by a read and concluded with a STOP command. After all 16 bits are read out, a conversion may be initiated by issuing a STOP command. The following conversion will be performed using the newly programmed data.

Synchronizing Multiple LTC2301/LTC2305s with a Global Address Call

In applications where several LTC2301/LTC2305s or other I^2C SAR ADCs from Linear Technology Corporation are used on the same I^2C bus, all converters can be synchronized through the use of a global address call. Prior to issuing the global address call, all converters must have completed a conversion cycle. The master then issues a START, followed by the global address 1101011, and a write request. All converters will be selected and acknowledge the request. The master then sends a write byte (optional) followed by the STOP command. This will update the channel selection (optional) and simultaneously initiate a conversion for all ADCs on the bus (see Figure 10). In order to synchronize multiple converters without changing the channel, a STOP command may be issued after acknowledgement of the global write command. Global read commands are not allowed and the converters will NACK a global read request.

Nap Mode

The ADCs enter nap mode after a conversion is complete (t_{CONV}) if the SLP bit is set to a logic 0. The supply current decreases to 225µA in nap mode between conversions, thereby reducing the average power dissipation as the sample rate decreases. For example, the LTC2301/LTC2305 draw an average of 300µA at a 1ksps sampling rate. The LTC2301/LTC2305 keep only the reference (V_{REF}) and reference buffer (REFCOMP) circuitry active when in nap mode.

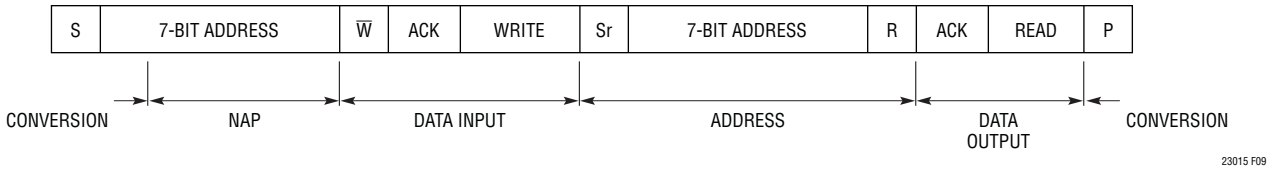


Figure 9. Write, Read, START Conversion

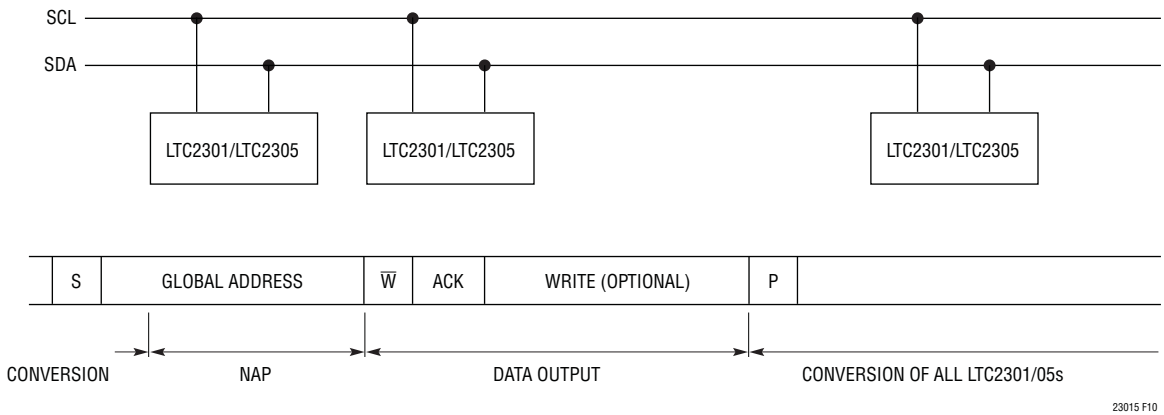


Figure 10. Synchronize Multiple LTC2301/LTC2305s with a Global Address Call

APPLICATIONS INFORMATION

Sleep Mode

The ADCs enter sleep mode after a conversion is complete (t_{CONV}) if the SLP bit is set to a logic 1. The ADCs draw only 7µA in sleep mode, provided that none of the digital inputs are switching. When the LTC2301/LTC2305 are properly addressed, the ADCs are released from sleep mode and require 200ms ($t_{REFWAKE}$) to wake up and charge the respective 2.2µF and 10µF bypass capacitors on the V_{REF} and REFCOMP pins. A new conversion should not be initiated before this time, as shown in Figure 11.

Acquisition

The LTC2301/LTC2305 begin acquiring the input signal at different instances depending on whether a read or write operation is being performed. If a read operation is being performed, acquisition of the input signal begins on the rising edge of the 9th clock pulse following the address frame, as shown in Figure 12a.

If a write operation is being performed, acquisition of the input signal begins on the falling edge of the sixth clock cycle after the D_{IN} word has been shifted in, as shown in Figure 12b. The LTC2301/LTC2305 will acquire the signal from the input channel that was most recently programmed by the D_{IN} word. A minimum of 240ns is required to acquire the input signal before initiating a new conversion.

Board Layout and Bypassing

To obtain the best performance, a printed circuit board with a solid ground plane is required. Layout for the printed board should ensure digital and analog signal lines are

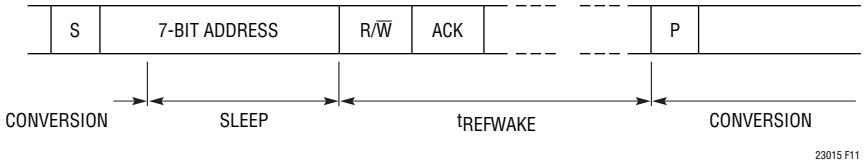


Figure 11. Exiting Sleep Mode and Starting a New Conversion

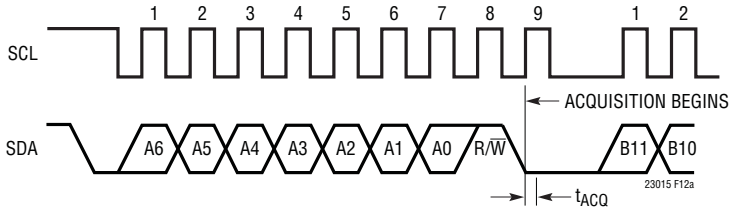


Figure 12a. Timing Diagram Showing Acquisition During a Read Operation

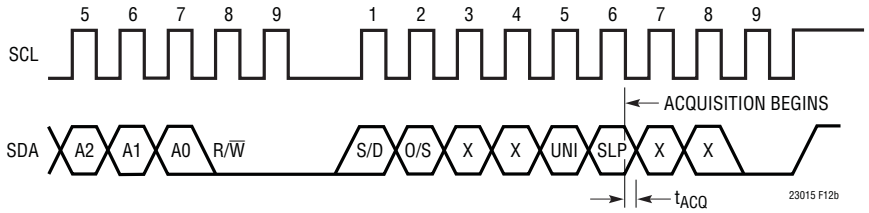


Figure 12b. Timing Diagram Showing Acquisition During a Write Operation

APPLICATIONS INFORMATION

separated as much as possible. Care should be taken not to run any digital signals alongside an analog signal. All analog inputs should be shielded by GND. V_{REF}, REFCOMP and V_{DD} should be bypassed to the ground plane as close to the pin as possible. Maintaining a low impedance path for the common return of these bypass capacitors is essential to the low noise operation of the ADC. These traces should be as wide as possible. See Figures 15a–15e for a suggested layout.

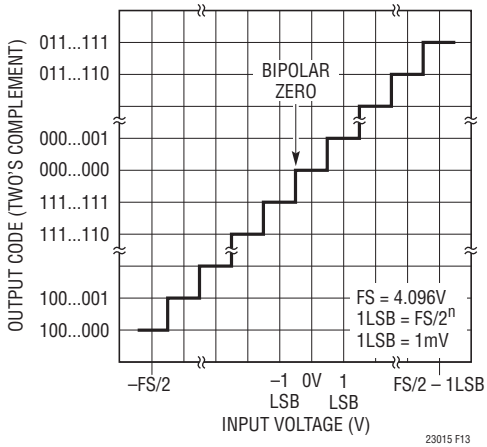


Figure 13. Bipolar Transfer Characteristics (2's Complement)

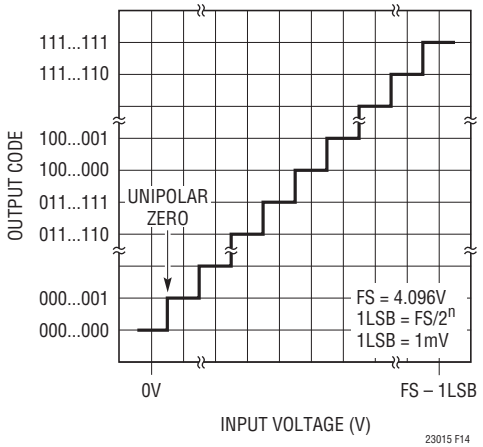


Figure 14. Unipolar Transfer Characteristics (Straight Binary)

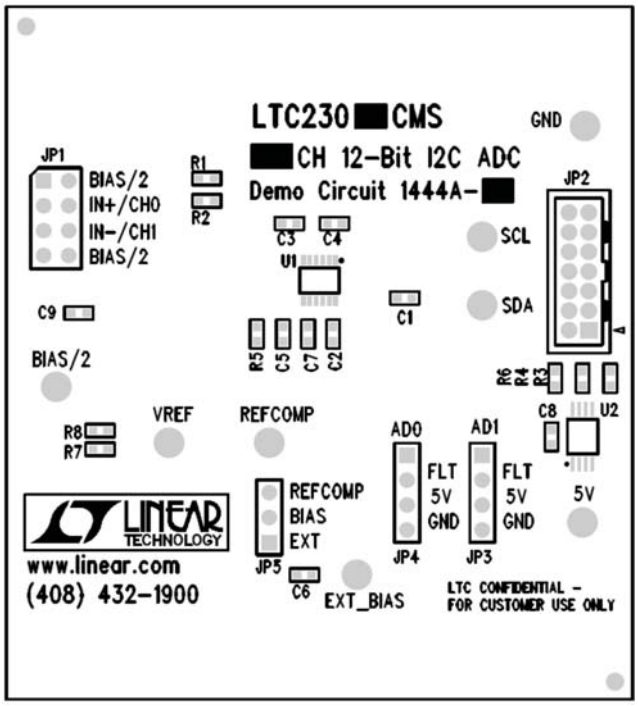


Figure 15a. Top Silkscreen

APPLICATIONS INFORMATION

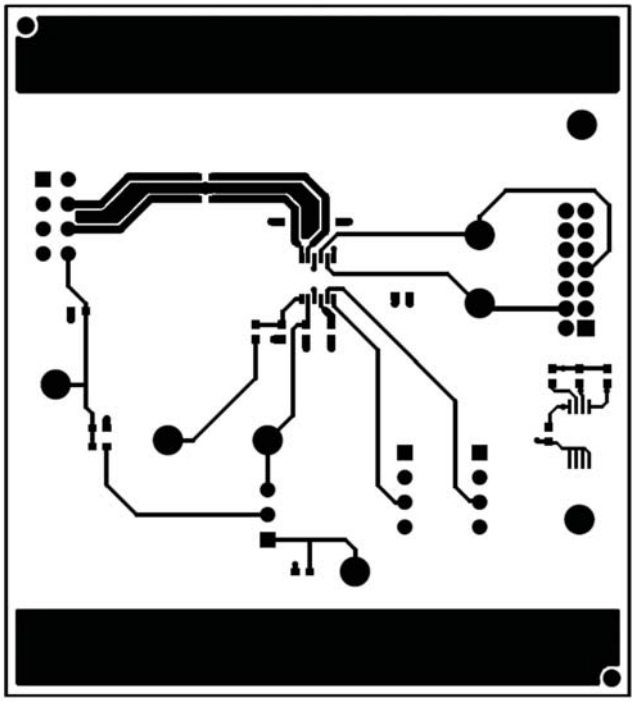


Figure 15b. Topside

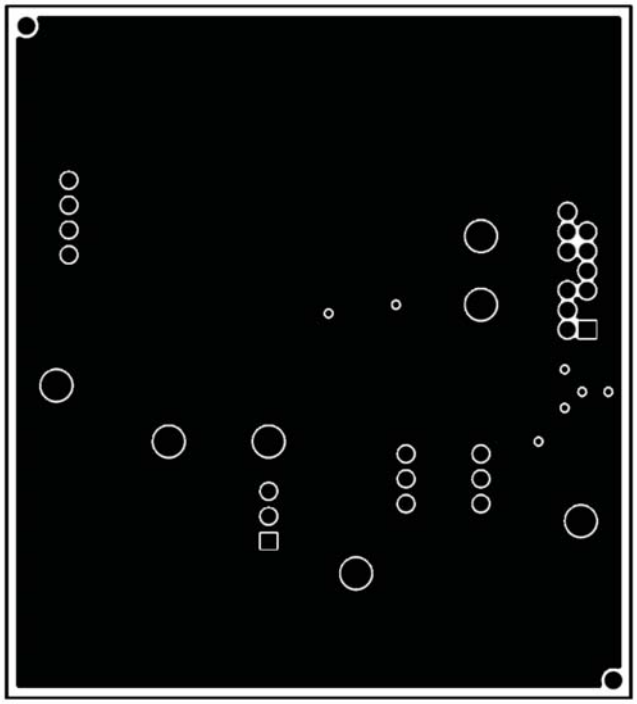


Figure 15c. Layer 2 Ground Plane

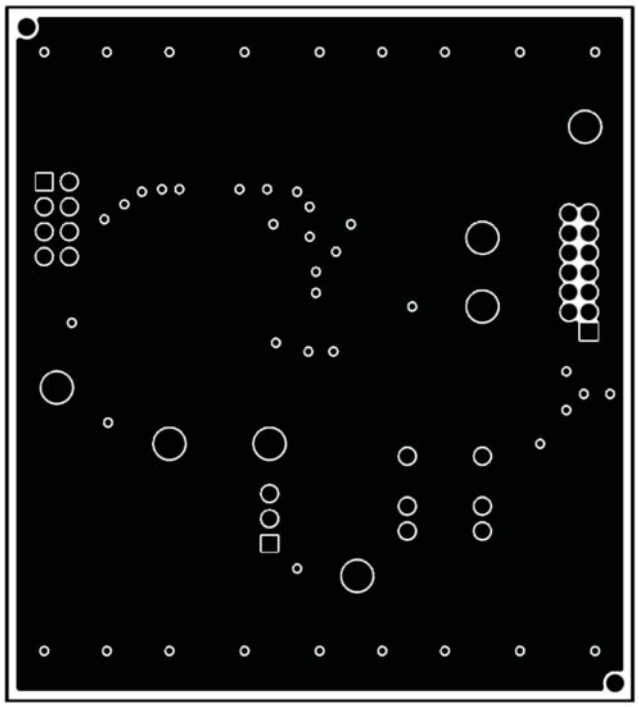


Figure 15d. Layer 3 Power Plane

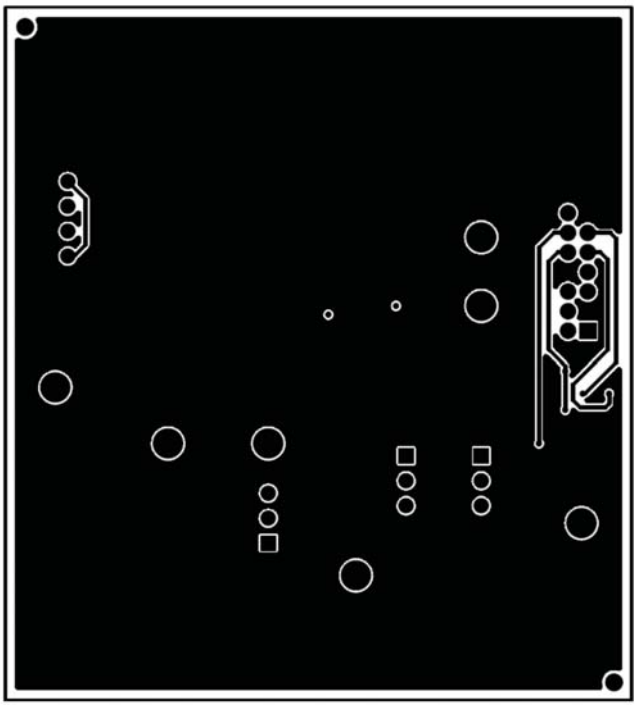
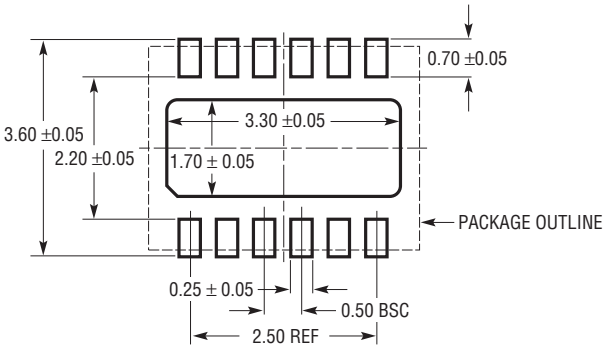


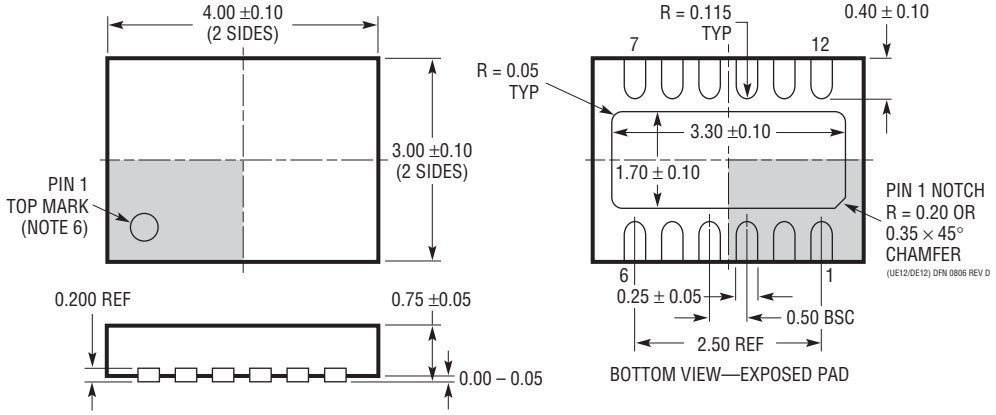
Figure 15e. Bottom Side

PACKAGE DESCRIPTION

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695)



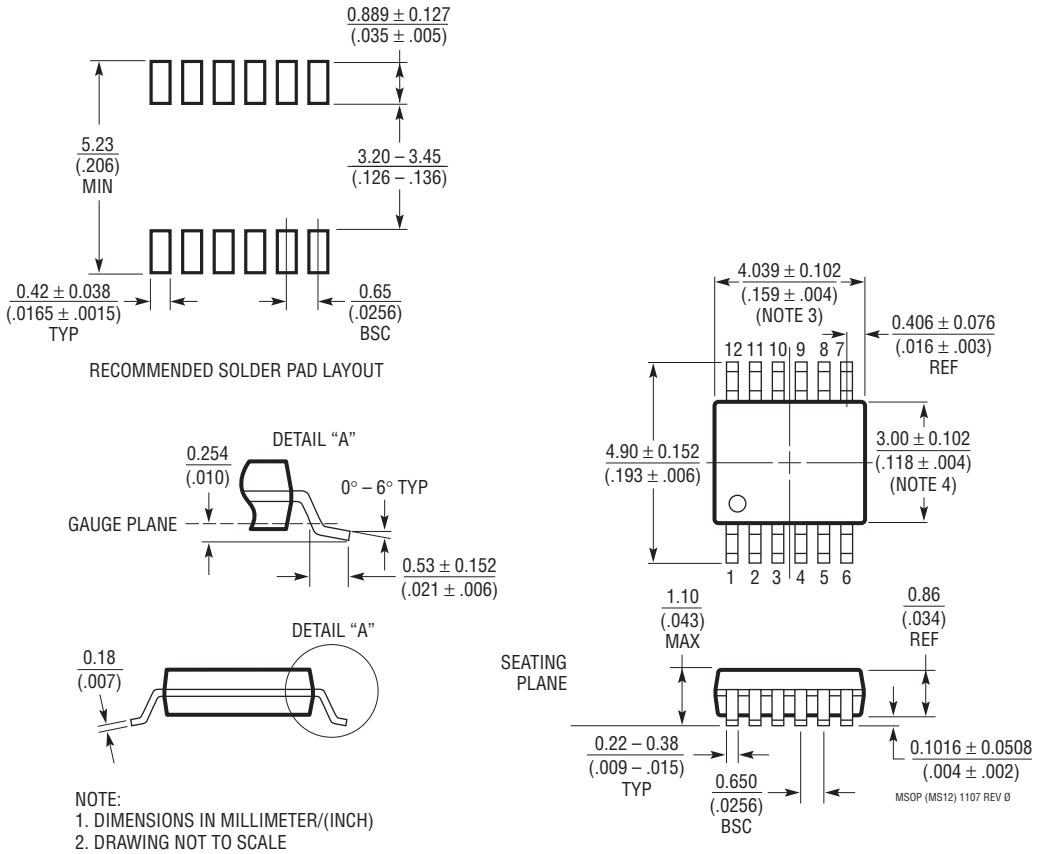
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS Package
12-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1668 Rev Ø)



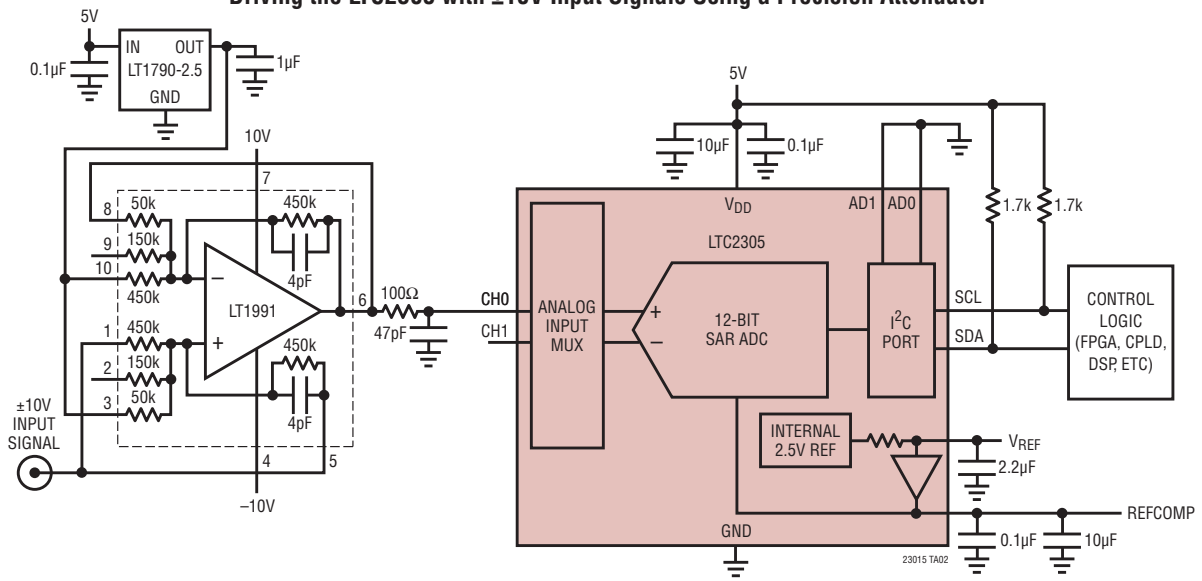
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	8/10	Revised Typical Performance Characteristics curves G03 and G12	7, 8
		Revised V_{REF}, REFCOMP and V_{DD} descriptions in Pin Functions section	9, 10
		Revised Figure 4 in Applications Information section	15
		Revised Figures 5a, 5b and 5c, Internal Reference section and I^2C Interface section in Applications Information	15, 16
		Changed “NAK” command to NACK	16, 17

TYPICAL APPLICATION

Driving the LTC2305 with ±10V Input Signals Using a Precision Attenuator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1417	14-Bit, 400ksps Serial ADC	20mW, Unipolar or Bipolar, Internal Reference, SSOP-16 Package
LTC1468/LT1469	Single/Dual 90MHz, 22V/µs, 16-Bit Accurate Op Amps	Low Input Offset: 75µV/125µV
LTC1609	16-Bit, 200ksps Serial ADC	65mW, Configurable Bipolar and Unipolar Input Ranges, 5V Supply
LTC1790	Micropower Low Dropout Reference	60µA Supply Current, 10ppm/°C, SOT-23 Package
LTC1850/LTC1851	10-Bit/12-Bit, 8-Channel, 1.25Msps ADC	Parallel Output, Programmable MUX and Sequencer, 5V Supply
LTC1852/LTC1853	10-Bit/12-Bit, 8-Channel, 400ksps ADC	Parallel Output, Programmable MUX and Sequencer, 3V or 5V Supply
LTC1860/LTC1861	12-Bit, 1-/2-Channel 250ksps ADC in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1860L/LTC1861L	3V, 12-Bit, 1-/2-Channel 150ksps ADC	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages
LTC1863/LTC1867	12-/16-Bit, 8-Channel 200ksps ADC	6.5mW, Unipolar or Bipolar, Internal Reference, SSOP-16 Package
LTC1863L/LTC1867L	3V, 12-/16-Bit, 8-Channel 175ksps ADC	2mW, Unipolar or Bipolar, Internal Reference, SSOP-16 Package
LTC1864/LTC1865	16-Bit, 1-/2-Channel 250ksps ADC in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1864L/LTC1865L	3V, 16-Bit, 1-/2-Channel 150ksps ADC in MSOP	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages
LTC2302/LTC2306	12-Bit, 1-/2-Channel 500ksps SPI ADCs in 3mm × 3mm DFN	14mW at 500ksps, Single 5V Supply, Software Compatible with LTC2308
LTC2308	12-Bit, 8-Channel 500ksps SPI ADC	5V, Internal Reference, 4mm × 4mm QFN Package, Software Compatible with LTC2302/LTC2306
LTC2309	12-Bit, 8-Channel ADC with I²C Interface	5V, Internal Reference, 4mm × 4mm QFN and 20-Pin TSSOP Packages, Software Compatible with LTC2301/LTC2305
LTC2451/LTC2453	Easy-to-Use, Ultra-Tiny 16-Bit I²C Delta Sigma ADCs	2 LSB INL, 50nA Sleep Current, 60Hz Output Rate, 3mm × 2mm DFN Package, Single-Ended/Differential Inputs
LTC2487/LTC2489/ LTC2493	2-/4-Channel Easy Drive I²C Delta Sigma ADCs	16-/24-Bits, PGA and Temp Sensor, 4mm × 3mm DFN Packages
LTC2495/LTC2497/ LTC2499	8-/16-Channel Easy Drive I²C Delta Sigma ADCs	16-/24-Bits, PGA and Temp Sensor, 5mm × 7mm QFN Packages

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