65V, 3.5A/5A Peak Synchronous Step-Down Silent Switcher with 2.5µA Quiescent Current

FEATURES

- **Silent Switcher® Architecture**
  - **Ultralow EMI Emissions**
  - **Spread Spectrum Frequency Modulation**
- **High Efficiency at High Frequency**
  - **Up to 95% Efficiency at 1MHz, $12V_{IN}$ to $5V_{OUT}$**
  - **Up to 94% Efficiency at 2MHz, $12V_{IN}$ to $5V_{OUT}$**
- **Wide Input Voltage Range: 3V to 65V**
- **3.5A Maximum Continuous, 5A Peak Transient Output**
- **Ultralow Quiescent Current Burst Mode® Operation**
  - **2.5µA I_Q Regulating $12V_{IN}$ to $3.3V_{OUT}$**
  - **Output Ripple < $10mV_{P-P}$**
- **Fast Minimum Switch On-Time: 35ns**
  - **True 2MHz Operation for $24V_{IN}$ Systems**
- **Low Dropout Under All Conditions: 130mV at 1A**
- Safely Tolerates Inductor Saturation in Overload
- Adjustable and Synchronizable: 200kHz to 3MHz
- Output Soft-Start and Tracking
- Small 18-Lead 3mm × 4mm Side Wettable QFN with Improved Solder Joint Reliability
- AEC-Q100 Qualified for Automotive Applications
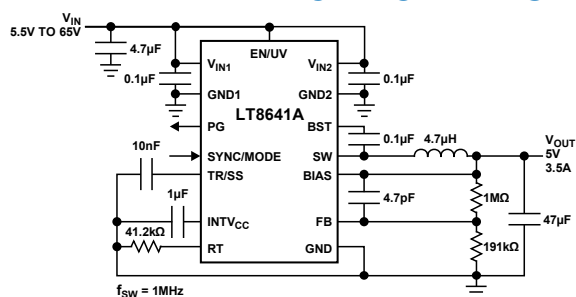
APPLICATIONS

- Automotive and Industrial Supplies
- General Purpose Step-Down

GENERAL DESCRIPTION

The LT®8641A step-down regulator features Silent Switcher architecture designed to minimize EMI emissions while delivering high efficiency at frequencies up to 3MHz. Assembled in a 3mm × 4mm side wettable QFN, the monolithic construction with integrated power switches and inclusion of all necessary circuitry yields a solution with a minimal PCB footprint. An ultralow 2.5µA quiescent current — with the output in full regulation — enables applications requiring highest efficiency at very small load currents. Transient response remains excellent and output voltage ripple is below $10mV_{P-P}$ at any load, from zero to full current.

The LT8641A allows high V_{IN} to low V_{OUT} conversion at high frequency with a fast minimum top switch on-time of 35ns. Operation is safe in overload even with a saturated inductor.

Essential features are included and easy to use: an open-drain PG pin signals when the output is in regulation. The SYNC/MODE pin selects between Burst Mode, pulse-skipping, or spread spectrum mode, and also allows synchronization to an external clock. Soft-start and tracking functionality are accessed through the TR/SS pin. An accurate enable threshold can be set using the EN/UV pin and a resistor at the RT pin programs switch frequency.

SIMPLIFIED APPLICATION DIAGRAM

Figure 1. 5V 3.5A Step-Down Converter
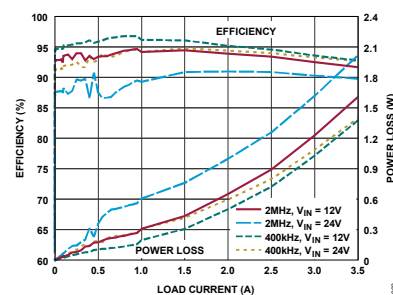
Figure 2. $12V_{IN}$ to $5V_{OUT}$ Efficiency

REVISION HISTORY

Nature of Change	Page Number
5/23 – REV 0	

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SPECIFICATIONS

Table 1. Electrical Characteristics

(T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Minimum Input Voltage	V_{IN}			2.6	3.0	V
V_{IN} Quiescent Current in Shutdown	$I_{Q(SHDN)}$	$V_{EN/UV}$ = 0V, V_{IN} = 12V, T_A = +25°C		0.75	3	μA
		$V_{EN/UV}$ = 0V, V_{IN} = 12V		0.75	10	
V_{IN} Quiescent Current in Sleep (Burst Mode)	$I_{Q(BURST)}$	$V_{EN/UV}$ = 2V, V_{FB} > 0.81V, V_{SYNC} = 0V, V_{IN} = 6V, T_A = +25°C		1.7	4	μA
		$V_{EN/UV}$ = 2V, V_{FB} > 0.81V, V_{SYNC} = 0V, V_{IN} = 6V		1.7	10	
V_{IN} Quiescent Current in Sleep (Pulse-Skip Mode)	$I_{Q(PSM)}$	$V_{EN/UV}$ = 2V, V_{FB} > 0.81V, V_{SYNC} = 2V, T_A = +25°C		0.30	0.51	mA
V_{IN} Current in Regulation	I_{IN}	V_{OUT} = 0.81V, V_{IN} = 6V, I_{LOAD} = 1mA, V_{SYNC} = 0V		200	390	μA
Feedback Reference Voltage	V_{FB}	V_{IN} = 6V, I_{LOAD} = 0.5A, T_A = +25°C	0.804	0.810	0.816	V
		V_{IN} = 6V, I_{LOAD} = 0.5A	0.790	0.810	0.822	
Feedback Voltage Line Regulation	$\Delta V_{FB(LINE)}$	V_{IN} = 4V to 42V		0.004	0.030	%/V
Feedback Pin Input Current	I_{FB}	V_{FB} = 1V, T_A = +25°C	−20		20	nA
BIAS Pin Current Consumption	I_{BIAS}	V_{BIAS} = 3.3V, f_{SW} = 2MHz		9		mA
Minimum On-Time	$t_{ON(MIN)}$	SYNC/MODE = 2V		35	50	ns
Minimum Off-Time	$t_{OFF(MIN)}$	T_A = +25°C		80	110	ns
Oscillator Frequency	f_{SW}	R_T = 221k	180	210	240	kHz
		R_T = 60.4k	665	700	735	
		R_T = 18.2k	1.80	1.95	2.10	MHz
Top Power NMOS On-Resistance	R_{TOP}	I_{SW} = 1A		105		mΩ
Top Power NMOS Current Limit	$I_{PEAK-LIMIT}$		6.2	8.2	9.9	A
Bottom Power NMOS On-Resistance	R_{BOT}	V_{INTVCC} = 3.4V, I_{SW} = 1A		55		mΩ
Bottom Power NMOS Current Limit	$I_{VALLEY-LIMIT}$	V_{INTVCC} = 3.4V, T_A = +25°C	4.80	5.80	7.25	A
SW Leakage Current	I_{SW-LKG}	V_{IN} = 42V, V_{SW} = 0V, 42V, T_A = +25°C	−3		3	μA
EN/UV Pin Threshold	V_{EN}	EN/UV Rising	0.95	1.01	1.07	V
		EN/UV Hysteresis		45		mV

(T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
EN/UV Pin Current	I_{EN}	$V_{EN/UV}$ = 2V, T_A = +25°C	−20		20	nA
PG Upper Threshold Offset from V_{FB}	PGH	V_{FB} Falling	5.00	7.50	10.25	%
PG Lower Threshold Offset from V_{FB}	PGL	V_{FB} Rising	−10.75	−8.00	−5.25	%
PG Hysteresis	PG_{HYS}			0.4		%
PG Leakage	I_{PG-LKG}	V_{PG} = 3.3V, T_A = +25°C	−40		40	nA
PG Pull-Down Resistance	R_{PG}	V_{PG} = 0.1V		750	2000	Ω
SYNC/MODE Threshold	$V_{SYNC/MODE}$	SYNC/MODE DC and Clock Low Level Voltage	0.7			V
		SYNC/MODE Clock High Level Voltage			1.5	
		SYNC/MODE DC High Level Voltage	2.2	2.6	2.9	
Spread Spectrum Modulation Frequency Range	Δf_{SSFM}	R_T = 60.4k, V_{SYNC} = 3.3V		22		%
Spread Spectrum Modulation Frequency	f_{SSFM}	V_{SYNC} = 3.3V		2.5		kHz
TR/SS Source Current	I_{SS}		1.3	2.0	2.7	µA
TR/SS Pull-Down Resistance	R_{SS}	Fault Condition, TR/SS = 0.1V		220		Ω

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings [1]

PARAMETER	RATING
V_{IN}, EN/UV	65V
PG	42V
BIAS	25V
FB, TR/SS	4V
SYNC/MODE Voltage	6V
Operating Junction Temperature Range [2][4] LT8641AR	−40°C to 150°C
Storage Temperature Range	−65°C to 150°C

1   Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those

indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

2 The LT8641AR is specified over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with the board layout, rated package thermal impedance, and other environmental factors.

The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (PD, in Watts) according to the formula:

$T_J = T_A + (PD \times \theta_{JA})$

where θ_{JA} (in °C/W) is the package thermal impedance.

3 θ values determined per JEDEC 51-7, 51-12. See the *Applications Information* section for information on improving the thermal resistance and for actual temperature measurements of a demo board in typical operating conditions.

4 This IC includes overtemperature protection intended to protect the device during overload conditions. Junction temperature exceeds 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature reduces lifetime.
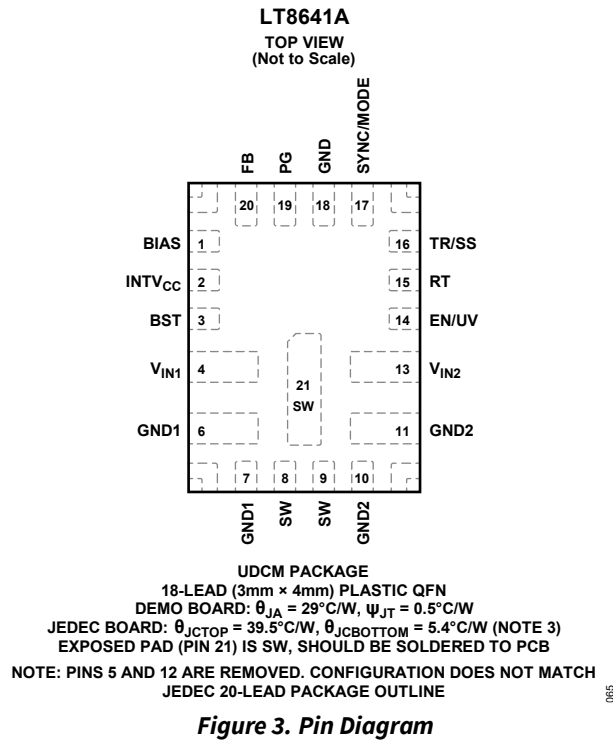
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

LT8641A
TOP VIEW
(Not to Scale)

FB | PG | GND | SYNC/MODE

| | | | |
| 20 | 19 | 18 | 17 |

BIAS | 1   16 | TR/SS
INTV$_{CC}$ | 2   15 | RT
BST | 3   14 | EN/UV
V$_{IN1}$ | 4   13 | V$_{IN2}$
    21 SW
GND1 | 6   11 | GND2

| 7 | 8 | 9 | 10 |

GND1 | SW | SW | GND2

UDCM PACKAGE
18-LEAD (3mm × 4mm) PLASTIC QFN
DEMO BOARD: θ$_{JA}$ = 29°C/W, ψ$_{JT}$ = 0.5°C/W
JEDEC BOARD: θ$_{JCTOP}$ = 39.5°C/W, θ$_{JCBOTTOM}$ = 5.4°C/W (NOTE 3)
EXPOSED PAD (PIN 21) IS SW, SHOULD BE SOLDERED TO PCB
NOTE: PINS 5 AND 12 ARE REMOVED. CONFIGURATION DOES NOT MATCH
JEDEC 20-LEAD PACKAGE OUTLINE

Figure 3. Pin Diagram

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	BIAS	The internal regulator draws current from BIAS instead of V$_{IN}$ when BIAS is tied to a voltage higher than 3.1V. For output voltages of 3.3V to 25V, tie this pin to V$_{OUT}$. If this pin is tied to a supply other than V$_{OUT}$, use a 1µF local bypass capacitor on this pin. If no supply is available, tie to GND.
2	INTV$_{CC}$	Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. INTV$_{CC}$ maximum output current is 20mA. Do not load the INTV$_{CC}$ pin with external circuitry. INTV$_{CC}$ current is supplied from BIAS if BIAS > 3.1V, otherwise current is drawn from V$_{IN}$. Voltage on INTV$_{CC}$ varies between 2.8V and 3.4V when BIAS is between 3.0V and 3.6V. Decouple this pin to power ground with at least a 1µF low ESR ceramic capacitor placed close to the IC.
3	BST	This pin is used to provide a drive voltage, higher than the input voltage, to the topside power switch. Place a 0.1µF boost capacitor as close as possible to the IC.
4	V$_{IN1}$	The LT8641A requires two 0.1µF small input bypass capacitors. Place one 0.1µF capacitor between V$_{IN1}$ and GND1. Place a second 0.1µF capacitor between V$_{IN2}$ and GND2. Place these capacitors as close as possible to the LT8641A. Place a third larger capacitor of 2.2µF or more close to the LT8641A with the positive terminal connected

		to V_{IN1} and V_{IN2}, and the negative terminal connected to ground. See the *Applications Information* section for sample layout.
6, 7	GND1	Power Switch Ground. These pins are the return path of the internal bottom side power switch and must be tied together. Place the negative terminal of the input capacitor as close to the GND1 pins as possible. Also be sure to tie GND1 to the ground plane. See the *Applications Information* section for sample layout.
8, 9	SW	The SW pins are the outputs of the internal power switches. Tie these pins together and connect them to the inductor and boost capacitor. This node should be kept small on the PCB for good performance and low EMI.
10, 11	GND2	Power Switch Ground. These pins are the return path of the internal bottom side power switch and must be tied together. Place the negative terminal of the input capacitor as close to the GND2 pins as possible. Also be sure to tie GND2 to the ground plane. See the *Applications Information* section for sample layout.
13	V_{IN2}	The LT8641A requires two 0.1µF small input bypass capacitors. Place one 0.1µF capacitor between V_{IN1} and GND1. Place a second 0.1µF capacitor between V_{IN2} and GND2. Place these capacitors as close as possible to the LT8641A. Place a third larger capacitor of 2.2µF or more close to the LT8641A with the positive terminal connected to V_{IN1} and V_{IN2}, and the negative terminal connected to ground. See the *Applications Information* section for sample layout.
14	EN/UV	The LT8641A is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 1.01V going up and 0.965V going down. Tie to V_{IN} if the shutdown feature is not used. An external resistor divider from V_{IN} can be used to program a V_{IN} threshold, below which the LT8641A enters shutdown.
15	RT	Tie a resistor between RT and ground to set the switching frequency.
16	TR/SS	Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. A TR/SS voltage below 0.81V forces the LT8641A to regulate the FB pin to equal the TR/SS pin voltage. When TR/SS is above 0.81V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current from $INTV_{CC}$ on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with an internal 200Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the tracking function is not needed.
17	SYNC/MODE	This pin programs four different operating modes: 1) Burst Mode. Tie this pin to ground for Burst Mode operation at low output loads. This results in ultralow quiescent current. 2) Pulse-skipping mode. Float this pin for pulse-skipping mode. This mode offers full frequency operation down to low output loads before pulse skipping occurs. When floating, pin leakage currents should be <1µA. See the *Block Diagram* for internal pull-up and pull-down resistance. 3) Spread spectrum mode. Tie this pin high to $INTV_{CC}$ (~3.4V) or an external supply of 3V to 4V for pulse-skipping mode with spread spectrum modulation. 4) Synchronization mode. Drive this pin with a clock source to synchronize to an external frequency. During synchronization, the part operates in pulse-skipping mode.
18	GND	LT8641A Ground Pin. Connect this pin to system ground and to the ground plane.

19	PG	The PG pin is the open-drain output of an internal comparator. PG remains low until the FB pin is within ±8% of the final regulation voltage, and there are no fault conditions. PG is valid when V_{IN} is above 3V, regardless of EN/UV pin state.
20	FB	The LT8641A regulates the FB pin to 0.81V. Connect the feedback resistor divider tap to this pin. Also, connect a phase lead capacitor between FB and V_{OUT}. Typically, this capacitor is 4.7pF to 22pF.
Exposed Pad Pin 21	SW	Connect and solder the exposed pads to the SW trace for good thermal performance. If necessary, due to manufacturing limitations, pins 21 and 22 may be left disconnected. However, thermal performance is degraded.
	Corner Pins	These pins are for mechanical support only and can be tied anywhere on the PCB, typically ground.

TYPICAL PERFORMANCE CHARACTERISTICS
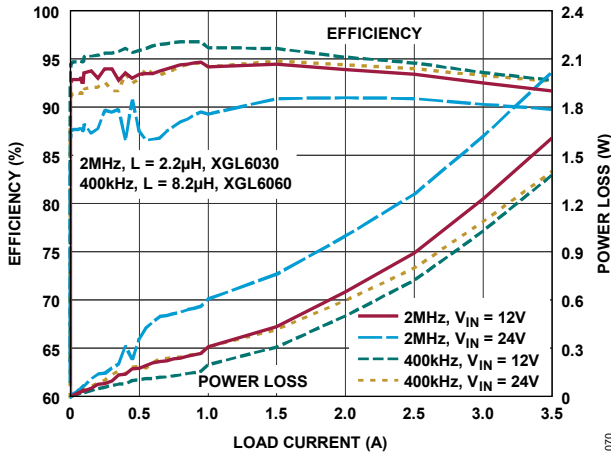
Figure 4. 12V$_{IN}$ to 5V$_{OUT}$ Efficiency vs. Frequency
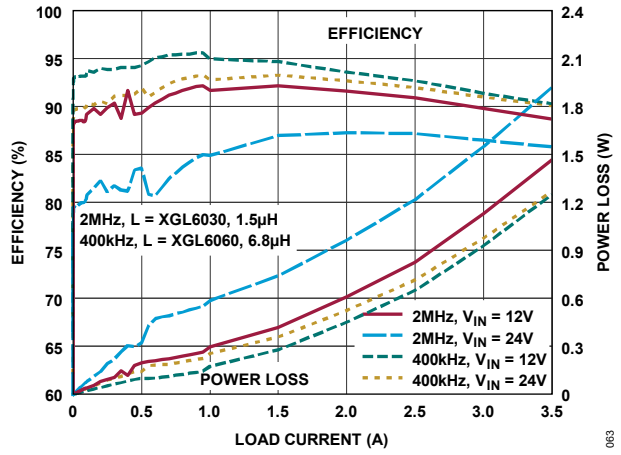
Figure 5. 12V$_{IN}$ to 3.3V$_{OUT}$ Efficiency vs. Frequency
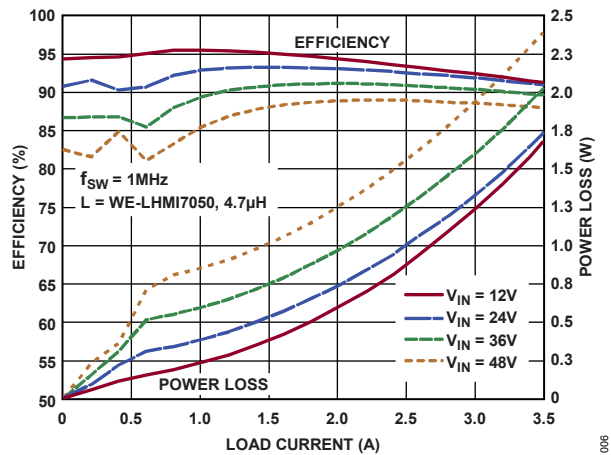
Figure 6. Efficiency at 5V$_{OUT}$
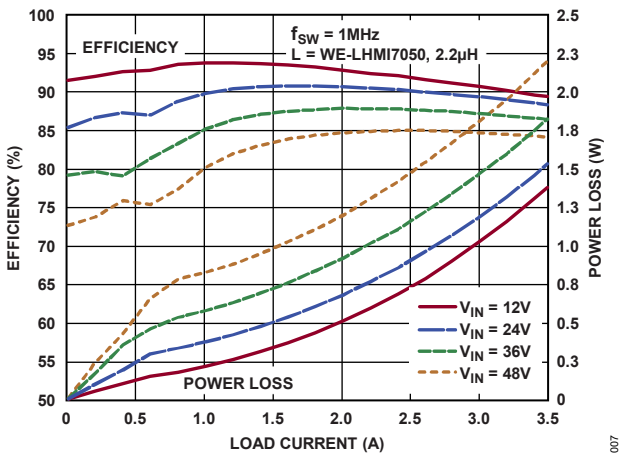
Figure 7. Efficiency at 3.3V$_{OUT}$
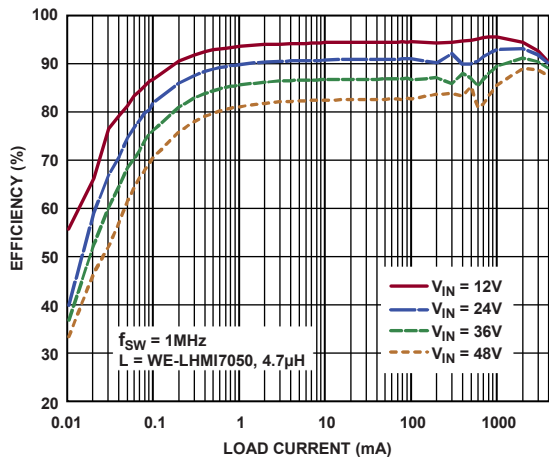
Figure 8. Efficiency at 5V$_{OUT}$
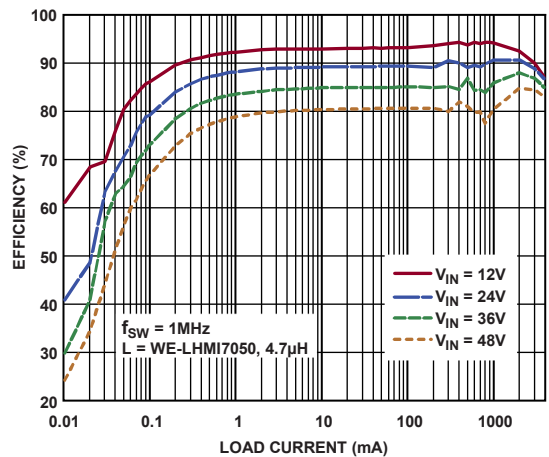
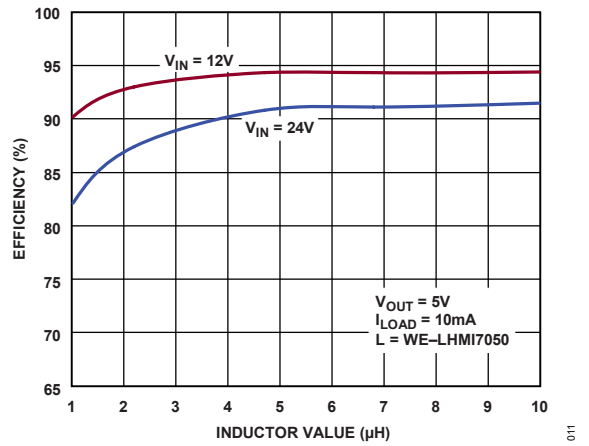*Figure 9. Efficiency at 3.3V$_{OUT}$*
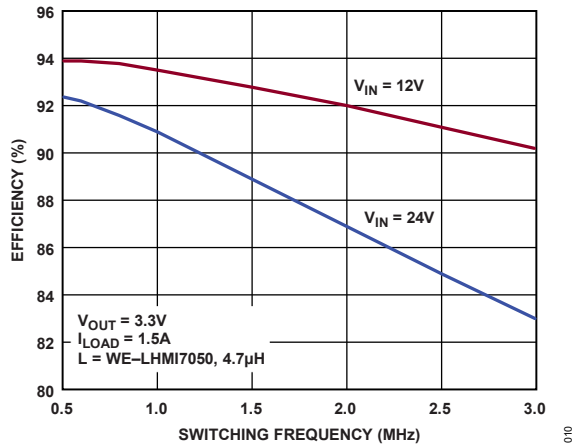
Figure 10. Efficiency vs. Frequency

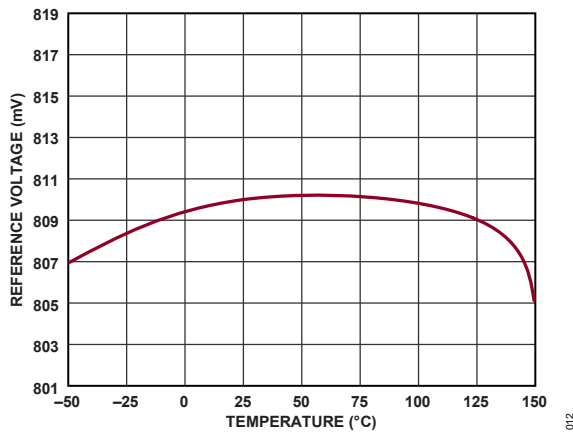Figure 11. Burst Mode Operation Efficiency vs. Inductor Value
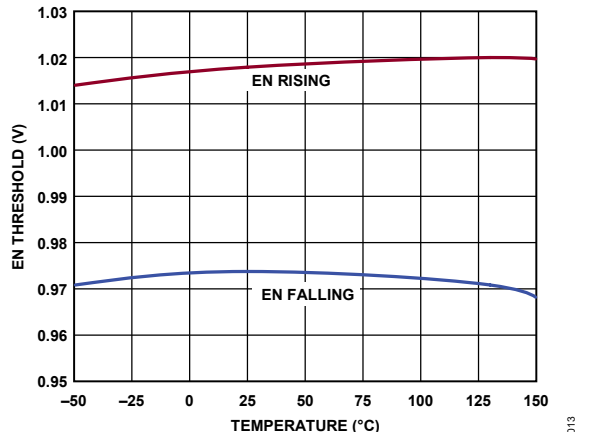

Figure 12. Reference Voltage

Figure 13. EN Pin Thresholds
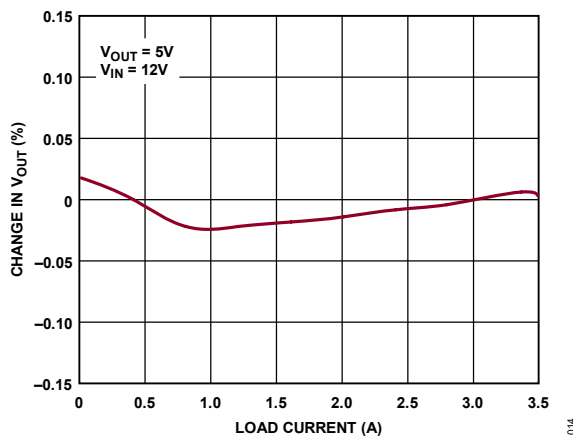
Figure 14. Load Regulation
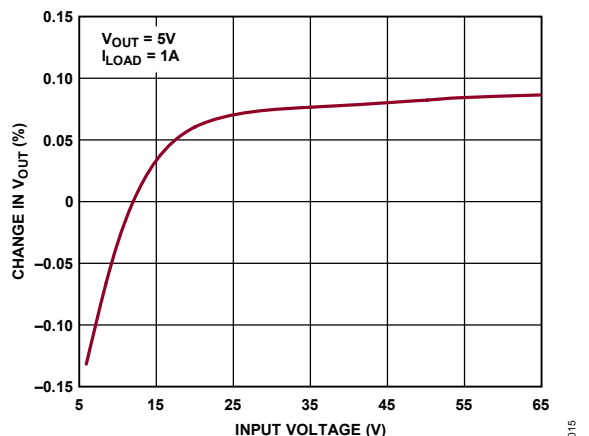
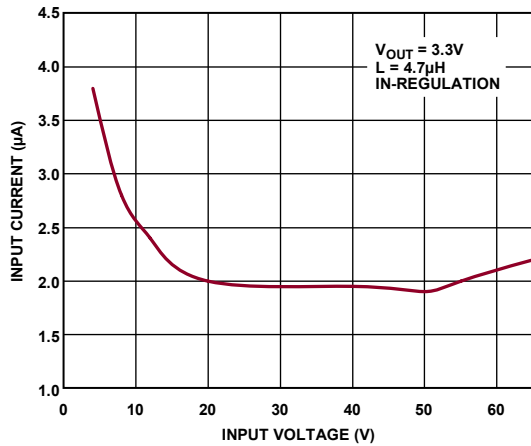

Figure 15. Line Regulation

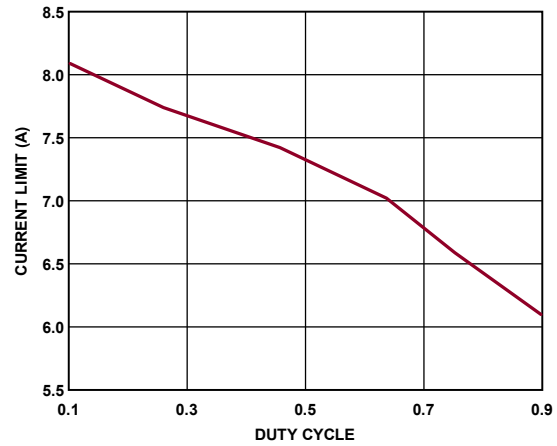Figure 16. No-Load Supply Current

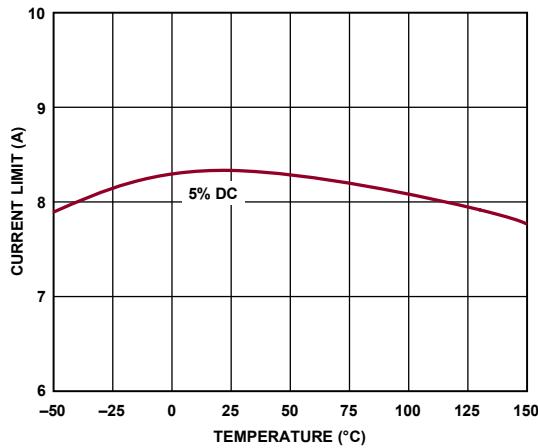

Figure 17. Top FET Current Limit vs. Duty Cycle
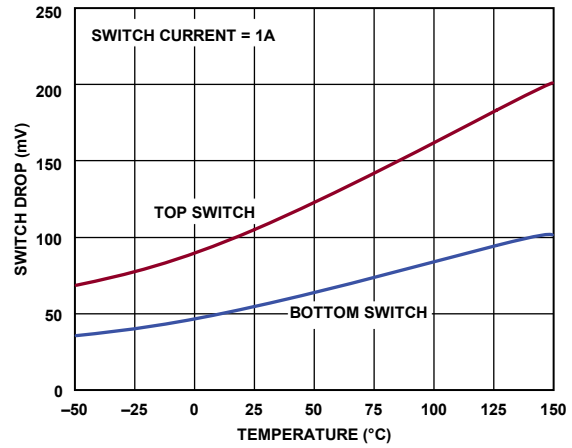

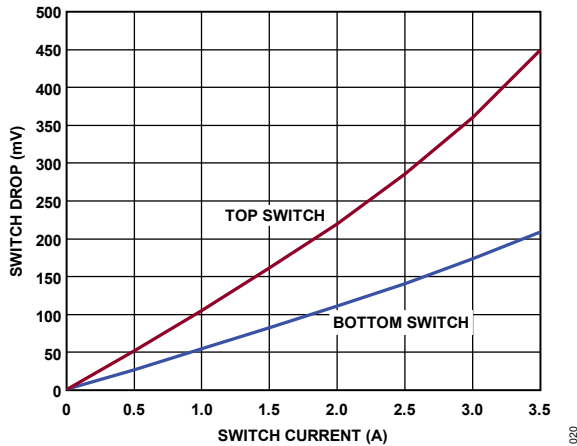Figure 18. Top FET Current Limit
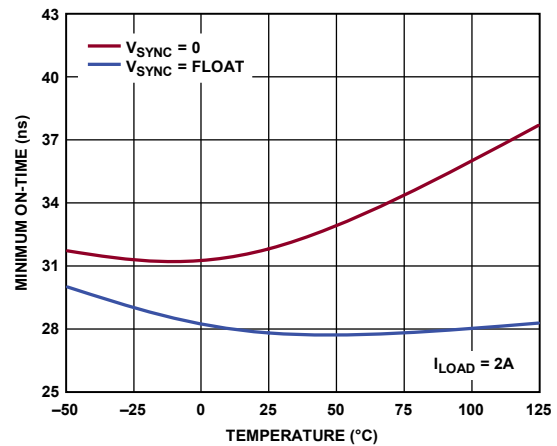

Figure 19. Switch Drop

Figure 20. Switch Drop

Figure 21. Minimum On-Time
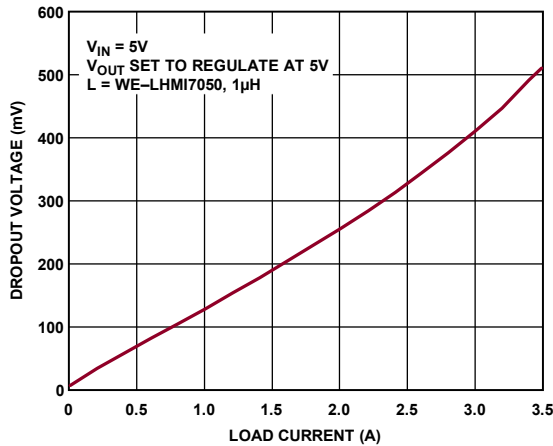
Figure 22. Dropout Voltage

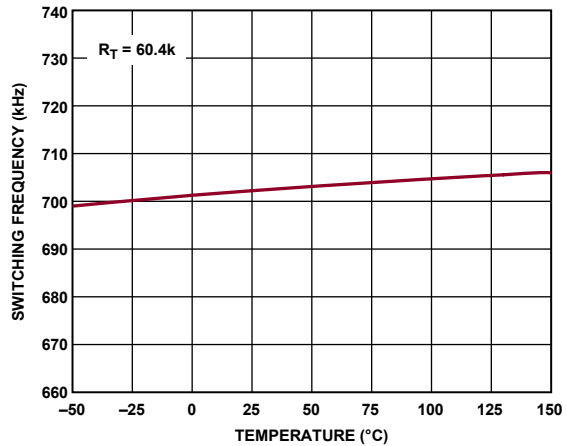Figure 23. Switching Frequency
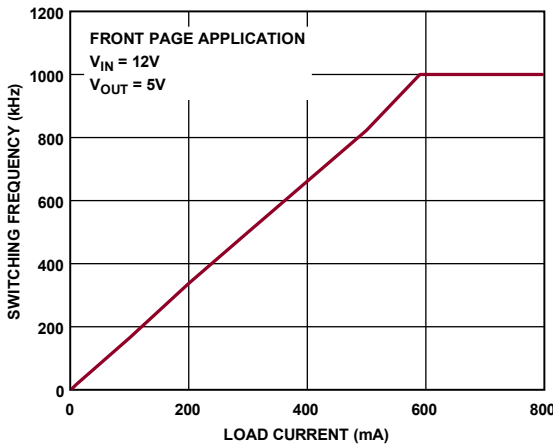

Figure 24. Burst Frequency
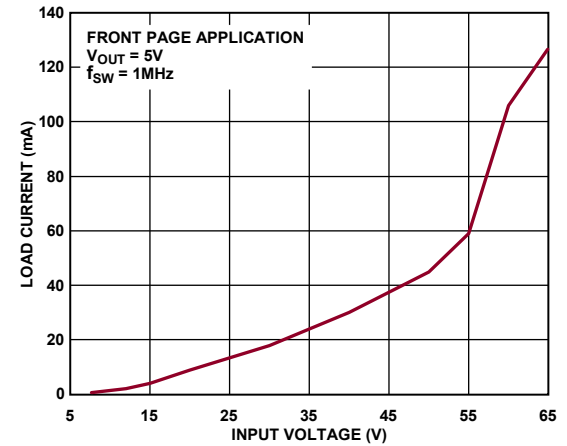
Figure 25. Minimum Load to Full Frequency (Pulse-Skipping Mode)
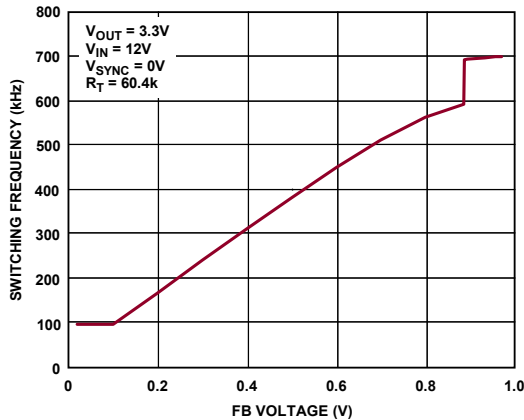
Figure 26. Frequency Foldback
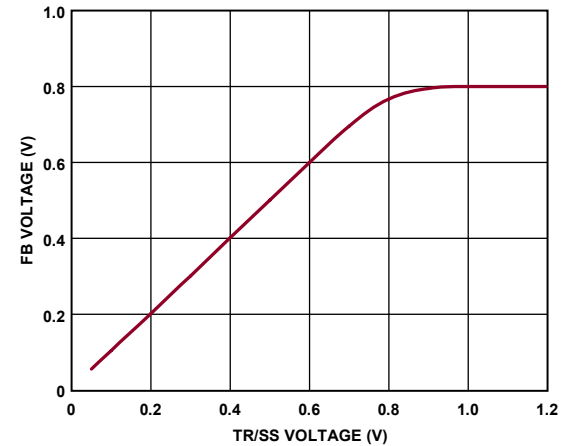
Figure 27. Soft-Start Tracking
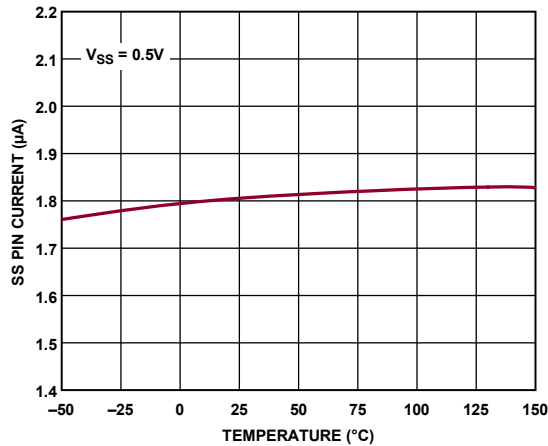
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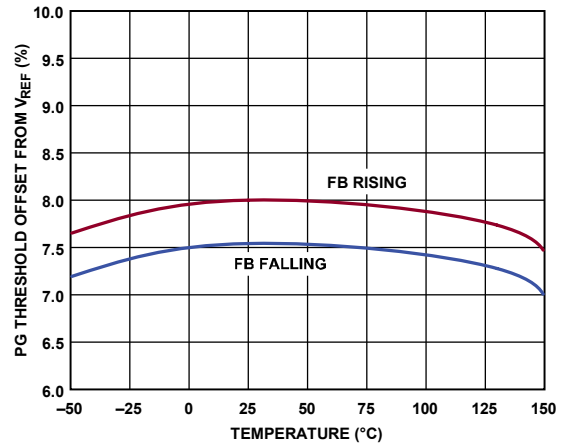
Figure 29. PG High Thresholds
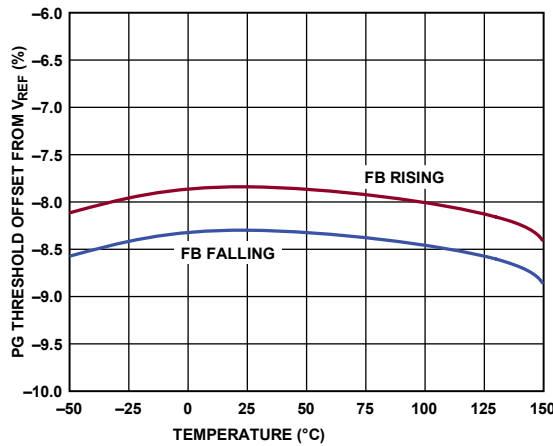
Figure 30. PG Low Thresholds
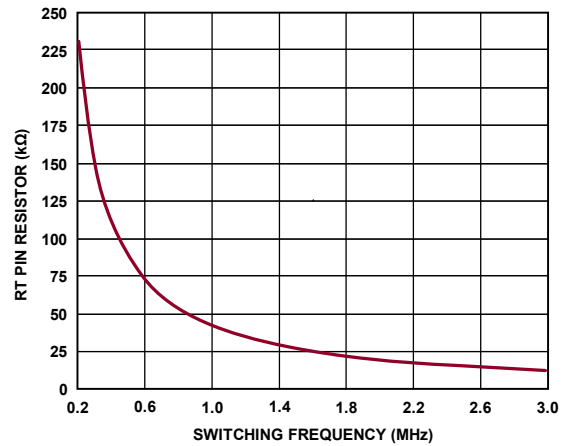
Figure 31. RT Programmed Switching Frequency
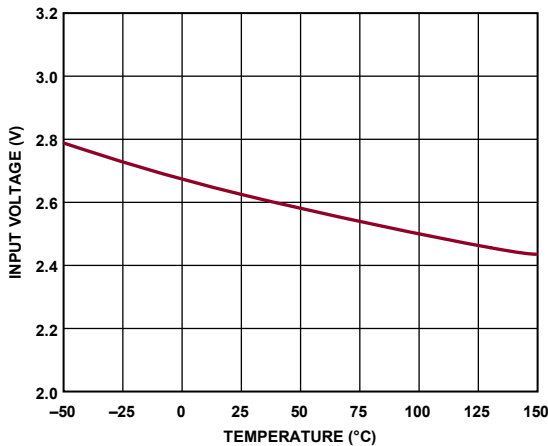
Figure 32. V_{IN} UVLO
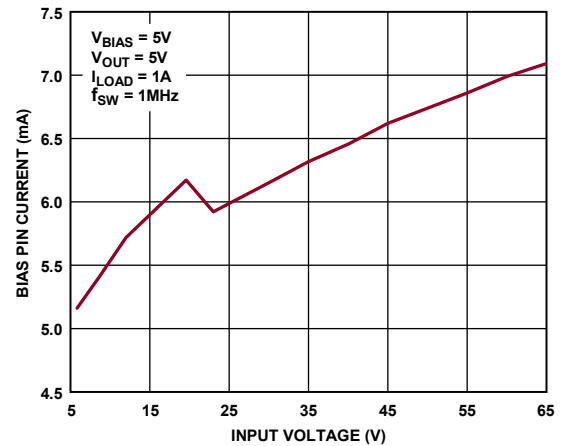
Figure 33. Bias Pin Current
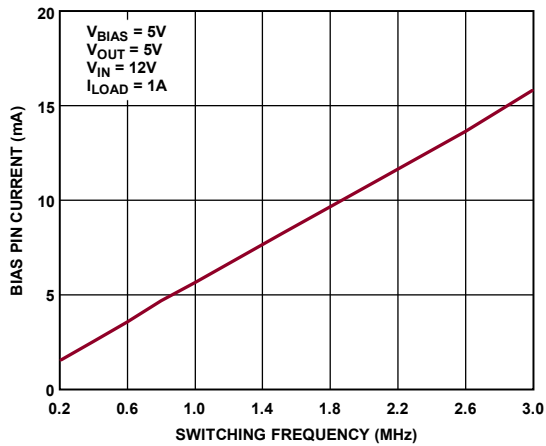
Figure 34. Bias Pin Current
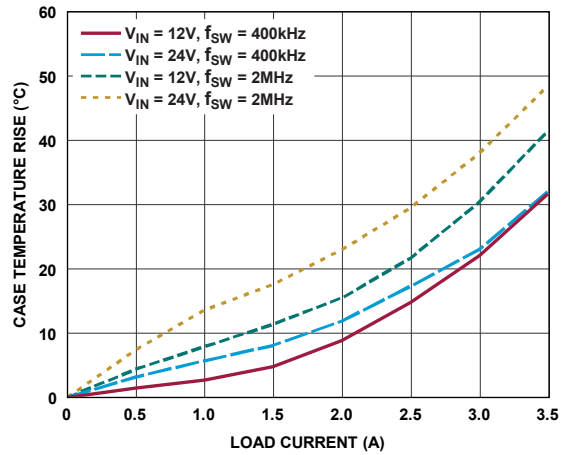
Figure 35. Case Temperature Rise
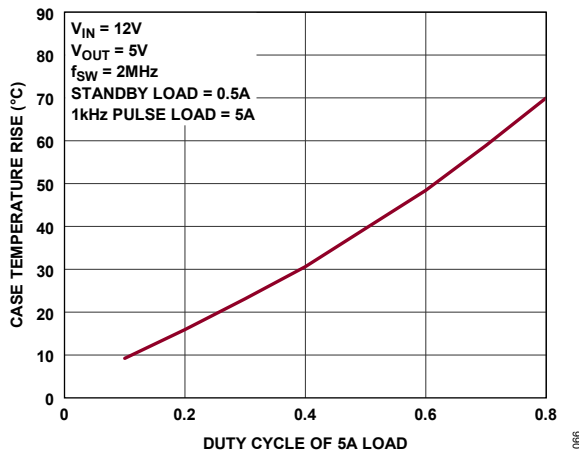
Figure 36. Case Temperature Rise vs. 5A Pulsed Load
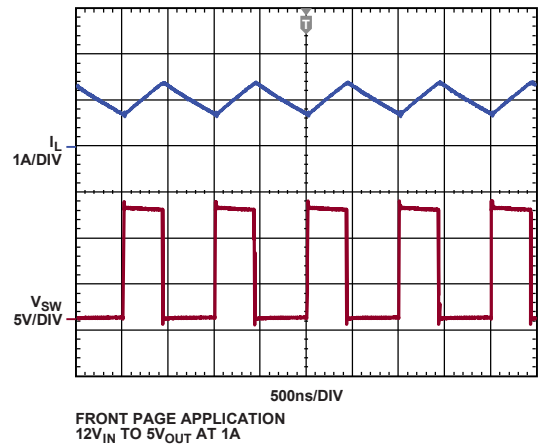
Figure 37. Switching Waveforms, Full Frequency Continuous Operation
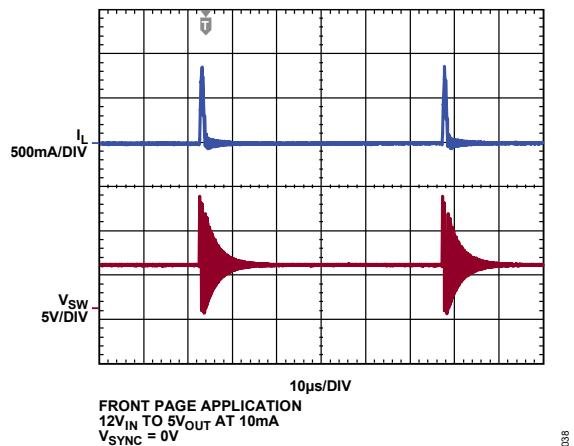
Figure 38. Switching Waveforms, Burst Mode Operation
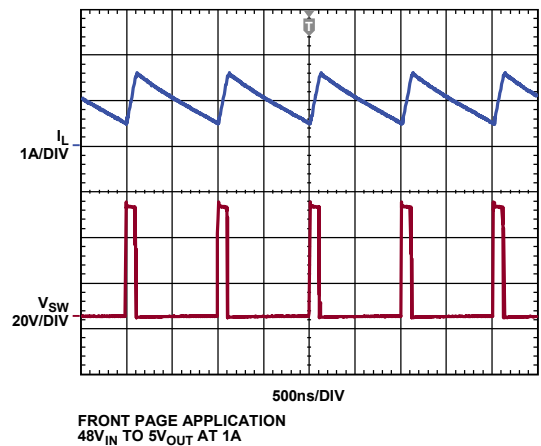
Figure 39. Switching Waveforms
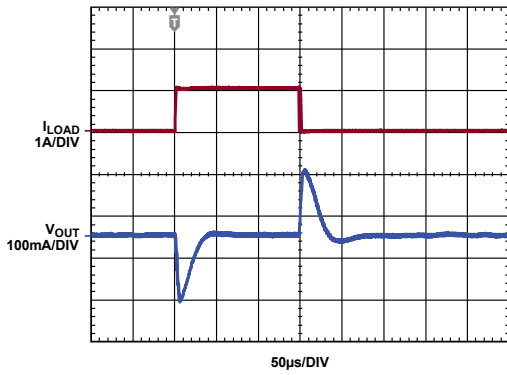
FRONT PAGE APPLICATION
1A TO 2A TRANSIENT
12V$_{IN}$, 5V$_{OUT}$
C$_{OUT}$ = 47µF

Figure 40. Transient Response; Load Current Stepped from 1A to 2A
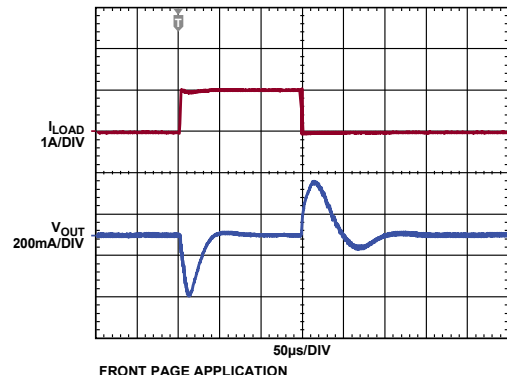
FRONT PAGE APPLICATION
300mA (BURST MODE OPERATION) TO
1.3A TRANSIENT
12V$_{IN}$, 5V$_{OUT}$
C$_{OUT}$ = 47µF

Figure 41. Transient Response; Load Current Stepped from 300mA (Burst Mode Operation) to 1.3A
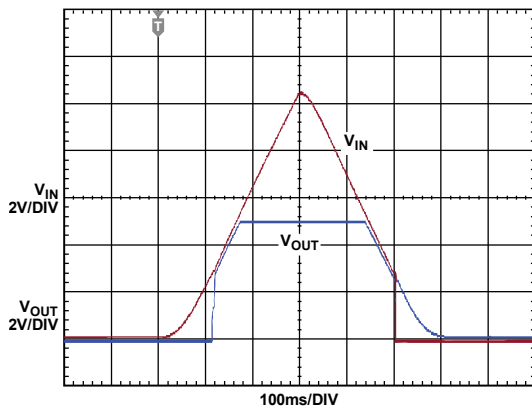
2.5Ω LOAD
(2A IN REGULATION)

Figure 42. Start-Up Dropout Performance
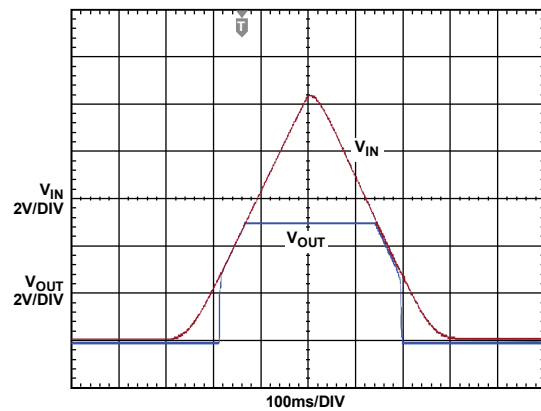
20Ω LOAD
(250mA IN REGULATION)

Figure 43. Start-Up Dropout Performance
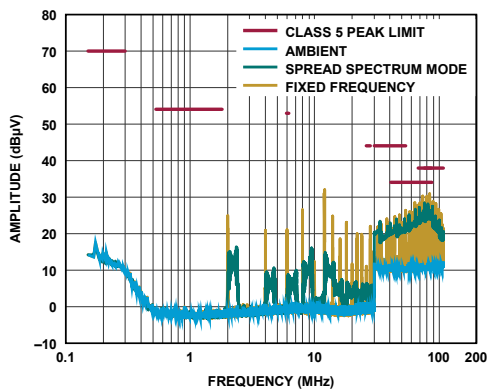
EVAL-LT8641A-AZ DEMO BOARD
(WITH EMI FILTER INSTALLED)
14V INPUT TO 5V OUTPUT AT 3.5A, f$_{SW}$ = 2MHz

Figure 44. Conducted EMI Performance
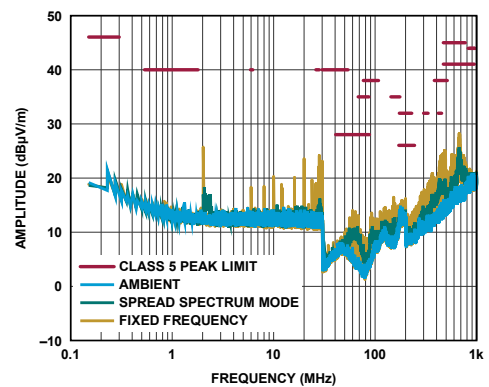
EVAL-LT8641A-AZ DEMO BOARD
(WITH EMI FILTER INSTALLED)
14V INPUT TO 5V OUTPUT AT 3.5A, f$_{SW}$ = 2MHz

Figure 45. Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)

BLOCK DIAGRAM
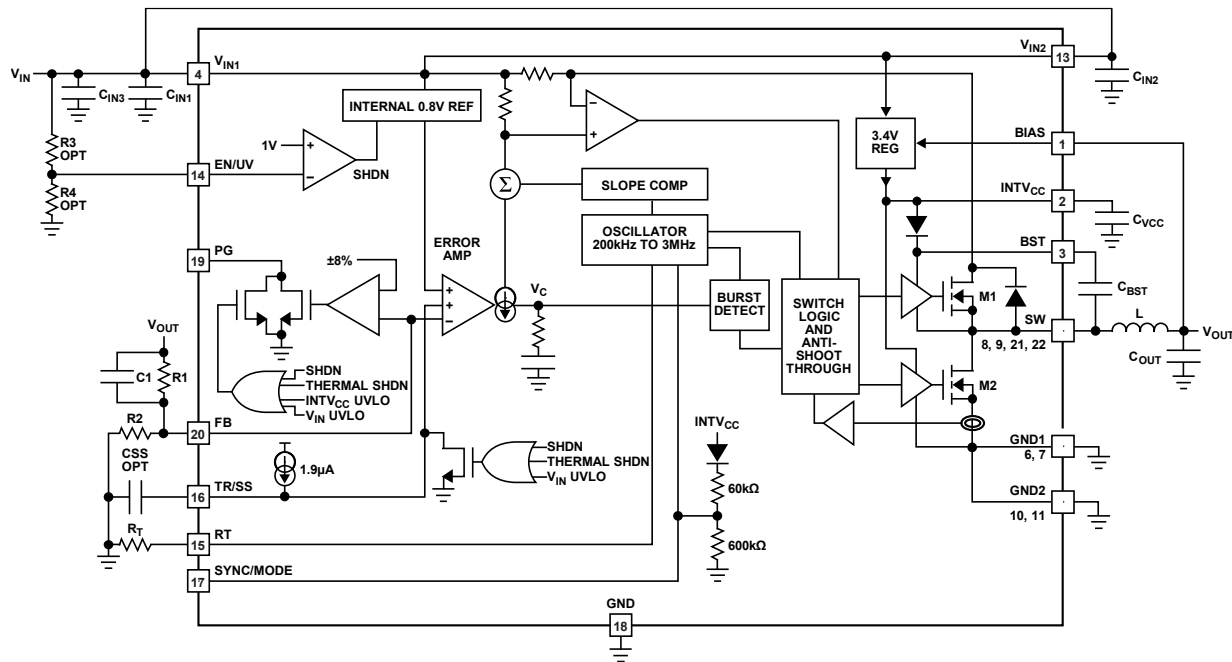
THEORY OF OPERATION

The LT8641A is a monolithic, constant frequency, current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the internal VC node. The error amplifier servos the VC node by comparing the voltage on the VFB pin with an internal 0.81V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the VC voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or inductor current falls to zero. If overload conditions result in more than 5.8A flowing through the bottom switch, the next clock cycle is delayed until switch current returns to a safe level.

If the EN/UV pin is low, the LT8641A is shut down and draws 0.75µA from the input. When the EN/UV pin is above 1.01V, the switching regulator becomes active.

To optimize efficiency at light loads, the LT8641A operates in Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 1.7µA. In a typical application, 2.5µA is consumed from the input supply when regulating with no load. The SYNC/MODE pin is tied low to use Burst Mode operation and can be floated to use pulse-skipping mode. If a clock is applied to the SYNC/MODE pin, the part synchronizes to an external clock frequency and operates in pulse-skipping mode. While in pulse-skipping mode, the oscillator operates continuously, and positive SW transitions are aligned to the clock. During light loads, switch pulses are skipped to regulate the output and the quiescent current becomes

several hundred μA. The SYNC/MODE pin may be tied high for pulse-skipping mode with spread spectrum modulation.

To improve EMI, the LT8641A can operate in spread spectrum mode. This feature varies the clock with a triangular frequency modulation of approximately +20%. For example, if the LT8641A's frequency is programmed to switch at 2MHz, spread spectrum mode modulates the oscillator between 2MHz and 2.4MHz.

To improve efficiency across all loads, source the supply current to internal circuitry from the BIAS pin when biased at 3.1V or above. Else, the internal circuitry draws current from V_{IN}. Connect the BIAS pin to V_{OUT} if the LT8641A output is programmed at 3.3V to 25V.

Comparators monitoring the FB pin voltage pull the PG pin low if the output voltage varies more than ±8% (typical) from the set point, or if a fault condition is present.

The oscillator reduces the LT8641A's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the inductor current when the output voltage is lower than the programmed value that occurs during start-up or overcurrent conditions. When a clock is applied to the SYNC/MODE pin, the SYNC/MODE pin is floated, or held DC high, the frequency foldback is disabled, and the switching frequency slows down only during overcurrent conditions.

APPLICATIONS INFORMATION

Low EMI PCB Layout

The LT8641A is specifically designed to minimize EMI emissions and also to maximize efficiency when switching at high frequencies. For optimal performance, the LT8641A requires the use of multiple V_{IN} bypass capacitors.

Place two small 1µF capacitors as close as possible to the LT8641A: Tie one capacitor to V_{IN1}/GND1; tie a second capacitor to V_{IN2}/ GND2. Place a third capacitor with a larger value, 2.2µF or higher, near V_{IN1} or V_{IN2}.

See *Figure 46* for a recommended PCB layout. For more detail and PCB design files, refer to the LT8641A demo board guide.
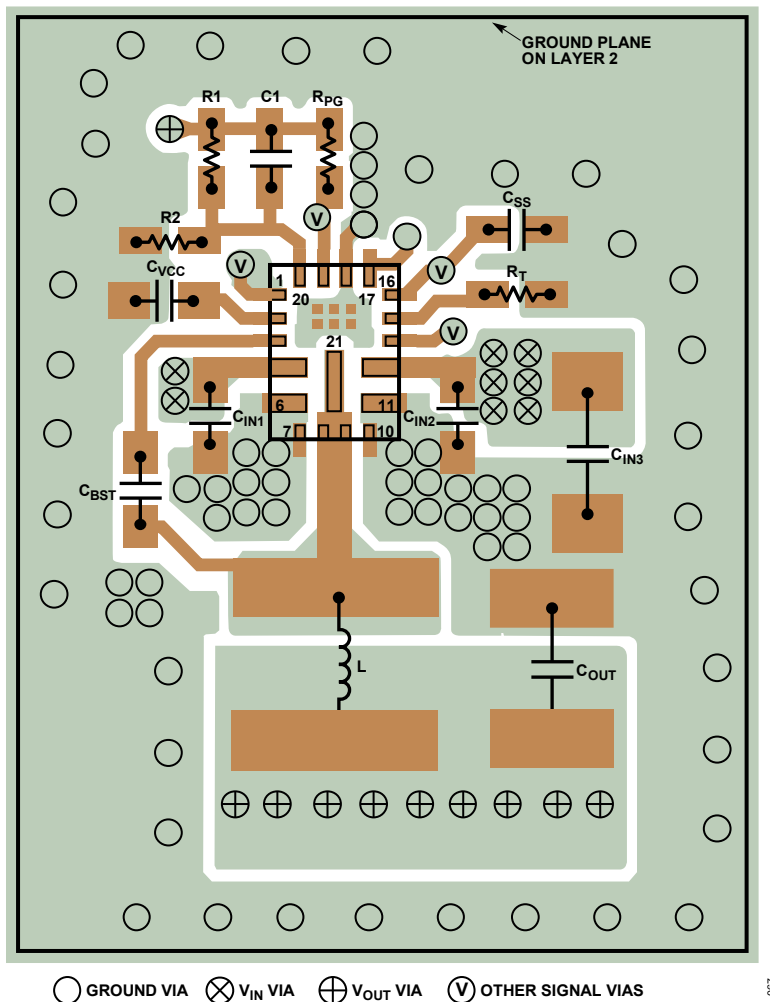
Figure 46. Recommended PCB Layout for the LT8641A

Note that large, switched currents flow in the LT8641A VIN1, VIN2, GND1, and GND2 pins, and the input capacitors (CIN1, CIN2). The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the VIN1/2 and GND1/2 pins. Capacitors with small case size such as 0603 are optimal due to lowest parasitic inductance.

Place the input capacitors, along with the inductor and output capacitors, on the same side of the circuit board, and connect these on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest

to the surface layer. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and RT nodes small so that the ground traces shield them from the SW and BOOST nodes. Solder the exposed pad on the bottom of the package to SW to reduce thermal resistance to ambient. To keep thermal resistance low, extend the ground plane from GND1 and GND2 as much as possible, and add thermal vias to additional ground planes within the circuit board and on the bottom side.

Achieving Ultralow Quiescent Current

To enhance efficiency at light loads, the LT8641A operates in low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and minimizing output voltage ripple. In Burst Mode operation, the LT8641A delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode, the LT8641A consumes 1.7µA.

As the output load decreases, the frequency of single current pulses decreases (see *Figure 47*) and the percentage of time the LT8641A is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter quiescent current approaches 2.5µA for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.

To achieve higher light load efficiency, more energy must be delivered to the output during the single small pulses in Burst Mode operation such that the LT8641A can stay in sleep mode longer between each pulse. This can be achieved using a larger value inductor (i.e., 4.7µH), and should be considered independent of switching frequency when choosing an inductor. For example, while a lower inductor value is typically used for a high switching frequency application, if high light load efficiency is desired, choose a higher inductor value. See the curve in *Typical Performance Characteristics*.

While in Burst Mode operation, the current limit of the top switch is approximately 950mA (see *Figure 48*), resulting in low output voltage ripple. Increasing the output capacitance decreases output ripple proportionally. As load ramps upward from zero, the switching frequency increases, but only up to the switching frequency programmed by the resistor at the RT pin, as shown in *Figure 47*. The output load at which the LT8641A reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice.

(47a)

(47b)
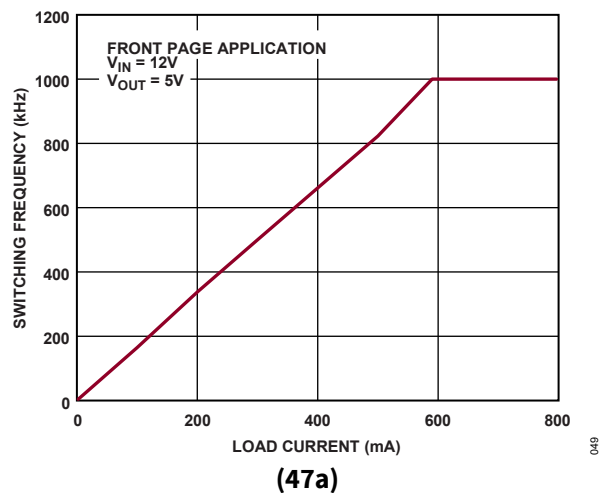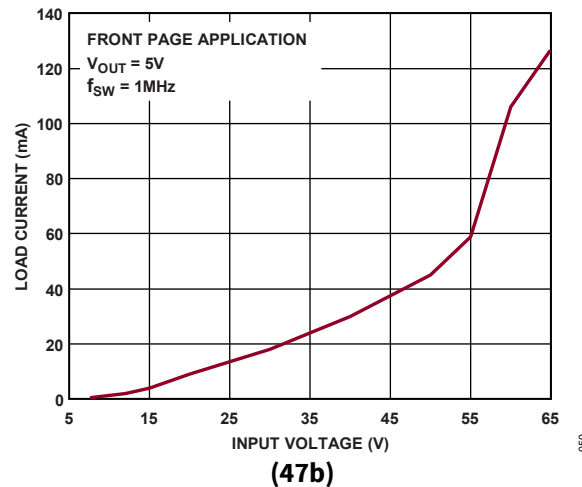
Figure 47. SW Frequency vs Load Information in Burst Mode Operation (47a) and Pulse-Skipping Mode (47b)
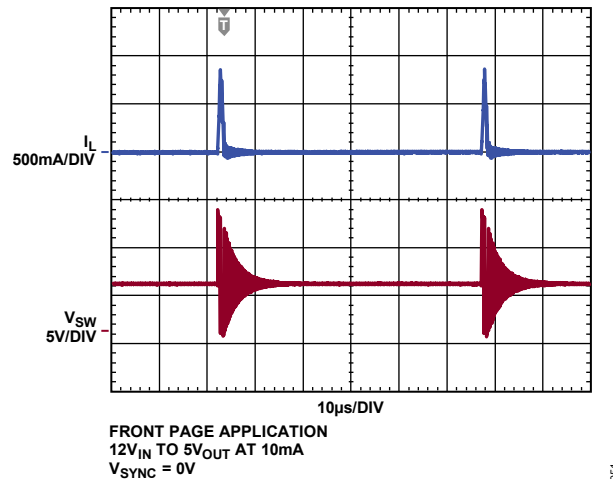
Figure 48. Burst Mode Operation

For some applications, it is desirable for the LT8641A to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First is the clock stays awake at all times and all switching cycles are aligned to the clock. In this mode, much of the internal circuitry is awake at all times, increasing quiescent current to several hundred μA. Second is that full switching frequency is reached at lower output load than in Burst Mode operation (see *Figure 47*). To enable pulse-skipping mode, float the SYNC/MODE pin. When a clock is applied to the SYNC/MODE pin, the LT8641A also operates in pulse-skipping mode.

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to Equation 1.

$$R1 \ = \ R2 \left(\frac{V_{OUT}}{0.81V} - 1\right) \qquad (1)$$

Reference designators refer to the *Block Diagram*. 1% resistors are recommended to maintain output voltage accuracy.

For low input quiescent current and good light-load efficiency, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current, and increases the no-load input current to the converter, which is approximately given by Equation 2.

$$I_Q = 1.7\mu A + (\frac{V_{OUT}}{R1+R2})(\frac{V_{OUT}}{V_{IN}})(\frac{1}{n}) \qquad (2)$$

where 1.7µA is the quiescent current of the LT8641A and the second term is the current in the feedback divider reflected to the input of the buck operating at its light load efficiency "n". For a 3.3V application with R1 = 1M and R2 = 324k, the feedback divider draws 2.5µA. With V_{IN} = 12V and n = 85%, this adds 0.8µA to the 1.7µA quiescent current, resulting in 2.5µA no-load current from the 12V supply. Note that Equation 2 implies that the no-load current is a function of V_{IN}; this is plotted in the section.

When using large FB resistors, connect a 4.7pF to 22pF phase-lead capacitor from V_{OUT} to FB.

Setting the Switching Frequency

The LT8641A uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 3MHz by using a resistor tied from the RT pin to ground. *Table 4* shows the necessary R_T value for a desired switching frequency.

Calculate the R_T resistor required for a desired switching frequency using:

$$R_T = \frac{46.5}{f_{SW}} - 5.2 \qquad (3)$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz.

Table 4. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.2	232
0.3	150
0.4	110
0.5	88.7
0.6	71.5
0.7	60.4
0.8	52.3
1.0	41.2
1.2	33.2
1.4	28.0
1.6	23.7
1.8	20.5
2.0	18.2
2.2	15.8
3.0	10.7

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

Calculate the highest switching frequency ($f_{SW(MAX)}$) for a given application as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}\,(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)})} \qquad (4)$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.4V, ~0.2V, respectively at maximum load), and $t_{ON(MIN)}$ is the minimum top switch on-time (see the *Specifications*). This equation shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

For transient operation, V_{IN} may go as high as the absolute maximum rating of 65V regardless of the R_T value, however the LT8641A reduces switching frequency as necessary to maintain control of inductor current to assure safe operation.

The LT8641A is capable of a maximum duty cycle of approximately 99%, and the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In this mode, the LT8641A skips switch cycles, resulting in a lower switching frequency than programmed by RT.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios, use the following formula to set switching frequency:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \times t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)} \qquad (5)$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.4V, ~0.2V, respectively at maximum load), f_{SW} is the switching frequency (set by RT), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency increases the minimum input voltage, below which cycles are dropped to achieve higher duty cycle.

Inductor Selection and Maximum Output Current

The LT8641A is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions, the LT8641A safely tolerates operation with a saturated inductor due to the use of a high-speed peak-current mode architecture.

A good first choice for the inductor value is:

$$L = \frac{V_{OUT} + V_{SW(BOT)}}{f_{SW}} \qquad (6)$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.15V), and L is the inductor value in µH.

To avoid overheating and poor efficiency, choose an inductor with an RMS current rating greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of the inductor ripple current:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \qquad (7)$$

where ΔI_L is the inductor ripple current as calculated in Equation 9 and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 2A output should use an inductor with an RMS rating of greater than 2A and an I_{SAT} of greater than 3A. During long duration overload or short-circuit conditions, the inductor RMS rating requirement is greater to avoid overheating of the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 0.04Ω, and the core material should be intended for high frequency applications.

The LT8641A limits the peak switch current to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is 8.2A at low duty cycles and decreases linearly to 6.4A at DC = 0.8. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\triangle I_L}{2} \qquad (8)$$

Calculate the peak-to-peak ripple current in the inductor as follows:

$$\triangle I_L = \frac{V_{OUT}}{L \times f_{SW}} \times (1 - \frac{V_{OUT}}{V_{IN(MAX)}}) \qquad (9)$$

where f_{SW} is the switching frequency of the LT8641A, and L is the value of the inductor. Therefore, the maximum output current that the LT8641A delivers depends on the switch current limit, inductor value, and input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$), given the switching frequency, and maximum input voltage used in the desired application.

To achieve higher light load efficiency, more energy must be delivered to the output during the single small pulses in Burst Mode operation such that the LT8641A can stay in sleep mode longer between each pulse. This can be achieved using a larger value inductor (i.e., 4.7µH), and should be considered independent of switching frequency when choosing an inductor. For example, while a lower inductor value is typically used for a high switching frequency application, if high light load efficiency is desired, choose a higher inductor value. See the curve in *Typical Performance Characteristics*.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower and the LT8641A may operate with higher ripple current. This allows use of a physically smaller inductor, or one with a lower DCR, resulting in higher efficiency. Be aware that low inductance may result in discontinuous mode operation, which further reduces maximum load current.

For more information about maximum output current and discontinuous operation, see *Application Note 44*.

For duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid subharmonic oscillation (see Equation 10). See *Application Note 19* for more details.

$$L_{MIN} = \frac{V_{IN} \times (2 \times DC - 1)}{2.5 \times f_{SW}} \qquad (10)$$

where DC is the duty cycle ratio (V_{OUT}/V_{IN}) and f_{SW} is the switching frequency.

Input Capacitors

The V_{IN} of the LT8641A should be bypassed with at least three ceramic capacitors for best performance. Place two small ceramic capacitors of 0.1µF close to the part; one at the V_{IN1}/GND1 pins and a second at V_{IN2}/GND2 pins. These capacitors should be 0402 or 0603 in size. For automotive applications requiring two series input capacitors, place two small 0402 or 0603 at each side of the LT8641A near the V_{IN1}/GND1 and V_{IN2}/GND2 pins.

Place a third, larger ceramic capacitor of 2.2µF or larger close to V_{IN1} or V_{IN2}. See the *Low EMI PCB Layout* section for more details. X7R or X5R capacitors are recommended for best performance across temperature and input voltage variations.

Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8641A circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8641A's voltage rating. This situation is easily avoided (see *Application Note 88*).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8641A to produce the DC output. In this role, it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy to satisfy transient loads and stabilize the LT8641A's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the *Typical Applications Circuits* section.

Use X5R or X7R types for low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and the addition of a feedforward capacitor placed between V_{OUT} and FB. Increasing the output capacitance also decreases the output voltage ripple. A lower value of output capacitor can be used to save space and cost, but transient performance suffers and may cause loop instability. See the *Typical Applications Circuits* section for suggested capacitor values.

When choosing a capacitor, pay special attention to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

Ceramic capacitors are small, robust, and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8641A due to their piezoelectric nature. When in Burst Mode operation, the LT8641A's switching frequency depends on the load current, and at very light loads, the LT8641A can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8641A operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LT8641A. As previously mentioned, a ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the LT8641A circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8641A's rating. This situation is easily avoided (see *Application Note 88*).

Enable Pin

The LT8641A is in shutdown when the EN pin is low and active when the pin is high. The rising threshold of the EN comparator is 1.01V, with 45mV of hysteresis. The EN pin can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN} to EN programs the LT8641A to regulate the output only when V_{IN} is above a desired voltage (see the *Block Diagram*). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source. So, source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. Adjust this threshold by setting the values R3 and R4 such that they satisfy the following equation:

$$V_{IN(EN)} = (\frac{R3}{R4} + 1) \times 1.01V \qquad (11)$$

where the LT8641A remains off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching does not stop until the input falls slightly below $V_{IN(EN)}$.

When operating in Burst Mode operation for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT8641A. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

INTV$_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from V_{IN} that powers the drivers and the internal bias circuitry. The INTV$_{CC}$ can supply enough current for the LT8641A's circuitry and must be bypassed to ground with a minimum of 1µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. To improve efficiency, the internal LDO can also draw current from the BIAS pin when the BIAS pin is at 3.1V or higher. Typically, the BIAS pin can be tied to the output of the LT8641A or to an external supply of 3.3V or above. If BIAS is connected to a supply other than V_{OUT}, be sure to bypass with a local ceramic capacitor. If the BIAS pin is below 3.0V, the internal LDO consumes current from V_{IN}. Applications with high input voltage and high switching frequency, where the internal LDO pulls current from V_{IN}, increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the INTV$_{CC}$ pin.

Output Voltage Tracking and Soft-Start

The LT8641A allows the user to program its output voltage ramp rate with the TR/SS pin. An internal 2µA pulls up the TR/SS pin to INTV$_{CC}$. Putting an external capacitor on TR/SS enables soft starting the output to prevent current surge on the input supply. During the soft-start ramp, the output voltage proportionally tracks the TR/SS pin voltage. For output tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 0.81V, the TR/SS voltage overrides the internal 0.81V reference input to the error amplifier, thus regulating the FB pin voltage to that of the TR/SS pin. When TR/SS is above 0.81V, tracking is disabled, and the feedback voltage regulates to the internal reference voltage. The TR/SS pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the TR/SS pin, which discharges the external soft-start capacitor in the case of fault conditions and restarts the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the EN/UV pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Output Power Good

When the LT8641A's output voltage is within the ±8% window of the regulation point, the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device pulls the PG pin low. To prevent glitching both the upper and lower thresholds, include 0.4% of hysteresis.

The PG pin is also actively pulled low during several fault conditions: EN/UV pin is below 1V, $INTV_{CC}$ has fallen too low, V_{IN} is too low, or thermal shutdown.

Synchronization and Spread Spectrum

To select low ripple Burst Mode operation, tie the SYNC pin below 0.4V (this can be ground or a logic low output). To synchronize the LT8641A oscillator to an external frequency, connect a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys below 0.4V and peaks above 1.5V (up to 6V).

The LT8641A does not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead pulse skips to maintain regulation. The LT8641A may be synchronized over a 200kHz to 3MHz range. Choose the R_T resistor to set the LT8641A switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal is 500kHz and higher, select the R_T for 500kHz. The slope compensation is set by the R_T value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency does not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by R_T, then the slope compensation is sufficient for all synchronization frequencies.

For some applications, it is desirable for the LT8641A to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First is the clock stays awake at all times and all switching cycles are aligned to the clock. Second is that full switching frequency is reached at lower output load than in Burst Mode operation. These two differences come at the expense of increased quiescent current. To enable pulse-skipping mode, the SYNC pin is floated. Leakage current on this pin should be <1µA. See the *Block Diagram* for internal pull-up and pull-down resistance.

The LT8641A features spread spectrum operation to further reduce EMI emissions. To enable spread spectrum operation, tie the SYNC/MODE pin high either to $INTV_{CC}$ (~3.4V) or an external supply of 3V to 4V. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by RT to approximately 20% higher than that value. The modulation frequency is approximately 3kHz. For example, when the LT8641A is programmed to 2MHz, the frequency varies from 2MHz to 2.4MHz at a 3kHz rate. When spread spectrum operation is selected, Burst Mode operation is disabled, and the part runs in pulse-skipping mode.

The LT8641A does not operate in forced continuous mode regardless of SYNC signal.

Shorted and Reversed Input Protection

The LT8641A tolerates a shorted output. Several features are used for protection during output short-circuit and brownout conditions. The first is the switching frequency is folded back while the output is lower than the set point to maintain inductor current control. Second, the bottom switch current is monitored such that if inductor current is beyond safe levels, switching of the top switch is delayed until such time as the inductor current falls to safe levels.

Frequency foldback behavior depends on the state of the SYNC pin: if the SYNC pin is low the switching frequency slows while the output voltage is lower than the programmed level. If the SYNC pin is connected to a clock source, floated, or tied high, the LT8641A stays at the programmed frequency without foldback and only slow switching if the inductor current exceeds safe levels.

There is another situation to consider in systems where the output is held high when the input to the LT8641A is absent. This may occur in battery charging applications or in battery-backup systems where a battery or some other supply is diode ORed with the LT8641A's output. If the V_{IN} pin is allowed to float and the EN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT8641A's internal circuitry pulls its quiescent current through its SW pin. This is acceptable if the system can tolerate several µA in this state. If the EN pin is grounded, the SW pin current drops to near 0.75µA. However, if the V_{IN} pin is grounded while the output is held high, regardless of EN, parasitic body diodes inside the LT8641A can pull current from the output through the SW pin and the V_{IN} pin, which may damage the IC. Figure 49 shows a connection of the V_{IN} and EN/UV pins that allows the LT8641A to run only when the input voltage is present and that protects against a shorted or reversed input.
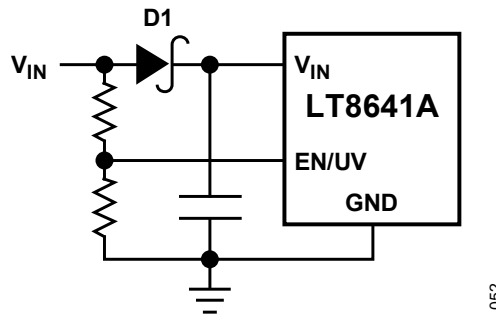
Figure 49. Reverse V_{IN} Protection

Thermal Considerations and Peak Output Current

For higher ambient temperatures, ensure care in the layout of the PCB for good heat sinking of the LT8641A. Solder the ground pins on the bottom of the package to a ground plane. Tie this ground to large copper layers below with thermal vias; these layers spread heat dissipated by the LT8641A. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Estimate the power dissipation within the LT8641A by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. Calculate the die temperature by multiplying the LT8641A power dissipation by the thermal resistance from junction to ambient.

The internal overtemperature protection monitors the junction temperature of the LT8641A. If the junction temperature reaches approximately 160°C, the LT8641A stops switching and indicates a fault condition until the temperature drops about 1°C cooler.
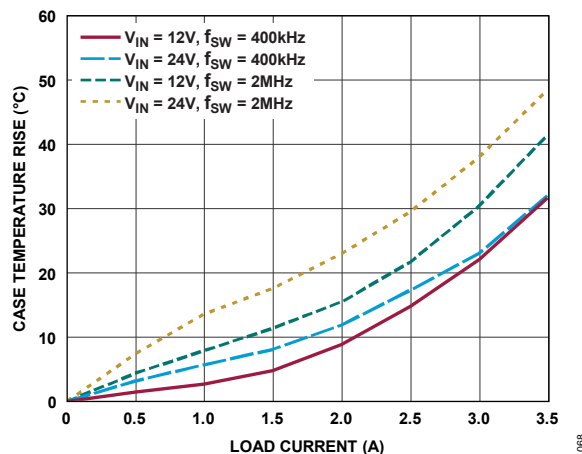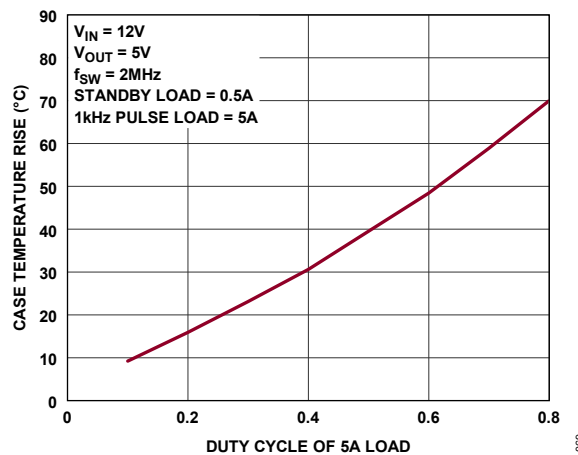

Figure 50. Case Temperature Rise

Temperature rise of the LT8641A is worst when operating at high load, high V_{IN}, and high switching frequency. If the case temperature is too high for a given application, then either V_{IN}, switching frequency, or load current can be decreased to reduce the temperature to an acceptable level. *Figure 50* shows examples of how case temperature rise can be managed by reducing V_{IN}, switching frequency, or load.

The LT8641A's internal power switches are capable of safely delivering up to 5A of peak output current. However, due to thermal limits, the package can only handle 5A loads for short periods of time. This time is determined by how quickly the case temperature approaches the maximum junction rating. *Figure 51* shows an example of how case temperature rise changes with the duty cycle of a 1kHz pulsed 5A load.

The LT8641A's top switch current limit decreases with higher duty cycle operation for slope compensation. This also limits the peak output current the LT8641A can deliver for a given application. See the curve in *Typical Performance Characteristics*.

Figure 51. Case Temperature Rise vs 5A Pulsed Load

TYPICAL APPLICATIONS CIRCUITS
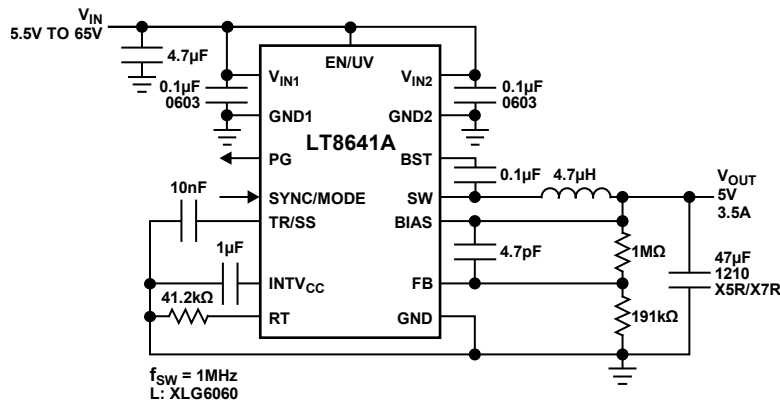
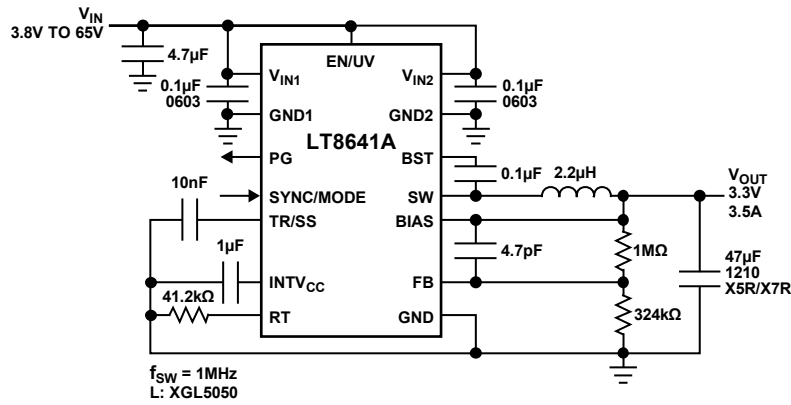*Figure 52. 5V 3.5A Step-Down Converter*
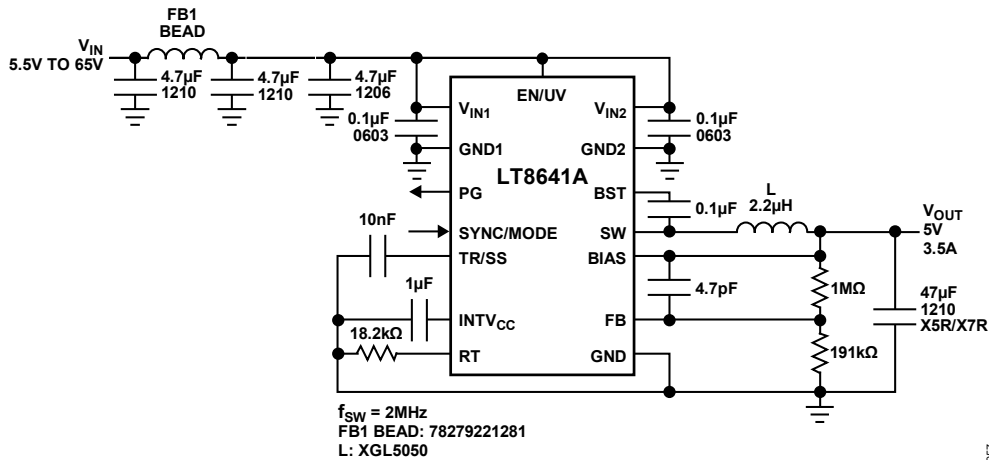

Figure 53. 3.3V, 3.5A Step-Down Converter

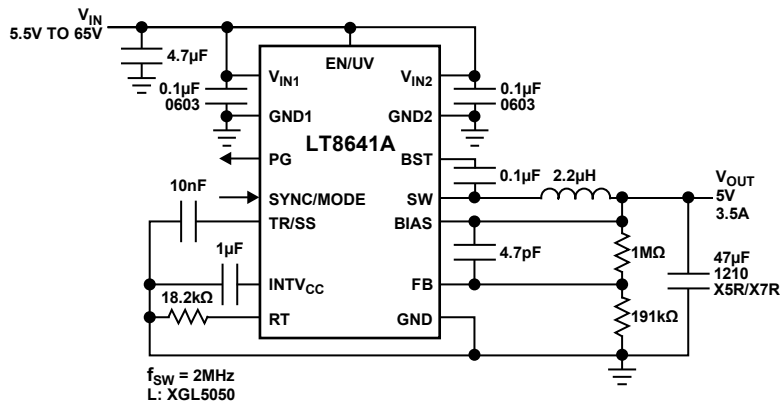*Figure 54. Ultralow EMI 5V, 3.5A Step-Down Converter*

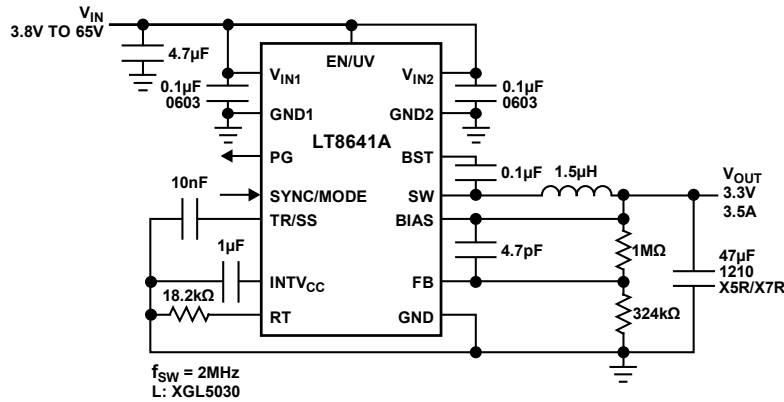*Figure 55. 2MHz 5V, 3.5A Step-Down Converter*

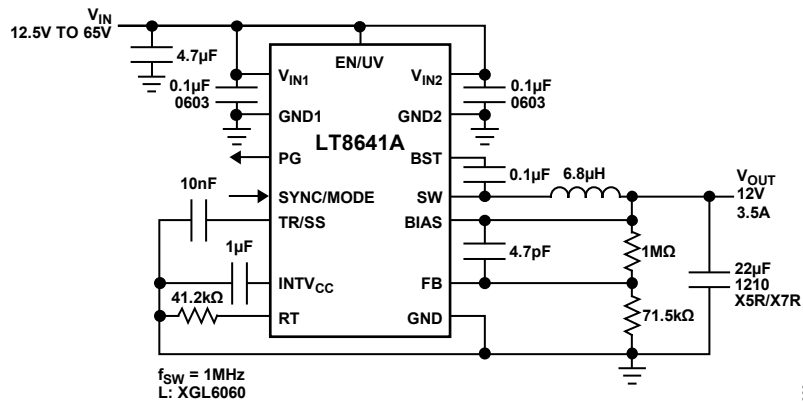*Figure 56. 2MHz 3.3V, 3.5A Step-Down Converter*

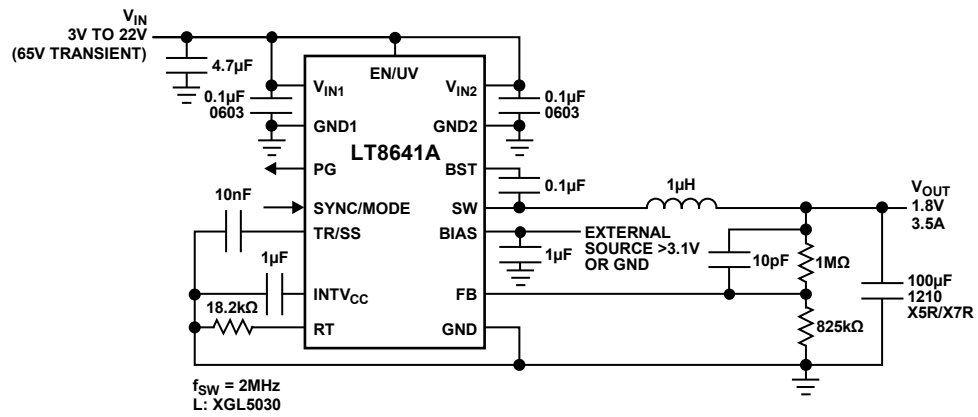
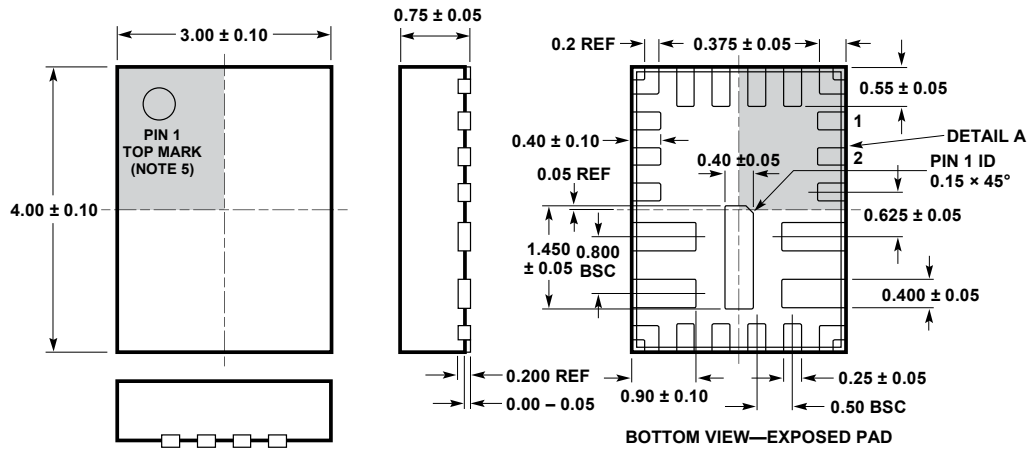*Figure 57. 12V, 3.5A Step-Down Converter*

Figure 58. 2MHz 1.8V, 3.5A Step-Down Converter

OUTLINE DIMENSIONS

UDCM Package
20(18)-Lead Plastic Side Wettable QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-7030 Rev A)
Exposed Pad Variation AA

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

BOTTOM VIEW—EXPOSED PAD

DETAIL A
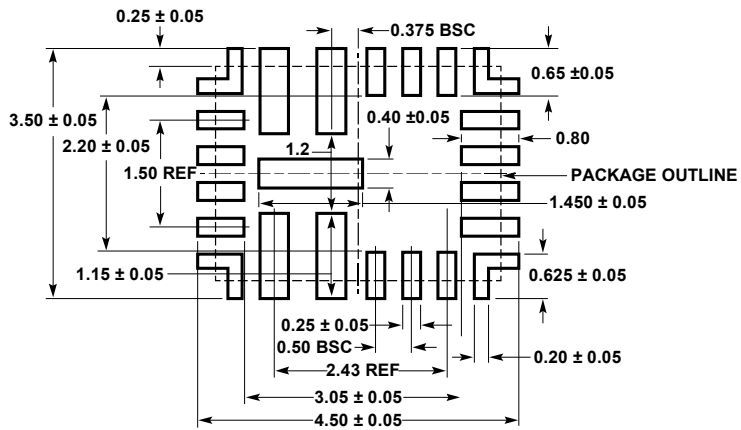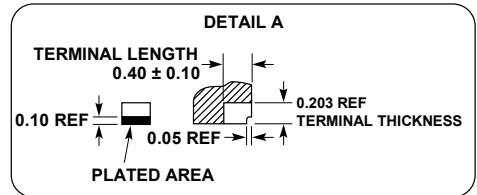
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

Figure 59. Package Drawing

ORDERING GUIDE

Table 5. Ordering Guide

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8641ARUDCM#PBF	LT8641ARUDCM#TRPBF	LHTC	18-Lead (3mm × 4mm) Plastic QFN	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8641ARUDCM#WPBF	LT8641ARUDCM#WTRPBF	LHTC	18-Lead (3mm × 4mm) Plastic QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

RELATED PARTS

Table 6. Related Parts

PART	DESCRIPTION	COMMENTS
LT8641	65V, 3.5A Synchronous Step-Down Silent Switcher with 2.5µA Quiescent Current	$V_{IN(MIN)} = 3V$, $V_{IN(MAX)} = 65V$, $V_{OUT(MIN)} = 0.8V$, $I_Q = 2.5µA$, $I_{SD} < 1µA$, 3mm × 4mm QFN-18
LT8640A	42V, 5A/8A Peak Synchronous Step-Down Silent Switcher with 2.5µA Quiescent Current	$V_{IN(MIN)} = 3.4V$, $V_{IN(MAX)} = 42V$, $V_{OUT(MIN)} = 0.97V$, $I_Q = 2.5µA$, $I_{SD} < 1µA$, 3mm × 4mm QFN-18
LT8645S/ LT8646S	65V, 8A Synchronous Step-Down Silent Switcher 2 with 2.5µA Quiescent Current	$V_{IN(MIN)} = 3.4V$, $V_{IN(MAX)} = 65V$, $V_{OUT(MIN)} = 0.97V$, $I_Q = 2.5µA$, $I_{SD} < 1µA$, 6mm × 4mm LQFN-32
LT8618	High Efficiency 65V/100mA Synchronous Bucks	$V_{IN(MIN)} = 3.4V$, $V_{IN(MAX)} = 65V$, $V_{OUT(MIN)} = 0.778V$, $I_Q = 2.5µA$, $I_{SD} = 1µA$, 2mm × 2mm LQFN-12, 3mm × 2mm DFN-10
LT8620	65V, 2A, 94% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with $I_Q = 2.5µA$	$V_{IN(MIN)} = 3.4V$, $V_{IN(MAX)} = 65V$, $V_{OUT(MIN)} = 0.97V$, $I_Q = 2.5µA$, $I_{SD} < 1µA$, MSOP-16E, 3mm × 5mm QFN-24
LT8608/ LT8608B	42V, 1.5A Synchronous Step-Down Regulator with 2.5µA Quiescent Current	$V_{IN(MIN)} = 3.2V$, $V_{IN(MAX)} = 42V$, $V_{OUT(MIN)} = 0.778V$, $I_Q = 2.5µA$, $I_{SD} = 1µA$, MSOP-10E, 2mm × 2mm DFN-8
LT8609/ LT8609A	42V, 3A, 94% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with $I_Q = 2.5µA$	$V_{IN(MIN)} = 3V$, $V_{IN(MAX)} = 42V$, $V_{OUT(MIN)} = 0.8V$, $I_Q = 2.5µA$, $I_{SD} < 1µA$, MSOP-10E, 3mm x 3mm DFN-10