

## FEATURES

- **Low Noise Voltage: 1.1nV/ $\sqrt{\text{Hz}}$**
- **Low Supply Current: 3.5mA/Amp Max**
- **Low Offset Voltage: 350 $\mu\text{V}$  Max**
- Gain Bandwidth Product:
  - LT6230: 215MHz;  $A_V \geq 1$
  - LT6230-10: 1450MHz;  $A_V \geq 10$
- Wide Supply Range: 3V to 12.6V
- Output Swings Rail-to-Rail
- Common Mode Rejection Ratio: 115dB Typ
- Output Current: 30mA
- Operating Temperature Range:  $-40^\circ\text{C}$  to  $85^\circ\text{C}$
- LT6230 Shutdown to 10 $\mu\text{A}$  Maximum
- LT6230/LT6230-10 in a Low Profile (1mm) ThinSOT™ Package
- Dual LT6231 in 8-Pin SO and Tiny DFN Packages
- LT6232 in a 16-Pin SSOP Package

## APPLICATIONS

- Ultrasound Amplifiers
- Low Noise, Low Power Signal Processing
- Active Filters
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers

## DESCRIPTION

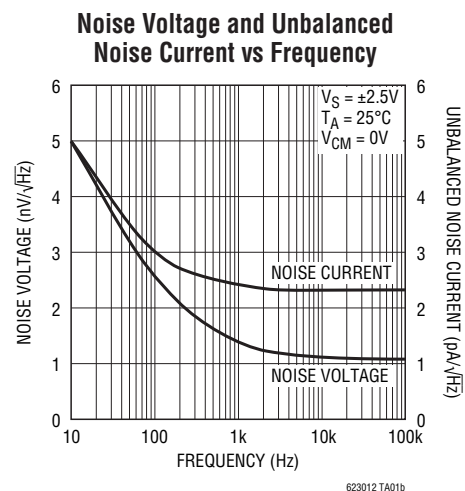
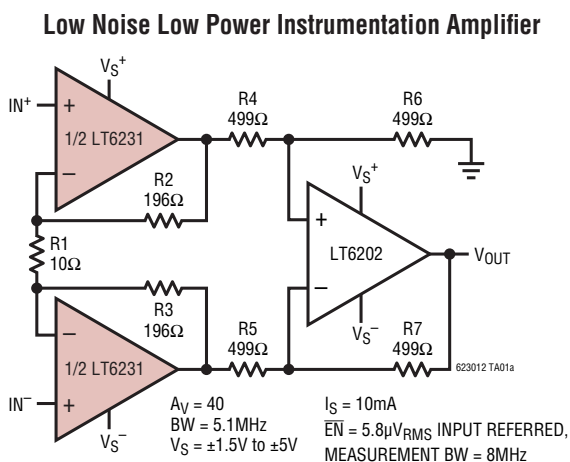
The LT®6230/LT6231/LT6232 are single/dual/quad low noise, rail-to-rail output unity-gain stable op amps that feature 1.1nV/ $\sqrt{\text{Hz}}$  noise voltage and draw only 3.5mA of supply current per amplifier. These amplifiers combine very low noise and supply current with a 215MHz gain-bandwidth product, a 70V/ $\mu\text{s}$  slew rate and are optimized for low supply voltage signal conditioning systems. The LT6230-10 is a single amplifier optimized for higher gain applications resulting in higher gain bandwidth and slew rate. The LT6230 and LT6230-10 include an enable pin that can be used to reduce the supply current to less than 10 $\mu\text{A}$ .

The amplifier family has an output that swings within 50mV of either supply rail to maximize the signal dynamic range in low supply applications and is specified on 3.3V, 5V and  $\pm 5\text{V}$  supplies. The  $e_n \cdot \sqrt{I_{\text{SUPPLY}}}$  product of 1.9 per amplifier is among the most noise efficient of any op amp.

The LT6230/LT6230-10 are available in the 6-lead SOT-23 package and the LT6231 dual is available in the 8-pin SO package with standard pinouts. For compact layouts, the dual is also available in a tiny dual fine pitch leadless package (DFN). The LT6232 is available in the 16-pin SSOP package.

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## TYPICAL APPLICATION



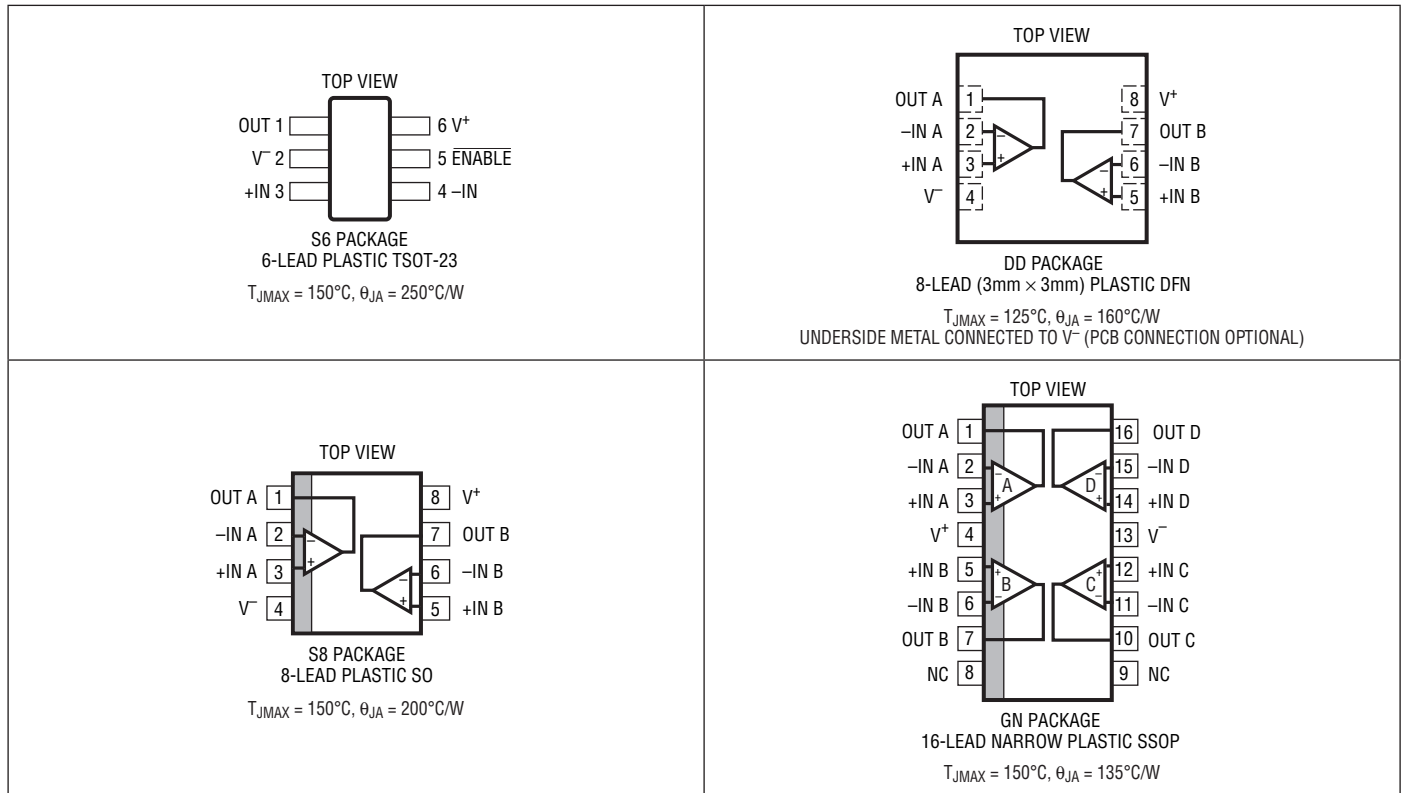
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## ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage ( $V^+$  to  $V^-$ ) ..... 12.6V  
 Input Current (Note 2).....  $\pm 40\text{mA}$   
 Output Short-Circuit Duration (Note 3) ..... Indefinite  
 Operating Temperature Range (Note 4)....  $-40^\circ\text{C}$  to  $85^\circ\text{C}$   
 Specified Temperature Range (Note 5) ....  $-40^\circ\text{C}$  to  $85^\circ\text{C}$   
 Junction Temperature .....  $150^\circ\text{C}$

Junction Temperature (DD Package).....  $125^\circ\text{C}$   
 Storage Temperature Range .....  $-65^\circ\text{C}$  to  $150^\circ\text{C}$   
 Storage Temperature Range  
 (DD Package) .....  $-65^\circ\text{C}$  to  $125^\circ\text{C}$   
 Lead Temperature (Soldering, 10 sec).....  $300^\circ\text{C}$

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6230CS6#PBF	LT6230CS6#TRPBF	LTAfJ	6-Lead Plastic TSOT-23	0°C to 70°C
LT6230IS6#PBF	LT6230IS6#TRPBF	LTAfJ	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6230CS6-10#PBF	LT6230CS6-10#TRPBF	LTAfK	6-Lead Plastic TSOT-23	0°C to 70°C
LT6230IS6-10#PBF	LT6230IS6-10#TRPBF	LTAfK	6-Lead Plastic TSOT-23	-40°C to 85°C
LT6231CS8#PBF	LT6230CS8#TRPBF	6231	8-Lead Plastic SO	0°C to 70°C
LT6231IS8#PBF	LT6230IS8#TRPBF	6231I	8-Lead Plastic SO	-40°C to 85°C
LT6231CDD#PBF	LT6231CDD#TRPBF	LAEU	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT6231IDD#PBF	LT6231IDD#TRPBF	LAEU	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LT6232CGN#PBF	LT6232CGN#TRPBF	6232	16-Lead Narrow Plastic SSOP	0°C to 70°C
LT6232IGN#PBF	LT6232IGN#TRPBF	6232I	16-Lead Narrow Plastic SSOP	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

## ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_S = 5\text{V}$ , $0\text{V}$ ; $V_S = 3.3\text{V}$ , $0\text{V}$ ; $V_{CM} = V_{OUT} = \text{half supply}$ , ENABLE = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage	LT6230S6, LT6230S6-10		100	500	$\mu\text{V}$
		LT6231S8, LT6232GN LT6231DD		50 75	350 450	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)			100	600	$\mu\text{V}$
$I_B$	Input Bias Current			5	10	$\mu\text{A}$
		$I_B$ Match (Channel-to-Channel) (Note 6)		0.1	0.9	$\mu\text{A}$
$I_{OS}$	Input Offset Current			0.1	0.6	$\mu\text{A}$
		Input Noise Voltage	0.1Hz to 10Hz		180	$\text{nV}_{P-P}$
$e_n$	Input Noise Voltage Density	$f = 10\text{kHz}$ , $V_S = 5\text{V}$		1.1	1.7	$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input Noise Current Density, Balanced Source Input Noise Current Density, Unbalanced Source	$f = 10\text{kHz}$ , $V_S = 5\text{V}$ , $R_S = 10\text{k}$		1		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 10\text{kHz}$ , $V_S = 5\text{V}$ , $R_S = 10\text{k}$		2.4		$\text{pA}/\sqrt{\text{Hz}}$
	Input Resistance	Common Mode		6.5		$\text{M}\Omega$
		Differential Mode		7.5		$\text{k}\Omega$
$C_{IN}$	Input Capacitance	Common Mode		2.9		$\text{pF}$
		Differential Mode		7.7		$\text{pF}$
$A_{VOL}$	Large-Signal Gain	$V_S = 5\text{V}$ , $V_O = 0.5\text{V}$ to $4.5\text{V}$ , $R_L = 10\text{k}$ to $V_S/2$	105	200		$\text{V}/\text{mV}$
		$V_S = 5\text{V}$ , $V_O = 0.5\text{V}$ to $4.5\text{V}$ , $R_L = 1\text{k}$ to $V_S/2$	21	40		$\text{V}/\text{mV}$
		$V_S = 5\text{V}$ , $V_O = 1\text{V}$ to $4\text{V}$ , $R_L = 100\Omega$ to $V_S/2$	5.4	9		$\text{V}/\text{mV}$
		$V_S = 3.3\text{V}$ , $V_O = 0.65\text{V}$ to $2.65\text{V}$ , $R_L = 10\text{k}$ to $V_S/2$	90	175		$\text{V}/\text{mV}$
$V_{CM}$	Input Voltage Range	Guaranteed by CMRR, $V_S = 5\text{V}$ , $0\text{V}$	1.5		4	$\text{V}$
		Guaranteed by CMRR, $V_S = 3.3\text{V}$ , $0\text{V}$	1.15		2.65	$\text{V}$
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}$ , $V_{CM} = 1.5\text{V}$ to $4\text{V}$	90	115		$\text{dB}$
		$V_S = 3.3\text{V}$ , $V_{CM} = 1.15\text{V}$ to $2.65\text{V}$	90	115		$\text{dB}$
	CMRR Match (Channel-to-Channel) (Note 6)	$V_S = 5\text{V}$ , $V_{CM} = 1.5\text{V}$ to $4\text{V}$	84	120		$\text{dB}$

## ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_S = 5\text{V}$ , $0\text{V}$ ; $V_S = 3.3\text{V}$ , $0\text{V}$ ; $V_{CM} = V_{OUT} = \text{half supply}$ , **ENABLE = 0V, unless otherwise noted.**

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	$V_S = 3\text{V to }10\text{V}$	90	115		dB
	PSRR Match (Channel-to-Channel) (Note 6)	$V_S = 3\text{V to }10\text{V}$	84	115		dB
	Minimum Supply Voltage (Note 7)		3			V
$V_{OL}$	Output Voltage Swing Low (Note 8)	No Load		4	40	mV
		$I_{SINK} = 5\text{mA}$		85	190	mV
		$V_S = 5\text{V}$ , $I_{SINK} = 20\text{mA}$		240	460	mV
		$V_S = 3.3\text{V}$ , $I_{SINK} = 15\text{mA}$		185	350	mV
$V_{OH}$	Output Voltage Swing High (Note 8)	No Load		5	50	mV
		$I_{SOURCE} = 5\text{mA}$		90	200	mV
		$V_S = 5\text{V}$ , $I_{SOURCE} = 20\text{mA}$		325	600	mV
		$V_S = 3.3\text{V}$ , $I_{SOURCE} = 15\text{mA}$		250	400	mV
$I_{SC}$	Short-Circuit Current	$V_S = 5\text{V}$	$\pm 30$	$\pm 45$		mA
		$V_S = 3.3\text{V}$	$\pm 25$	$\pm 40$		mA
$I_S$	Supply Current per Amplifier			3.15	3.5	mA
	Disabled Supply Current per Amplifier	ENABLE = $V^+ - 0.35\text{V}$		0.2	10	$\mu\text{A}$
$I_{ENABLE}$	ENABLE Pin Current	ENABLE = $0.3\text{V}$		-25	-75	$\mu\text{A}$
$V_L$	ENABLE Pin Input Voltage Low				0.3	V
$V_H$	ENABLE Pin Input Voltage High		$V^+ - 0.35\text{V}$			V
	Output Leakage Current	ENABLE = $V^+ - 0.35\text{V}$ , $V_O = 1.5\text{V to }3.5\text{V}$		0.2	10	$\mu\text{A}$
$t_{ON}$	Turn-On Time	ENABLE = $5\text{V to }0\text{V}$ , $R_L = 1\text{k}$ , $V_S = 5\text{V}$		300		ns
$t_{OFF}$	Turn-Off Time	ENABLE = $0\text{V to }5\text{V}$ , $R_L = 1\text{k}$ , $V_S = 5\text{V}$		41		$\mu\text{s}$
GBW	Gain-Bandwidth Product	Frequency = $1\text{MHz}$ , $V_S = 5\text{V}$		200		MHz
		LT6230-10		1300		MHz
SR	Slew Rate	$V_S = 5\text{V}$ , $A_V = -1$ , $R_L = 1\text{k}$ , $V_O = 1.5\text{V to }3.5\text{V}$	42	60		$\text{V}/\mu\text{s}$
		LT6230-10, $V_S = 5\text{V}$ , $A_V = -10$ , $R_L = 1\text{k}$ , $V_O = 1.5\text{V to }3.5\text{V}$		250		$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth	$V_S = 5\text{V}$ , $V_{OUT} = 3V_{P-P}$ (Note 9)	4.8	6.3		MHz
		LT6230-10, HD2 = HD3 = $\leq 1\%$		11		MHz
$t_S$	Settling Time (LT6230, LT6231, LT6232)	0.1%, $V_S = 5\text{V}$ , $V_{STEP} = 2\text{V}$ , $A_V = -1$ , $R_L = 1\text{k}$		55		ns

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the 0°C < T<sub>A</sub> < 70°C temperature range. V<sub>S</sub> = 5V, 0V; V<sub>S</sub> = 3.3V, 0V; V<sub>CM</sub> = V<sub>OUT</sub> = half supply, ENABLE = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OS</sub>	Input Offset Voltage	LT6230CS6, LT6230CS6-10	●		600	μV
		LT6231CS8, LT6232CGN	●		450	μV
		LT6231CDD	●		550	μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●		800	μV
V <sub>OS TC</sub>	Input Offset Voltage Drift (Note 10)	V <sub>CM</sub> = Half Supply	●	0.5	3	μV/°C
I <sub>B</sub>	Input Bias Current		●		11	μA
	I <sub>B</sub> Match (Channel-to-Channel) (Note 6)		●		1	μA
I <sub>OS</sub>	Input Offset Current		●		0.7	μA
A <sub>VOL</sub>	Large-Signal Gain	V <sub>S</sub> = 5V, V <sub>O</sub> = 0.5V to 4.5V, R <sub>L</sub> = 10k to V <sub>S</sub> /2	●	78		V/mV
		V <sub>S</sub> = 5V, V <sub>O</sub> = 0.5V to 4.5V, R <sub>L</sub> = 1k to V <sub>S</sub> /2	●	17		V/mV
		V <sub>S</sub> = 5V, V <sub>O</sub> = 1V to 4V, R <sub>L</sub> = 100Ω to V <sub>S</sub> /2	●	4.1		V/mV
		V <sub>S</sub> = 3.3V, V <sub>O</sub> = 0.65V to 2.65V, R <sub>L</sub> = 10k to V <sub>S</sub> /2	●	66		V/mV
		V <sub>S</sub> = 3.3V, V <sub>O</sub> = 0.65V to 2.65V, R <sub>L</sub> = 1k to V <sub>S</sub> /2	●	13		V/mV
V <sub>CM</sub>	Input Voltage Range	Guaranteed by CMRR	●			
		V <sub>S</sub> = 5V, 0V	●	1.5	4	V
		V <sub>S</sub> = 3.3V, 0V	●	1.15	2.65	V
CMRR	Common Mode Rejection Ratio	V <sub>S</sub> = 5V, V <sub>CM</sub> = 1.5V to 4V	●	90		dB
		V <sub>S</sub> = 3.3V, V <sub>CM</sub> = 1.15V to 2.65V	●	85		dB
		CMRR Match (Channel-to-Channel) (Note 6)	●	84		dB
PSRR	Power Supply Rejection Ratio	V <sub>S</sub> = 3V to 10V	●	85		dB
		PSRR Match (Channel-to-Channel) (Note 6)	●	79		dB
		Minimum Supply Voltage (Note 7)	●	3		V
V <sub>OL</sub>	Output Voltage Swing Low (Note 8)	No Load	●		50	mV
		I <sub>SINK</sub> = 5mA	●		200	mV
		V <sub>S</sub> = 5V, I <sub>SINK</sub> = 20mA	●		500	mV
		V <sub>S</sub> = 3.3V, I <sub>SINK</sub> = 15mA	●		380	mV
V <sub>OH</sub>	Output Voltage Swing High (Note 8)	No Load	●		60	mV
		I <sub>SOURCE</sub> = 5mA	●		215	mV
		V <sub>S</sub> = 5V, I <sub>SOURCE</sub> = 20mA	●		650	mV
		V <sub>S</sub> = 3.3V, I <sub>SOURCE</sub> = 15mA	●		430	mV
I <sub>SC</sub>	Short-Circuit Current	V <sub>S</sub> = 5V	●	±25		mA
		V <sub>S</sub> = 3.3V	●	±20		mA
I <sub>S</sub>	Supply Current per Amplifier		●		4.2	mA
	Disabled Supply Current per Amplifier	ENABLE = V <sup>+</sup> - 0.25V	●	1		μA
I <sub>ENABLE</sub>	ENABLE Pin Current	ENABLE = 0.3V	●		-85	μA
V <sub>L</sub>	ENABLE Pin Input Voltage Low		●		0.3	V
V <sub>H</sub>	ENABLE Pin Input Voltage High		●	V <sup>+</sup> - 0.25V		V
	Output Leakage Current	ENABLE = V <sup>+</sup> - 0.25V, V <sub>O</sub> = 1.5V to 3.5V	●	1		μA
t <sub>ON</sub>	Turn-On Time	ENABLE = 5V to 0V, R <sub>L</sub> = 1k, V <sub>S</sub> = 5V	●	300		ns
t <sub>OFF</sub>	Turn-Off Time	ENABLE = 0V to 5V, R <sub>L</sub> = 1k, V <sub>S</sub> = 5V	●	65		μs
SR	Slew Rate	V <sub>S</sub> = 5V, A <sub>V</sub> = -1, R <sub>L</sub> = 1k, V <sub>O</sub> = 1.5V to 3.5V	●	35		V/μs
		LT6230-10, A <sub>V</sub> = -10, R <sub>L</sub> = 1k, V <sub>O</sub> = 1.5V to 3.5V	●	225		V/μs
FPBW	Full-Power Bandwidth (Note 9)	V <sub>S</sub> = 5V, V <sub>OUT</sub> = 3V <sub>P-P</sub> ; LT6230C, LT6231C, LT6232C	●	3.7		MHz

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$  temperature range.  $V_S = 5\text{V}, 0\text{V}$ ;  $V_S = 3.3\text{V}, 0\text{V}$ ;  $V_{CM} = V_{OUT} = \text{half supply}$ ,  $\overline{\text{ENABLE}} = 0\text{V}$ , unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage	LT6230IS6, LT6230IS6-10	●		700	$\mu\text{V}$
		LT6231IS8, LT6232IGN	●		550	$\mu\text{V}$
		LT6231IDD	●		650	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●		1000	$\mu\text{V}$
$V_{OS\ TC}$	Input Offset Voltage Drift (Note 10)	$V_{CM} = \text{Half Supply}$	●	0.5	3	$\mu\text{V}/^{\circ}\text{C}$
$I_B$	Input Bias Current		●		12	$\mu\text{A}$
	$I_B$ Match (Channel-to-Channel) (Note 6)		●		1.1	$\mu\text{A}$
$I_{OS}$	Input Offset Current		●		0.8	$\mu\text{A}$
$A_{VOL}$	Large-Signal Gain	$V_S = 5\text{V}, V_O = 0.5\text{V to } 4.5\text{V}, R_L = 10\text{k to } V_S/2$	●	72		$\text{V/mV}$
		$V_S = 5\text{V}, V_O = 0.5\text{V to } 4.5\text{V}, R_L = 1\text{k to } V_S/2$	●	16		$\text{V/mV}$
		$V_S = 5\text{V}, V_O = 1\text{V to } 4\text{V}, R_L = 100\Omega \text{ to } V_S/2$	●	3.6		$\text{V/mV}$
		$V_S = 3.3\text{V}, V_O = 0.65\text{V to } 2.65\text{V}, R_L = 10\text{k to } V_S/2$	●	60		$\text{V/mV}$
		$V_S = 3.3\text{V}, V_O = 0.65\text{V to } 2.65\text{V}, R_L = 1\text{k to } V_S/2$	●	12		$\text{V/mV}$
$V_{CM}$	Input Voltage Range	Guaranteed by CMRR	●			
		$V_S = 5\text{V}, 0\text{V}$ $V_S = 3.3\text{V}, 0\text{V}$	●	1.5 1.15	4 2.65	V V
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}, V_{CM} = 1.5\text{V to } 4\text{V}$ $V_S = 3.3\text{V}, V_{CM} = 1.15\text{V to } 2.65\text{V}$	●	90		dB
	CMRR Match (Channel-to-Channel) (Note 6)	$V_S = 5\text{V}, V_{CM} = 1.5\text{V to } 4\text{V}$	●	85		dB
PSRR	Power Supply Rejection Ratio	$V_S = 3\text{V to } 10\text{V}$	●	85		dB
	PSRR Match (Channel-to-Channel) (Note 6)	$V_S = 3\text{V to } 10\text{V}$	●	79		dB
	Minimum Supply Voltage (Note 7)		●	3		V
$V_{OL}$	Output Voltage Swing Low (Note 8)	No Load	●		60	mV
		$I_{SINK} = 5\text{mA}$	●		210	mV
		$V_S = 5\text{V}, I_{SINK} = 15\text{mA}$	●		510	mV
		$V_S = 3.3\text{V}, I_{SINK} = 15\text{mA}$	●		390	mV
$V_{OH}$	Output Voltage Swing High (Note 6)	No Load	●		70	mV
		$I_{SOURCE} = 5\text{mA}$	●		220	mV
		$V_S = 5\text{V}, I_{SOURCE} = 20\text{mA}$	●		675	mV
		$V_S = 3.3\text{V}, I_{SOURCE} = 15\text{mA}$	●		440	mV
$I_{SC}$	Short-Circuit Current	$V_S = 5\text{V}$	●	$\pm 15$		mA
		$V_S = 3.3\text{V}$	●	$\pm 15$		mA
$I_S$	Supply Current per Amplifier		●		4.4	mA
	Disabled Supply Current per Amplifier	$\overline{\text{ENABLE}} = V^+ - 0.2\text{V}$	●	1		$\mu\text{A}$
$I_{\overline{\text{ENABLE}}}$	ENABLE Pin Current	$\overline{\text{ENABLE}} = 0.3\text{V}$	●		-100	$\mu\text{A}$
$V_L$	ENABLE Pin Input Voltage Low		●		0.3	V
$V_H$	ENABLE Pin Input Voltage High		●	$V^+ - 0.2\text{V}$		V
	Output Leakage Current	$\overline{\text{ENABLE}} = V^+ - 0.2\text{V}, V_O = 1.5\text{V to } 3.5\text{V}$	●	1		$\mu\text{A}$
$t_{ON}$	Turn-On Time	$\overline{\text{ENABLE}} = 5\text{V to } 0\text{V}, R_L = 1\text{k}, V_S = 5\text{V}$	●	300		ns
$t_{OFF}$	Turn-Off Time	$\overline{\text{ENABLE}} = 0\text{V to } 5\text{V}, R_L = 1\text{k}, V_S = 5\text{V}$	●	72		$\mu\text{s}$
SR	Slew Rate	$V_S = 5\text{V}, A_V = -1, R_L = 1\text{k}, V_O = 1.5\text{V to } 3.5\text{V}$	●	31		$\text{V}/\mu\text{s}$
		LT6230-10, $A_V = -10, R_L = 1\text{k}, V_O = 1.5\text{V to } 3.5\text{V}$	●	185		$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth (Note 9)	$V_S = 5\text{V}, V_{OUT} = 3\text{V}_{P-P}$ ; LT6230I, LT6231I, LT6232I	●	3.3		MHz

**ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$ ,  $\overline{\text{ENABLE}} = 0\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{OS}}$	Input Offset Voltage	LT6230, LT6230-10		100	500	$\mu\text{V}$
		LT6231S8, LT6232GN		50	350	$\mu\text{V}$
		LT6231DD		75	450	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)			100	600	$\mu\text{V}$
$I_{\text{B}}$	Input Bias Current			5	10	$\mu\text{A}$
	$I_{\text{B}}$ Match (Channel-to-Channel) (Note 6)			0.1	0.9	$\mu\text{A}$
$I_{\text{OS}}$	Input Offset Current			0.1	0.6	$\mu\text{A}$
	Input Noise Voltage	0.1Hz to 10Hz		180		$\text{nV}_{\text{P-P}}$
$e_{\text{n}}$	Input Noise Voltage Density	$f = 10\text{kHz}$		1.1	1.7	$\text{nV}/\sqrt{\text{Hz}}$
$i_{\text{n}}$	Input Noise Current Density, Balanced Source	$f = 10\text{kHz}$ , $R_{\text{S}} = 10\text{k}$		1		$\text{pA}/\sqrt{\text{Hz}}$
	Input Noise Current Density, Unbalanced Source	$f = 10\text{kHz}$ , $R_{\text{S}} = 10\text{k}$		2.4		$\text{pA}/\sqrt{\text{Hz}}$
	Input Resistance	Common Mode		6.5		$\text{M}\Omega$
		Differential Mode		7.5		$\text{k}\Omega$
$C_{\text{IN}}$	Input Capacitance	Common Mode		2.4		$\text{pF}$
		Differential Mode		6.5		$\text{pF}$
$A_{\text{VOL}}$	Large-Signal Gain	$V_{\text{O}} = \pm 4.5\text{V}$ , $R_{\text{L}} = 10\text{k}$	140	260		$\text{V}/\text{mV}$
		$V_{\text{O}} = \pm 4.5\text{V}$ , $R_{\text{L}} = 1\text{k}$	35	65		$\text{V}/\text{mV}$
		$V_{\text{O}} = \pm 2\text{V}$ , $R_{\text{L}} = 100\Omega$	8.5	16		$\text{V}/\text{mV}$
$V_{\text{CM}}$	Input Voltage Range	Guaranteed by CMRR	-3		4	$\text{V}$
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -3\text{V}$ to $4\text{V}$	95	120		$\text{dB}$
	CMRR Match (Channel-to-Channel) (Note 6)	$V_{\text{CM}} = -3\text{V}$ to $4\text{V}$	89	125		$\text{dB}$
PSRR	Power Supply Rejection Ratio	$V_{\text{S}} = \pm 1.5\text{V}$ to $\pm 5\text{V}$	90	115		$\text{dB}$
	PSRR Match (Channel-to-Channel) (Note 6)	$V_{\text{S}} = \pm 1.5\text{V}$ to $\pm 5\text{V}$	84	115		$\text{dB}$
$V_{\text{OL}}$	Output Voltage Swing Low (Note 8)	No Load		4	40	$\text{mV}$
		$I_{\text{SINK}} = 5\text{mA}$		85	190	$\text{mV}$
		$I_{\text{SINK}} = 20\text{mA}$		240	460	$\text{mV}$
$V_{\text{OH}}$	Output Voltage Swing High (Note 8)	No Load		5	50	$\text{mV}$
		$I_{\text{SOURCE}} = 5\text{mA}$		90	200	$\text{mV}$
		$I_{\text{SOURCE}} = 20\text{mA}$		325	600	$\text{mV}$
$I_{\text{SC}}$	Short-Circuit Current		$\pm 30$			$\text{mA}$
$I_{\text{S}}$	Supply Current per Amplifier			3.3	3.9	$\text{mA}$
	Disabled Supply Current per Amplifier	$\overline{\text{ENABLE}} = 4.65\text{V}$		0.2		$\mu\text{A}$
$I_{\overline{\text{ENABLE}}}$	$\overline{\text{ENABLE}}$ Pin Current	$\overline{\text{ENABLE}} = 0.3\text{V}$		-35	-85	$\mu\text{A}$
$V_{\text{L}}$	$\overline{\text{ENABLE}}$ Pin Input Voltage Low				0.3	$\text{V}$
$V_{\text{H}}$	$\overline{\text{ENABLE}}$ Pin Input Voltage High		4.65			$\text{V}$
	Output Leakage Current	$\overline{\text{ENABLE}} = V^+ - 4.65\text{V}$ , $V_{\text{O}} = \pm 1\text{V}$		0.2	10	$\mu\text{A}$
$t_{\text{ON}}$	Turn-On Time	$\overline{\text{ENABLE}} = 5\text{V}$ to $0\text{V}$ , $R_{\text{L}} = 1\text{k}$		300		$\text{ns}$
$t_{\text{OFF}}$	Turn-Off Time	$\overline{\text{ENABLE}} = 0\text{V}$ to $5\text{V}$ , $R_{\text{L}} = 1\text{k}$		62		$\mu\text{s}$
GBW	Gain-Bandwidth Product	Frequency = $1\text{MHz}$ LT6230-10	150	215		$\text{MHz}$
			1000	1450		$\text{MHz}$
SR	Slew Rate	$A_{\text{V}} = -1$ , $R_{\text{L}} = 1\text{k}$ , $V_{\text{O}} = -2\text{V}$ to $2\text{V}$	50	70		$\text{V}/\mu\text{s}$
		LT6230-10, $A_{\text{V}} = -10$ , $R_{\text{L}} = 1\text{k}$ , $V_{\text{O}} = -2\text{V}$ to $2\text{V}$		320		$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth	$V_{\text{OUT}} = 3\text{V}_{\text{P-P}}$ (Note 9)	5.3	7.4		$\text{MHz}$
		LT6230-10, $\text{HD2} = \text{HD3} \leq 1\%$		11		$\text{MHz}$
$t_{\text{S}}$	Settling Time (LT6230, LT6231, LT6232)	0.1%, $V_{\text{STEP}} = 2\text{V}$ , $A_{\text{V}} = -1$ , $R_{\text{L}} = 1\text{k}$		50		$\text{ns}$

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the  $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$  temperature range.  $V_S = \pm 5\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$ ,  $\text{ENABLE} = 0\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{OS}}$	Input Offset Voltage	LT6230CS6, LT6230CS6-10	●		600	$\mu\text{V}$
		LT6231CS8, LT6232CGN	●		450	$\mu\text{V}$
		LT6231CDD	●		550	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●		800	$\mu\text{V}$
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 10)		●	0.5	3	$\mu\text{V}/^{\circ}\text{C}$
$I_B$	Input Bias Current		●		11	$\mu\text{A}$
	$I_B$ Match (Channel-to-Channel) (Note 6)		●		1	$\mu\text{A}$
$I_{\text{OS}}$	Input Offset Current		●		0.7	$\mu\text{A}$
$A_{\text{VOL}}$	Large-Signal Gain	$V_O = \pm 4.5\text{V}$ , $R_L = 10\text{k}$	●	100		$\text{V}/\text{mV}$
		$V_O = \pm 4.5\text{V}$ , $R_L = 1\text{k}$	●	27		$\text{V}/\text{mV}$
		$V_O = \pm 2\text{V}$ , $R_L = 100\Omega$	●	6		$\text{V}/\text{mV}$
$V_{\text{CM}}$	Input Voltage Range	Guaranteed by CMRR	●	-3	4	V
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -3\text{V}$ to $4\text{V}$	●	95		dB
	CMRR Match (Channel-to-Channel) (Note 6)	$V_{\text{CM}} = -3\text{V}$ to $4\text{V}$	●	89		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.5\text{V}$ to $\pm 5\text{V}$	●	85		dB
	PSRR Match (Channel-to-Channel) (Note 6)	$V_S = \pm 1.5\text{V}$ to $\pm 5\text{V}$	●	79		dB
$V_{\text{OL}}$	Output Voltage Swing Low (Note 8)	No Load	●		50	mV
		$I_{\text{SINK}} = 5\text{mA}$	●		200	mV
		$I_{\text{SINK}} = 20\text{mA}$	●		500	mV
$V_{\text{OH}}$	Output Voltage Swing High (Note 8)	No Load	●		60	mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●		215	mV
		$I_{\text{SOURCE}} = 20\text{mA}$	●		650	mV
$I_{\text{SC}}$	Short-Circuit Current		●	$\pm 25$		mA
$I_S$	Supply Current per Amplifier		●		4.6	mA
	Disabled Supply Current per Amplifier	$\text{ENABLE} = 4.75\text{V}$	●	1		$\mu\text{A}$
$I_{\text{ENABLE}}$	ENABLE Pin Current	$\text{ENABLE} = 0.3\text{V}$	●		-95	$\mu\text{A}$
$V_L$	ENABLE Pin Input Voltage Low		●		0.3	V
$V_H$	ENABLE Pin Input Voltage High		●	4.75		V
	Output Leakage Current	$\text{ENABLE} = 4.75\text{V}$ , $V_O = \pm 1\text{V}$	●	1		$\mu\text{A}$
$t_{\text{ON}}$	Turn-On Time	$\text{ENABLE} = 5\text{V}$ to $0\text{V}$ , $R_L = 1\text{k}$	●	300		ns
$t_{\text{OFF}}$	Turn-Off Time	$\text{ENABLE} = 0\text{V}$ to $5\text{V}$ , $R_L = 1\text{k}$	●	85		$\mu\text{s}$
SR	Slew Rate	$A_V = -1$ , $R_L = 1\text{k}$ , $V_O = -2\text{V}$ to $2\text{V}$	●	44		$\text{V}/\mu\text{s}$
		LT6230-10, $A_V = -10$ , $R_L = 1\text{k}$ , $V_O = -2\text{V}$ to $2\text{V}$	●	315		$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth	$V_{\text{OUT}} = 3V_{\text{P-P}}$ (Note 9) LT6230C, LT6231C, LT6232C	●	4.66		MHz



**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$  temperature range.  $V_S = \pm 5\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = 0\text{V}$ ,  $\text{ENABLE} = 0\text{V}$ , unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{OS}}$	Input Offset Voltage	LT6230I, LT6230I-10	●		700	$\mu\text{V}$
		LT6231IS8, LT6232IGN	●		550	$\mu\text{V}$
		LT6231IDD	●		650	$\mu\text{V}$
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●		1000	$\mu\text{V}$
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 10)		●	0.5	3	$\mu\text{V}/^{\circ}\text{C}$
$I_B$	Input Bias Current		●		12	$\mu\text{A}$
	$I_B$ Match (Channel-to-Channel) (Note 6)		●		1.1	$\mu\text{A}$
$I_{\text{OS}}$	Input Offset Current		●		0.8	$\mu\text{A}$
$A_{\text{VOL}}$	Large-Signal Gain	$V_O = \pm 4.5\text{V}$ , $R_L = 10\text{k}$	●	93		$\text{V}/\text{mV}$
		$V_O = \pm 4.5\text{V}$ , $R_L = 1\text{k}$	●	25		$\text{V}/\text{mV}$
		$V_O = \pm 1.5\text{V}$ , $R_L = 100\Omega$	●	4.8		$\text{V}/\text{mV}$
$V_{\text{CM}}$	Input Voltage Range	Guaranteed by CMRR	●	-3	4	V
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = -3\text{V}$ to $4\text{V}$	●	95		dB
	CMRR Match (Channel-to-Channel) (Note 6)	$V_{\text{CM}} = -3\text{V}$ to $4\text{V}$	●	89		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.5\text{V}$ to $\pm 5\text{V}$	●	85		dB
	PSRR Match (Channel-to-Channel) (Note 6)	$V_S = \pm 1.5\text{V}$ to $\pm 5\text{V}$	●	79		dB
$V_{\text{OL}}$	Output Voltage Swing Low (Note 8)	No Load	●		60	mV
		$I_{\text{SINK}} = 5\text{mA}$	●		210	mV
		$I_{\text{SINK}} = 15\text{mA}$	●		510	mV
$V_{\text{OH}}$	Output Voltage Swing High (Note 8)	No Load	●		70	mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●		220	mV
		$I_{\text{SOURCE}} = 20\text{mA}$	●		675	mV
$I_{\text{SC}}$	Short-Circuit Current		●	$\pm 15$		mA
$I_S$	Supply Current per Amplifier		●		4.85	mA
	Disabled Supply Current per Amplifier	$\text{ENABLE} = 4.8\text{V}$	●	1		$\mu\text{A}$
$I_{\text{ENABLE}}$	ENABLE Pin Current	$\text{ENABLE} = 0.3\text{V}$	●		-110	$\mu\text{A}$
$V_L$	ENABLE Pin Input Voltage Low		●		0.3	V
$V_H$	ENABLE Pin Input Voltage High		●	4.8		V
	Output Leakage Current	$\text{ENABLE} = 4.8\text{V}$ , $V_O = \pm 1\text{V}$	●	1		$\mu\text{A}$
$t_{\text{ON}}$	Turn-On Time	$\text{ENABLE} = 5\text{V}$ to $0\text{V}$ , $R_L = 1\text{k}$	●	300		ns
$t_{\text{OFF}}$	Turn-Off Time	$\text{ENABLE} = 0\text{V}$ to $5\text{V}$ , $R_L = 1\text{k}$	●	72		$\mu\text{s}$
SR	Slew Rate	$A_V = -1$ , $R_L = 1\text{k}$ , $V_O = -2\text{V}$ to $2\text{V}$	●	37		$\text{V}/\mu\text{s}$
		LT6230-10, $A_V = -10$ , $R_L = 1\text{k}$ , $V_O = -2\text{V}$ to $2\text{V}$	●	260		$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth (Note 9)	$V_{\text{OUT}} = 3V_{\text{P-P}}$ ; LT6230I, LT6231I, LT6232I	●	3.9		MHz

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Inputs are protected by back-to-back diodes. If the differential input voltage exceeds 0.7V, the input current must be limited to less than 40mA.

**Note 3:** A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

**Note 4:** The LT6230C/LT6230I, the LT6231C/LT6231I, and LT6232C/LT6232I are guaranteed functional over the temperature range of  $-40^{\circ}\text{C}$  and  $85^{\circ}\text{C}$ .

**Note 5:** The LT6230C/LT6231C/LT6232C are guaranteed to meet specified performance from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ . The LT6230C/LT6231C/LT6232C are designed, characterized and expected to meet specified performance from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , but are not tested or QA sampled at these temperatures. The LT6230I/LT6231I/LT6232I are guaranteed to meet specified performance from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

## ELECTRICAL CHARACTERISTICS

**Note 6:** Matching parameters are the difference between the two amplifiers A and D and between B and C of the LT6232; between the two amplifiers of the LT6231. CMRR and PSRR match are defined as follows: CMRR and PSRR are measured in  $\mu\text{V}/\text{V}$  on the matched amplifiers. The difference is calculated between the matching sides in  $\mu\text{V}/\text{V}$ . The result is converted to dB.

**Note 7:** Minimum supply voltage is guaranteed by power supply rejection ratio test.

**Note 8:** Output voltage swings are measured between the output and power supply rails.

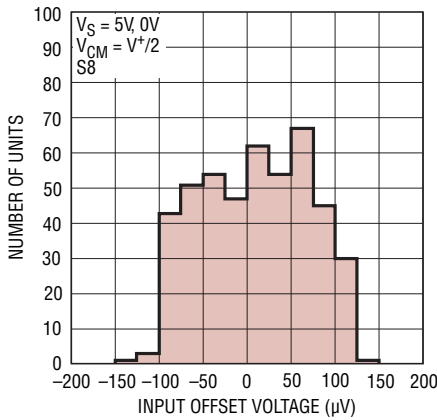
**Note 9:** Full-power bandwidth is calculated from the slew rate:

$$\text{FPBW} = \text{SR}/2\pi V_P$$

**Note 10:** This parameter is not 100% tested.

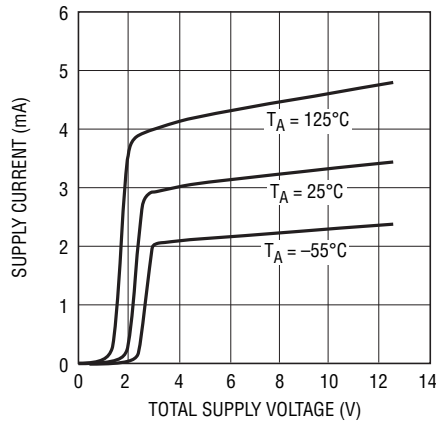
## TYPICAL PERFORMANCE CHARACTERISTICS (LT6230/LT6231/LT6232)

**$V_{OS}$  Distribution**



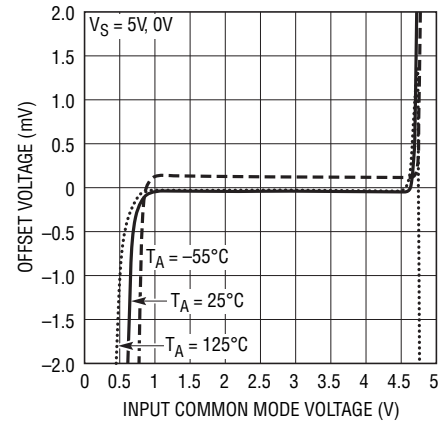
623012 G01

**Supply Current vs Supply Voltage  
(Per Amplifier)**



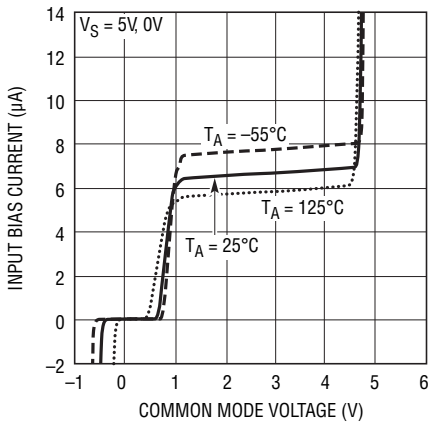
623012 G02

**Offset Voltage vs Input Common Mode Voltage**



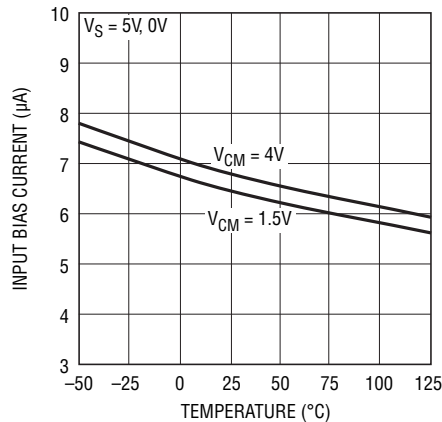
623012 G03

**Input Bias Current  
vs Common Mode Voltage**



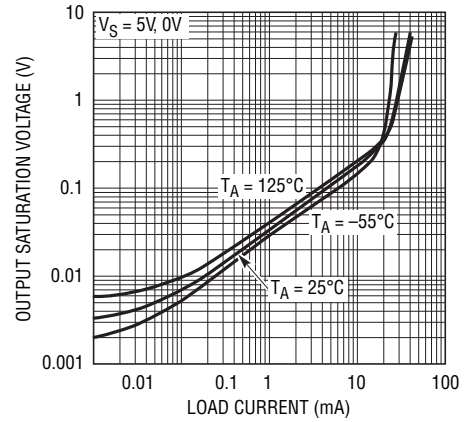
623012 G04

**Input Bias Current vs Temperature**



623012 G05

**Output Saturation Voltage  
vs Load Current (Output Low)**

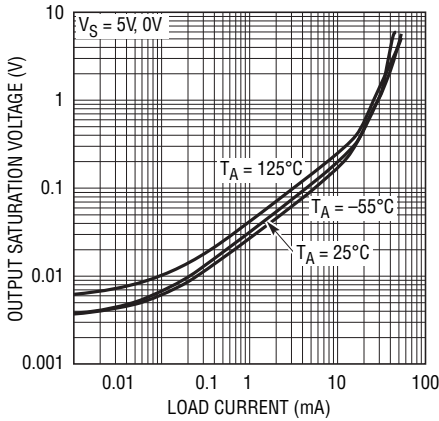


623012 G06

# TYPICAL PERFORMANCE CHARACTERISTICS

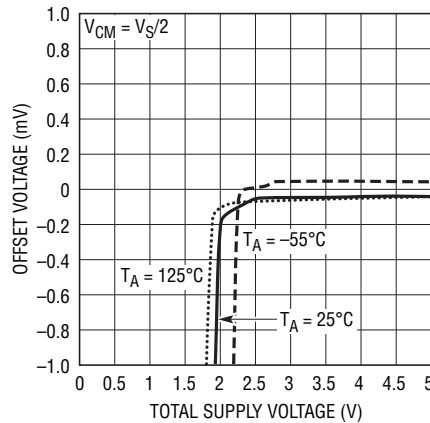
(LT6230/LT6231/LT6232)

**Output Saturation Voltage vs Load Current (Output High)**



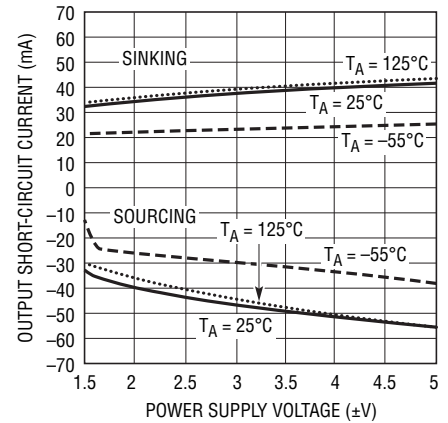
623012 G07

**Minimum Supply Voltage**



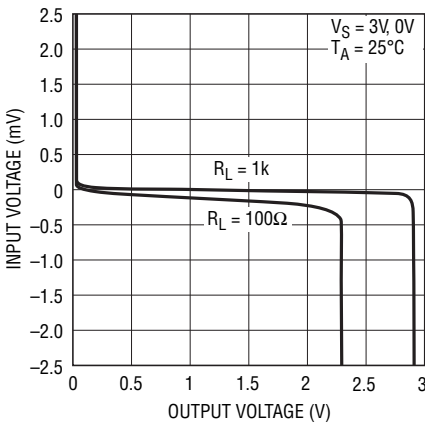
623012 G08

**Output Short-Circuit Current vs Power Supply Voltage**



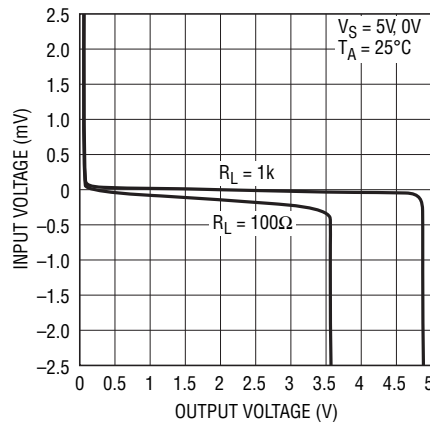
623012 G09

**Open-Loop Gain**



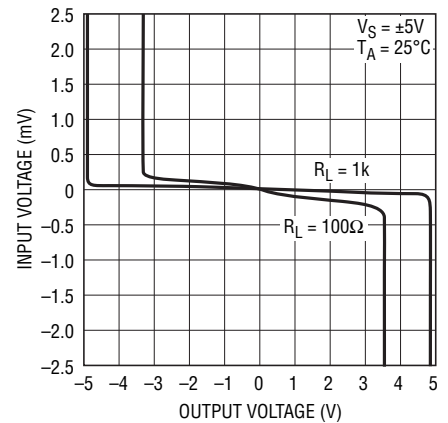
623012 G10

**Open-Loop Gain**



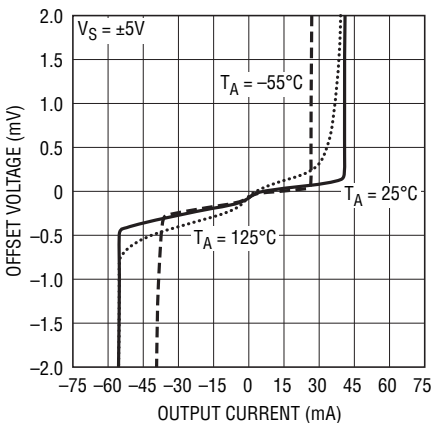
623012 G11

**Open-Loop Gain**



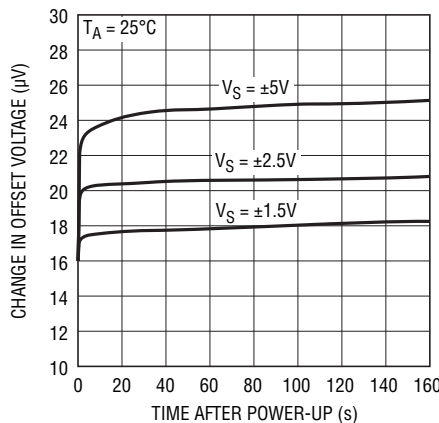
623012 G12

**Offset Voltage vs Output Current**



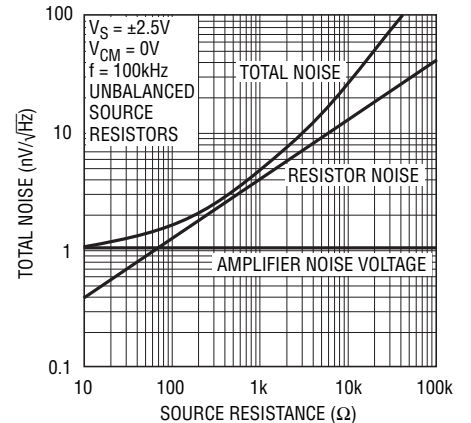
623012 G13

**Warm-Up Drift vs Time**



623012 G14

**Total Noise vs Total Source Resistance**

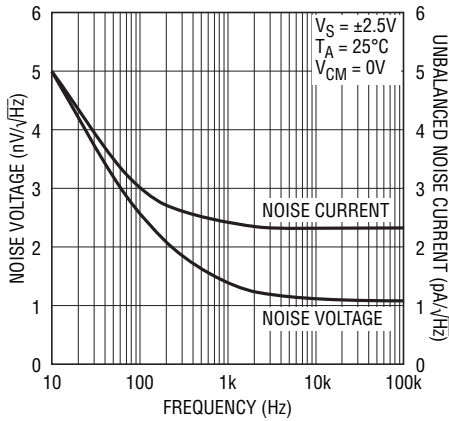


623012 G15

# TYPICAL PERFORMANCE CHARACTERISTICS

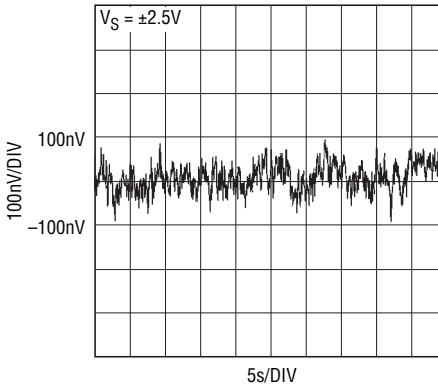
(LT6230/LT6231/LT6232)

**Noise Voltage and Unbalanced Noise Current vs Frequency**



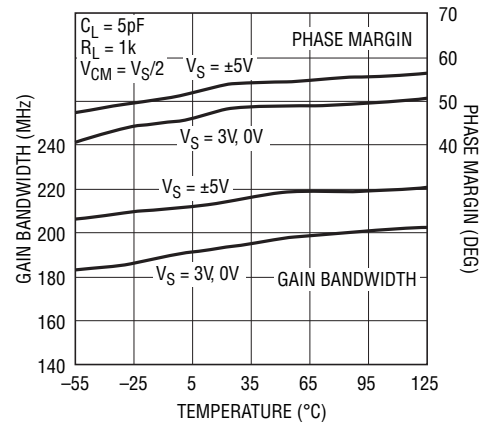
623012 G16

**0.1Hz to 10Hz Output Voltage Noise**



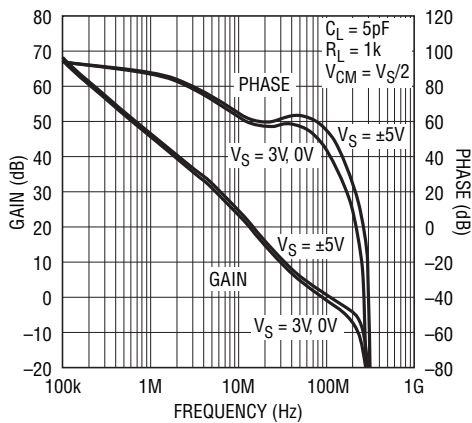
623012 G17

**Gain Bandwidth and Phase Margin vs Temperature**



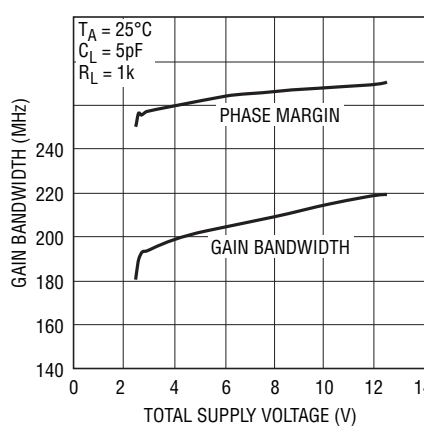
623012 G18

**Open-Loop Gain vs Frequency**



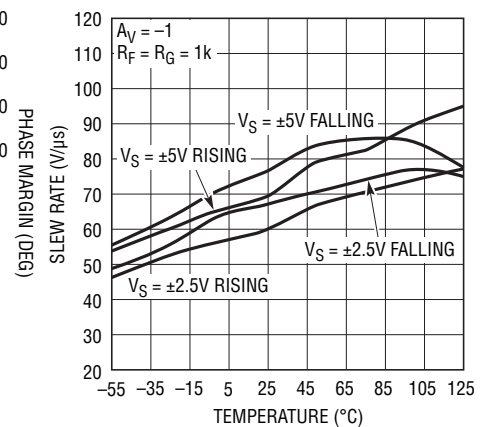
623012 G19

**Gain Bandwidth and Phase Margin vs Supply Voltage**



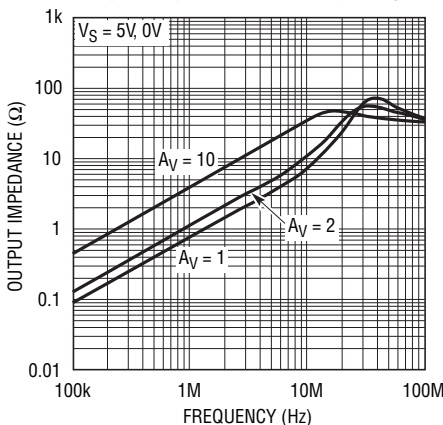
623012 G20

**Slew Rate vs Temperature**



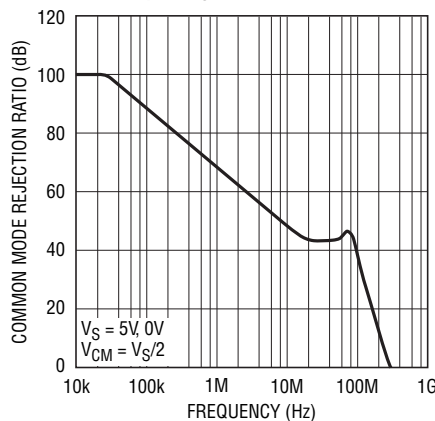
623012 G21

**Output Impedance vs Frequency**



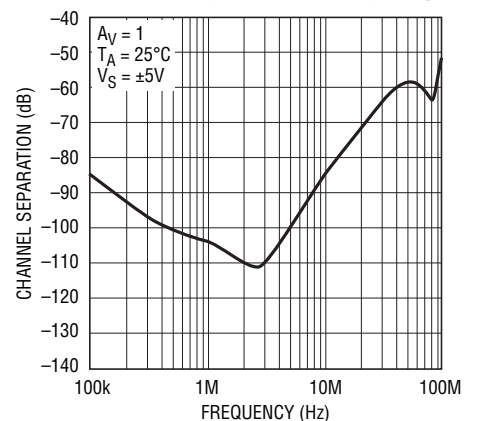
623012 G22

**Common Mode Rejection Ratio vs Frequency**



623012 G23

**Channel Separation vs Frequency**



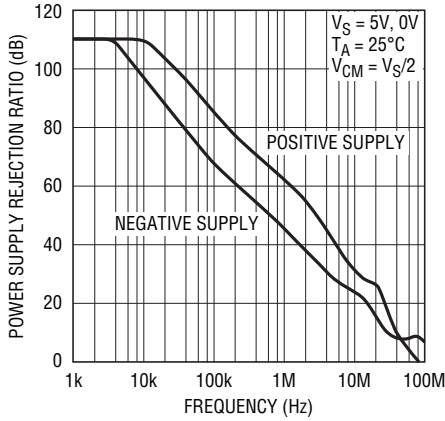
623012 G24

623012fc

# TYPICAL PERFORMANCE CHARACTERISTICS

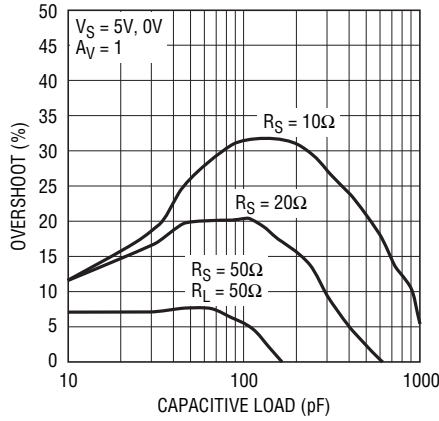
(LT6230/LT6231/LT6232)

**Power Supply Rejection Ratio vs Frequency**



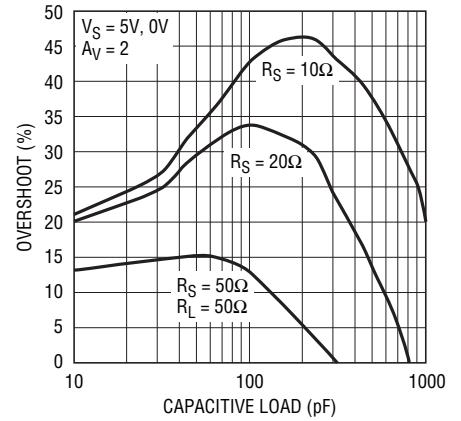
623012 G25

**Series Output Resistance and Overshoot vs Capacitive Load**



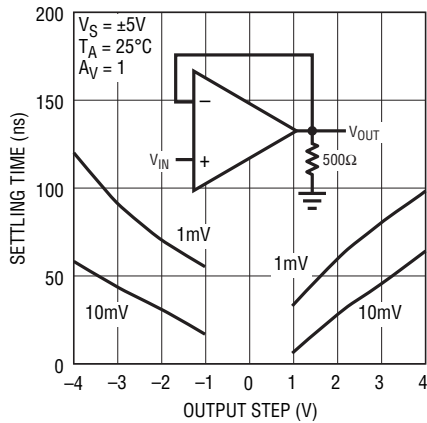
623012 G26

**Series Output Resistance and Overshoot vs Capacitive Load**



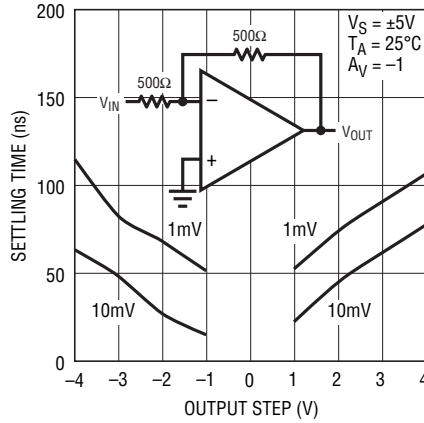
623012 G27

**Settling Time vs Output Step (Noninverting)**



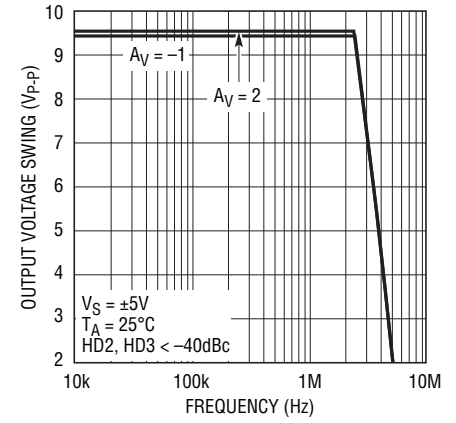
623012 G28

**Settling Time vs Output Step (Inverting)**



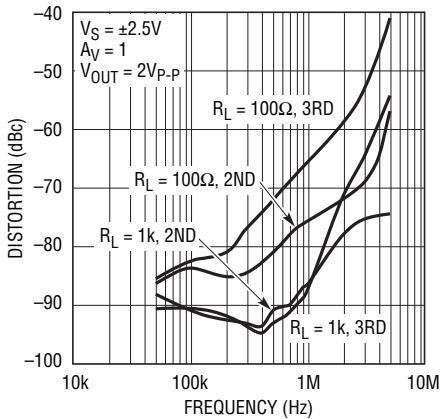
623012 G29

**Maximum Undistorted Output Signal vs Frequency**



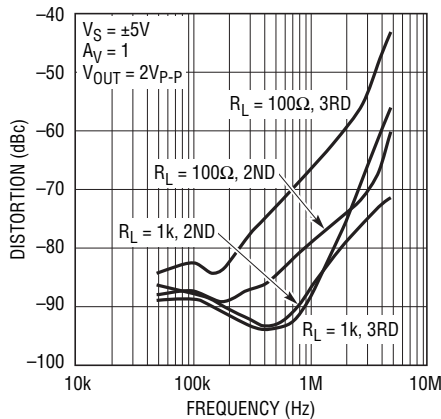
623012 G30

**Distortion vs Frequency**



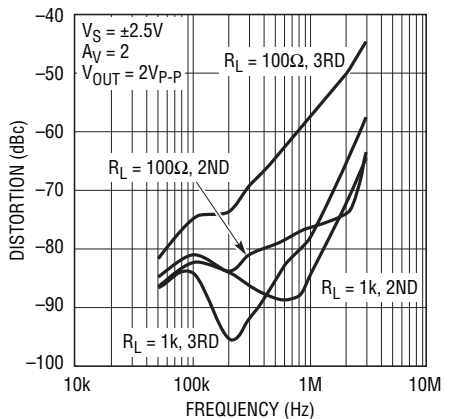
623012 G31

**Distortion vs Frequency**



623012 G32

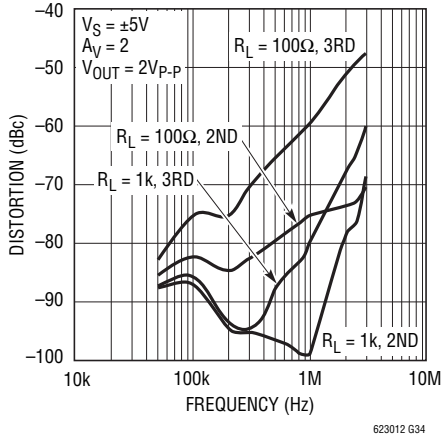
**Distortion vs Frequency**



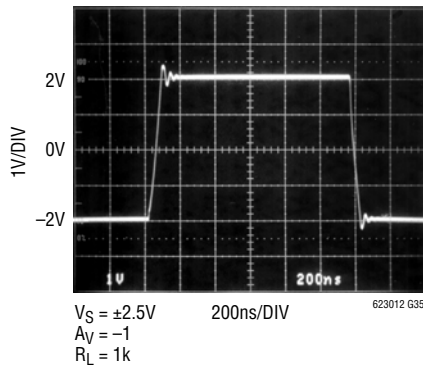
623012 G33

## TYPICAL PERFORMANCE CHARACTERISTICS (LT6230/LT6231/LT6232)

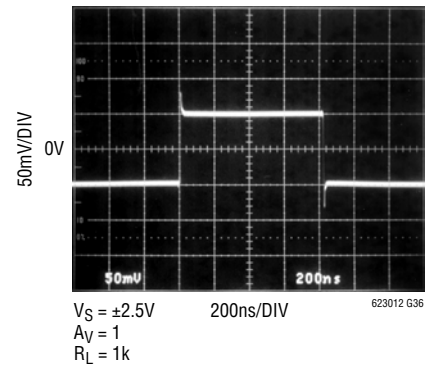
### Distortion vs Frequency



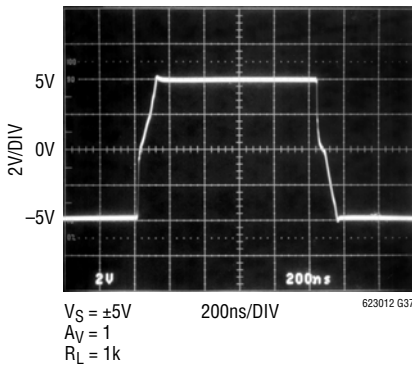
### Large-Signal Response



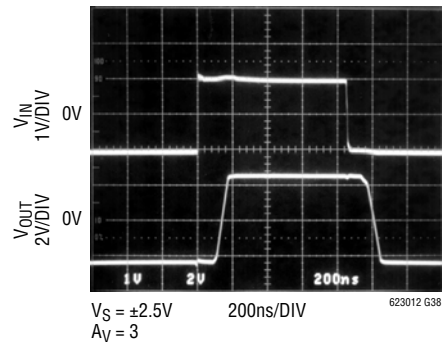
### Small-Signal Response



### Large-Signal Response

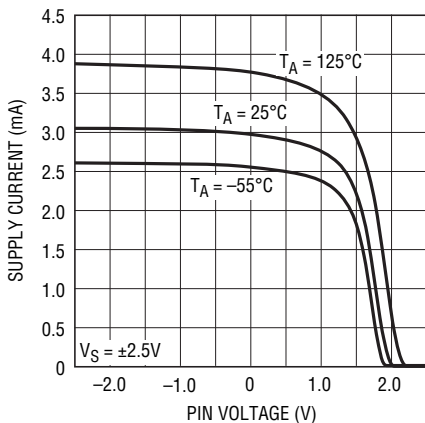


### Output Overdrive Recovery

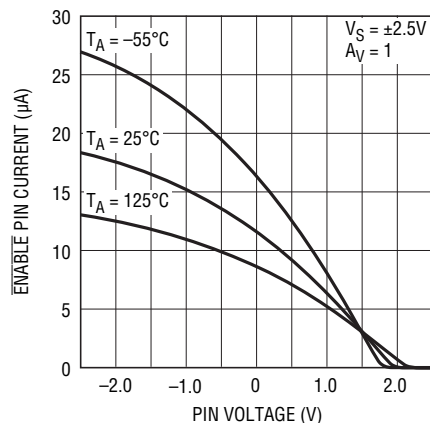


## (LT6230) ENABLE Characteristics

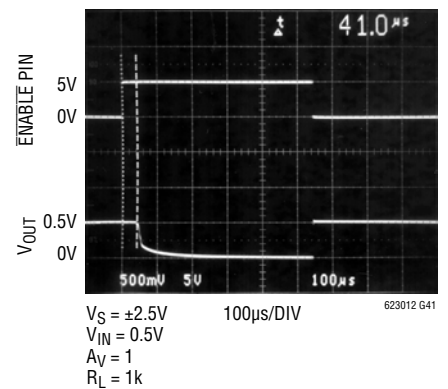
### Supply Current vs ENABLE Pin Voltage



### ENABLE Pin Current vs ENABLE Pin Voltage



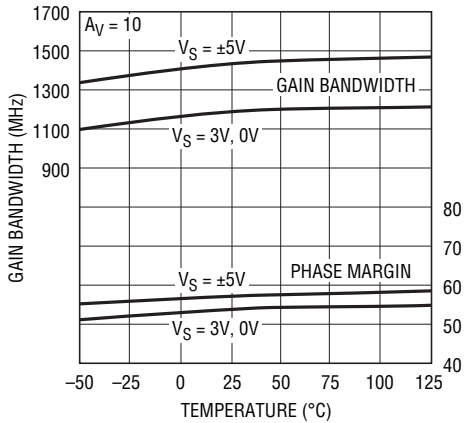
### ENABLE Pin Response Time



# TYPICAL PERFORMANCE CHARACTERISTICS

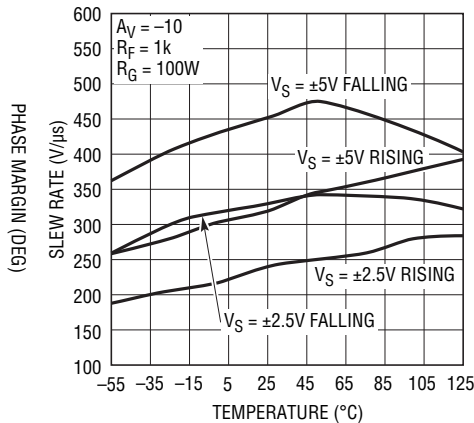
(LT6230-10)

**Gain Bandwidth and Phase Margin vs Temperature**



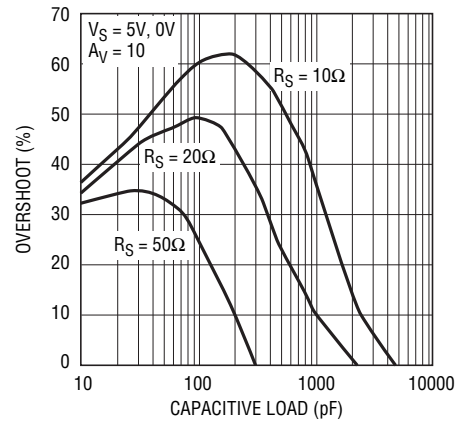
623012 G42

**Slew Rate vs Temperature**



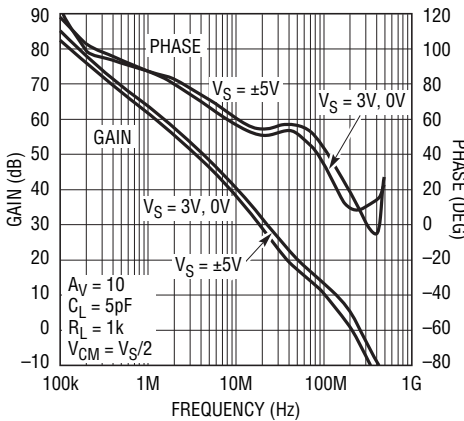
623012 G43

**Series Output Resistor and Overshoot vs Capacitive Load**



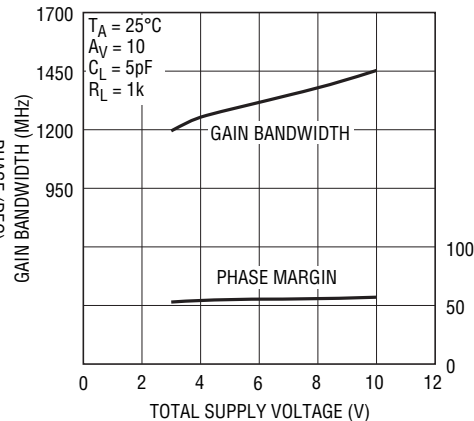
623012 G44

**Open-Loop Gain and Phase vs Frequency**



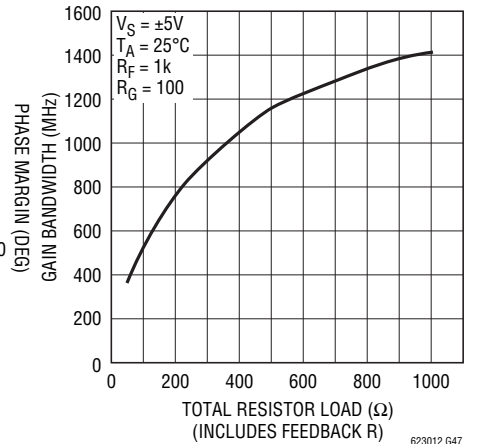
623012 G45

**Gain Bandwidth and Phase Margin vs Supply Voltage**



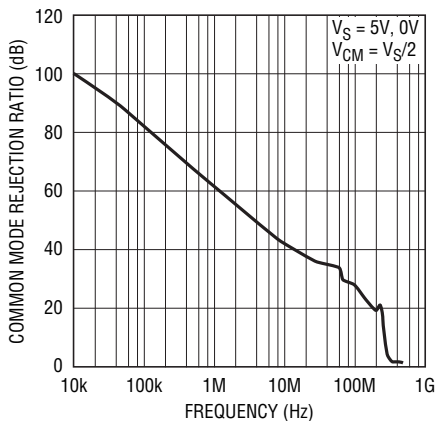
623012 G46

**Gain Bandwidth vs Resistor Load**



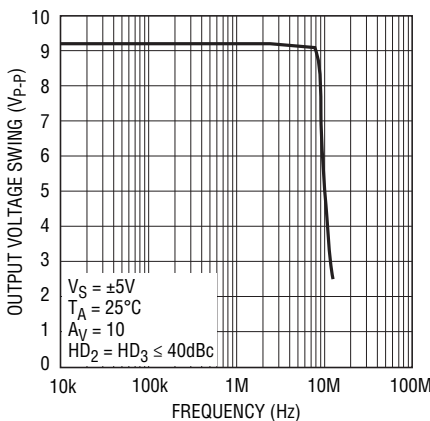
623012 G47

**Common Mode Rejection Ratio vs Frequency**



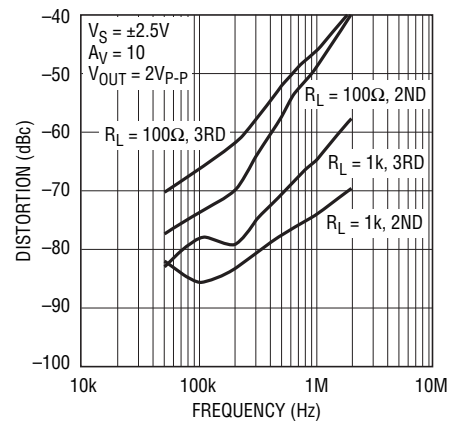
623012 G48

**Maximum Undistorted Output Signal vs Frequency**



623012 G49

**2nd and 3rd Harmonic Distortion vs Frequency**



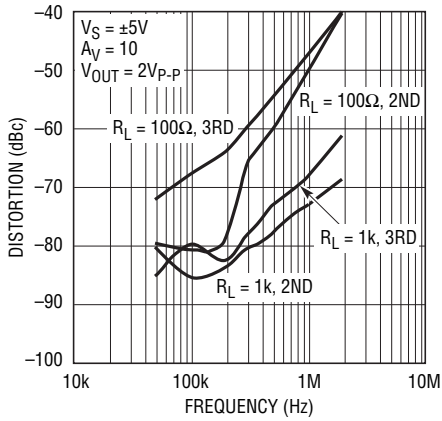
623012 G50

623012fC

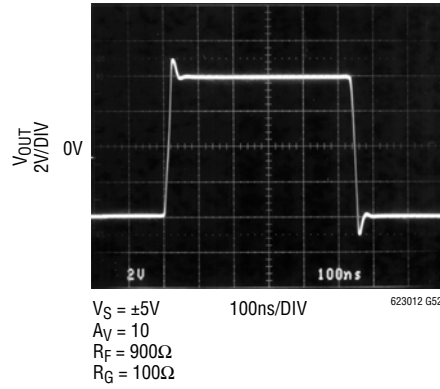
# TYPICAL PERFORMANCE CHARACTERISTICS

(LT6230-10)

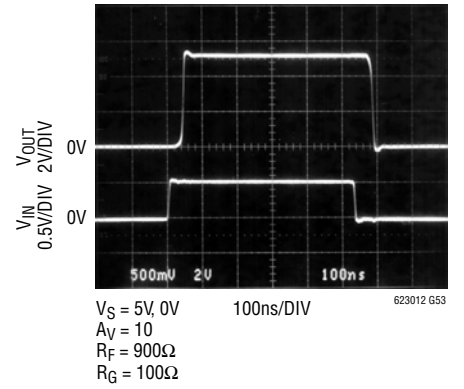
**2nd and 3rd Harmonic Distortion vs Frequency**



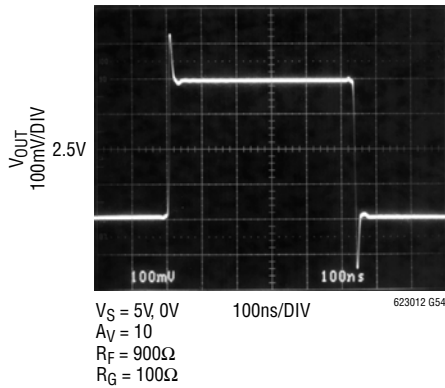
**Large-Signal Response**



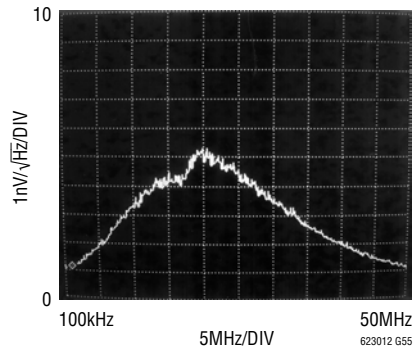
**Output-Overload Recovery**



**Small-Signal Response**



**Input Referred High Frequency Noise Spectrum**





## APPLICATIONS INFORMATION

### Amplifier Characteristics

Figure 1 is a simplified schematic of the LT6230/LT6231/LT6232, which has a pair of low noise input transistors Q1 and Q2. A simple current mirror, Q3/Q4, converts the differential signal to a single-ended output, and these transistors are degenerated to reduce their contribution to the overall noise.

Capacitor C1 reduces the unity-cross frequency and improves the frequency stability without degrading the gain bandwidth of the amplifier. Capacitor C<sub>M</sub> sets the overall amplifier gain bandwidth. The differential drive generator supplies current to transistors Q5 and Q6 that swing the output from rail-to-rail.

### Input Protection

There are back-to-back diodes, D1 and D2 across the + and – inputs of these amplifiers to limit the differential input voltage to  $\pm 0.7V$ . The inputs of the LT6230/LT6231/LT6232 do not have internal resistors in series with the input transistors. This technique is often used to protect the input devices from overvoltage that causes excessive current to flow. The addition of these resistors would significantly degrade the low noise voltage of these amplifiers. For instance, a 100 $\Omega$  resistor in series with each input would generate 1.8nV/ $\sqrt{Hz}$  of noise, and the total amplifier noise voltage would rise from 1.1nV/ $\sqrt{Hz}$  to 2.1nV/ $\sqrt{Hz}$ . Once the input differential voltage exceeds  $\pm 0.7V$ , steady-state current conducted through the protection diodes should

be limited to  $\pm 40mA$ . This implies 25 $\Omega$  of protection resistance is necessary per volt of overdrive beyond  $\pm 0.7V$ . These input diodes are rugged enough to handle transient currents due to amplifier slew rate overdrive and clipping without protection resistors.

The photo of Figure 2 shows the output response to an input overdrive with the amplifier connected as a voltage follower. With the input signal low, current source I<sub>1</sub> saturates and the differential drive generator drives Q6 into saturation so the output voltage swings all the way to V<sup>-</sup>. The input can swing positive until transistor Q2 saturates into current mirror Q3/Q4. When saturation occurs, the output tries to phase invert, but diode D2 conducts current from the signal source to the output through the feedback connection. The output is clamped a diode drop below the input. In this photo, the input signal generator is limiting at about 20mA.

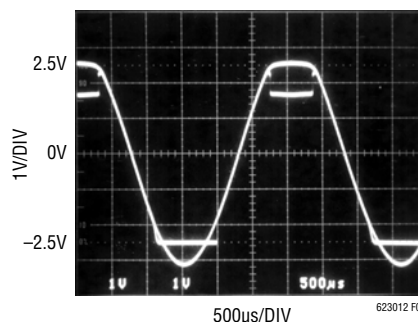


Figure 2. V<sub>S</sub> =  $\pm 2.5V$ , A<sub>V</sub> = 1 with Large Overdrive

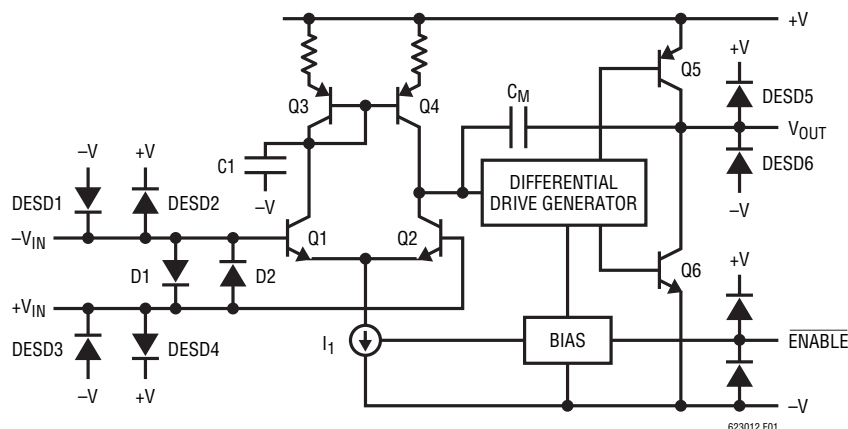


Figure 1. Simplified Schematic

## APPLICATIONS INFORMATION

With the amplifier connected in a gain of  $A_V \geq 2$ , the output can invert with very heavy overdrive. To avoid this inversion, limit the input overdrive to 0.5V beyond the power supply rails.

### ESD

The LT6230/LT6231/LT6232 have reverse-biased ESD protection diodes on all inputs and outputs as shown in Figure 1. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to one hundred milliamps or less, no damage to the device will occur.

### Noise

The noise voltage of the LT6230/LT6231/LT6232 is equivalent to that of a  $75\Omega$  resistor, and for the lowest possible noise it is desirable to keep the source and feedback resistance at or below this value, i.e.,  $R_S + R_G || R_{FB} \leq 75\Omega$ . With  $R_S + R_G || R_{FB} = 75\Omega$  the total noise of the amplifier is:

$$e_N = \sqrt{(1.1\text{nV})^2 + (1.1\text{nV})^2} = 1.55\text{nV}/\sqrt{\text{Hz}}$$

Below this resistance value, the amplifier dominates the noise, but in the region between  $75\Omega$  and about  $3\text{k}$ , the noise is dominated by the resistor thermal noise. As the total resistance is further increased beyond  $3\text{k}$ , the amplifier noise current multiplied by the total resistance eventually dominates the noise.

The product of  $e_N \cdot \sqrt{I_{\text{SUPPLY}}}$  is an interesting way to gauge low noise amplifiers. Most low noise amplifiers with low  $e_N$  have high  $I_{\text{SUPPLY}}$  current. In applications that require low noise voltage with the lowest possible supply current, this product can prove to be enlightening. The LT6230/LT6231/LT6232 have an  $e_N \cdot \sqrt{I_{\text{SUPPLY}}}$  product of only 1.9 per amplifier, yet it is common to see amplifiers with similar noise specifications to have  $e_N \cdot \sqrt{I_{\text{SUPPLY}}}$  as high as 13.5.

For a complete discussion of amplifier noise, see the LT1028 data sheet.

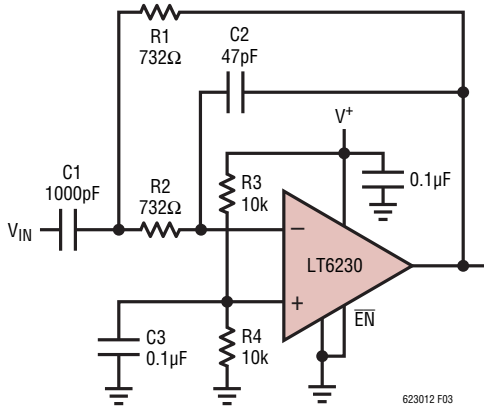
### ENABLE Pin

The LT6230 includes an  $\overline{\text{ENABLE}}$  pin that shuts down the amplifier to  $10\mu\text{A}$  maximum supply current. The  $\overline{\text{ENABLE}}$  pin must be driven low to operate the amplifier with normal supply current. The  $\overline{\text{ENABLE}}$  pin must be driven high to within  $0.35\text{V}$  of  $V^+$  to shut down the supply current. This can be accomplished with simple gate logic; however care must be taken if the logic and the LT6230 operate from different supplies. If this is the case, then open-drain logic can be used with a pull-up resistor to ensure that the amplifier remains off. See the Typical Performance Characteristics.

The output leakage current when disabled is very low; however, current can flow into the input protection diodes D1 and D2 if the output voltage exceeds the input voltage by a diode drop.

# TYPICAL APPLICATIONS

## Single Supply, Low Noise, Low Power, Bandpass Filter with Gain = 10



$$f_0 = \frac{1}{2\pi RC} = 1\text{MHz}$$

$$C = \sqrt{C1C2}, R = R1 = R2$$

$$f_0 = \left(\frac{732\Omega}{R}\right)\text{MHz, MAXIMUM } f_0 = 1\text{MHz}$$

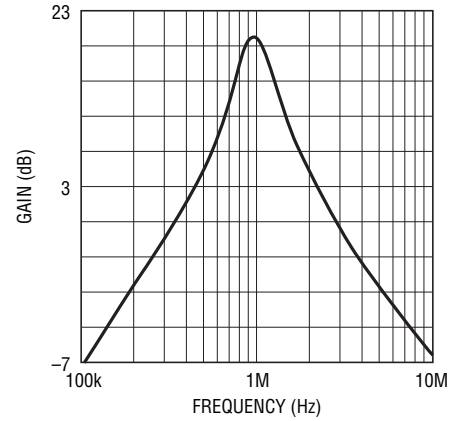
$$f_{-3dB} = \frac{f_0}{2.5}$$

$$A_V = 20\text{dB at } f_0$$

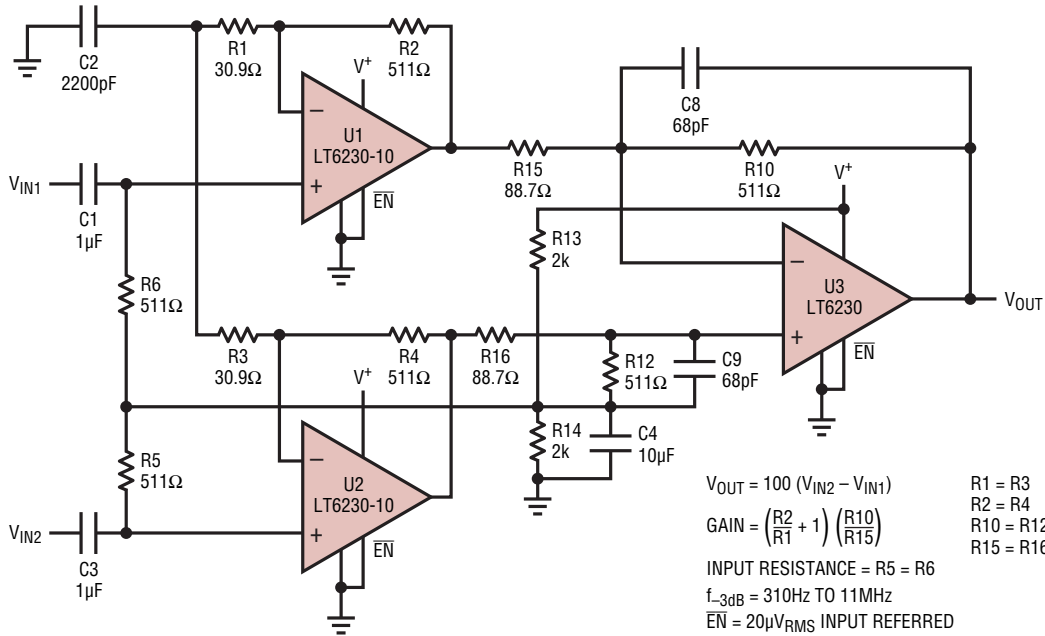
$$\overline{EN} = 4\mu\text{VRMS INPUT REFERRED}$$

$$I_S = 3.7\text{mA FOR } V^+ = 5\text{V}$$

Frequency Response Plot of Bandpass Filter



## Low Noise, Low Power, Single Supply, Instrumentation Amplifier with Gain = 100



$$V_{OUT} = 100 (V_{IN2} - V_{IN1})$$

$$GAIN = \left(\frac{R2}{R1} + 1\right) \left(\frac{R10}{R15}\right)$$

INPUT RESISTANCE =  $R5 = R6$

$$f_{-3dB} = 310\text{Hz TO } 11\text{MHz}$$

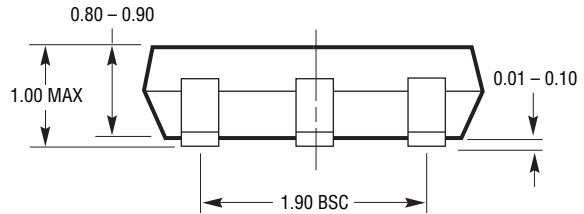
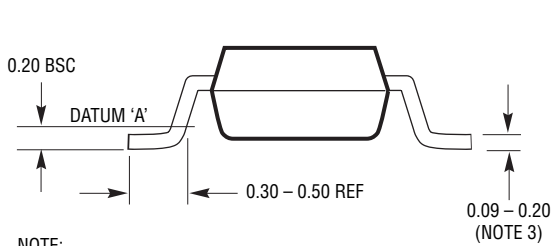
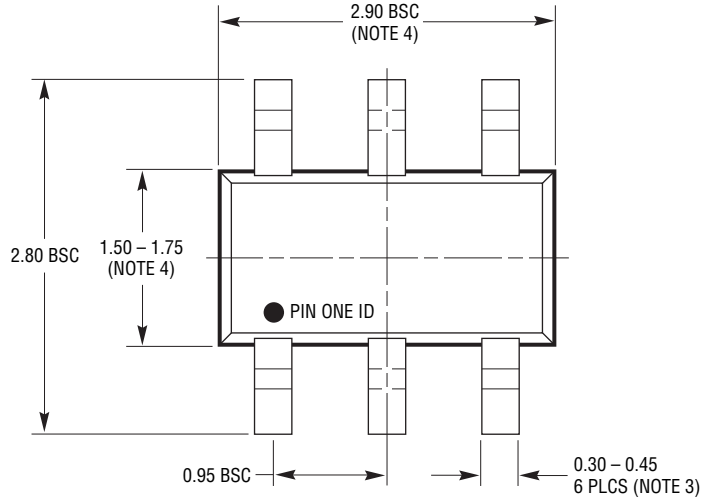
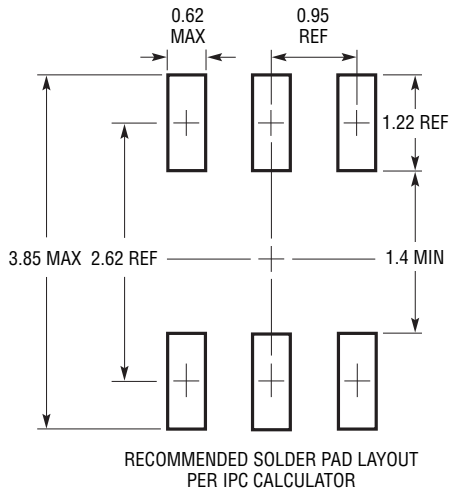
$$\overline{EN} = 20\mu\text{VRMS INPUT REFERRED}$$

$$I_S = 10.5\text{mA FOR } V_S = 5\text{V, } 0\text{V}$$

623012 F05

# PACKAGE DESCRIPTION

**S6 Package**  
**6-Lead Plastic TSOT-23**  
 (Reference LTC DWG # 05-08-1636)

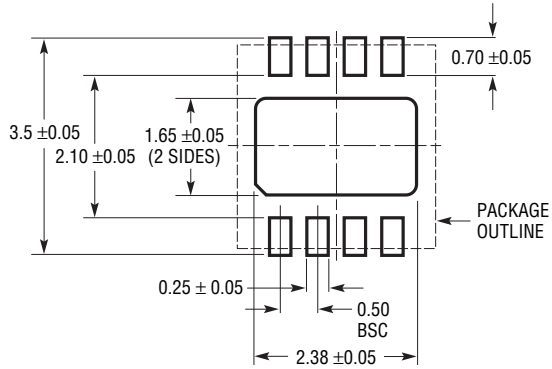


S6 TSOT-23 0302 REV B

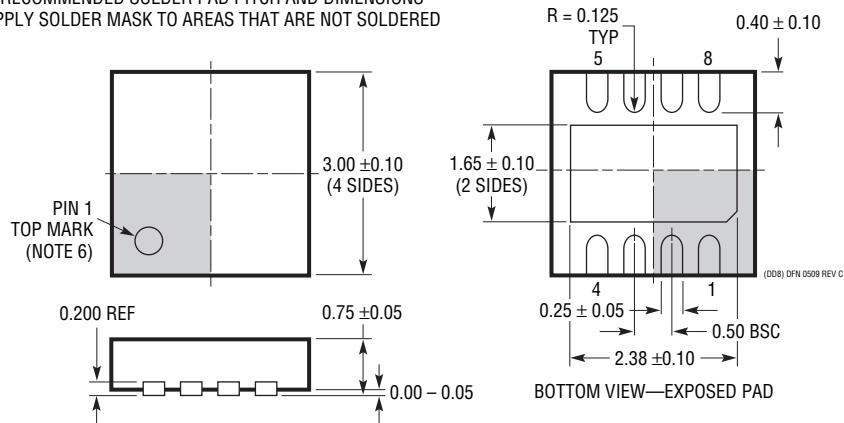
- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
  2. DRAWING NOT TO SCALE
  3. DIMENSIONS ARE INCLUSIVE OF PLATING
  4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
  5. MOLD FLASH SHALL NOT EXCEED 0.254mm
  6. JEDEC PACKAGE REFERENCE IS MO-193

# PACKAGE DESCRIPTION

**DD Package**  
**8-Lead Plastic DFN (3mm × 3mm)**  
 (Reference LTC DWG # 05-08-1698 Rev C)



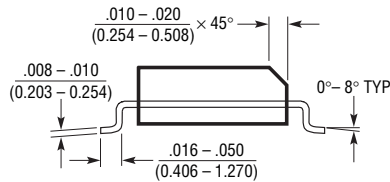
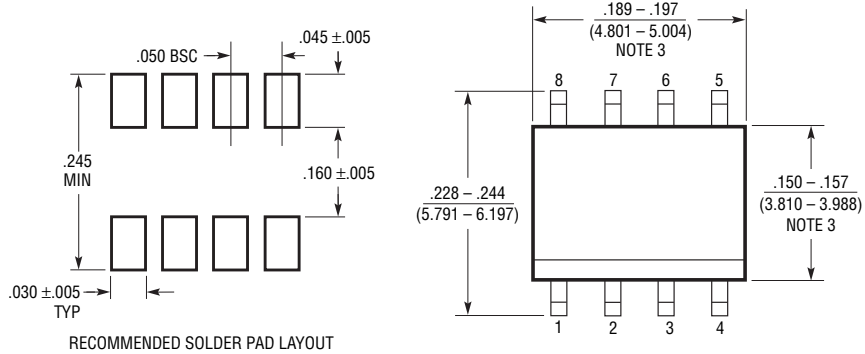
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS  
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



- NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
  2. DRAWING NOT TO SCALE
  3. ALL DIMENSIONS ARE IN MILLIMETERS
  4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
  5. EXPOSED PAD SHALL BE SOLDER PLATED
  6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

**PACKAGE DESCRIPTION**

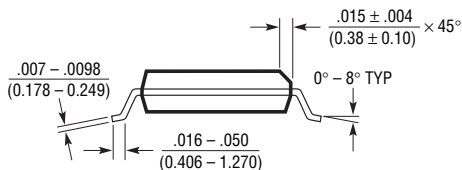
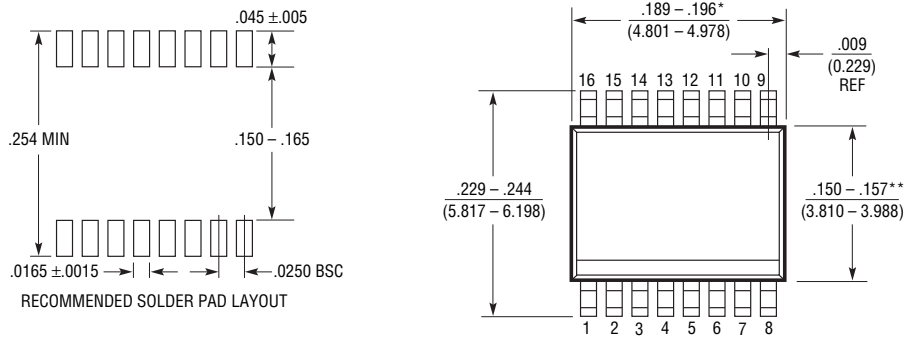
**S8 Package**  
**8-Lead Plastic Small Outline (Narrow .150 Inch)**  
 (Reference LTC DWG # 05-08-1610)



- NOTE:  
 1. DIMENSIONS IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$   
 2. DRAWING NOT TO SCALE  
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S08 0303

**GN Package**  
**16-Lead Plastic SSOP (Narrow .150 Inch)**  
 (Reference LTC DWG # 05-08-1641)



- NOTE:  
 1. CONTROLLING DIMENSION: INCHES  
 2. DIMENSIONS ARE IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$   
 3. DRAWING NOT TO SCALE  
 \*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
 \*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0204

**REVISION HISTORY** (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	1/11	Updated ENABLE Pin section in Applications Information	18

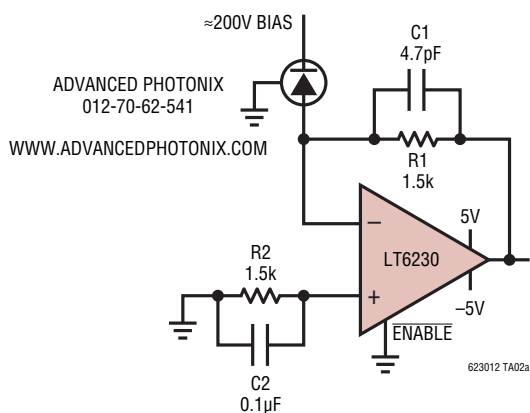
## TYPICAL APPLICATIONS

The LT6230 is applied as a transimpedance amplifier with an I-to-V conversion gain of  $1.5\text{k}\Omega$  set by R1. The LT6230 is ideally suited to this application because of its low input offset voltage and current, and its low noise. This is because the  $1.5\text{k}\Omega$  resistor has an inherent thermal noise of  $5\text{nV}/\sqrt{\text{Hz}}$  or  $3.4\text{pA}/\sqrt{\text{Hz}}$  at room temperature, while the LT6230 contributes only  $1.1\text{nV}$  and  $2.4\text{pA}/\sqrt{\text{Hz}}$ . So, with respect to both voltage and current noises, the LT6230 is actually quieter than the gain resistor.

The circuit uses an avalanche photodiode with the cathode biased to approximately  $200\text{V}$ . When light is incident on

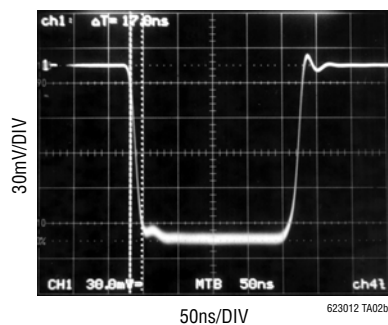
the photodiode, it induces a current  $I_{\text{PD}}$  which flows into the amplifier circuit. The amplifier output falls negative to maintain balance at its inputs. The transfer function is therefore  $V_{\text{OUT}} = -I_{\text{PD}} \cdot 1.5\text{k}$ . C1 ensures stability and good settling characteristics. Output offset was measured at  $280\mu\text{V}$ , so low in part because R2 serves to cancel the DC effects of bias current. Output noise was measured at  $1.1\text{mV}_{\text{P-P}}$  on a  $100\text{MHz}$  measurement bandwidth, with C2 shunting R2's thermal noise. As shown in the scope photo, the rise time is  $17\text{ns}$ , indicating a signal bandwidth of  $20\text{MHz}$ .

**Low Power Avalanche Photodiode Transimpedance Amplifier**  
 $I_{\text{S}} = 3.3\text{mA}$



OUTPUT OFFSET =  $500\mu\text{V}$  TYPICAL  
 BANDWIDTH =  $20\text{MHz}$   
 OUTPUT NOISE =  $1.1\text{mV}_{\text{P-P}}$  ( $100\text{MHz}$  MEASUREMENT BW)

**Photodiode Amplifier Time Domain Response**



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1028	Single, Ultralow Noise 50MHz Op Amp	$0.85\text{nV}/\sqrt{\text{Hz}}$
LT1677	Single, Low Noise Rail-to-Rail Amplifier	3V Operation, 2.5mA, $4.5\text{nV}/\sqrt{\text{Hz}}$ , $60\mu\text{V}$ Max $V_{\text{OS}}$
LT1806/LT1807	Single/Dual, Low Noise 325MHz Rail-to-Rail Amplifier	2.5V Operation, $550\mu\text{V}$ Max $V_{\text{OS}}$ , $3.5\text{nV}/\sqrt{\text{Hz}}$
LT6200/LT6201	Single/Dual, Low Noise 165MHz	$0.95\text{nV}/\sqrt{\text{Hz}}$ , Rail-to-Rail Input and Output
LT6202/LT6203/LT6204	Single/Dual/Quad, Low Noise, Rail-to-Rail Amplifier	$1.9\text{nV}/\sqrt{\text{Hz}}$ , 3mA Max, $100\text{MHz}$ Gain Bandwidth