Dual 60MHz, 20V/µs, Low Power, Rail-to-Rail Input and Output Precision Op Amps

FEATURES

- **Gain Bandwidth Product: 60MHz**
- **Input Common Mode Range Includes Both Rails**
- **Output Swings Rail-to-Rail**
- **Low Quiescent Current: 1mA Max**
- **Input Offset Voltage: 350µV Max**
- **Input Bias Current: 150nA Max**
- Wide Supply Range: 2.2V to 12.6V
- Large Output Current: 50mA Typ
- Low Voltage Noise: 10nV/√Hz Typ
- Slew Rate: 20V/µs Typ
- Common Mode Rejection: 102dB Typ
- Power Supply Rejection: 105dB Typ
- Open-Loop Gain: 100V/mV Typ
- Operating Temperature Range: –40°C to 85°C
- Single in the 8-Lead SO and 5-Lead Low Profile (1mm) ThinSOT™ Packages
- Dual in the 8-Lead SO and (3mm × 3mm) DFN Packages
- Quad in the 16-Lead SSOP Package

APPLICATIONS

- Low Voltage, High Frequency Signal Processing
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers
- Active Filters
- Video Amplifiers
- Fast Current Sensing Amplifiers

DESCRIPTION

The LT®6220/LT6221/LT6222 are single/dual/quad, low power, high speed rail-to-rail input and output operational amplifiers with excellent DC performance. The LT6220/LT6221/LT6222 feature reduced supply current, lower input offset voltage, lower input bias current and higher DC gain than other devices with comparable bandwidth.

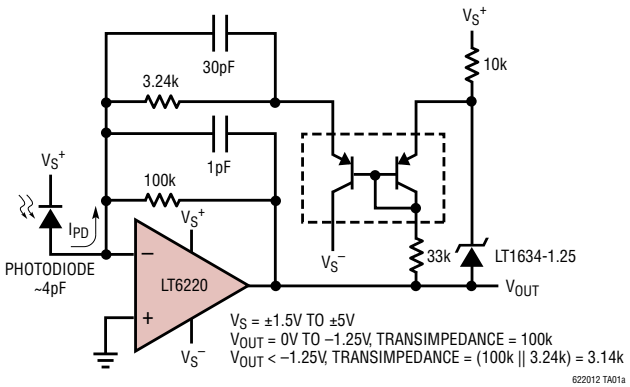
Typically, the LT6220/LT6221/LT6222 have an input offset voltage of less than 100µV, an input bias current of less than 15nA and an open-loop gain of 100V/mV. The parts have an input range that includes both supply rails and an output that swings within 10mV of either supply rail to maximize the signal dynamic range in low supply applications.

The LT6220/LT6221/LT6222 maintain performance for supplies from 2.2V to 12.6V and are specified at 3V, 5V and ±5V supplies. The inputs can be driven beyond the supplies without damage or phase reversal of the output.

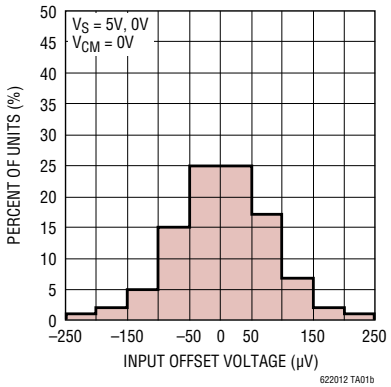
The LT6220 is housed in the 8-lead SO package with the standard op amp pinout as well as the 5-lead SOT-23 package. The LT6221 is available in 8-lead SO and DFN (3mm×3mm low profile dual fine pitch leadless) packages with the standard op amp pinout. The LT6222 features the standard quad op amp configuration and is available in the 16-lead SSOP package. The LT6220/LT6221/LT6222 can be used as plug-in replacements for many op amps to improve input/output range and performance.

TYPICAL APPLICATION

Stepped-Gain Photodiode Amplifier



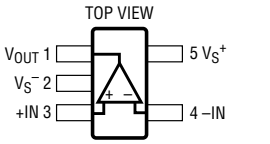
V_{OS} Distribution, V_{CM} = 0V (S8, PNP Stage)



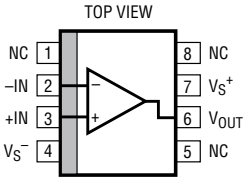
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V_S^- to V_S^+) 12.6V
Input Voltage (Note 2) ..... $\pm V_S$
Input Current (Note 2) ..... ±10mA
Output Short Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) .... –40°C to 85°C
Specified Temperature Range (Note 5) .... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
(DD Package) ..... 125°C
Storage Temperature ..... –65°C to 150°C
(DD Package) ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

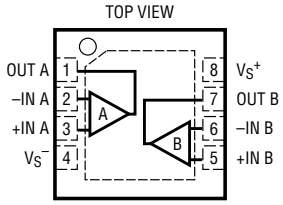
PIN CONFIGURATION



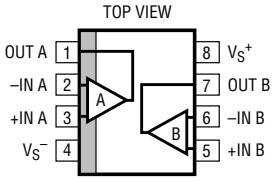
S5 PACKAGE
5-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 250°C/W (NOTE 10)



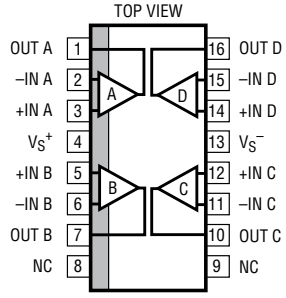
S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 190°C/W



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 160°C/W (NOTE 10)
EXPOSED PAD INTERNALLY CONNECTED TO V_S^-
(PCB CONNECTION OPTIONAL)



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 190°C/W



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 135°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6220CS5#PBF	LT6220CS5#TRPBF	LTAFP	5-Lead Plastic TSOT-23	0°C to 70°C
LT6220IS5#PBF	LT6220IS5#TRPBF	LTAFP	5-Lead Plastic TSOT-23	–40°C to 85°C
LT6220CS8#PBF	LT6220CS8#TRPBF	6220	8-Lead Plastic SO	0°C to 70°C
LT6220IS8#PBF	LT6220IS8#TRPBF	6220I	8-Lead Plastic SO	–40°C to 85°C
LT6221CDD#PBF	LT6221CDD#TRPBF	LADZ	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT6221IDD#PBF	LT6221IDD#TRPBF	LADZ	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT6221CS8#PBF	LT6221CS8#TRPBF	6221	8-Lead Plastic SO	0°C to 70°C
LT6221IS8#PBF	LT6221IS8#TRPBF	6221I	8-Lead Plastic SO	–40°C to 85°C
LT6222CGN#PBF	LT6222CGN#TRPBF	6222	16-Lead Narrow Plastic SSOP	0°C to 70°C
LT6222IGN#PBF	LT6222IGN#TRPBF	6222I	16-Lead Narrow Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 0V V_{CM} = 0V (DD Package) V_{CM} = 0V (S5 Package) V_{CM} = V_S V_{CM} = V_S (S5 Package)		70 150 200 0.5 0.5	350 700 850 2.5 3	µV µV µV mV mV
ΔV_{OS}	Input Offset Voltage Shift	V_S = 5V, V_{CM} = 0V to 3.5V V_S = 3V, V_{CM} = 0V to 1.5V		30 15	195 120	µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = 0V V_{CM} = 0V (DD Package)		100 150	600 1100	µV µV
I_B	Input Bias Current	V_{CM} = 1V V_{CM} = V_S		15 250	150 600	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = 1V V_{CM} = V_S		15 20	175 250	nA nA
I_{OS}	Input Offset Current	V_{CM} = 1V V_{CM} = V_S		15 15	100 100	nA nA
	Input Noise Voltage	0.1Hz to 10Hz		0.5		μV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz		10		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz		0.8		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			2		pF
A_{VOL}	Large Signal Voltage Gain	V_S = 5V, V_{OUT} = 0.5V to 4.5V, R_L = 1k at V_S/2 V_S = 5V, V_{OUT} = 1V to 4V, R_L = 100Ω at V_S/2 V_S = 3V, V_{OUT} = 0.5V to 2.5V, R_L = 1k at V_S/2	35 3.5 30	100 10 90		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 0V to 3.5V V_S = 3V, V_{CM} = 0V to 1.5V	85 82	102 102		dB dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_S = 5V, V_{CM} = 0V to 3.5V V_S = 3V, V_{CM} = 0V to 1.5V	79 76	100 100		dB dB
	Input Common Mode Range		0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	84	105		dB
	PSRR Match (Channel-to-Channel) (Note 9)		79	105		dB
	Minimum Supply Voltage (Note 6)			2.2	2.5	V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 20mA		5 100 325	40 200 650	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA		5 130 475	40 250 900	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	20 20	45 35		mA mA
I_S	Supply Current Per Amplifier			0.9	1	mA
GBW	Gain-Bandwidth Product	V_S = 5V, Frequency = 1MHz	35	60		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L= 1k, V_{OUT} = 4V	10	20		V/µs
FPBW	Full Power Bandwidth	V_S = 5V, A_V = 1, V_{OUT} = $4V_{P-P}$		1.6		MHz
HD	Harmonic Distortion	V_S = 5V, A_V = 1, R_L= 1k, V_{OUT} = $2V_{P-P}$, f_C = 500kHz		–77.5		dBc
t_S	Settling Time	0.01%, V_S = 5V, V_{STEP} = 2V, A_V = 1, R_L= 1k		300		ns
ΔG	Differential Gain (NTSC)	V_S = 5V, A_V = 2, R_L= 1k		0.3		%
Δθ	Differential Phase (NTSC)	V_S = 5V, A_V = 2, R_L= 1k		0.3		Deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 0V	●		90	500	µV
		V_{CM} = 0V (DD Package)	●		180	850	µV
		V_{CM} = 0V (S5 Package)	●		230	1250	µV
		V_{CM} = V_S	●		0.5	3	mV
		V_{CM} = V_S (S5 Package)	●		0.5	3.5	mV
ΔV_{OS}	Input Offset Voltage Shift	V_S = 5V, V_{CM} = 0V to 3.5V	●		30	280	µV
		V_S = 3V, V_{CM} = 0V to 1.5V	●		15	190	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = 0V	●		110	850	µV
		V_{CM} = 0V (DD Package)	●		180	1400	µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		1.5	5	µV/°C
		(S5 Package)	●		3.5	10	µV/°C
I_B	Input Bias Current	V_{CM} = 1V	●		20	175	nA
		V_{CM} = V_S – 0.2V	●		275	800	nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = 1V	●		15	200	nA
		V_{CM} = V_S – 0.2V	●		20	300	nA
I_{OS}	Input Offset Current	V_{CM} = 1V	●		15	125	nA
		V_{CM} = V_S – 0.2V	●		15	125	nA
A_{VOL}	Large Signal Voltage Gain	V_S = 5V, V_{OUT} = 0.5V to 4.5V, R_L = 1k at V_S/2	●	30	90		V/mV
		V_S = 5V, V_{OUT} = 1V to 4V, R_L = 100Ω at V_S/2	●	3	9		V/mV
		V_S = 3V, V_{OUT} = 0.5V to 2.5V, R_L = 1k at V_S/2	●	25	80		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 0V to 3.5V	●	82	100		dB
		V_S = 3V, V_{CM} = 0V to 1.5V	●	78	100		dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_S = 5V, V_{CM} = 0V to 3.5V	●	77	100		dB
		V_S = 3V, V_{CM} = 0V to 1.5V	●	73	100		dB
	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	●	81	104		dB
	PSRR Match (Channel-to-Channel) (Note 9)		●	76	104		dB
	Minimum Supply Voltage (Note 6)		●		2.2	2.5	V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load	●		8	50	mV
		I_{SINK} = 5mA	●		110	220	mV
		I_{SINK} = 20mA	●		375	750	mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load	●		8	50	mV
		I_{SOURCE} = 5mA	●		150	300	mV
		I_{SOURCE} = 20mA	●		600	1100	mV
I_{SC}	Short-Circuit Current	V_S = 5V	●	20	40		mA
		V_S = 3V	●	20	30		mA
I_S	Supply Current Per Amplifier		●		1	1.4	mA
GBW	Gain-Bandwidth Product	V_S = 5V, Frequency = 1MHz	●	30	60		MHz
SR	Slew Rate	V_S = 5V, AV = –1, R_L = 1k, V_{OUT} = $4V_{P-P}$	●	9	18		V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C ≤ T_A ≤ 85°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 0V V_{CM} = 0V (DD Package) V_{CM} = 0V (S5 Package) V_{CM} = V_S V_{CM} = V_S (S5 Package)	● ● ● ● ●		125 300 350 0.75 1	700 1300 2000 3.5 4.5	µV µV µV mV mV
ΔV_{OS}	Input Offset Voltage Shift	V_S = 5V, V_{CM} = 0V to 3.5V V_S = 3V, V_{CM} = 0V to 1.5V	● ●		30 30	300 210	µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = 0V V_{CM} = 0V (DD Package)	● ●		175 300	1200 2200	µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	 (S5 Package)	● ●		1.5 3.5	7.5 15	µV/°C µV/°C
I_B	Input Bias Current	V_{CM} = 1V V_{CM} = V_S – 0.2V	● ●		25 300	200 900	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = 1V V_{CM} = V_S – 0.2V	● ●		15 20	250 350	nA nA
I_{OS}	Input Offset Current	V_{CM} = 1V V_{CM} = V_S – 0.2V	● ●		20 20	150 150	nA nA
A_{VOL}	Large Signal Voltage Gain	V_S = 5V, V_{OUT} = 0.5V to 4.5V, R_L = 1k at V_S/2 V_S = 5V, V_{OUT} = 1.5V to 3.5V, R_L = 100Ω at V_S/2 V_S = 3V, V_{OUT} = 0.5V to 2.5V, R_L= 1k at V_S/2	● ● ●	25 2.5 20	70 8 60		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 0V to 3.5V V_S = 3V, V_{CM} = 0V to 1.5V	● ●	81 77	100 100		dB dB
	CMRR Match (Channel-to-Channel) (Note 9)	V_S = 5V, V_{CM} = 0V to 3.5V V_S = 3V, V_{CM} = 0V to 1.5V	● ●	76 72	100 100		dB dB
	Input Common Mode Range		●	0		V_S	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	●	79	104		dB
	PSRR Match (Channel-to-Channel) (Note 9)		●	74	104		dB
	Minimum Supply Voltage (Note 6)		●		2.2	2.5	V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 10mA	● ● ●		10 120 220	60 240 450	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 10mA	● ● ●		10 160 325	60 325 650	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	12.5 12.5	30 25		mA mA
I_S	Supply Current Per Amplifier		●		1.1	1.5	mA
GBW	Gain-Bandwidth Product	V_S = 5V, Frequency = 1MHz	●	25	50		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_{OUT} = 4V	●	8	15		V/µs

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = –5V V_{CM} = –5V (DD Package) V_{CM} = –5V (S5 Package) V_{CM} = 5V V_{CM} = 5V (S5 Package)		80 150 200 0.7 0.7	500 750 900 2.5 3	µV µV µV mV mV
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = –5V to 3.5V		70	675	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = –5V V_{CM} = –5V (DD Package)		100 150	850 1300	µV µV
I_B	Input Bias Current	V_{CM} = –4V V_{CM} = 5V		20 250	150 700	nA nA
	Input Bias Current Match (Channel-to-Channel)	V_{CM} = –4V V_{CM} = 5V		15 20	175 250	nA nA
I_{OS}	Input Offset Current	V_{CM} = –4V V_{CM} = 5V		15 15	100 100	nA nA
	Input Noise Voltage	0.1Hz to 10Hz		0.5		μV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz		10		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz		0.8		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance	f = 100kHz		2		pF
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = –4V to 4V, R_L = 1k V_{OUT} = –2V to 2V, R_L = 100Ω	35 3.5	95 10		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = –5V to 3.5V	82	102		dB
	CMRR Match (Channel-to-Channel)		77	100		dB
	Input Common Mode Range		V_S^-		V_S^+	V
PSRR	Power Supply Rejection Ratio	V_S^+ = 2.5V to 10V, V_S^- = 0V, V_{CM} = 0V	84	105		dB
	PSRR Match (Channel-to-Channel)		79	105		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 20mA		5 100 325	40 200 650	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA		5 130 475	40 250 900	mV mV mV
I_{SC}	Short-Circuit Current		25	50		mA
I_S	Supply Current Per Amplifier			1	1.5	mA
GBW	Gain-Bandwidth Product	Frequency = 1MHz		60		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_{OUT} = ±4V, Measure at V_{OUT} = ±2V		20		V/µs
FPBW	Full Power Bandwidth	$V_{OUT} = 8V_{P-P}$		0.8		MHz
HD	Harmonic Distortion	A_V = 1, R_L= 1k, $V_{OUT} = 2V_{P-P}$, f_C = 500kHz		–77.5		dBc
t_S	Settling Time	0.01%, V_{STEP} = 5V, A_V = 1, R_L = 1k		375		ns
ΔG	Differential Gain (NTSC)	A_V = 2, R_L = 1k		0.15		%
Δθ	Differential Phase (NTSC)	A_V = 2, R_L = 1k		0.6		Deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = –5V V_{CM} = –5V (DD Package) V_{CM} = –5V (S5 Package) V_{CM} = 5V V_{CM} = 5V (S5 Package)	● ● ● ● ●		100 180 230 0.75 0.75	650 900 1300 3 3.5	µV µV µV mV mV
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = –5V to 3.5V	●		90	850	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = –5V V_{CM} = –5V (DD Package)	● ●		90 180	1100 1500	µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	 (S5 Package)	● ●		1.5 3.5	5 10	µV/°C µV/°C
I_B	Input Bias Current	V_{CM} = –4V V_{CM} = 4.8V	● ●		20 275	175 800	nA nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = –4V V_{CM} = 4.8V	● ●		15 20	200 300	nA nA
I_{OS}	Input Offset Current	V_{CM} = –4V V_{CM} = 4.8V	● ●		15 15	125 125	nA nA
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = –4V to 4V, R_L = 1k V_{OUT} = –2V to 2V, R_L =100Ω	● ●	30 3	90 9		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = –5V to 3.5V	●	80	100		dB
	CMRR Match (Channel-to-Channel) (Note 9)		●	75	100		dB
	Input Common Mode Range		●	V_S^-		V_S^+	V
PSRR	Power Supply Rejection Ratio	V_S^+ = 2.5V to 10V, V_S^- = 0V, V_{CM} = 0V	●	81	104		dB
	PSRR Match (Channel-to-Channel) (Note 9)		●	76	104		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 20mA	● ● ●		8 110 375	50 220 750	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA	● ● ●		8 150 600	50 300 1100	mV mV mV
I_{SC}	Short-Circuit Current		●	20	40		mA
I_S	Supply Current Per Amplifier		●		1.2	2	mA
GBW	Gain-Bandwidth Product	Frequency = 1MHz	●		60		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_{OUT} = ±4V, Measure at V_{OUT} = ±2V	●		18		V/µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C ≤ T_A ≤ 85°C temperature range. V_S = ±5V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = –5V	●		150	800	µV
		V_{CM} = –5V (DD Package)	●		300	1300	µV
		V_{CM} = –5V (S5 Package)	●		350	2000	µV
		V_{CM} = 5V	●		0.75	3.5	mV
		V_{CM} = 5V (S5 Package)	●		1	4.5	mV
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = – 5V to 3.5V	●		90	950	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 9)	V_{CM} = –5V	●		175	1350	µV
		V_{CM} = –5V (DD Package)	●		300	2200	µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)		●		1.5	7.5	µV/°C
		(S5 Package)	●		3.5	15	µV/°C
I_B	Input Bias Current	V_{CM} = –4V	●		25	200	nA
		V_{CM} = 4.8V	●		300	900	nA
	Input Bias Current Match (Channel-to-Channel) (Note 9)	V_{CM} = –4V	●		15	250	nA
		V_{CM} = 4.8V	●		20	350	nA
I_{OS}	Input Offset Current	V_{CM} = –4V	●		20	150	nA
		V_{CM} = 4.8V	●		20	150	nA
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = –4V to 4V, R_L = 1k	●	25	70		V/mV
		V_{OUT} = –1V to 1V, R_L = 100Ω	●	2.5	8		V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = –5V to 3.5V	●	79	100		dB
	CMRR Match (Channel-to-Channel) (Note 9)		●	74	100		dB
	Input Common Mode Range		●	–5		5	V
PSRR	Power Supply Rejection Ratio	V_S^+ = 2.5V to 10V, V_S^- = 0V, V_{CM} = 0V	●	79	104		dB
	PSRR Match (Channel-to-Channel) (Note 9)		●	74	104		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load	●		10	60	mV
		I_{SINK} = 5mA	●		120	240	mV
		I_{SINK} = 10mA	●		220	450	mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load	●		10	60	mV
		I_{SOURCE} = 5mA	●		160	325	mV
		I_{SOURCE} = 10mA	●		325	650	mV
I_{SC}	Short-Circuit Current		●	12.5	30		mA
I_S	Supply Current		●		1.4	2.25	mA
GBW	Gain-Bandwidth Product	Frequency = 1MHz	●		50		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_{OUT} = ±4V, Measure at V_{OUT} = ±2V	●		15		V/µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT6220C/LT6221C/LT6222C and LT6220I/LT6221I/LT6222I are guaranteed functional over the temperature range of –40°C and 85°C.

Note 5: The LT6220C/LT6221C/LT6222C are guaranteed to meet specified performance from 0°C to 70°C. The LT6220C/LT6221C/LT6222C are designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT6220I/LT6221I/LT6222I are guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Minimum supply voltage is guaranteed by power supply rejection ratio test.

Note 7: Output voltage swings are measured between the output and power supply rails.

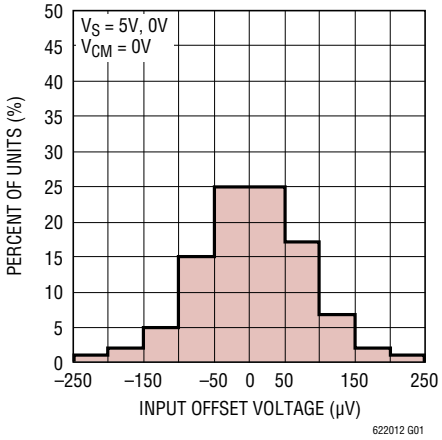
Note 8: This parameter is not 100% tested.

Note 9: Matching parameters are the difference between amplifiers A and D and between B and C on the LT6222; between the two amplifiers on the LT6221.

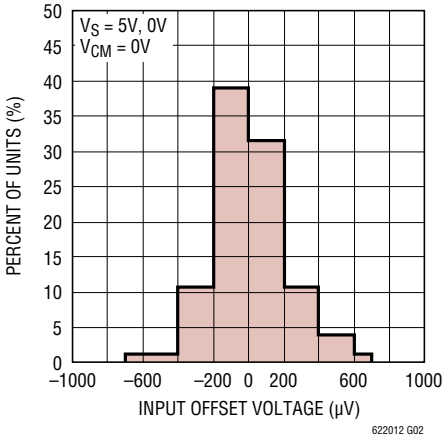
Note 10: Thermal resistance (θ_{JA}) varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads. If desired, the thermal resistance can be substantially reduced by connecting Pin 2 of the LT6220CS5/LT6220IS5 or the underside metal of DD packages to a larger metal area (V_S^- trace).

TYPICAL PERFORMANCE CHARACTERISTICS

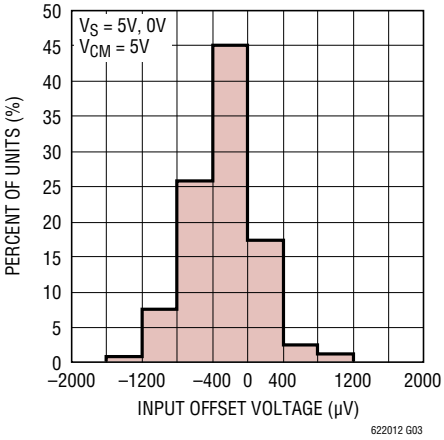
V_{OS} Distribution, V_{CM} = 0V (S8, PNP Stage)



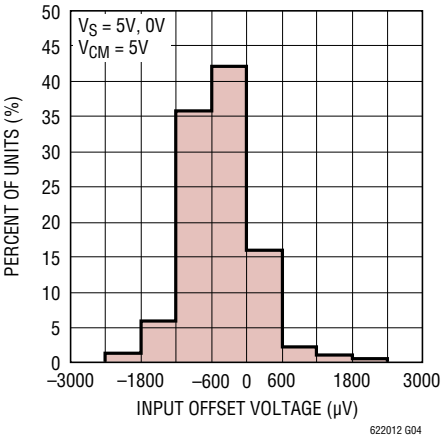
V_{OS} Distribution, V_{CM} = 0V (SOT5, PNP Stage)



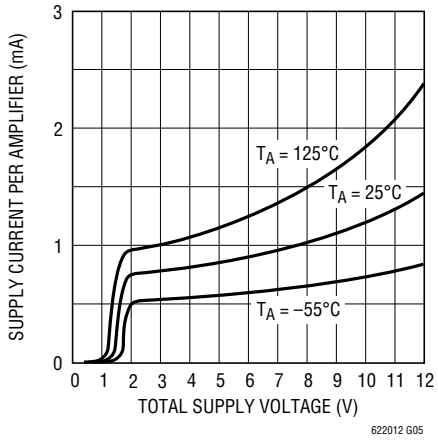
V_{OS} Distribution, V_{CM} = 5V (S8, NPN Stage)



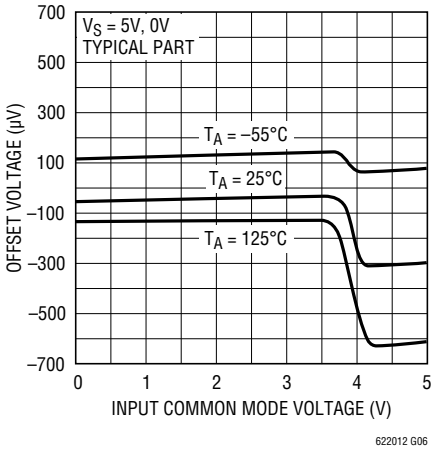
V_{OS} Distribution, V_{CM} = 5V (SOT5, NPN Stage)



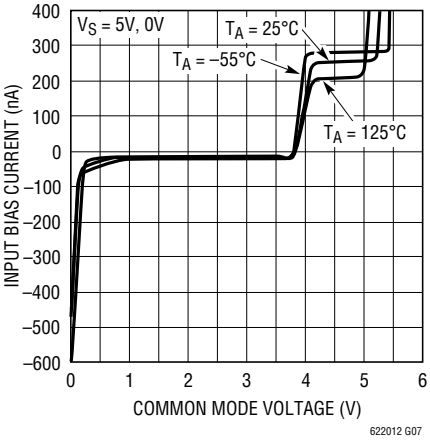
Supply Current vs Supply Voltage



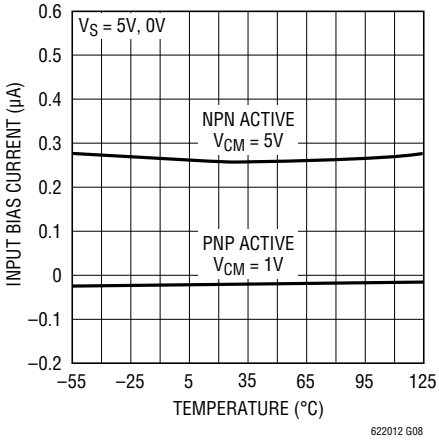
Offset Voltage vs Input Common Mode Voltage



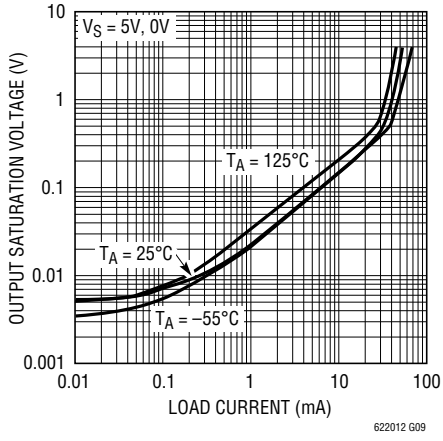
Input Bias Current vs Common Mode Voltage



Input Bias Current vs Temperature

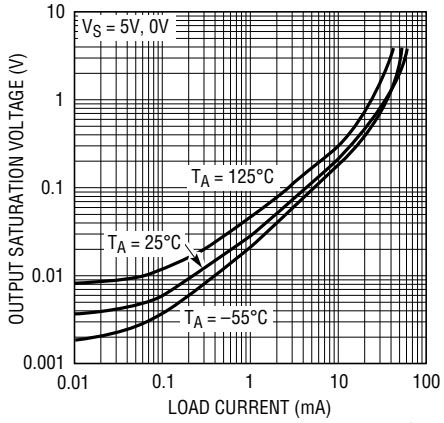


Output Saturation Voltage vs Load Current (Output Low)

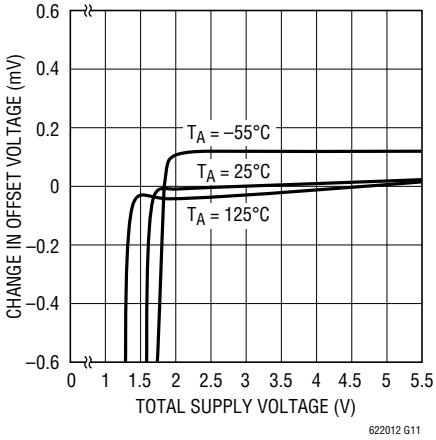


TYPICAL PERFORMANCE CHARACTERISTICS

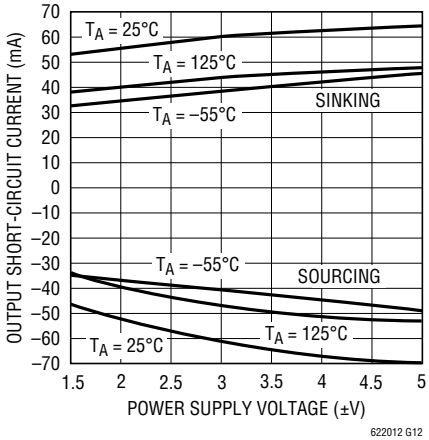
Output Saturation Voltage vs Load Current (Output High)



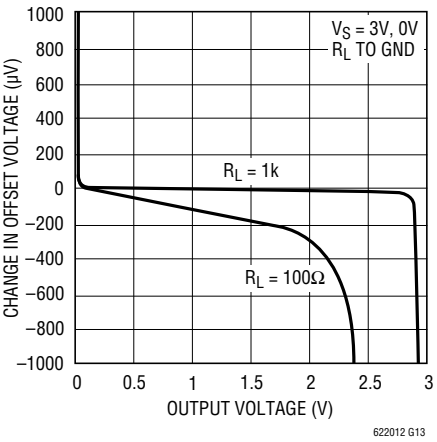
Minimum Supply Voltage



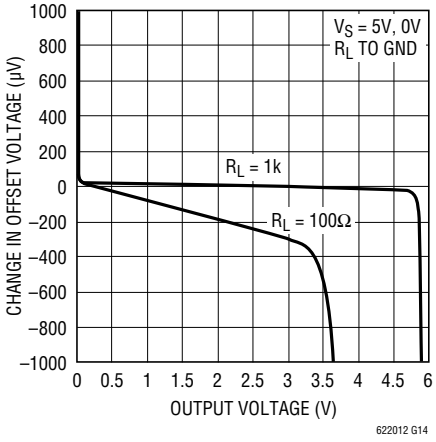
Output Short-Circuit Current vs Power Supply Voltage



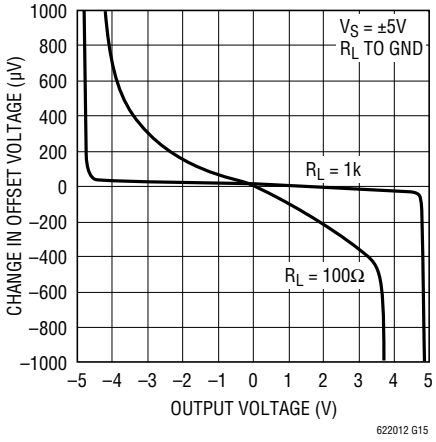
Open-Loop Gain



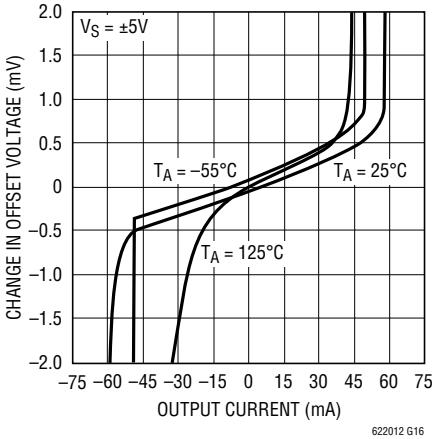
Open-Loop Gain



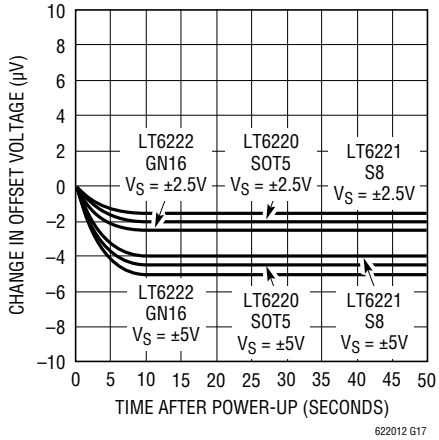
Open-Loop Gain



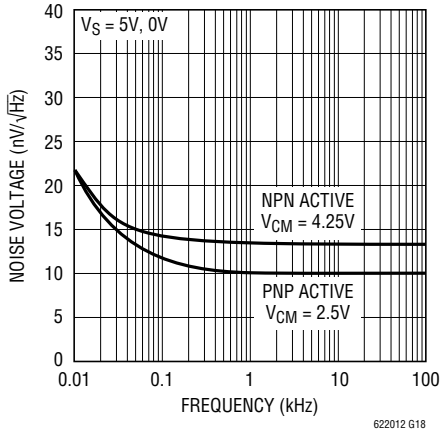
Offset Voltage vs Output Current



Warm-Up Drift vs Time

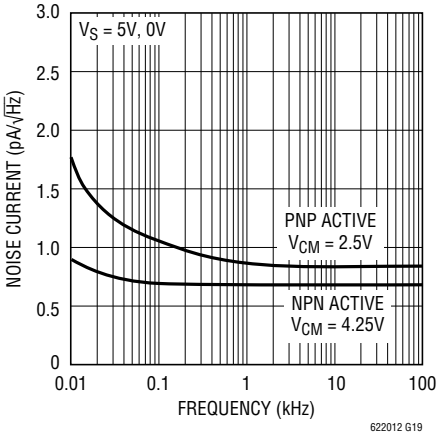


Input Noise Voltage vs Frequency

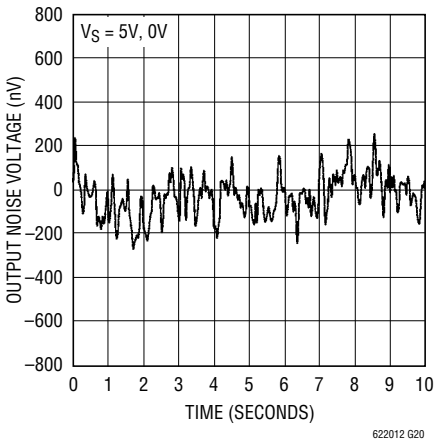


TYPICAL PERFORMANCE CHARACTERISTICS

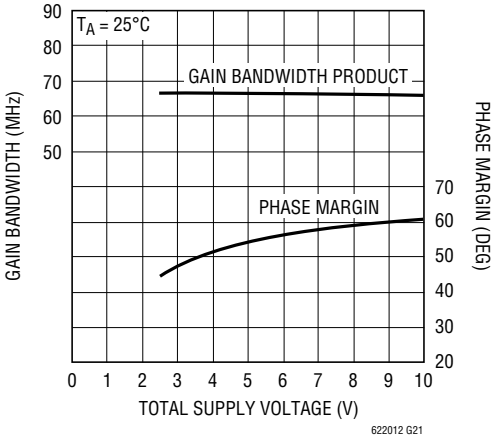
Input Current Noise vs Frequency



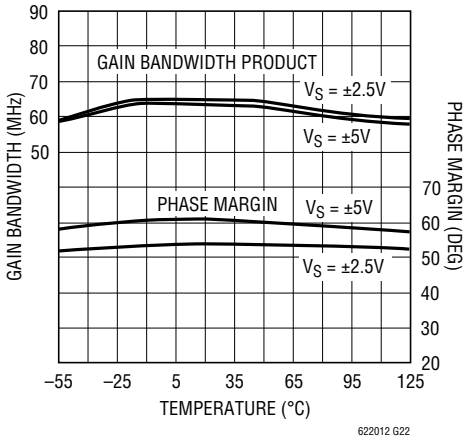
0.1Hz to 10Hz Output Voltage Noise



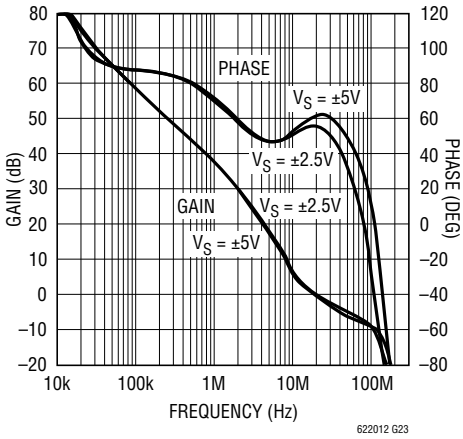
Gain Bandwidth and Phase Margin vs Supply Voltage



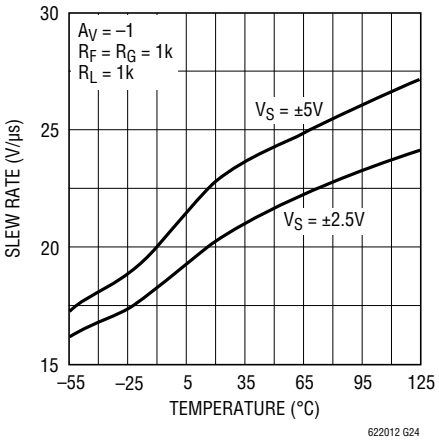
Gain Bandwidth and Phase Margin vs Temperature



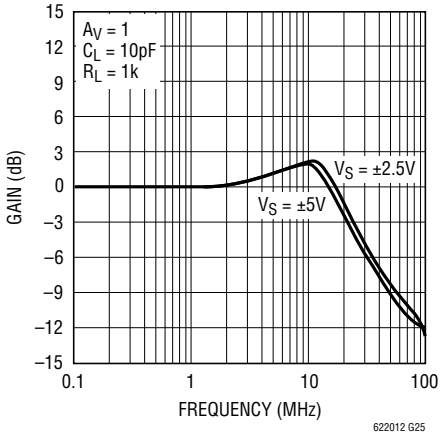
Gain and Phase vs Frequency



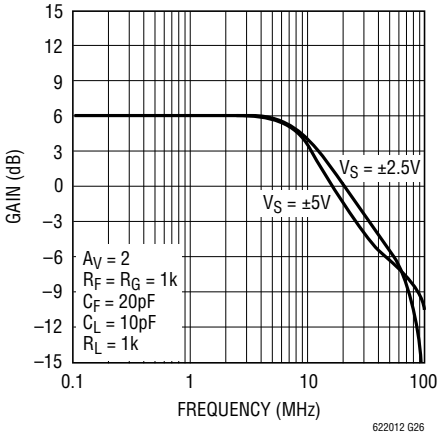
Slew Rate vs Temperature



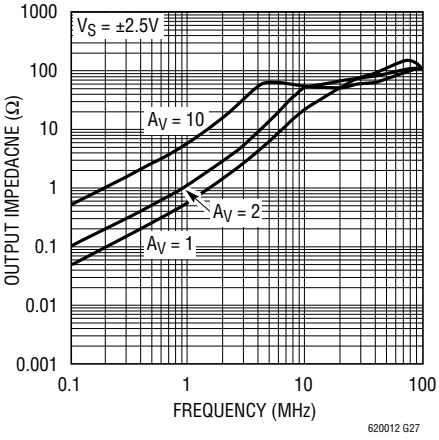
Gain vs Frequency (A_V = 1)



Gain vs Frequency (A_V = 2)

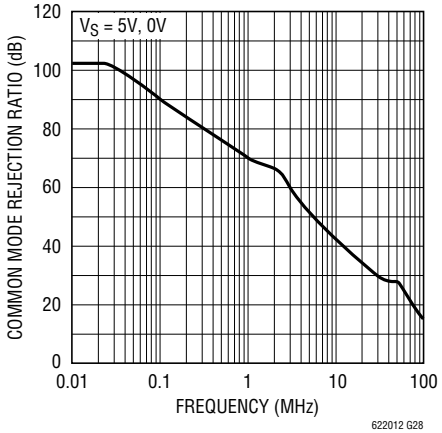


Output Impedance vs Frequency

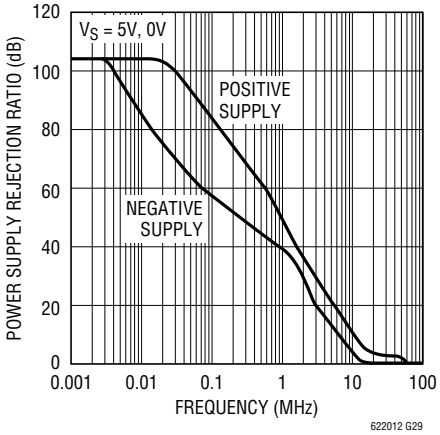


TYPICAL PERFORMANCE CHARACTERISTICS

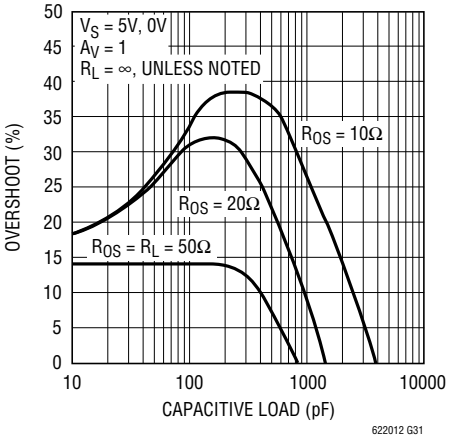
Common Mode Rejection Ratio vs Frequency



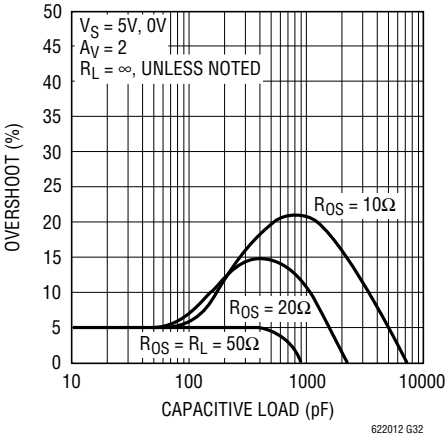
Power Supply Rejection Ratio vs Frequency



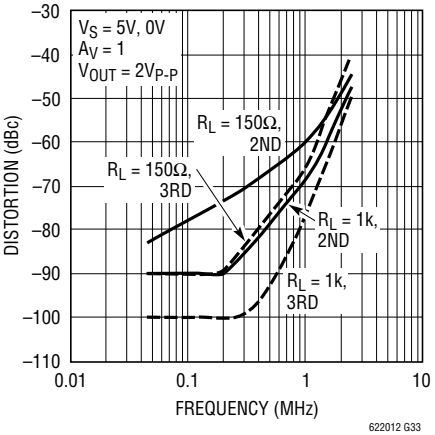
Series Output Resistor vs Capacitive Load



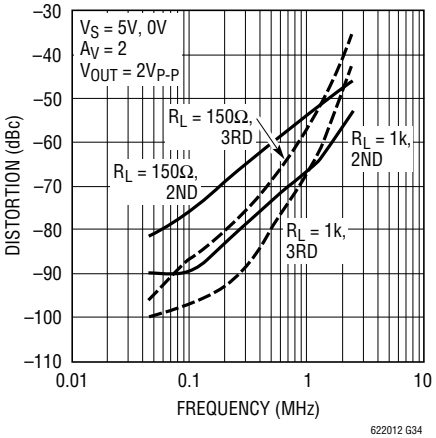
Series Output Resistor vs Capacitive Load



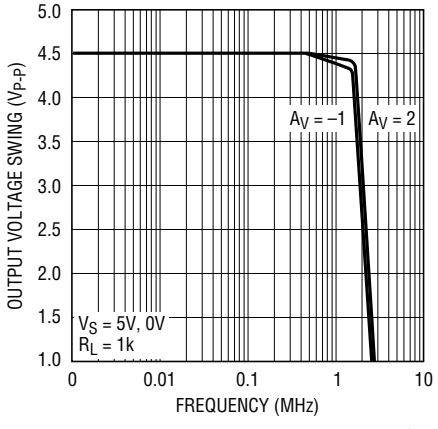
Distortion vs Frequency



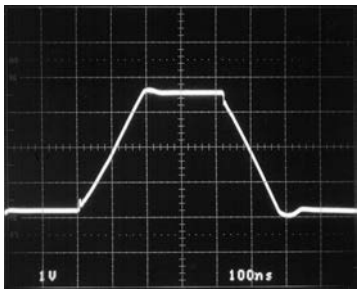
Distortion vs Frequency



Maximum Undistorted Output Signal vs Frequency

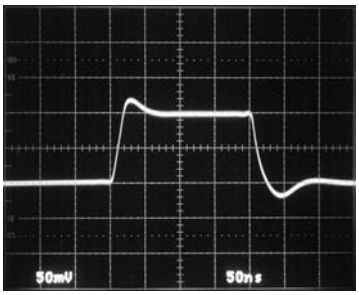


5V Large-Signal Response



V_S = 5V, 0V
A_V = 1
R_L = 1k
100ns/DIV
622012 G36

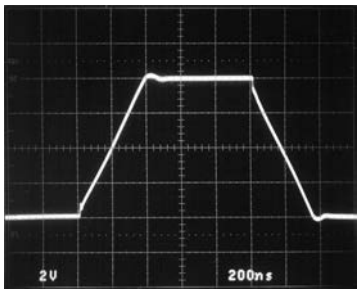
5V Small-Signal Response



V_S = 5V, 0V
A_V = 1
R_L = 1k
50ns/DIV
622012 G37

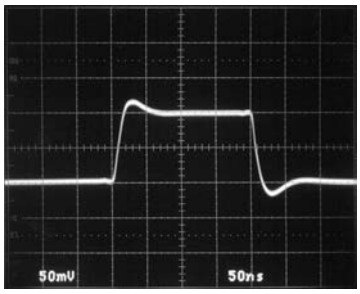
TYPICAL PERFORMANCE CHARACTERISTICS

±5V Large-Signal Response



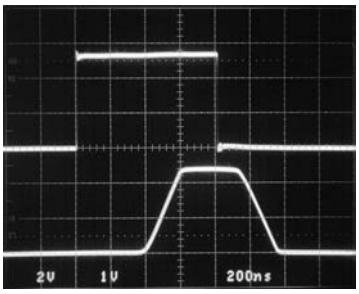
V_S = ±5V
A_V = 1
R_L = 1k
200ns/DIV
622012 G38

±5V Small-Signal Response



V_S = ±5V
A_V = 1
R_L = 1k
50ns/DIV
622012 G39

Output Overdriven Recovery



V_S = 5V, 0V
A_V = 2
R_L = 1k
200ns/DIV
622012 G40

APPLICATIONS INFORMATION

Circuit Description

The LT6220/LT6221/LT6222 have an input and output signal range that covers from the negative power supply to the positive power supply. Figure 1 depicts a simplified schematic of the amplifier. The input stage comprises two differential amplifiers, a PNP stage, Q1/Q2, and an NPN stage, Q3/Q4, that are active over different ranges of common mode input voltage. The PNP stage is active between the negative supply to approximately 1.2V below the positive supply. As the input voltage moves closer toward the positive supply, the transistor Q5 will steer the tail current, I_1, to the current mirror, Q6/Q7, activating the NPN differential pair and the PNP pair becomes inactive for the rest of the input common mode range up to the positive supply. Also, at the input stage, devices Q17 to Q19 act to cancel the bias current of the PNP input pair. When Q1/Q2 are active, the current in Q16 is controlled to be the same as the current Q1/Q2. Thus, the base current of Q16 is nominally equal to the base current of the input devices. The base current of Q16 is then mirrored by devices Q17-Q19 to cancel the base current of the input devices Q1/Q2.

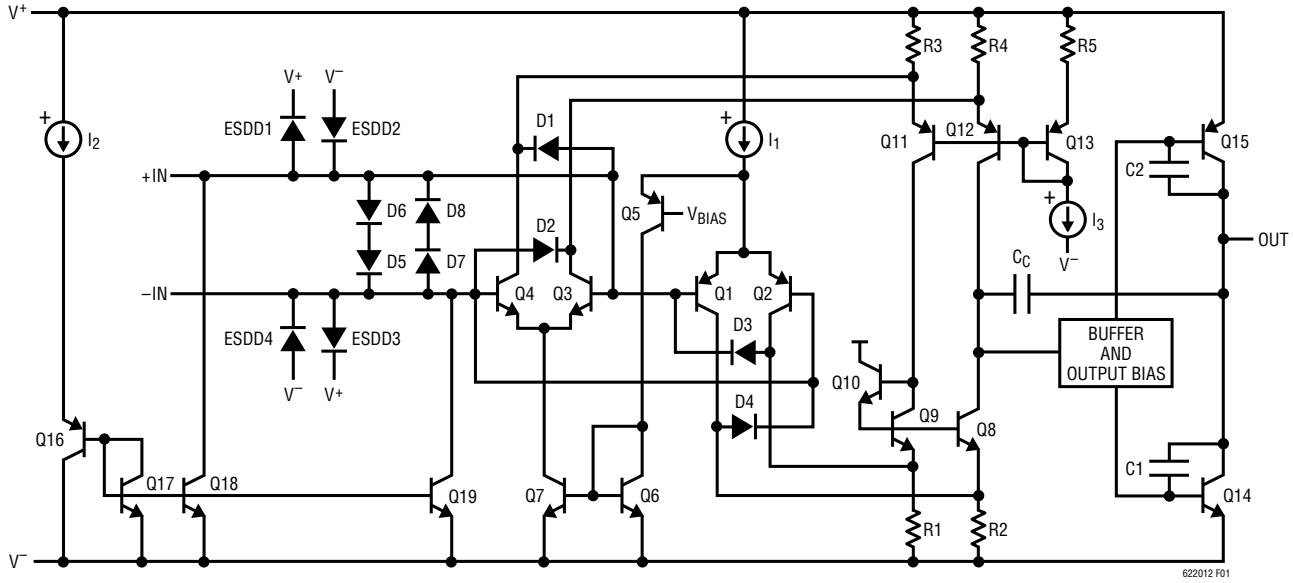


Figure 1. LT6220/LT6221/LT6222 Simplified Schematic Diagram

APPLICATIONS INFORMATION

A pair of complementary common emitter stages Q14/Q15 that enable the output to swing from rail-to-rail construct the output stage. The capacitors C2 and C3 form the local feedback loops that lower the output impedance at high frequency. These devices are fabricated by Linear Technology's proprietary high speed complementary bipolar process.

Power Dissipation

The LT6222, with four amplifiers, is housed in a small 16-lead SSOP package and typically has a thermal resistance (θ_{JA}) of 135°C/W. It is necessary to ensure that the die's junction temperature does not exceed 150°C. The junction temperature, T_J, is calculated from the ambient temperature, T_A, power dissipation, P_D, and thermal resistance, θ_{JA}:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The power dissipation in the IC is the function of the supply voltage, output voltage and the load resistance. For a given supply voltage, the worst-case power dissipation $P_{D(MAX)}$ occurs when the maximum supply current and the output voltage is at half of either supply voltage for a given load resistance. $P_{D(MAX)}$ is given by:

$$P_{D(MAX)} = \left(V_S \bullet I_{S(MAX)}\right) + \left(\frac{V_S}{2}\right)^2 / R_L$$

Example: For an LT6222 in a 16-lead SSOP package operating on ±5V supplies and driving a 100Ω load, the worst-case power dissipation is given by:

$$P_{D(MAX)}/Amp = (10 \bullet 1.8mA) + (2.5)^2 / 100$$
$$= 0.018 + 0.0625 = 80.5mW$$

If all four amplifiers are loaded simultaneously, then the total power dissipation is 322mW.

The maximum ambient temperature at which the part is allowed to operate is:

$$T_A = T_J - (P_{D(MAX)} \bullet 135°C/W)$$
$$= 150°C - (0.322W \bullet 135°C/W) = 106.5°C$$

Input Offset Voltage

The offset voltage will change depending upon which input stage is active. The PNP input stage is active from the negative supply rail to 1.2V below the positive supply rail, then the NPN input stage is activated for the remaining input range up to the positive supply rail during which the PNP stage remains inactive. The offset voltage is typically less than 70µV in the range that the PNP input stage is active.

Input Bias Current

The LT6220/LT6221/LT6222 employ a patent pending technique to trim the input bias current to less than 150nA for the input common mode voltage of 0.2V above the negative supply rail to 1.2V below the positive rail. The low input offset voltage and low input bias current of the LT6220/LT6221/LT6222 provide precision performance especially for high source impedance applications.

Output

The LT6220/LT6221/LT6222 can deliver a large output current, so the short-circuit current limit is set around 50mA to prevent damage to the device. Attention must be paid to keep the junction temperature of the IC below the absolute maximum rating of 150°C (refer to the Power Dissipation section) when the output is in continuous short circuit. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to several hundred milliamperes, no damage will occur to the device.

Overdrive Protection

When the input voltage exceeds the power supplies, two pair of crossing diodes, D1 to D4, will prevent the output from reversing polarity. If the input voltage exceeds either power supply by 700mV, diode D1/D2 or D3/D4 will turn on to keep the output at the proper polarity. For the phase reversal protection to perform properly, the input current must be limited to less than 5mA. If the amplifier

APPLICATIONS INFORMATION

is severely overdriven, an external resistor should be used to limit the overdriven current.

The LT6220/LT6221/LT6222's input stages are also protected against a large differential input voltage of 1.4V or higher by a pair of back-to-back diodes, D5/D8, to prevent the emitter-base breakdown of the input transistors. The current in these diodes should be limited to less than 10mA when they are active. The worse-case differential input voltage usually occurs when the input is driven while the output is shorted to ground in a unity-gain configuration. In addition, the amplifier is protected against ESD strikes up to 3kV on all pins by a pair of protection diodes on each pin that are connected to the power supplies as shown in Figure 1.

Capacitive Load

The LT6220/LT6221/LT6222 are optimized for high bandwidth, low power and precision applications. They can drive a capacitive load up to 100pF in a unity-gain configuration and more for higher gain. When driving a larger capacitive load, a resistor of 10Ω to 50Ω should be connected between the output and the capacitive load to avoid ringing or oscillation. The feedback should still be taken from the output so that the resistor will isolate the capacitive load to ensure stability. Graphs on capacitive loads show the transient response of the amplifier when driving capacitive load with specified series resistors.

Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input does not degrade stability. For instance, the LT6220/LT6221/LT6222, set up with a noninverting gain of 2, two 5k resistors and a capacitance of 5pF (part plus PC board), will probably oscillate. The pole is formed at 12.7MHz that will reduce phase margin by 52 degrees when the crossover frequency of the amplifier is around 10MHz. A capacitor of 10pF or higher connecting across the feedback resistor will eliminate any ringing or oscillation.

TYPICAL APPLICATIONS

Stepped-Gain Photodiode Amplifier

The circuit of Figure 2 is a stepped gain transimpedance photodiode amplifier. At low signal levels, the circuit has a high 100kΩ gain, but at high signal levels the circuit automatically and smoothly changes to a low 3.2kΩ gain. The benefit of a stepped gain approach is that it maximizes dynamic range, which is very useful on limited supplies. Put another way, in order to get 100kΩ sensitivity and still handle a 1mA signal level without resorting to gain reduction, the circuit would need a 100V negative voltage supply.

The operation of the circuit is quite simple. At low photodiode currents (below 10μA) the output and inverting input of the op amp will be no more than 1V below ground. The LT1634 in parallel with R3 and Q2 keep a constant current though Q2 of about 20μA. R4 maintains quiescent current through the LT1634 and pulls Q2's emitter above ground, so Q1 is reverse biased and no current flows through R2. So for small signals, the only feedback path is R1 (and C1) and the circuit is a simple transimpedance amplifier with 100kΩ gain.

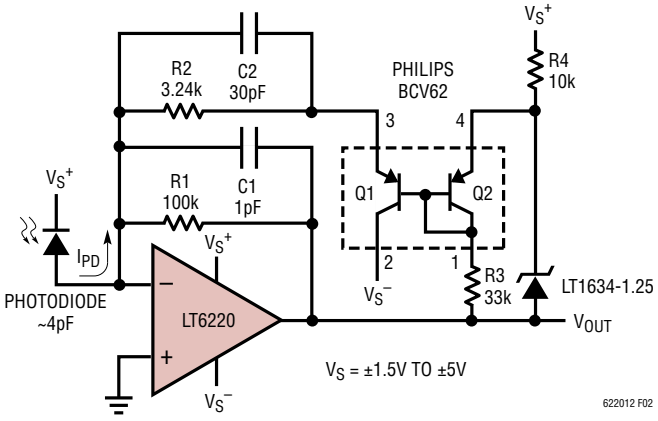


Figure 2. Stepped-Gain Photodiode Amplifier

TYPICAL APPLICATIONS

As the signal level increases though, the output of the op amp goes more negative. At 12.5µA of photodiode current, the 100kΩ gain dictates that the LT6220 output will be about 1.25V below ground. However, at that point the emitter of Q2 will be at ground, and the base of Q1 will be 1V below ground. Thus, Q1 turns on and photodiode current starts to flow through R2. The transimpedance gain is therefore now reduced to R1||R2, or about 3.1kΩ. The circuit response is shown in Figure 3. Note the smooth transition between the two operating gains, as well as the linearity.

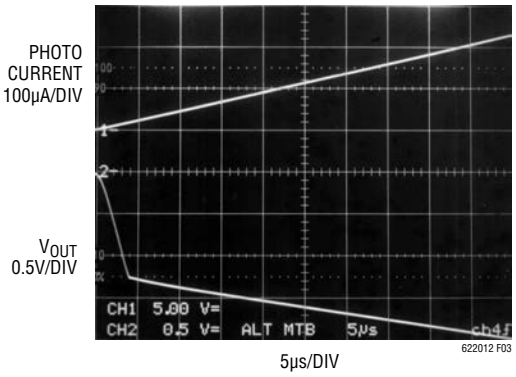


Figure 3. Stepped-Gain Photodiode Amplifier Response

Single 3V Supply, 1MHz, 4th Order Butterworth Filter

The circuit shown in Figure 4 makes use of the low voltage operation and the wide bandwidth of the LT6221 to create a DC accurate 1MHz 4th order lowpass filter powered from a 3V supply. The amplifiers are configured in the inverting mode for the lowest distortion and the output can swing rail-to-rail for maximum dynamic range. Figure 5 displays the frequency response of the filter. Stopband attenuation is greater than 100dB at 50MHz.

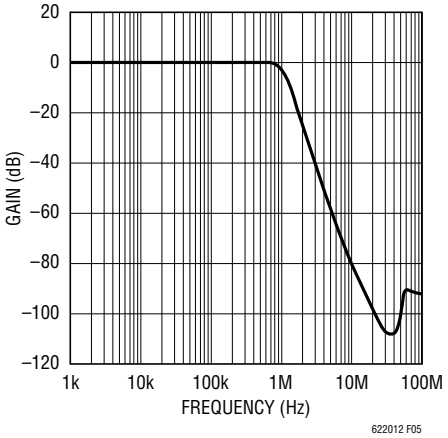


Figure 5. Frequency Response of Filter

Differential-In/Differential-Out Amplifier

The circuit of Figure 6 shows the LT6222 applied as a buffered differential-in differential-out amplifier with a gain of 2. Op amps A and B are configured as simple unity-gain buffers, offering high input impedance to upstream circuitry. Resistors R1 and R2 perform an averaging function on the common mode input voltage and R3 attenuates it by a factor of 2/3 and references it to the voltage source V_{OCM}. The resultant voltage, $V_{MID} = 2/3 \bullet V_{ICM}$, is placed at the noninverting inputs of op amps C and D. The other four resistors set gains of +3 from the noninverting input and –2 through the inverting path. Thus the output voltage of the upper path is:

$$-OUT = 3 \bullet (2/3 \bullet V_{ICM} + 1/3 \bullet V_{OCM}) - 2 \bullet (V_{ICM} + V_{DIFF}/2)$$
$$= 2V_{ICM} + V_{OCM} - 2V_{ICM} - V_{DIFF}$$
$$= V_{OCM} - V_{DIFF}$$

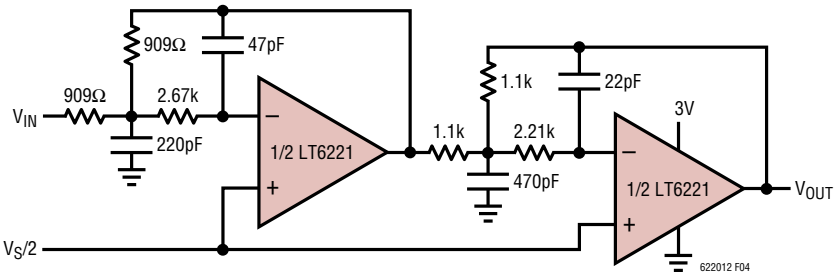


Figure 4. 3V, 1MHz, 4th Order Butterworth Filter

TYPICAL APPLICATIONS

and the output of the lower path is:

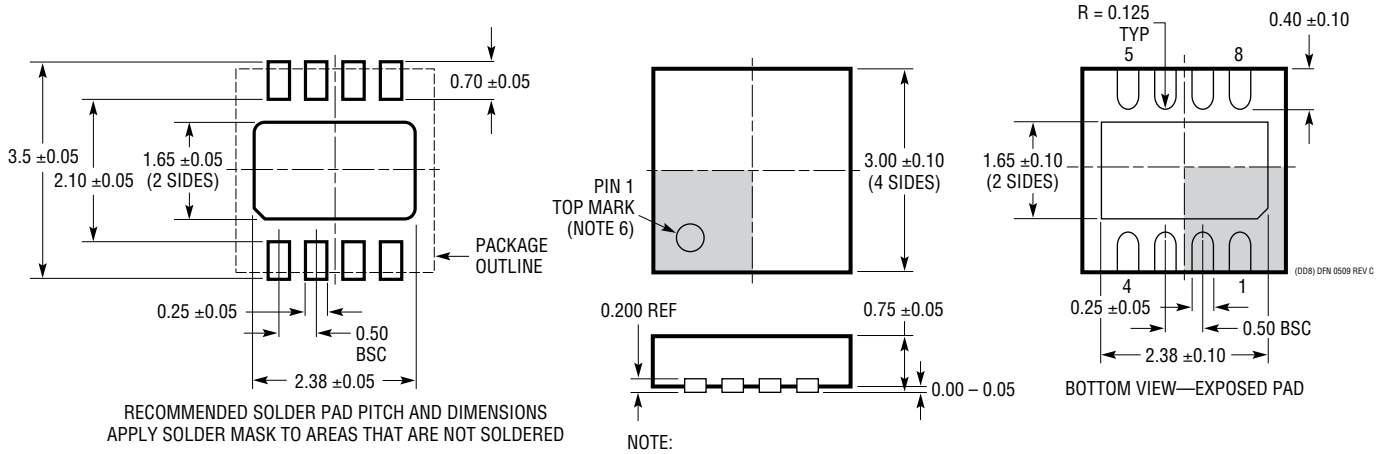
$$+OUT = 3 \bullet (2/3 \bullet V_{ICM} + 1/3 \bullet V_{OCM}) - 2 \bullet (V_{ICM} - V_{DIFF}/2)$$
$$= 2V_{ICM} + V_{OCM} - 2V_{ICM} + V_{DIFF}$$
$$= V_{OCM} + V_{DIFF}$$

Note that the input common mode voltage does not appear in the output as either a common mode or a difference mode term. However the voltage V_{OCM} does appear in the output terms, and with the same polarity, so it sets up the output DC level. Also, the differential input voltage V_{DIFF} appears fully at both outputs with opposite polarity, giving rise to the effective differential gain of 2. Calculations show that using 1% resistors gives worst-case input common mode feedthrough better than –31dB, whether looking at the output common mode or difference mode. Considering the 6dB of gain, worst-case common mode rejection ratio is 37dB. (Remember this is assuming 1% resistors. Of course, this can be improved with more precise resistors.) Results achieved on the bench with typical 1% resistors showed 67dB of CMRR at low frequency and 40dB CMRR at 1MHz. Gains other than 2 can be achieved by setting R3 = α • (R1||R2), R5 = α • R4 and R7 = α • R6 where gain = α.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)

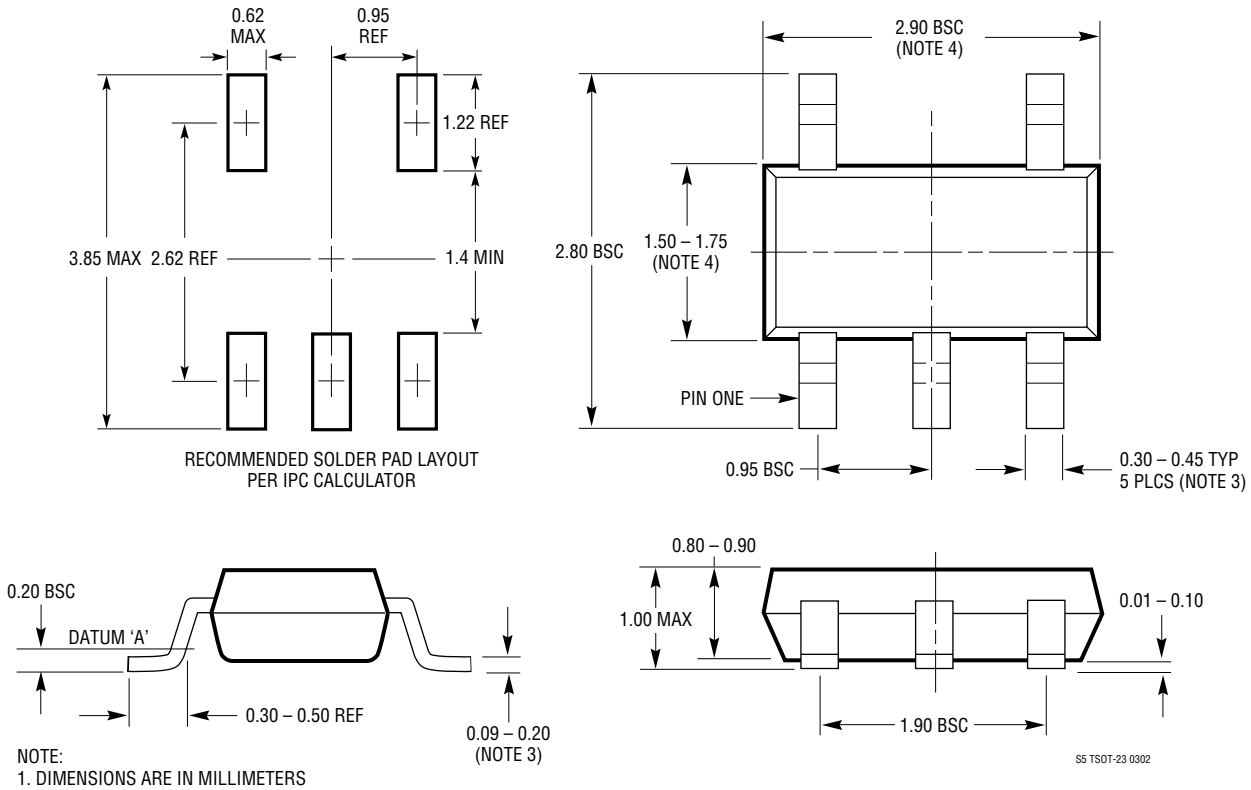


NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)

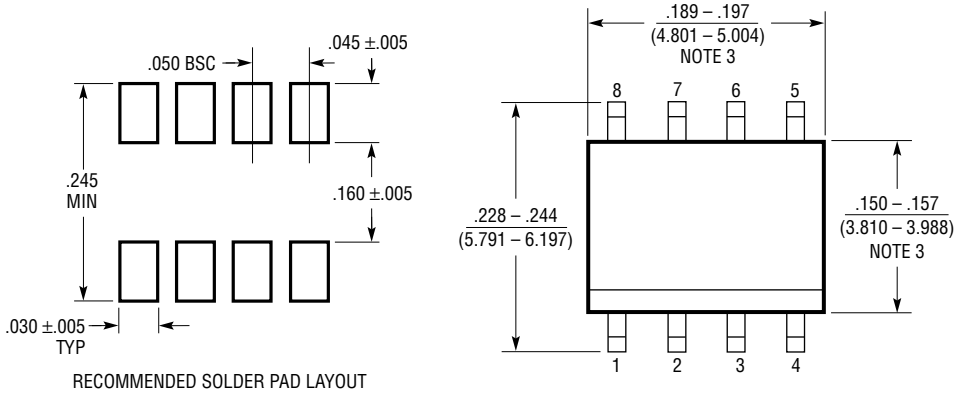


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



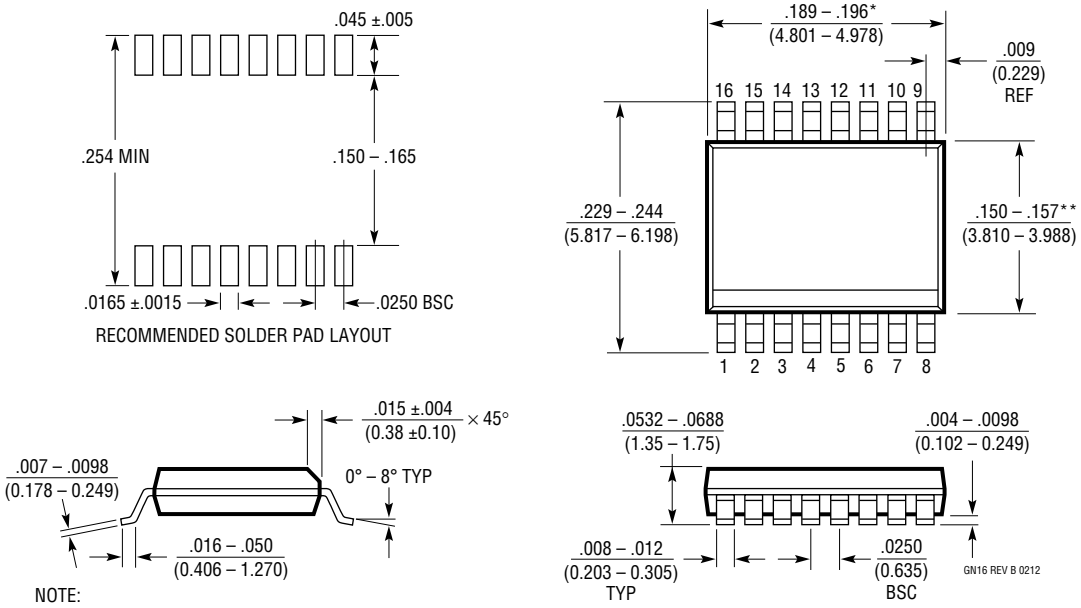
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	05/14	Added V_{OUT} information to Typical Application. Updated the Order Information table.	1 2
C	05/15	Updated Order Information table to reflect Specified Temperature Range	2

TYPICAL APPLICATION

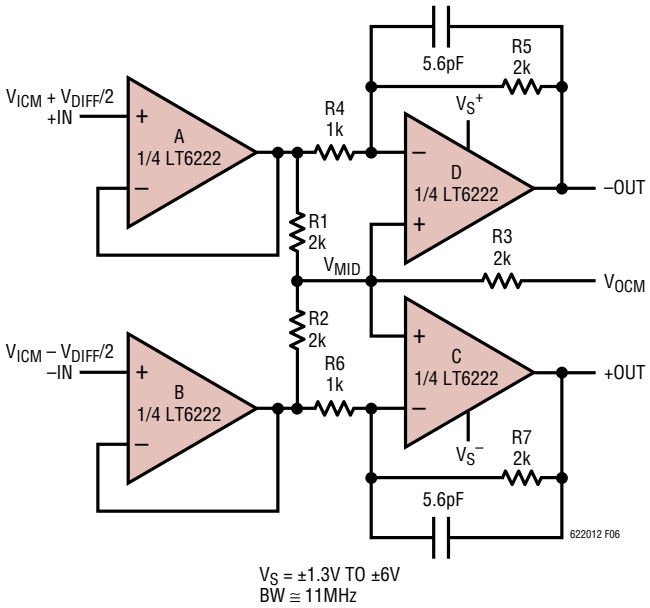


Figure 6. Buffered Gain of 2 Differential-In/Differential-Out Amplifier

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1498/LT1499	Dual/Quad 10MHz, 6V/µs Rail-to-Rail Input/ Output C_{LOAD} Op Amps	High DC Accuracy, 475µV $V_{OS(MAX)}$ Max Supply Current 2.2mA/Amp, Wide Supply Range, 2.2V to 30V
LT1800/LT1801/LT1802	Single/Dual/Quad 80MHz, 25V/µs, Low Power Rail-to-Rail Input/Output Precision Op Amps	350µV $V_{OS(MAX)}$, 250nA $I_{BIAS(MAX)}$, Max Supply Current 2mA/Amp
LT1803/LT1804/LT1805	Single/Dual/Quad 85MHz, 100V/µs Rail-to-Rail Input/Output Op Amps	2mV $V_{OS(MAX)}$, Max Supply Current 3mA/Amp
LT1806/LT1807	Single/Dual 325MHz, 140V/µs Rail-to-Rail Input/ Output Op Amps	High DC Accuracy, 550µV $V_{OS(MAX)}$ Max Low Noise 3.5nV/$\sqrt{Hz}$ Low Distortion –80dBc at 5MHz, Power Down (LT1806)
LT1809/LT1810	Single/Dual 180MHz, Rail-to-Rail Input/Output Op Amps	350V/µs Slew Rate, Low Distortion –90dBc at 5MHz, Power Down (LT1809)

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