60V LED Driver with 4A Switch Current

FEATURES

- **4000:1 True Color PWM™ Dimming**
- **4A, 60V Internal DMOS Switch**
- **Wide Input Voltage Range: 3V to 42V**
- **0V to 60V Output Current Regulation with Monitor**
- **PMOS Switch Driver for PWM and Output Disconnect**
- **LED Short-Circuit Protection and $\overline{\text{SHORTLED}}$ Flag**
- **Internal Spread Spectrum Frequency Modulation**
- Constant-Current and Constant-Voltage Regulation
- Input Current Limit and Monitor
- Adjustable Frequency: 200kHz to 3MHz, Synchronizable to an External Clock
- 10:1 Analog Dimming
- Programmable Open-LED Protection with $\overline{\text{OPENLED}}$ Flag
- Programmable V_{IN} Undervoltage and Overvoltage Lockout
- Available in a 28-Lead TSSOP Package

APPLICATIONS

- Display Backlighting
- Automotive and Avionic Lighting
- Accurate Current-Limited Voltage Regulators

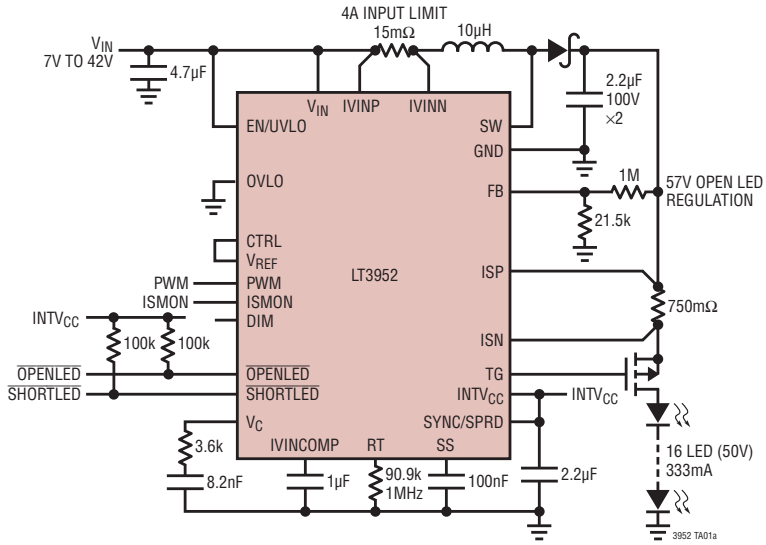
DESCRIPTION

The LT®3952 is a current mode step-up DC/DC converter with an internal, 60V, 80mΩ DMOS power switch. The LT3952 is specifically designed to drive high power LEDs in multiple configurations. It combines input and output current regulation loops with output voltage regulation to operate as a flexible current/voltage source.

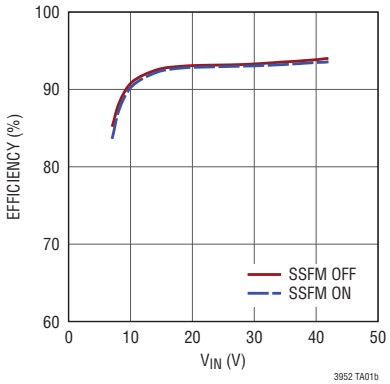
Programmable switching frequency with optional spread-spectrum modulation provides EMI reduction, while still allowing optimization of the external components for efficiency or component size. The LED current is programmable with an external sense resistor, and can be adjusted from zero to full scale with a voltage at the CTRL pin. The external PWM input provides LED ON/OFF control and 4000:1 dimming ratio, and an internal PWM generator delivers the efficiency of PWM dimming to standalone or I/O limited applications. The LT3952 is available in the thermally enhanced 28-lead TSSOP package.

TYPICAL APPLICATION

Short-Circuit Robust Boost LED Driver with Spread Spectrum Frequency Modulation



Efficiency vs Input Voltage

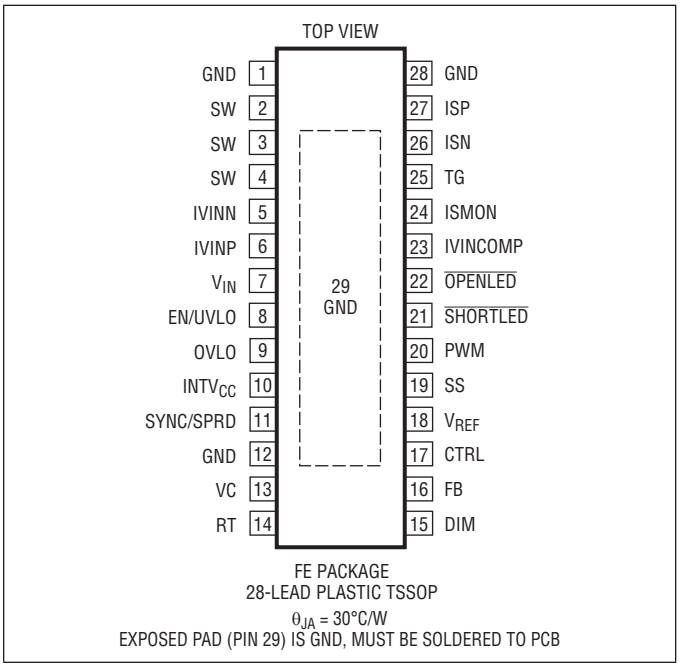


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, IVINP, IVINN, $\overline{SHORTLED}$, $\overline{OPENLED}$, EN/UVLO 42V
OVLO 12V
SW, ISP, ISN, TG 60V
IVINP-IVINN ..... –1V to 3V
CTRL, FB, DIM, SYNC/SPRD, PWM ..... $INTV_{CC}$ + 0.3V
VC, SS, ISMON, IVINCOMP 3V
RT, V_{REF} 2V
$INTV_{CC}$ (Note 4) 3.6V
Operating Junction Temperature Range (Notes 2, 3)
LT3952E/LT3952I ..... –40°C to 125°C
LT3952H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



FE PACKAGE
28-LEAD PLASTIC TSSOP
θ_{JA} = 30°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3952EFE#PBF	LT3952EFE#TRPBF	LT3952FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3952IFE#PBF	LT3952IFE#TRPBF	LT3952FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3952HFE#PBF	LT3952HFE#TRPBF	LT3952FE	28-Lead Plastic TSSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = IVINP = IVINN = 12V, ISP = ISN = 24V, EN/UVLO = PWM = 3V, CTRL = 2V, OVLO = 0V unless otherwise noted

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage					3	V
Supply Current	FB = 1.3V, R_T = 40.2k, CTRL = 0V EN/UVLO = 0V, CTRL = 0V EN/UVLO = 1.15V, CTRL = 0V			1.5 0 35	2.2 1 60	mA µA µA
Internal Regulator						
$INTV_{CC}$ Output Voltage	CTRL = 0V		2.90	3.00	3.10	V
$INTV_{CC}$ Dropout Voltage	V_{IN} = 3V, CTRL = 0V			150		mV
$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Rising, CTRL = 0V		2.62	2.68	2.74	V
$INTV_{CC}$ UVLO Hysteresis	CTRL = 0V			200		mV
Reference Voltage Output						
V_{REF} Voltage	I_{VREF} = –100µA , CTRL = 0V	●	1.955	2.000	2.045	V
V_{REF} Line Regulation	3V < V_{IN} < 42V , CTRL = 0V			0.01		%/V
V_{REF} Load Regulation	0µA < I_{VREF} < –100µA , CTRL = 0V			0.6		%
Current Feedback						
CTRL Range for Current Sense Threshold Adjustment			0.2		1.2	V
CTRL PWM Shutdown Threshold	CTRL Falling			100	125	mV
CTRL PWM Threshold Hysteresis				12.5		mV
CTRL Zero-Scale Offset				200		mV
CTRL Input Bias Current	CTRL = 0V, Current Out of Pin			20	100	nA
Current Sense Common Mode Input Range	CTRL = 1.5V		0		60	V
Full-Scale Current Sense Accuracy (V_{ISP}-V_{ISN})	ISP = 60V, CTRL = 1.5V	●	245	250	255	mV
Midrange Current Sense Accuracy (V_{ISP}-V_{ISN})	ISP = 60V, CTRL = 0.7V		115	125	135	mV
1/10th Scale Current Sense Accuracy (V_{ISP}-V_{ISN})	ISP = 60V, CTRL = 0.3V		10	25	40	mV
Low Side Current Sense Accuracy (V_{ISP}-V_{ISN})	ISP = 0V, CTRL = 1.5V	●	240	250	260	mV
Overcurrent Sense Threshold		●	350	375	390	mV
ISP to VC Transconductance	CTRL = 1.5V			275		µS
ISP/ISN Input Bias Current	PWM = 5V (Active), ISP = 60V PWM = 0V (Standby), ISP = 60V			250 0	 0.1	µA µA
Current Sense Monitor Ratio (V_{ISMON})/(V_{ISP}-V_{ISN})	CTRL = 0.4V, 0.8V			4		V/V
Current Sense Monitor Accuracy (V_{ISMON})	CTRL = 1.5V , ISP = 60V		0.950	1.000	1.050	V
Input Current Sense Amplifier						
Amplifier Supply Current (From IVINP)	IVINP = IVINN = 42V			35	60	µA
I_{VIN} Regulation Threshold ($V_{IVINP-IVINN}$)		●	55	60	65	mV
$I_{VINCOMP}$ to VC Transconductance				1650		µS
Input Common Mode Minimum Voltage					3	V
IVINP/IVINN to Monitor Voltage Gain	$V_{IVINP-IVINN}$ = 30mV			20		V/V

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TG Gate Driver						
PWM Input High Threshold	PWM Rising	●	1.15	1.2	1.25	V
PWM Hysteresis				20		mV
TG On Voltage	V_{ISP-TG}, V_{ISP} > 10V			7.5	9.5	V
TG Off Voltage	V_{ISP-TG}, PWM = 0V			0	0.3	V
TG Turn-On Time	C_{LOAD} = 470pF, PWM Rising			100		ns
TG Turn-Off Time	C_{LOAD} = 470pF, PWM Falling			150		ns
Output Voltage Feedback						
FB Voltage Regulation Threshold (V_{FB})	CTRL = 1.5V	 ●	1.188 1.182	1.200 1.200	1.212 1.218	V V
FB Open-LED Threshold	FB Rising		V_{FB} – 65mV	V_{FB} – 45mV	V_{FB} – 25mV	V
FB Open-LED Threshold Hysteresis				15		mV
FB Overvoltage Threshold	FB Rising		V_{FB} + 15mV	V_{FB} + 30mV	V_{FB} + 40mV	V
FB Overvoltage Threshold Hysteresis				15		mV
FB Pin Bias Current		●		20	100	nA
Feedback Line Regulation	3V < V_{IN} < 42V			0.0003		%/V
FB to VC Transconductance				450		µS
VC Output Impedance				5000		kΩ
Soft-Start						
Soft-Start Sourcing Current	Current Out of Pin, SS = 0.1V		18	25	37	µA
Soft-Start Sinking Current	SS = 1.8V		1.5	2.5	4.1	µA
Soft-Start Hiccup Retry Threshold				200		mV
Soft-Start Strong Pull-Down On-Resistance				120		Ω
Oscillator						
RT Voltage				1.20		V
Switching Frequency	R_T = 470k R_T = 90.9k R_T = 40.2k R_T = 25.5k	 ● 	180 0.95 1.90 2.75	215 1.0 2.0 3.0	250 1.05 2.10 3.25	kHz MHz MHz MHz
Maximum Duty Cycle	R_T = 470k SYNC = 300kHz Clock Signal, R_T = 470k R_T = 90.9k R_T = 40.2k R_T = 25.5k	 ● 	98 97 92 85	99 98 95 90 80		% % % % %
Minimum Off-Time				50		ns
Minimum On-Time				75		ns
SYNC/SPRD Pin Resistance to GND	V_{SYNC} = 2V			100		kΩ
SYNC/SPRD Input High Threshold			1.5			V
SYNC/SPRD Input Low Threshold					0.4	V
Spread Spectrum Minimum Step as Percentage of f_{SW}				1		%
Spread Spectrum Maximum Step as Percentage of f_{SW}				31		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = IVINP = IVINN = 12V, ISP = ISN = 24V, EN/UVLO = PWM = 3V, CTRL = 2V, OVLO = 0V unless otherwise noted

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PWM Generator						
PWM Pin Pull-Up/Pull-Down Current	PWM = 1.2V, DIM = 0.7V	●	5	10	15	µA
PWM Generator Lower Threshold Offset	0.2V < DIM < 1.2V		V_{DIM} – 15	V_{DIM} + 0	V_{DIM} + 15	mV
PWM Generator Upper Threshold Offset	0.2V < DIM < 1.2V		V_{DIM} + 825	V_{DIM} + 950	V_{DIM} + 1075	mV
PWM Generator Frequency	DIM = 0.7V, C_{PWM} = 22nF			230		Hz
DIM Pin Output Current	DIM = 0.7V	●	10	20	30	µA
TG Duty Cycle Using PWM Generator	DIM = 0.345V DIM = 0.535V DIM = 0.725V DIM = 1.105V		1 21 42.5 86	10 30 50 90	21 39 57.5 94	% % % %
Power Switch						
Switch On-Resistance	I_{SW} = 500mA			80		mΩ
Switch Leakage Current	SW = 60V, CTRL = 0V				2	µA
VC to Current Threshold Transconductance				7.5		S
Maximum Power Switch Current Limit	VC = 2V		4	4.5	5	A
Logic Inputs/Outputs						
EN/UVLO Disable Threshold	EN/UVLO Falling	●	1.191	1.230	1.269	V
EN/UVLO Threshold Internal Hysteresis				75		mV
EN/UVLO Hysteresis Current	EN/UVLO = 1.25V, Device in Shutdown EN/UVLO = 1.5V, Device in Operation			2 0	 0.4	µA µA
OVLO Threshold	OVLO Rising	●	1.191	1.230	1.269	V
OVLO Threshold Hysteresis				25		mV
OVLO Input Bias Current	OVLO = 1V			15	100	nA
$\overline{\text{SHORTLED}}$ On-Resistance	$I_{\overline{\text{SHORTLED}}}$ = 1mA			60		Ω
$\overline{\text{SHORTLED}}$ Output Low Voltage	$I_{\overline{\text{SHORTLED}}}$ = 2mA				0.3	V
$\overline{\text{SHORTLED}}$ Off-State Leakage	$\overline{\text{SHORTLED}}$ = 42V				1	µA
$\overline{\text{OPENLED}}$ On-Resistance	$I_{\overline{\text{OPENLED}}}$ = 1mA			60		Ω
$\overline{\text{OPENLED}}$ Output Low Voltage	$I_{\overline{\text{OPENLED}}}$ = 2mA				0.3	V
$\overline{\text{OPENLED}}$ Off-State Leakage	$\overline{\text{OPENLED}}$ = 42V				1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

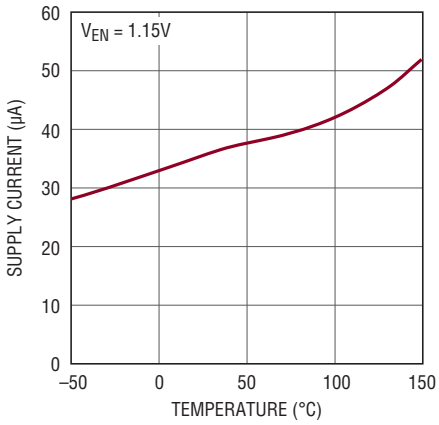
Note 2: The LT3952E is guaranteed to meet specified performance from 0°C to 125°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3952I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range. The LT3952H is guaranteed to meet performance specifications over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: The LT3952 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature is active. Continuous operating above the specified maximum operating junction temperature may impair device reliability.

Note 4: $INTV_{CC}$ is an output and is not meant to be externally driven.

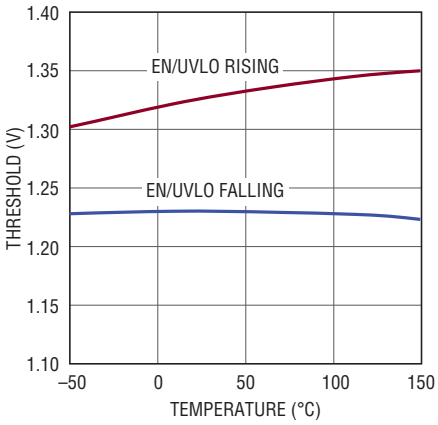
TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown Current vs Temperature



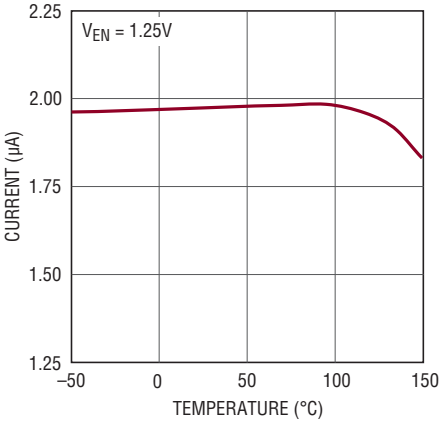
3952 G01

EN/UVLO Thresholds vs Temperature



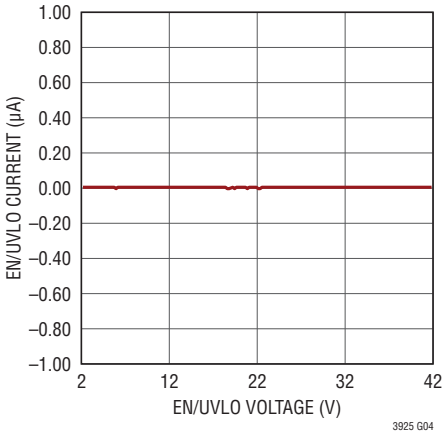
3952 G02

EN/UVLO Hysteresis Current vs Temperature



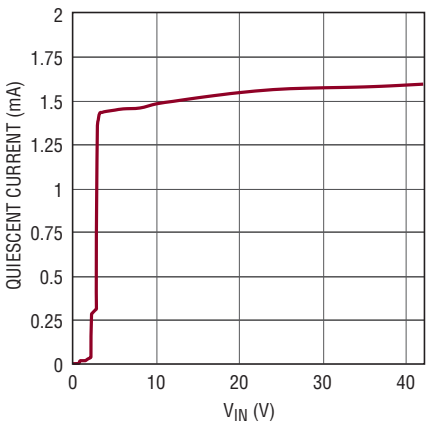
3952 G03

EN/UVLO Bias Current above Threshold



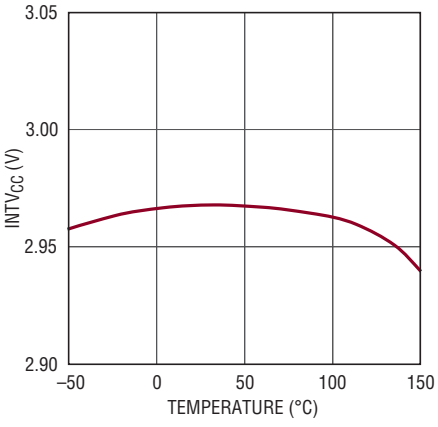
3925 G04

Quiescent Current vs Input Voltage



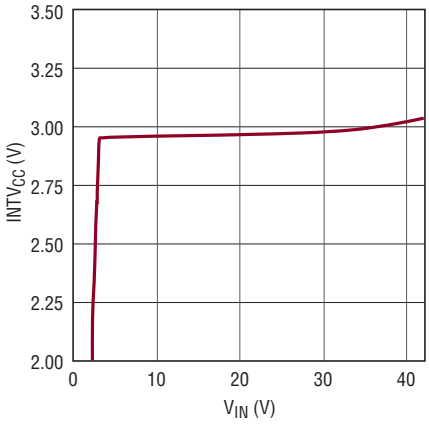
3952 G05

$INTV_{CC}$ Voltage vs Temperature



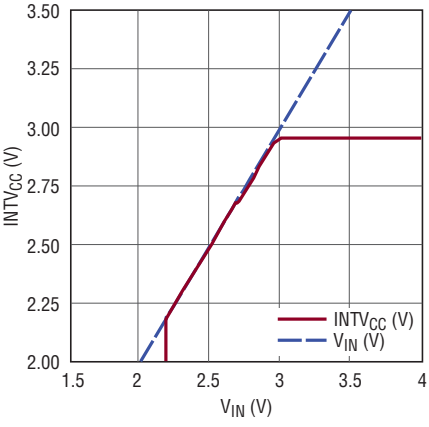
3952 G06

$INTV_{CC}$ vs Input Voltage



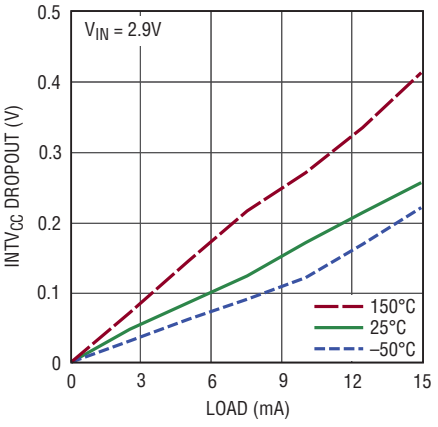
3952 G07

$INTV_{CC}$ vs Input Voltage, Dropout



3952 G08

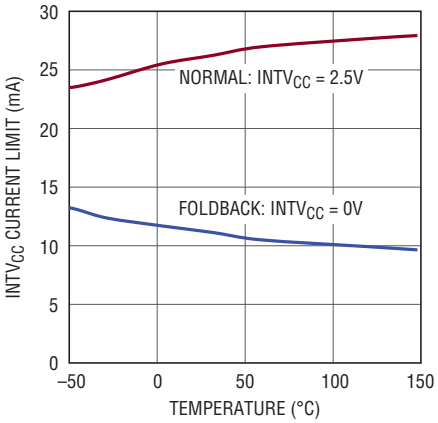
$INTV_{CC}$ Dropout vs Load and Temperature



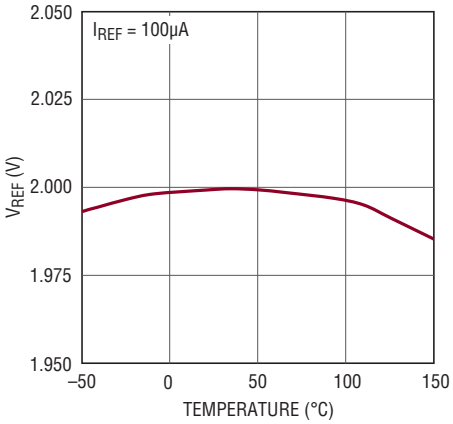
3952 G09

TYPICAL PERFORMANCE CHARACTERISTICS

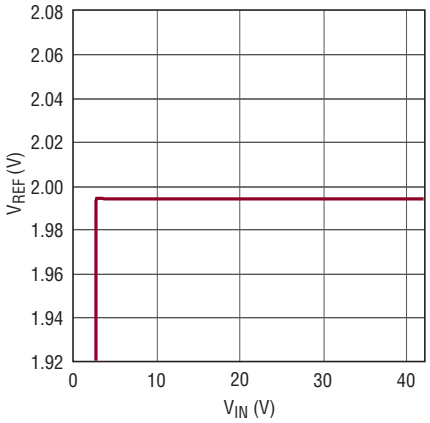
$INTV_{CC}$ Current Limit vs Temperature



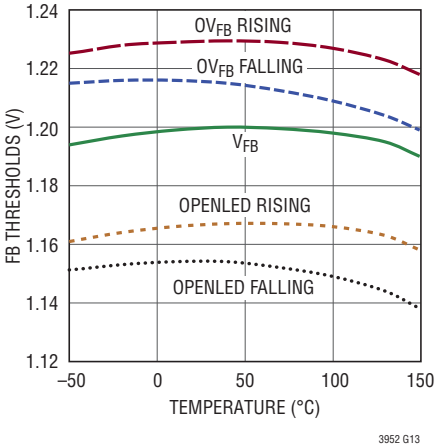
V_{REF} Voltage vs Temperature



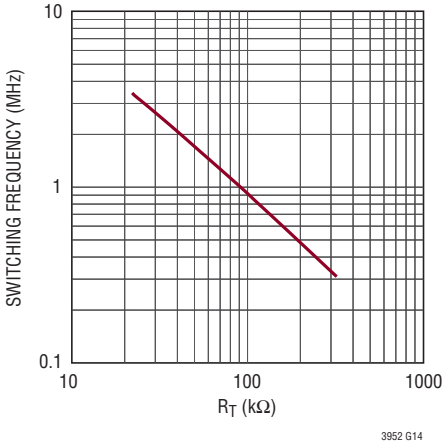
Reference Voltage vs Input Voltage



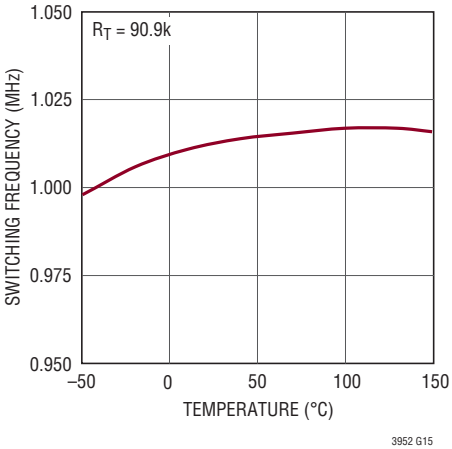
FB Thresholds vs Temperature



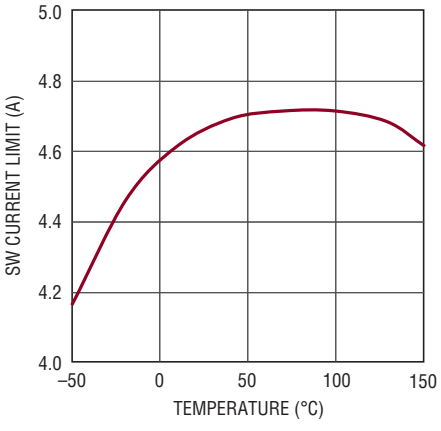
Switching Frequency vs R_T



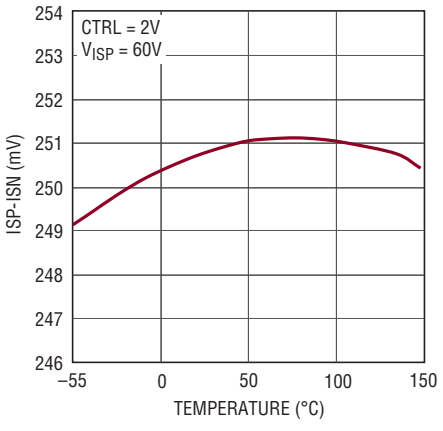
Switching Frequency vs Temperature



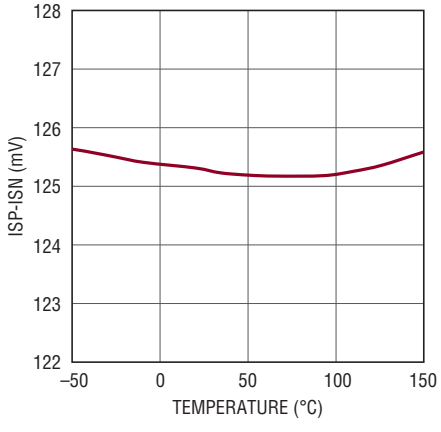
SW Current Limit vs Temperature



ISP/ISN Full-Scale Threshold vs Temperature

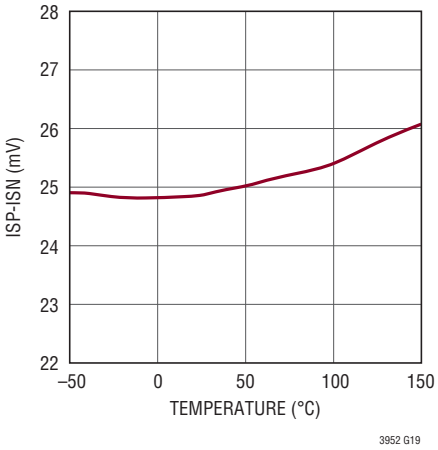


ISP/ISN Mid-Scale Threshold (CTRL = 0.7V) vs Temperature

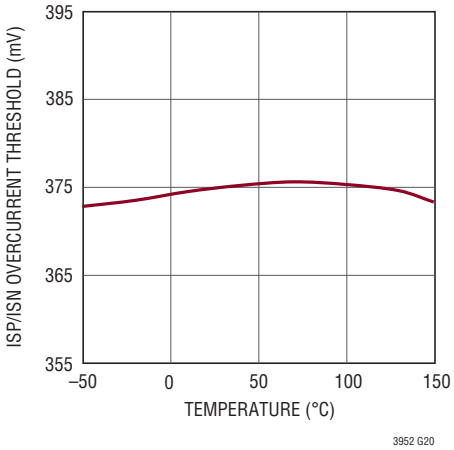


TYPICAL PERFORMANCE CHARACTERISTICS

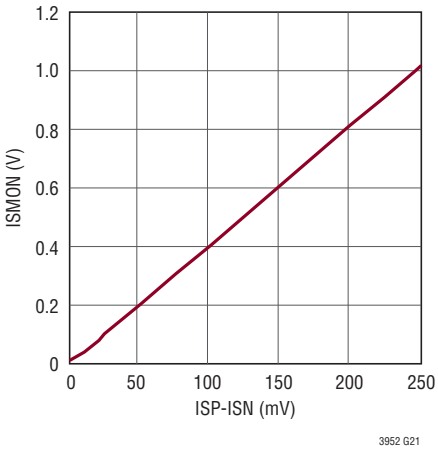
ISP/ISN 1/10th Scale Threshold (CTRL = 0.3V) vs Temperature



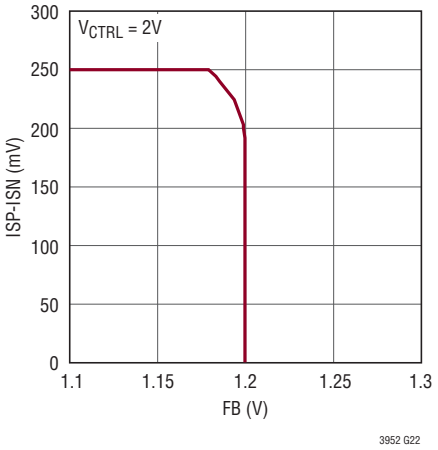
ISP/ISN Overcurrent Threshold vs Temperature



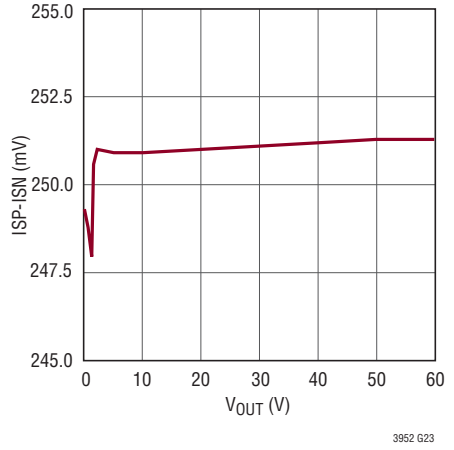
ISMON Voltage vs ISP-ISN Voltage



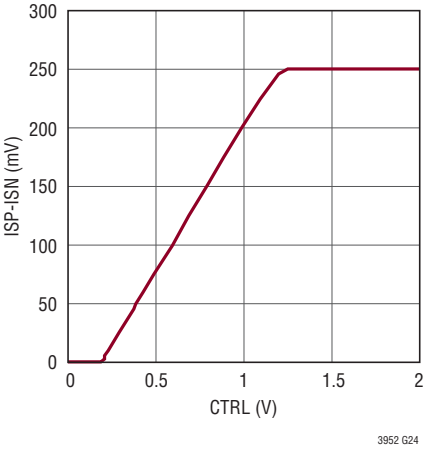
$V_{ISP-ISN}$ Threshold vs FB Voltage



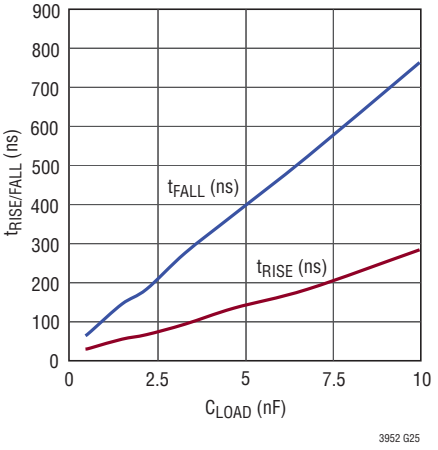
ISP-ISN Threshold vs Output Voltage



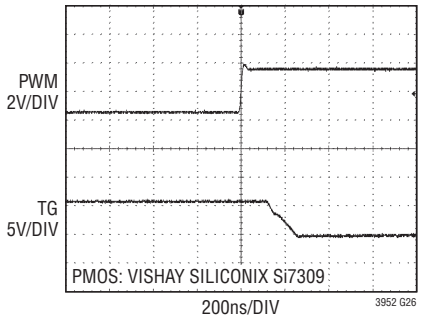
$V_{ISP-ISN}$ Threshold vs CTRL



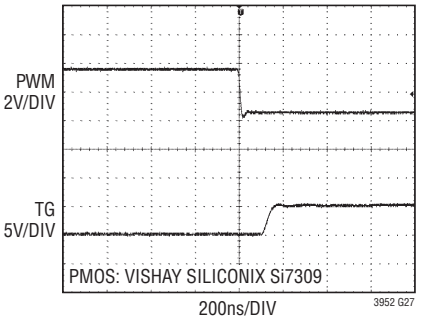
TG Rise/Fall Time vs Capacitance



TG Driver Turn-On

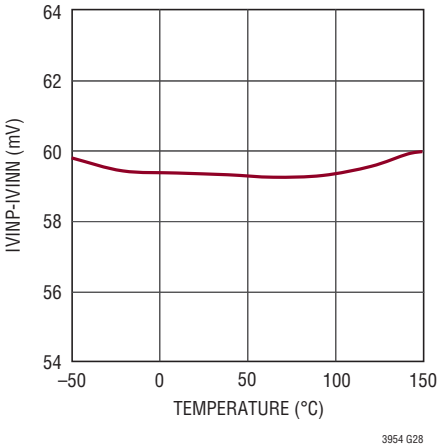


TG Driver Turn-Off

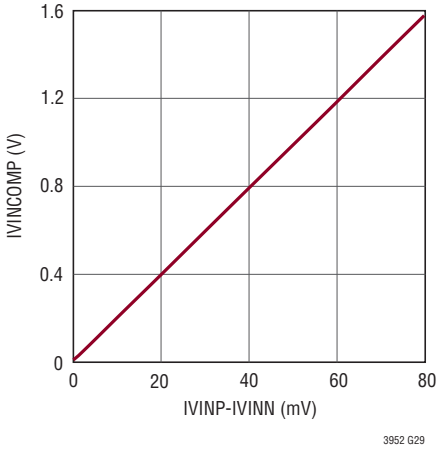


TYPICAL PERFORMANCE CHARACTERISTICS

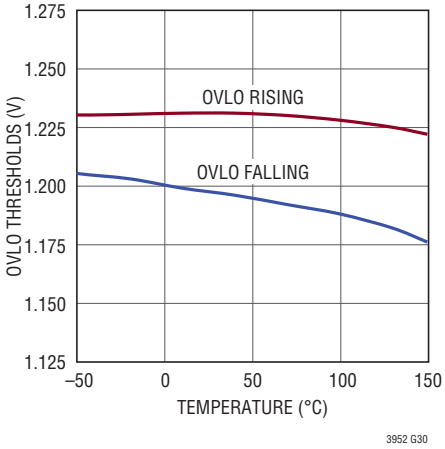
IVINP-IVINN Threshold vs Temperature



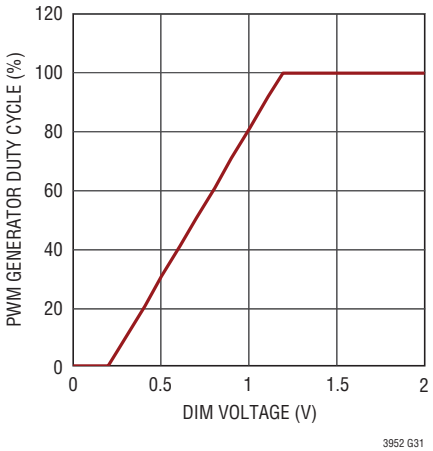
IVINCOMP vs IVINN-IVINP



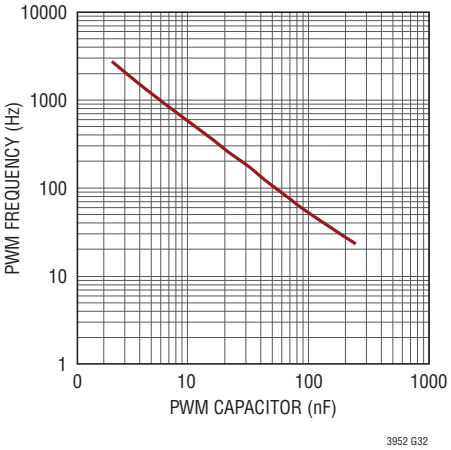
OVLO Thresholds vs Temperature



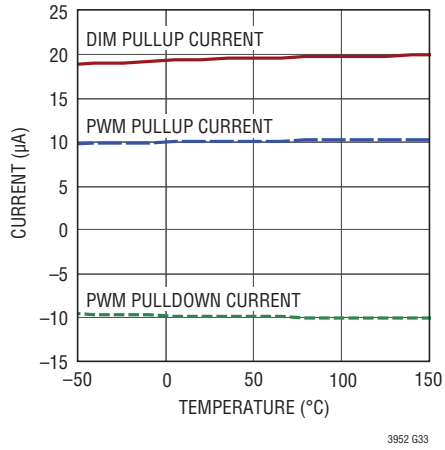
PWM Generator Duty Cycle vs DIM Voltage



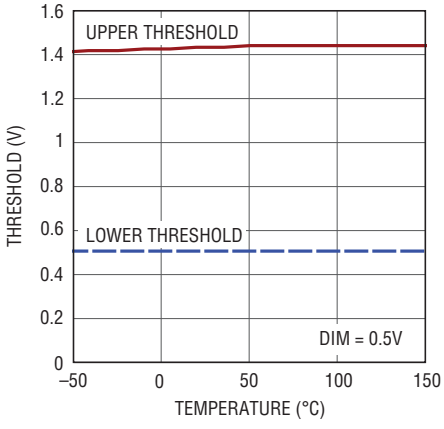
PWM Generator Frequency vs PWM Capacitor



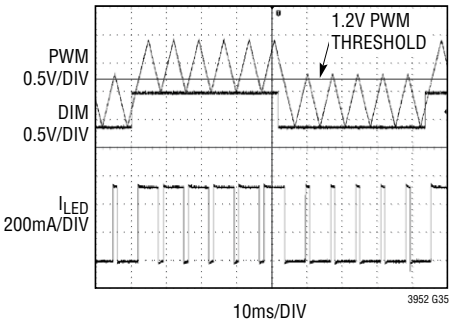
PWM Generator Currents vs Temperature



PWM Generator Thresholds vs Temperature



PWM Generator Operation and Step



PIN FUNCTIONS

GND (1, 12, 28, Exposed Pad Pin 29): Ground Pins. The exposed pad of the LT3952 acts as both GND and heat sink. It must be connected to a large copper area for proper operation.

SW (Pins 2, 3, 4): Switch Pins. Minimize copper area at these pins to increase efficiency and reduce EMI.

IVINN (Pin 5): Input Current Sense Amplifier Negative Input. The input current sense amplifier reduces the switching current in the case of an overload. VC is reduced when the IVINP-IVINN voltage exceeds the 60mV built-in potential. Tie IVINP-IVINN across an external sense resistor to set auxiliary current limit. If unused, tie to V_{IN}.

IVINP (Pin 6): Auxiliary Current Sense Amplifier Positive Input. Also acts as the bias supply for the amplifier to provide a function independent from the V_{IN} pin. The IVINP/IVINN amplifier can operate from voltages either above or below V_{IN}. Tie this pin to the positive terminal of a sense resistor, and do not use resistance in series with this pin. If unused, tie to V_{IN}.

V_{IN} (Pin 7): Input Supply Pin. Bypass this pin with a capacitor to GND as close to the IC as possible.

EN/UVLO (Pin 8): Master Enable and V_{IN} Undervoltage Lockout. When low, the IC is put into shutdown mode and the Q current is reduced to <1µA. This pin utilizes a 1.23V comparator with hysteresis, as well as a hysteresis current source for programming additional hysteresis externally. Drive with a digital signal greater than 1.5V for simple on/off control. Tie to a resistor divider between V_{IN} and GND to set an external UVLO threshold.

OVLO (Pin 9): Overvoltage Lock Out Comparator. This pin disables switching and TG in the case of an overvoltage. This pin utilizes a 1.23V comparator with hysteresis. When the voltage at OVLO exceeds the threshold, the switching is disabled until the voltage at OVLO falls 25mV below the threshold. Tie to GND if unused.

$INTV_{CC}$ (Pin 10): Internal Low Dropout Regulator Output. $INTV_{CC}$ is regulated to 3V, and must be bypassed with an external capacitor of at least 2.2µF. $INTV_{CC}$ is the power supply for the internal DMOS gate driver and control circuitry. Users may apply <5mA loads to $INTV_{CC}$. Overloading $INTV_{CC}$ can cause unintentional device shutdown from $INTV_{CC}$ falling below the 2.68V UVLO threshold.

SYNC/SPRD (Pin 11): Frequency Synchronization and Spread Spectrum Enable Pin. Tie low for fixed internal clock, tie to $INTV_{CC}$ for spread spectrum internal clock, or drive with an external clock for frequency synchronization with no spread spectrum. When using an external clock for frequency synchronization, R_T resistor should be chosen to program a switching frequency 20% lower than the SYNC pulse frequency. Synchronization (switch turn-on) occurs 50ns after the rising edge of SYNC.

VC (Pin 13): g_m Amplifier Output for External Loop Compensation. Stabilize the loop with a C or series RC network. This pin is set to a high impedance state during PWM dimming off-time.

RT (Pin 14): Switching Frequency Adjustment Pin. Set switching frequency using a resistor to GND (see Typical Performance Characteristics for values). For SYNC function, set the frequency 20% slower than the SYNC pulse frequency. Do not leave this pin open. PCB layout must have this component close to the IC.

DIM (Pin 15): PWM Generator Control Voltage. This pin outputs a fixed 20µA current, and controls a triangle wave generator on the PWM pin to determine the PWM duty cycle. 0.2V to 1.2V range on DIM adjusts PWM duty from 0% to 100%. Float this pin or tie to $INTV_{CC}$ if unused, tie a resistor from DIM to GND to set a fixed voltage, or apply an external voltage to DIM for adjustable PWM duty cycle.

FB (Pin 16): Output Voltage Loop Feedback Pin. Connect to a resistor divider from V_{OUT}. In constant-voltage applications, FB sets the output voltage. In constant-current applications, the FB divider is set higher than the expected output voltage to act as open-LED protection. As the voltage at FB rises to within 45mV of the regulation point, the $\overline{\text{OPENLED}}$ flag is asserted if the output current also falls below one-tenth the full-scale value. If the FB voltage exceeds the regulation point by 30mV, the switching is terminated and the TG pin pulls high in order to disconnect the LED load.

PIN FUNCTIONS

CTRL (Pin 17): Output Current Sense Adjust Pin. Sets voltage regulation threshold across ISP/ISN current sense resistor. 0.2V to 1.2V range on CTRL adjusts ISP/ISN threshold from 0mV to 250mV. Tie to V_{REF} or $INTV_{CC}$ for fixed 250mV threshold. Below 100mV, the CTRL pin acts as an auxiliary PWM input for combination PWM/analog dimming on a single pin.

V_{REF} (Pin 18): Reference Voltage Output. This pin outputs a fixed 2V reference, and supplies up to 100µA for use in generating a reference voltage for the CTRL pin. When using a resistor divider, bypass this pin with 100nF to GND.

SS (Pin 19): Soft-Start and Hiccup Control Pin. This pin modulates oscillator frequency and VC voltage clamp when it is below 1.7V. A capacitor on the pin sets the soft-start interval as well as hiccup retry timing in fault mode. The SS pin has a 25µA pull-up current in normal mode, a 2.5µA pull-down current in hiccup mode, and a 120Ω pull-down resistance in start-up mode. Optional latchoff mode is set with a 750k pull-up resistor from $INTV_{CC}$ to SS.

PWM (Pin 20): On/Off Control. Used for TG on/off control and PWM dimming of the LED. Logic low idles regulator to a lower Q current, makes the TG pin drive to I_{SP} level, and makes the VC pin high impedance. Logic high turns on error amplifier, enables switching and TG. The PWM threshold is 1.2V. Tie to V_{REF} or $INTV_{CC}$ for continuous operation. The PWM pin also supplies ±10µA switched current sources to generate a triangle wave on external capacitor for the PWM dimming generator. It is safe to overdrive these currents with an external signal.

$\overline{\text{SHORTLED}}$ (Pin 21): Open-Drain Short-Circuit Indicator. $\overline{\text{SHORTLED}}$ pulls low in the case of an LED overcurrent fault, and releases during the start-up phase of the next soft-start cycle. The state of $\overline{\text{SHORTLED}}$ is only updated when the PWM pin is high. Tie this pin to desired logic high voltage with an external resistor. The maximum recommended sink current is 2mA to limit excess power dissipation. Leave the pin open if unused.

$\overline{\text{OPENLED}}$ (Pin 22): Open-Drain Open-LED Indicator. $\overline{\text{OPENLED}}$ pulls low when the voltage at the FB pin is within 45mV of the regulation point and the LED current has dropped to 10% of the full-scale output. $\overline{\text{OPENLED}}$ releases when the FB voltage falls below the threshold. The state of $\overline{\text{OPENLED}}$ is only updated when the PWM pin is high. Tie this pin to desired logic high voltage with an external resistor. The maximum recommended sink current is 2mA to limit excess power dissipation. Leave the pin open if unused.

IVINCOMP (Pin 23): Auxiliary Current Sense Amplifier Monitor Output. The voltage at IVINCOMP is a 20× amplified and buffered version of the IVINP-IVINN differential voltage, and the VC voltage will be reduced when IVINCOMP reaches its 1.2V threshold. A 1µF capacitor to GND is suggested to filter inductor ripple and compensate the input current loop. During PWM dimming, the IVINCOMP pin stores the input current regulation loop value on the capacitor during the PWM off time. Do not load this pin. If the input current regulation loop is not used, this pin may be connected to GND.

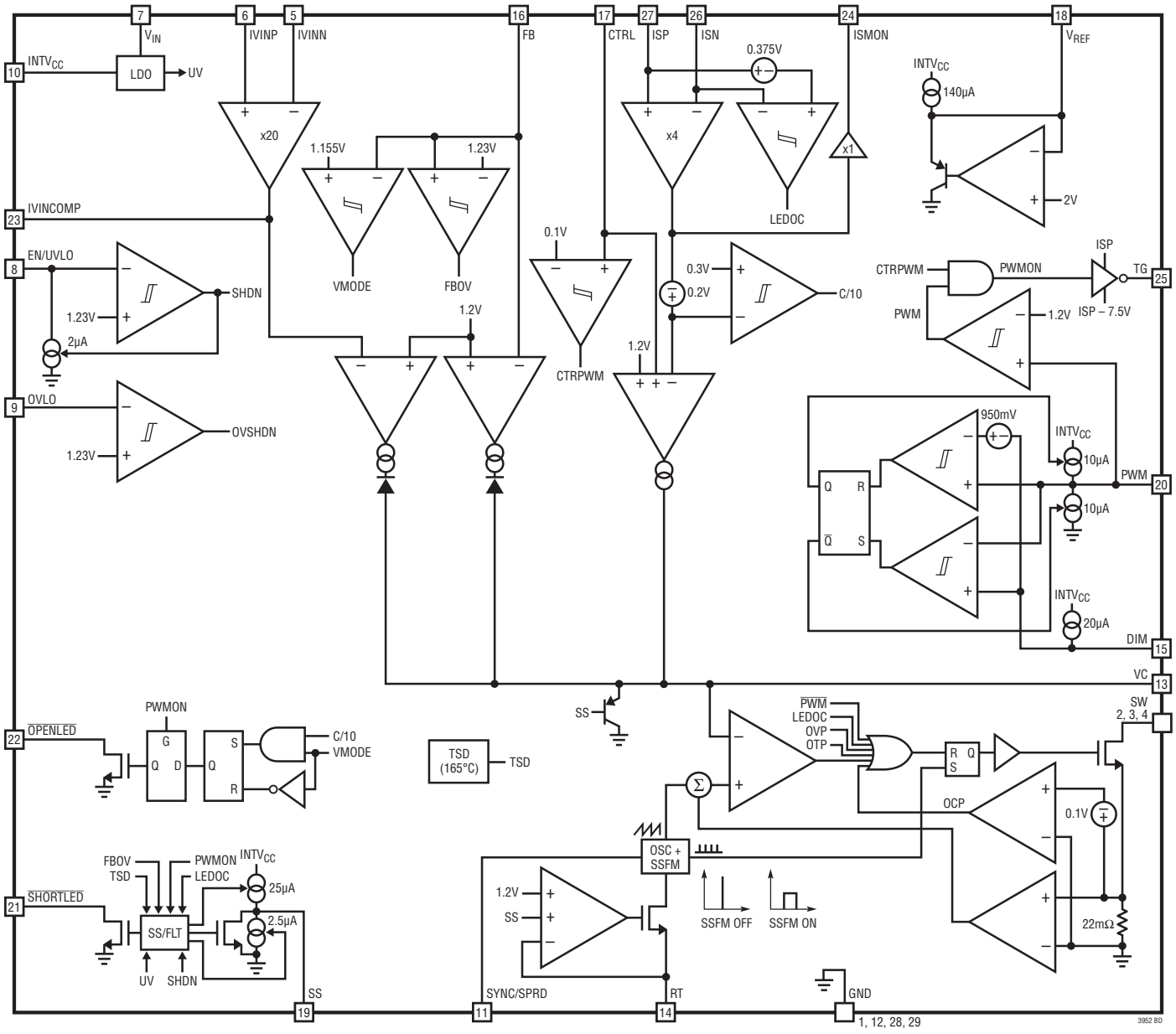
ISMON (Pin 24): Output Current Monitor Pin. The voltage at ISMON is a 4× amplified and buffered version of the ISP, ISN differential voltage. During PWM dimming, the ISMON voltage continues to reflect the instantaneous output current, falling during the PWM low time.

TG (Pin 25): Top Gate Driver Output. An inverted and level-shifted version of the PWM input signal. Drives the gate of an external PMOS transistor between V_{ISP} and V_{ISP} – 7.5V to provide load-side on/off control, PWM dimming, and fault mode disconnect. Leave TG unconnected if not used.

ISN (Pin 26): Output Current Sense Amplifier Negative Input. Connect this pin to the load side of the output current sense resistor. If unused, tie to output voltage.

ISP (Pin 27): Output Current Sense Amplifier Positive Input. Also serves as the positive rail for the TG driver. Limit impedance in series with this pin.If unused, tie to output voltage.

BLOCK DIAGRAM



OPERATION

The LT3952 is a fixed-frequency, current mode boost converter with a feature set ideal for driving high power LED lamps. It provides input and output current regulation, as well as output voltage regulation and fault handling. The operation of the LT3952 is best understood by referring to the Block Diagram. In normal operation, with the PWM pin low, the switching is disabled, the TG pin is pulled high to ISP to turn off the PMOS disconnect switch, the VC pin is high impedance to store the previous switching state on the external compensation capacitor, and the ISP/ISN pin bias currents are reduced to leakage levels.

When the PWM pin transitions high, the TG pin transitions low after a short delay. At the same time, the internal oscillator wakes up and generates a pulse to set the PWM latch, turning on the internal NMOS power switch. The switch current is sensed and added to a stabilizing slope compensation ramp, and the resultant signal is compared to the VC voltage. The inductor current increases linearly during the switch on-time. When the current sense signal exceeds the VC value, the latch is reset and the internal NMOS power switch is turned off. During the switch off-time, energy is transferred from the inductor and the inductor current decreases. At the completion of each oscillator cycle, internal signals such as slope compensation return to their starting points and a new cycle begins with the set pulse from the oscillator.

Through this repetitive action, the IC establishes a switching duty cycle to regulate a current or voltage in the load. The VC signal is integrated over many switching cycles, and is an amplified version of the difference between the LED current sense voltage, measured between ISP and ISN, and the target difference voltage set by the CTRL pin. In this manner, the error amplifier sets the correct peak switch current level to keep the LED current in regulation. If the error amplifier output increases, more current is demanded in the switch; if it decreases, less current is demanded. If the switch current exceeds the internal 4.5A current limit, the latch is reset regardless of the state of the PWM comparator. Likewise, in any fault condition; i.e., FB overvoltage (V_{FB} > 1.23V), LED overcurrent ($V_{ISP-ISN}$ > 375mV), overvoltage lockout or $INTV_{CC}$ undervoltage the switching is immediately disabled.

In addition to the $V_{ISP-ISN}$ to CTRL feedback loop, the LT3952 also provides additional loops to control input current and output voltage. The loops are connected in a wired-OR configuration, where the auxiliary loops are only allowed to reduce the value of VC in the event that one or more exceeds its threshold. This means that even if one or more of the auxiliary loops is below its regulation point, VC will not rise unless the output (LED) current sense is also below its regulation point.

The first auxiliary loop is the output voltage feedback loop using the FB pin. It is typically used to prevent the output voltage from exceeding a safe value. The voltage at the FB pin is compared to an internal reference voltage of 1.2V, and the amplified difference pulls down the VC pin in the case that FB exceeds 1.2V. As VC drops, the switching current reduces and in this manner the output voltage is regulated so that FB = 1.2V.

OPERATION

The second auxiliary loop is the input current limit using the IVINN, IVINP, and IVINCOMP pins. Similar to the output (LED) current loop, the input current is sensed as the differential voltage across a sense resistor. As the average IVINP/IVINN differential voltage exceeds 60mV, IVINCOMP reaches its 1.2V threshold, and VC is reduced in order to limit the input current to the 60mV threshold.

$INTV_{CC}$ Bypass Capacitor

$INTV_{CC}$ is the internal power supply for the IC, and supplies the gate drive to the internal power switch. A bypass capacitor is required from $INTV_{CC}$ to GND for stability and filtering of the switching noise. For best results, use a ceramic capacitor of 2.2µF or greater, and place the capacitor as close to the IC as possible.

V_{REF} Bypass Capacitor

V_{REF} is the 2V reference output and can be bypassed with 100nF to GND. For best results, place the bypass capacitor close to the IC and away from the noisy switching nodes.

Programming the Turn-On/Turn-Off Thresholds with the EN/UVLO Pin

The LT3952 provides an adjustable V_{IN} undervoltage lockout (UVLO) function using the EN/UVLO pin. The EN/UVLO function provides a precision 1.23V falling threshold with 75mV internal hysteresis as well as a 2µA pull-down current in the off state to provide additional, user-programmable hysteresis. This pin can also be driven with a logic level greater than 1.5V or tied to V_{IN} for always-on operation.

In order to program an external UVLO, tie the EN/UVLO pin to a resistor divider between V_{IN} and GND. The divider ratio determines the baseline turn-off/turn-on thresholds and the value of the upper resistor determines the additional hysteresis.

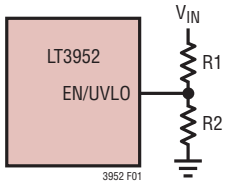


Figure 1

The most important (and precise) threshold is the turn-off threshold from V_{IN} falling. The following equations determine the resistor values:

$$V_{UV(FALLING)} = 1.23 \bullet \left(1 + \frac{R1}{R2}\right)$$

$$V_{UV(RISING)} = 1.305 \bullet \left(1 + \frac{R1}{R2}\right) + 2\mu A \bullet R1$$

For example, a 12V falling UVLO with roughly 10% total hysteresis requires 185k for R1. The closest standard value is 187k, therefore:

R1 = 187k

R2 = 21.5k

$V_{UV(FALLING)}$ = 11.93V

$V_{UV(RISING)}$ = 13.03V

OPERATION

Programming the Overvoltage Disable with the OVLO Pin

It is also possible to program a disable threshold if the input voltage rises too high. The OVLO pin has a 1.23V comparator with 25mV internal hysteresis. If the voltage at OVLO exceeds the 1.23V threshold, the switching is disabled, TG pulls high, and the SS pin pulls low. The device begins a new soft-start sequence when the voltage at OVLO has fallen 25mV below the threshold.

Although it is possible to connect this pin with an independent resistor divider, the component count is minimized by splitting the bottom resistance of the standard EN/UVLO divider to generate an additional tap point.

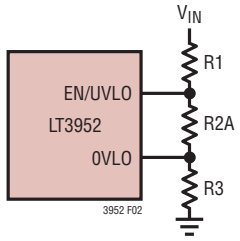


Figure 2

Using the previous values of R1 and R2 from the UVLO section, the new R3 value is computed using the desired rising threshold by:

$$R3 = 1.23 \bullet \left(\frac{R1+R2}{V_{OV(RISING)}} \right)$$

The middle resistor will be designated R2A. To obtain the value for R2A, subtract the calculated value of R3 from the old R2 value.

Continuing the previous equation, the desired value of R3 is 8k for an OVLO threshold of 32V. Subtract this from the previous value of R2 in order to find the value of R2A. In our case, R3 = 8.06k and the closest 1% resistor for the new R2A value is 13.3k. The thresholds are recalculated if desired from the expanded divider ratios:

$$V_{UV(FALLING)} = 1.23 \bullet \left(1 + \frac{R1}{R2A+R3} \right)$$

$$V_{UV(RISING)} = 1.305 \bullet \left(1 + \frac{R1}{R2A+R3} \right) + 2\mu A \bullet R1$$

$$V_{OV(RISING)} = 1.23 \bullet \left(1 + \frac{R1+R2A}{R3} \right)$$

$$V_{OV(FALLING)} = 1.205 \bullet \left(1 + \frac{R1+R2A}{R3} \right)$$

In our example:

R1 = 187k, R2A = 13.3k, R3 = 8.06k

$V_{UV(FALLING)}$ = 11.998V

$V_{UV(RISING)}$ = 13.104V

$V_{OV(RISING)}$ = 31.796V

$V_{OV(FALLING)}$ = 31.151V

OPERATION

LED Current Control and Monitor

The LED current is programmed through the combination of an external sense resistor and a voltage on the CTRL pin. The CTRL voltage adjusts the setpoint of the current sense amplifier on the ISP and ISN pins from 0mV to 250mV, and the external sense resistor defines the output current for a given setpoint. The current sense resistor is typically placed at the top of the LED strand, although the rail-to-rail ISP/ISN inputs allow placement at the bottom of the strand as well.

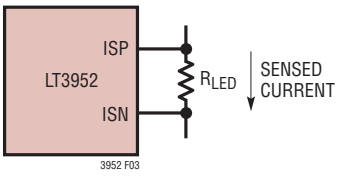


Figure 3

The required sense resistor for a desired output current is computed by:

$$R_{LED} = \frac{V_{ISP-ISN}}{I_{OUT}}$$

In the case of the fixed 250mV setpoint:

$$R_{LED} = \frac{0.25}{I_{OUT}}$$

For example, a 500mA output requires a 0.5Ω sense resistor when using the fixed 250mV setpoint.

In adjustable mode, the working range of CTRL is from 0.2V to 1.2V and adjusts the setpoint of ISP and ISN from 0mV to 250mV. In this manner, analog dimming is achieved.

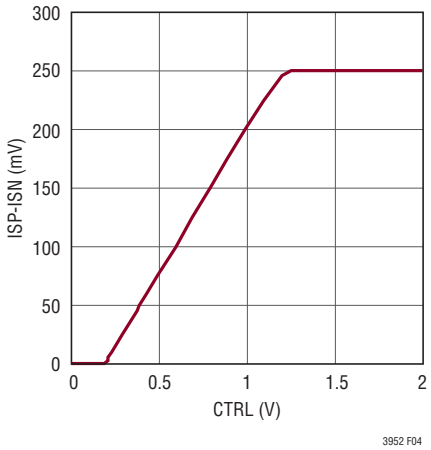


Figure 4

The required CTRL voltage for a desired analog setpoint is computed by:

$$V_{CTRL} = 0.2 + 4 \bullet V_{ISP-ISN}$$

As the CTRL voltage nears 1.2V, a crossover from adjustable threshold to a precision internal 250mV setpoint takes place and some nonlinearity occurs as shown in the ISP-ISN vs CTRL graph in the Typical Performance Characteristics. It is therefore desirable to drive the CTRL pin well above 1.2V when the 250mV setpoint is desired. Tying CTRL to the 2V V_{REF} output is an excellent method of doing so.

LED Current Monitoring

The ISMON pin provides a buffered output representing the differential voltage on ISP-ISN for current monitoring applications. The normal working range of ISMON is from 0V to 1V, and the gain from ISP-ISN to ISMON is 4. This corresponds to a 1V output at ISMON when the ISP-ISN differential voltage has reached the 250mV maximum.

OPERATION

External PWM Dimming

The PWM pin, in combination with an external PMOS transistor driven from the TG pin, allows on/off control and PWM dimming of the LED current.

The PWM pin has a fixed 1.2V threshold, and driving PWM higher than 1.2V enables the device for switching and causes the TG pin to drive to a level roughly 7.5V lower than the voltage at ISP. During the low time of PWM, the TG pin is driven to the voltage at ISP to turn off the external PMOS, and the LT3952 is put into a low power standby state. Switching and the error amplifiers are disabled and the VC pin is three-stated to preserve the value of VC voltage for accelerated start-up upon the next rising edge of PWM.

The CTRL pin also offers a PWM function to allow analog and digital dimming on a single pin. Below 0.1V on CTRL, the device is also put into standby mode with SW, TG, and the error amplifiers disabled. Keep in mind that between 0.2V and 0.1V on CTRL, the device is not disabled, although the output current is commanded to 0. The value of VC reduces towards the minimum, and TG keeps the output PMOS enabled, which discharges the output through the LED lamps. For effective PWM dimming using the CTRL pin, please ensure that the low voltage on CTRL is below 0.1V. This is easily obtained using an external open-drain device to pull down a resistor divider used to generate the CTRL setpoint. Alternately, enabling and disabling a DAC output driving CTRL also gives excellent results.

Internal PWM Generator

The PWM pin can also provide a self-oscillating PWM generator for standalone operation by simply tying a small capacitor from PWM to GND. In this configuration, 10µA pull-up and pull-down current sources generate a triangle waveform on the PWM pin whose peak and valley points are defined by the voltage on the DIM pin and whose frequency is defined by the external capacitor.

$$V_{PWM\text{-}VALLEY} = V_{DIM}$$

$$V_{PWM\text{-}PEAK} = V_{DIM} + 950mV$$

$$f_{PWM} = \frac{5200}{C_{PWM}(\mu F)}$$

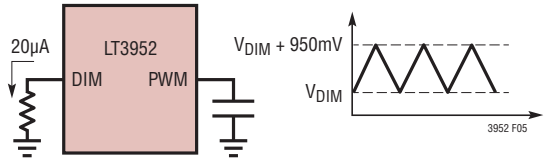


Figure 5

By raising and lowering the voltage on the DIM pin, the triangle wave intersects the 1.2V PWM threshold at different points, changing the PWM duty cycle.

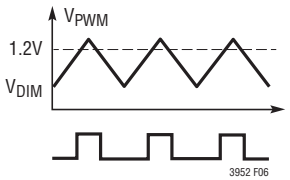


Figure 6. Lower DIM Voltage

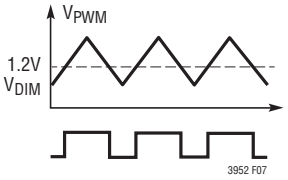


Figure 7. Higher DIM Voltage

OPERATION

As the DIM pin exceeds 1.2V, the PWM duty cycle will be 100%. As the DIM pin exceeds 2.3V, the internal PWM generator is disabled along with the switched 10µA pull-down on PWM. The PWM pin will continue to be pulled to $INTV_{CC}$ with the 10µA pull-up current. For applications utilizing external PWM dimming, it is recommended to disable the internal PWM generator by floating the DIM pin or tying it to $INTV_{CC}$. This will provide the fastest PWM response for high dimming ratios.

Programming the frequency of PWM dimming consists only of selecting the proper capacitor for the PWM pin according to:

$$C\,(nF) = \frac{5200}{f_{PWM}\,(Hz)}$$

A common selection is 39nF for roughly 133Hz.

Programming the PWM duty cycle consists of setting a voltage on the DIM pin according to:

$$V_{DIM(V)} = 0.95 \bullet Duty + 0.25$$

As shown in Figure 5, a single resistor in combination with the 20µA output current of DIM can be used to program the duty cycle.

$$R_{DIM(k\Omega)} = 47.5 \bullet Duty + 12.5$$

For adjustable duty cycle control, an external voltage can be applied at the DIM pin using a DAC or external supply.

To slowly increase the light output upon start-up or restart, a capacitor can also be used with the DIM circuit. To fade from dark to full brightness, only a capacitor is required. To fade from dark to a fixed duty cycle, place a capacitor in parallel with the DIM resistor.

Upon start-up or fault retry, an internal pull-down with 2k series resistance is applied to the DIM pin to discharge any external capacitor before the start-up sequence begins. Be aware that this will temporarily load an external voltage applied to DIM.

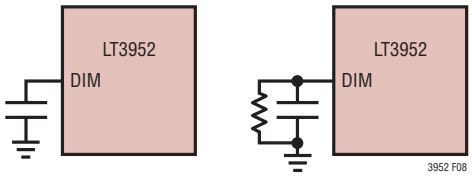


Figure 8. Fade on to Full Brightness, or to Preset Duty

OPERATION

Input Current Limit

The LT3952 provides adjustable input current limiting through the IVINP/IVINN/IVINCOMP amplifier. Connect the IVINP and IVINN sensing terminals across a resistor in series with the input. A 20x amplified version of the IVINP–IVINN differential is generated at IVINCOMP. A capacitor at IVINCOMP provides filtering and averaging of the input ripple.

As the average IVINP–IVINN differential reaches 60mV, the IVINCOMP voltage will reach its 1.2V regulation threshold and the cycle-by-cycle switch current will be reduced. In this manner, the input current is regulated to 60mV differential between IVINP and IVINN.

$$R_{SENSE}\ (m\Omega) = \frac{60mV}{I_{IN(LIM)}(A)}$$

For example, a 2.4A input current limit is programmed with a 25mΩ sense resistor.

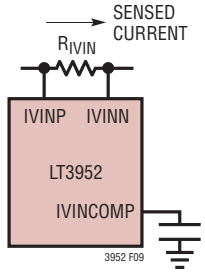


Figure 9

In some cases, such as deep discontinuous conduction, a large input ripple current may cause the input current limit to activate early, cutting into the typical regulation profile. In this situation, it is possible to filter the ripple down to a smoother level using an external RC network.

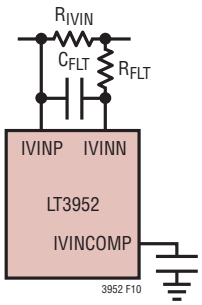


Figure 10

Be aware that input current on start-up and PWM dimming is larger than steady state due to the output current required to fill the output capacitor. It is recommended to set the input limit appropriately to prevent interruption of the regulated output.

Input Current Monitor

An input current monitor is available as the voltage on IVINCOMP, which reflects a voltage equal to 20× the IVINP-IVINN differential voltage and has a working range of 0V to 1.2V as the IVINP-IVINN voltage varies from 0mV to 60mV.

IVINCOMP is a high impedance output and should not be loaded. Averaging of current sense ripple, and compensation of the feedback loop is achieved using a 1µF capacitor from IVINCOMP to GND.

Output Voltage Regulation/Limiting

The LT3952 provides a voltage-feedback error amplifier through the FB pin to provide output voltage regulation and limiting for open-LED protection.

In the case of an open-LED strand, the current commanded by CTRL is never achieved and the device continues to drive the output voltage higher. If left unchecked, this could result in overvoltage damage to the external components and the power switch itself, and therefore an output voltage limit is required.

By connecting FB to a resistor divider between V_{OUT} and GND, the maximum output voltage regulates at the 1.2V threshold of the FB pin. The maximum output voltage is computed as follows:

$$V_{OUT}\ (V) = 1.2 \bullet \left(1 + \frac{R4}{R5}\right)$$

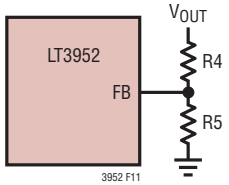


Figure 11

OPERATION

A simple method to determine the proper resistor values is to choose a value of R5 that draws a tolerable amount of current at the 1.2V regulation point, and to compute R4 by using:

$$R4 = \left(V_{OUT} - 1.2\right) \bullet \frac{R5}{1.2}$$

For example, R5 = 24k draws 50µA at the regulation point, and for a 24V output limit, the desired value of R4 is 456k. The closest standard value to this is 453k, providing 23.85V output voltage limit.

It is necessary to set the regulation point slightly higher than the worst-case voltage drop of the LEDs to avoid cut-in of the voltage limit during normal regulation.

Open LED Flag and Overvoltage Protection

The LT3952 provides an indicator of the open-LED condition on the $\overline{\text{OPENLED}}$ pin, as well as an internal overvoltage detection to prevent output overshoot if the LED strand goes open under load. Both of these features are based on the voltage at the FB pin.

The $\overline{\text{OPENLED}}$ pin consists of an open-drain NMOS pull down to be connected with an external pull-up resistor to the user's desired voltage. This pin tolerates up to 42V, and has a pull-down strength of 60Ω. Please be aware of power dissipation and keep the $\overline{\text{OPENLED}}$ current to a few mA maximum.

The $\overline{\text{OPENLED}}$ pin pulls low when the following two conditions are met:

1. The voltage at FB rises to within 45mV of the 1.2V regulation point.
2. The output current is detected to be less than one-tenth of the value commanded by CTRL.

The $\overline{\text{OPENLED}}$ pin releases when the voltage at FB falls to 65mV below the 1.2V regulation point. This sequence prevents false $\overline{\text{OPENLED}}$ flags from momentary overshoot.

An overvoltage condition is detected by the voltage at FB rising to 30mV above the 1.2V regulation point. Upon detection of an overvoltage condition, the switching is disabled and TG is pulled high to disconnect and protect the load. Switching is re-enabled when the FB voltage falls by 15mV. An overvoltage condition does not affect the state of the $\overline{\text{OPENLED}}$ pin.

Switching Frequency

The switching frequency is programmed with a resistor from the RT pin to GND. The RT pin is regulated to 1.2V, and the output current of R_T adjusts the oscillator frequency.

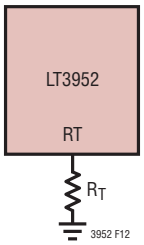


Figure 12

OPERATION

The overall switching period is defined by the sum of two parts: a fixed 50ns off-time that defines D_{MAX}, and a variable time defined by the RT current. To determine the proper R_T value for a desired switching frequency, using the following equation:

$$R_T\ (k\Omega) = \frac{88.9}{f_{SW}\ (MHz)^{1.13}}$$

For example, a 2MHz switching frequency results in a desired R_T resistance of 40.6k, which has 40.2k as the closest standard value.

Table 1 provides some commonly used values.

Table 1. Switching Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
3.0	25.5
2.0	40.2
1.0	90.9
0.4	243
0.215	470

Frequency Synchronization and Spread Spectrum

The LT3952 SYNC pin acts as both an external clock input for frequency synchronization and the enable signal for internal spread spectrum feature. Tie the SYNC/SPRD pin low for fixed-frequency internal clock, tie to $INTV_{CC}$ for spread-spectrum internal clock, or drive with an external clock for frequency synchronization with no internal spread spectrum.

When synchronizing to an external clock, the R_T resistor should be chosen to program a switching frequency 20% lower than the external clock frequency. Even when synchronizing, a soft-start cycle will first start the oscillator in frequency foldback to minimize inrush current. As the soft-start cycle nears completion, the device will then transition to the external frequency.

When the SYNC/SPRD pin is tied high for greater than 32 clock cycles, the device will enable spread-spectrum clocking for EMI reduction. By continuously varying the oscillator frequency, spread spectrum distributes the EMI power generated during the switching cycle over a group of frequencies rather than concentrating it at a single frequency. Therefore, the measured EMI power at any single frequency is reduced compared to that of fixed-frequency operation.

In spread-spectrum mode, the oscillator frequency is varied in a pseudorandom manner from the nominal frequency to 31% above nominal in 1% steps. This unidirectional adjustment allows LT3952 to avoid a sensitive band in the system simply by programming the nominal frequency slightly above it. The proportional step size allows the user to easily determine R_T value for their specified EMI test bin size, and the pseudorandom method provides tone suppression from the frequency variation itself.

OPERATION

The pseudorandom value is updated proportionally to the oscillator frequency, using a rate of $f_{SW}/32$. This rate allows multiple passes of the entire group of frequencies during standard EMI test dwell times.

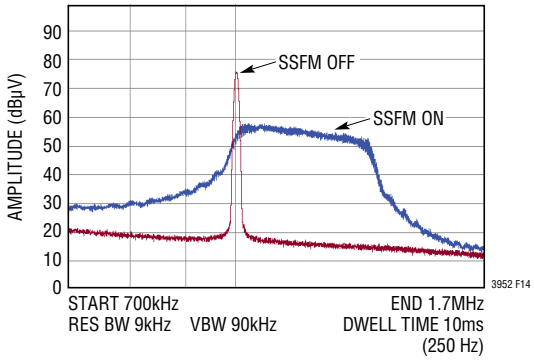


Figure 13. Average Conducted EMI – 1MHz

Inductor Selection

Inductor selection consists of two parameters: saturation current rating and inductance value. A higher switching frequency allows the use of a smaller inductance value at the expense of increased switching loss.

The saturation current rating of the inductor is selected appropriately for the 4A current limit of the device.

An approximation for maximum inductor current (efficiency = 100%) is based on the maximum LED current and the input/output ratio:

$$I_{L(MAX)}(A) = \left(\frac{V_{LED(MAX)}}{V_{IN(MIN)}}\right) \bullet I_{LED}$$

The maximum steady-state inductor current, $I_{L(MAX)}$, should be less than 3A to allow for current ripple and transient response. The desired inductance is determined based on the steady-state current ripple. A typical rule of thumb is to set the inductor current ripple to a maximum of 25% of the switch current limit.

Boost:

$$L_{BOOST} \geq \frac{V_{IN(MIN)}\left(V_{LED(MAX)} - V_{IN(MIN)}\right)}{V_{LED(MAX)} \bullet 1A \bullet f_{SW}}$$

Buck:

$$L_{BUCK} \geq \frac{V_{LED(MAX)}\left(V_{IN(MIN)} - V_{LED(MAX)}\right)}{V_{IN(MIN)} \bullet 1A \bullet f_{SW}}$$

Buck-Boost:

$$L_{BB} \geq \frac{\left(\frac{V_{IN(MIN)} \bullet V_{LED(MAX)}}{V_{LED(MAX)} + V_{IN(MIN)}}\right)}{f_{SW} \bullet 1A}$$

Table 2 provides some recommended inductor vendors.

Table 2. Inductor Manufacturers

VENDOR	WEB
Wurth Elektronik	www.we-online.com
Coilcraft	www.coilcraft.com
Cooper	www.cooperet.com

OPERATION

Output Capacitor Selection

In the case of driving LEDs, their exponential current/voltage characteristic dictates that output voltage ripple translates almost directly to LED current ripple. Although the effect is not visible to the eye, large LED current ripple may affect the output current accuracy and color spectrum and it is therefore advisable to keep the output voltage ripple below a few percent.

For the boost and buck-boost topologies, output current is delivered in pulses and the filtering requirement is higher than for the buck topology with its continuous output current. Assuming a low ESR ceramic capacitor and 25% inductor current ripple, use the following equations to compute the required output capacitance for a desired output ripple voltage, ΔV_{LED}.

Boost, Buck-Boost:

$$C_{OUT} = \frac{I_{LED} \bullet (V_{LED} - V_{IN})}{V_{LED} \bullet \Delta V_{LED} \bullet f_{SW}}$$

Buck:

$$C_{OUT} = \frac{0.3 \bullet I_{LED}}{8 \bullet \Delta V_{LED} \bullet f_{SW}}$$

Input Capacitor Selection

The input capacitor is also selected based on desired voltage ripple. Complementary to output capacitor selection, the discontinuous input current of the buck topology requires more filtering than the continuous input current of the boost or buck-boost. Use the following equations to determine the input capacitance required for a desired input ripple voltage, ΔV_{IN}.

Boost, Buck-Boost:

$$C_{IN} = \frac{0.3 \bullet I_{LED} \bullet \frac{V_{LED}}{V_{IN}}}{8 \bullet \Delta V_{IN} \bullet f_{SW}}$$

Buck:

$$C_{IN} = \frac{V_{IN} \bullet I_{LED} \bullet (V_{IN} - V_{LED})}{\Delta V_{IN} \bullet V_{IN}^2 \bullet f_{SW}}$$

Schottky Rectifier Selection

The power Schottky diode conducts the switching current during the switch off-time. Select a diode rated for at least $1.5 \bullet I_{LED}$ to account for current variation from efficiency and inductor ripple. The reverse-breakdown voltage should be at least 20% greater than the maximum reverse voltage expected in circuit.

Loop Compensation

The LT3952 uses an internal transconductance error amplifier whose VC output compensates the control loop. The external inductor, output capacitor and the compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor at VC are selected to optimize control loop response and stability. For typical LED applications, a 6.8nF to 10nF compensation capacitor at VC is adequate, and a series resistor increases the slew rate on the VC pin to maintain tighter regulation of LED current during fast transients on the input supply of the converter.

External PMOS Disconnect/PWM Switch

A high side PMOS disconnect switch with a minimum V_{TH} of –2V is recommended in most LT3952 applications. This switch is enabled and disabled during PWM dimming, and disconnects the output in shutdown and during fault conditions. Select a PMOS transistor with a V_{DS} rating greater than the open-LED regulation voltage set by FB, and with a continuous current rating greater than I_{LED}.

Soft-Start

The LT3952 incorporates flexible soft-start and the option of hiccup or latchoff mode for customizing fault response. The SS pin provides a 25µA pull-up current for charging, a 2.5µA pull-down current for discharging, and a 120Ω NMOS pull-down switch for clearing an external soft-start capacitor. The state of each of these components is determined by the soft-start/fault sequence, and will be described herein.

Shutdown Mode: During shutdown mode, all SS currents and the pull-down switch are disabled, effectively

OPERATION

three-stating the SS pin. This is to avoid sinking quiescent current in the case that an external resistor pull-up is connected to SS.

When the device leaves shutdown mode, the NMOS pull-down switch is activated to clear the voltage at the soft-start capacitor. The device waits in this state until the voltage at SS drops below 0.2V, and until start-up is enabled as defined by PWM > 1.2V and CTRL > 100mV. If both enable signals are already valid upon leaving shutdown mode, the NMOS pull-down is activated for 10µs longer than is required to pull the SS voltage below 0.2V. In all cases, this action provides a start-up profile where the initial voltage at SS can be considered approximately 0V.

In the event that the device is shut down by EN/UVLO or the $INTV_{CC}$ voltage dropping below 2.68V, the SS pin initially goes high impedance and then restarts the clear, charge sequence as described.

Start-Up Mode: Once start-up is enabled by PWM and CTRL both valid, the NMOS pull-down switch is disabled and the 25µA charging current is enabled. The voltage at SS begins ramping in a linear manner until it reaches 0.2V, at which point switching and the TG driver are enabled. From 0.2V to 1.7V on SS, the frequency and the current limit are increased linearly with SS voltage to provide a smooth start-up profile with low inrush current. The required soft-start capacitor for a desired start-up time is computed from the 1.5V range of SS and the 25µA charge current.

$$C_{SS}\ (nF) = 16.67 \bullet t_{SS}\ (ms)$$

For example, a soft-start time of roughly 0.5ms is generated with an 8.2nF capacitor.

Depending on output and load conditions the device may enter regulation before SS reaches 1.7V, however it is the combination of the 1.7V threshold and the sensing of at least one-tenth of the output current defined by CTRL that signifies the successful completion of soft-start. This becomes important when start-up is enabled by a low duty cycle PWM signal. The explanation is as follows:

A low duty cycle PWM signal could cause excessive start-up times if it were allowed to interrupt the soft-start sequence. Therefore, once start-up is initiated by PWM > 1.2V and CTRL > 150mV, it temporarily ignores a logical disable by either of those signals. The device continues to soft-start with switching and TG enabled until either the voltage at SS reaches the 1.7V level, or the output current reaches one-tenth of the full-scale value. At this point the device begins following the dimming control as designated by PWM or CTRL. If at any time an output overcurrent is detected, SW and TG will be disabled even as SS continues to charge. This will be discussed in further detail in the Fault Handling section.

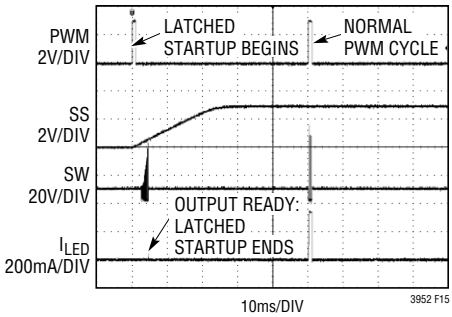


Figure 14. PWM Latched Startup

One note is when PWM dimming using CTRL, the output current is commanded to zero during the low time of CTRL even as the soft-start voltage rises.

Fault Handling: Although the fault handling sequence may change based on the soft-start conditions, the switching is disabled and the TG driver immediately pulls high upon detection of an output overcurrent fault. This provides safe output disconnect even in the case of a dead short on the output.

When an overcurrent is detected and TG and SW are disabled, SS is still required to charge to the 1.7V upper threshold before it begins discharging back down using the 2.5µA current source. If SS is already at or above 1.7V, it begins discharging immediately upon the disable of TG and SW. If SS is still in the start-up phase when an output overcurrent fault is detected, then SS continues charging even as TG and SW are disabled. It charges to the 1.7V level before reversing direction and discharging to the 0.2V level with the 2.5µA current source. This provides additional delay to allow the system to recover from the overcurrent condition.

OPERATION

Once SS has discharged to the 0.2V level, the sequence of clearing SS with the 120Ω NMOS pull-down and restarting the 25µA charge phase reoccurs as previously described. Switching and TG are not re-enabled until SS again climbs to the 0.2V threshold. If at this point an overcurrent is still detected, then SW and TG are again disabled as SS continues to climb to the 1.7V threshold before reversing direction. In this manner, a hiccup retry cycle is obtained with a maximum switching duty cycle of 10%, the ratio of 25µA pull-up to 2.5µA pull-down currents. This low hiccup duty cycle reduces input power during sustained overload conditions.

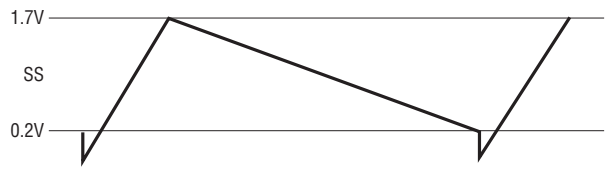


Figure 15. SS in Sustained Hiccup Mode

If a latched-off response is desired, a user simply sets a pull-up resistor from $INTV_{CC}$ to SS with a value low enough to prevent SS from discharging to the 0.2V level. For the low pull-down current of 2.5µA, even a relatively large value of 750k to $INTV_{CC}$ prevents SS from reaching the automatic retry threshold and effectively provides a fault latchoff. At this point, a manual retry is obtained by entering and exiting shutdown mode, upon which the 120Ω NMOS pull-down clears the SS voltage in preparation for retry.

$\overline{\text{SHORTLED}}$ Flag: The LT3952 provides an open-drain $\overline{\text{SHORTLED}}$ pin to flag the overcurrent detection. This pin is connected with a pull-up resistor to the user's voltage (up to 42V), and has a pull-down strength of 60Ω. Please be aware of power dissipation and keep the pull-up current to a few mA maximum.

The $\overline{\text{SHORTLED}}$ pull-down activates immediately upon detection of a fault and stays on throughout the charge/discharge phase of the hiccup cycle. The pull-down releases as the SS capacitor is cleared to 0V during the restart phase and stays released as SS re-charges to the 0.2V retry threshold. If at this point a fault is again detected, the pin is again pulled down as the hiccup retry cycle continues. For the user detecting fault with an IRQ, this falling edge is used to count a desired number of faults before full system shutdown, or the rising edge is used to prepare the system for a new start-up cycle.

Board Layout

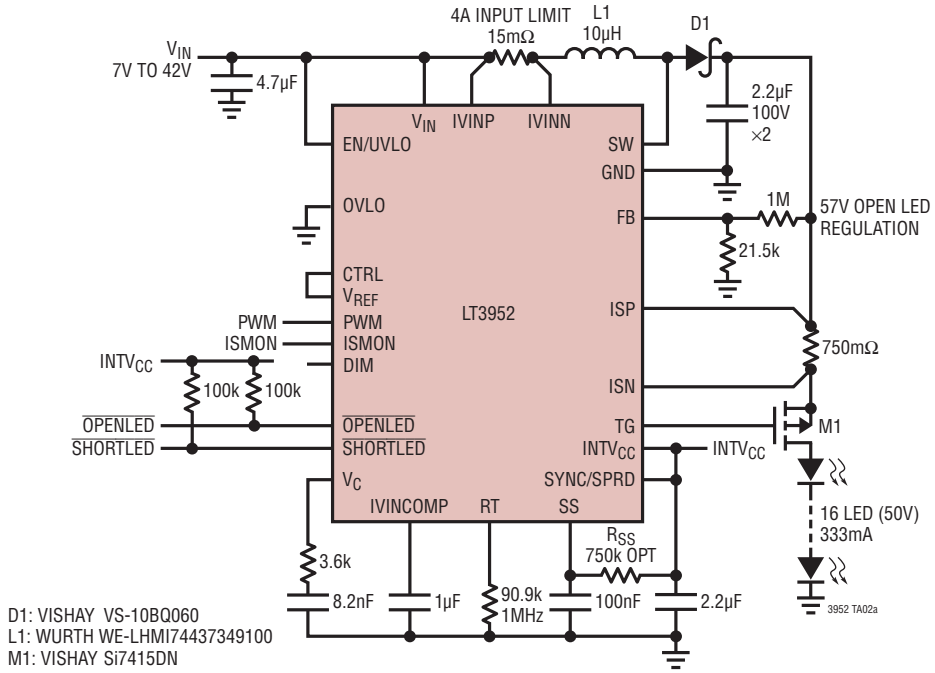
The high speed operation of the LT3952 demands careful attention to board layout and component placement. The exposed pad of the package is the GND terminal of the IC and is also important for thermal management of the IC. It is crucial to achieve a good electrical and thermal contact between the exposed pad and the ground place of the board. To reduce electromagnetic interference (EMI), it is important to minimize the area of the high dV/dt switching node between the inductor, SW pins, and anode of the Schottky rectifier.

Use a ground plane under the switching node to eliminate interplane coupling to sensitive signals. The length of the high dI/dt trace from the SW pin through the Schottky rectifier and filter capacitor to GND should be minimized, and the IC GND pins should be connected to the large copper area beneath the IC. The GND terminal of the $INTV_{CC}$ capacitor should be placed near the GND of the switching path. The ground for the V_{REF} capacitor, the IVINCOMP capacitor, the compensation network, and other DC control signals should be star connected to the underside of the IC. Do not route high impedance signals such as FB, DIM, IVINN, RT and VC near the switching nodes, and minimize the length of their routes to avoid picking up switching noise.

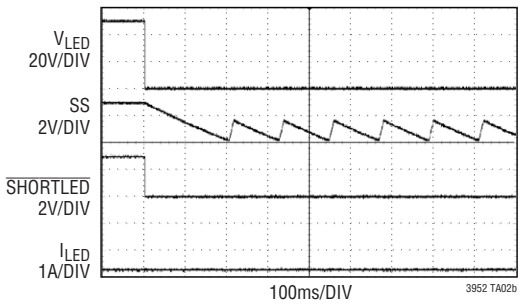
Since there is a small, but variable, DC bias current on the ISP/ISN/IVINP/IVINN inputs, minimize resistance in series with these pins to avoid creating an offset. Kelvin connecting these lines to the terminals of their respective sense resistors provides best performance.

TYPICAL APPLICATIONS

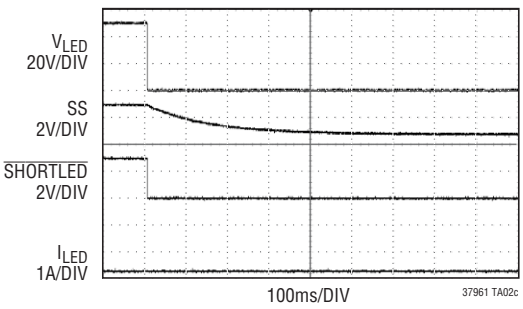
Short-Circuit Robust Boost LED Driver with Spread Spectrum Frequency Modulation



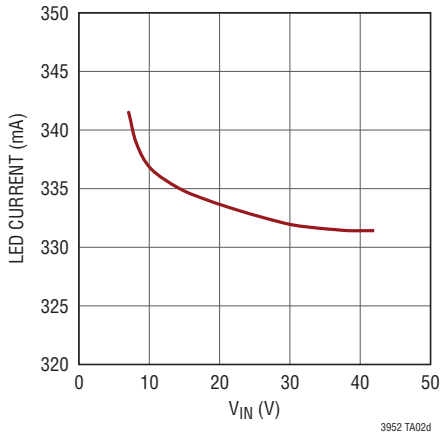
Short LED Protection without R_{SS}: Hiccup Mode



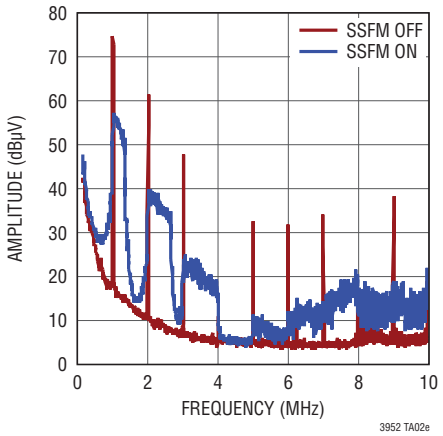
Short LED Protection with R_{SS}: Latchoff Mode



LED Current vs Input Voltage

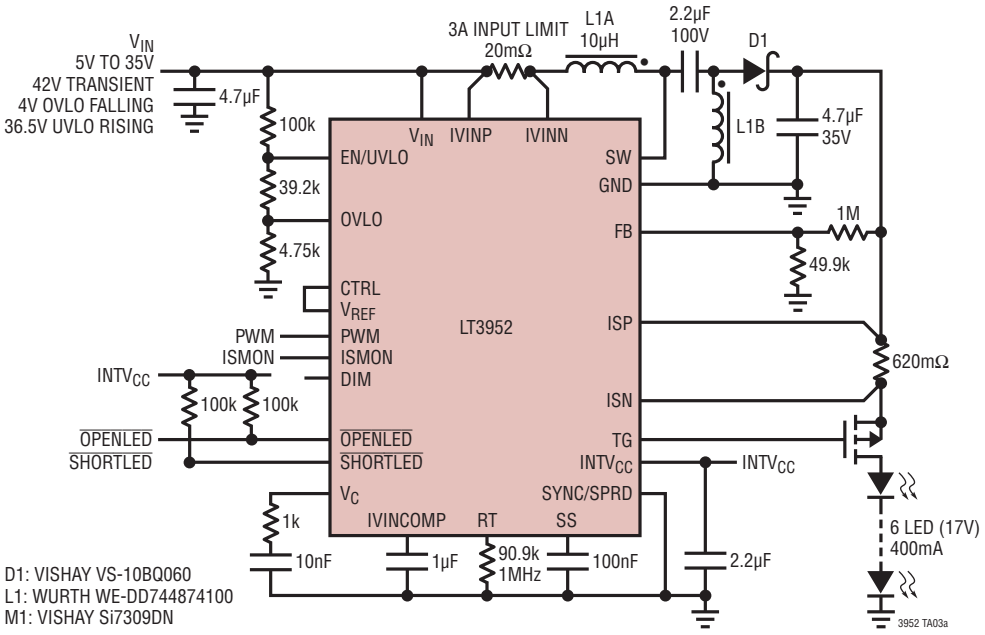


Average Conducted EMI Comparison

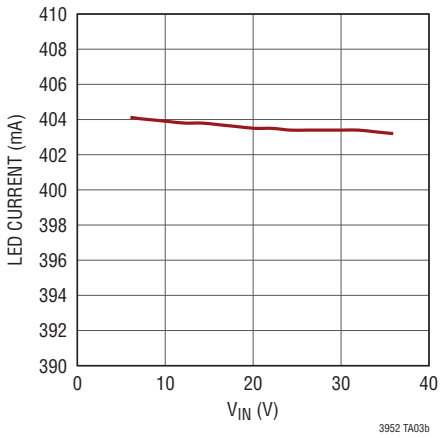


TYPICAL APPLICATIONS

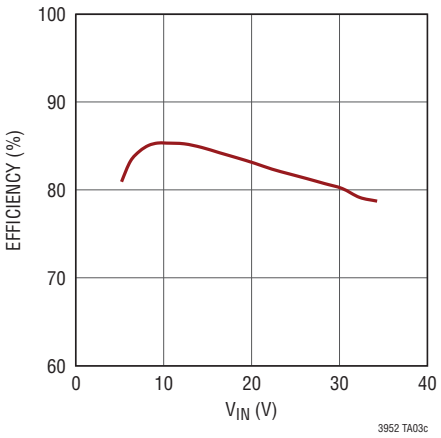
SEPIC LED Driver with Input Current Limit



LED Current vs Input Voltage

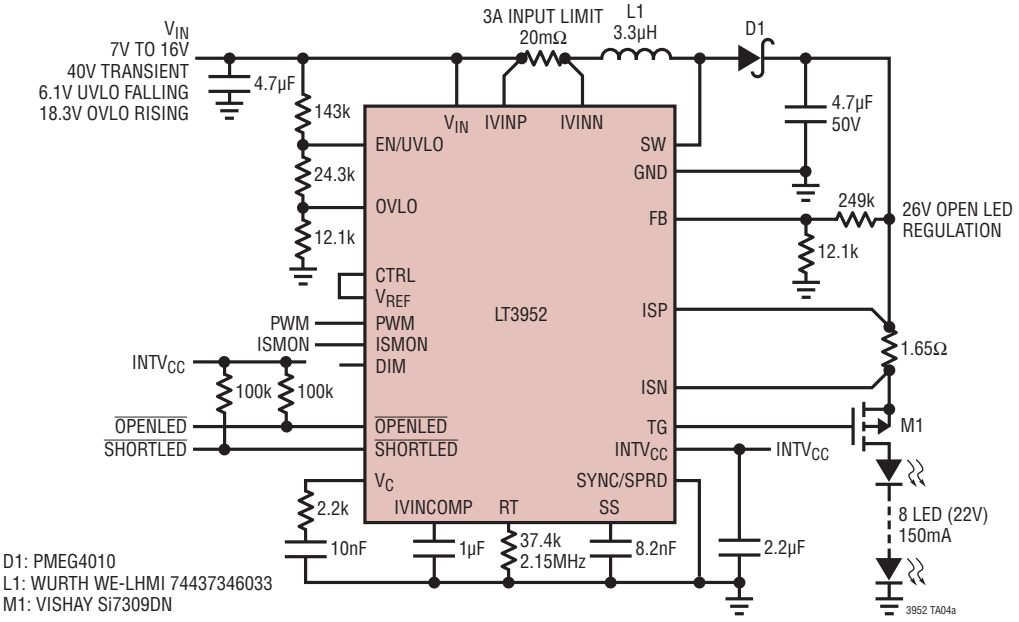


SEPIC Efficiency vs Input Voltage

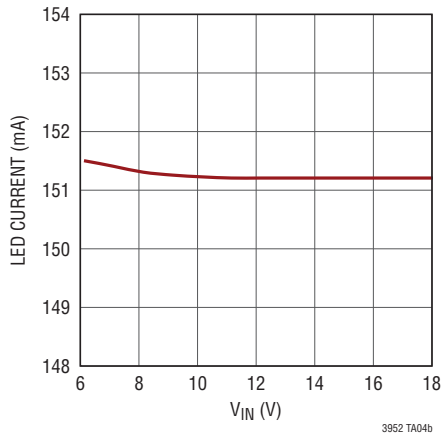


TYPICAL APPLICATIONS

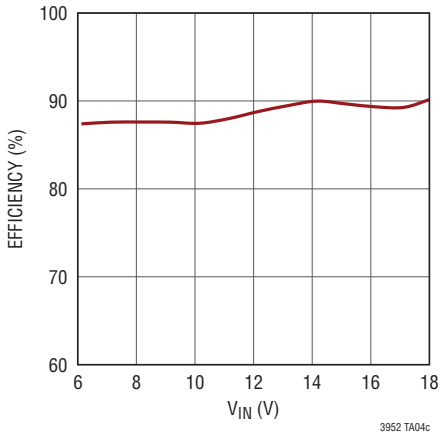
2MHz Boost LED Driver with 4000:1 PWM Dimming and Overvoltage Protection



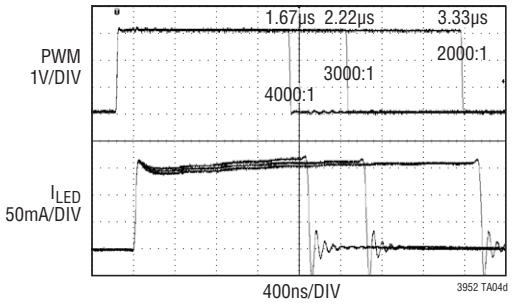
LED Current vs Input Voltage



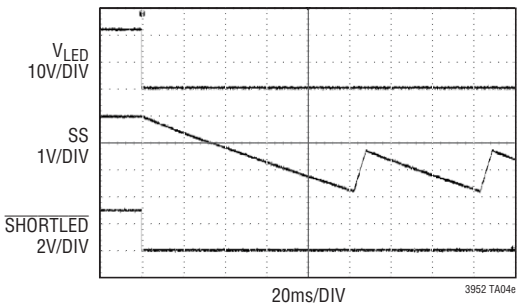
Efficiency Over Working Range



High PWM Dimming Ratio

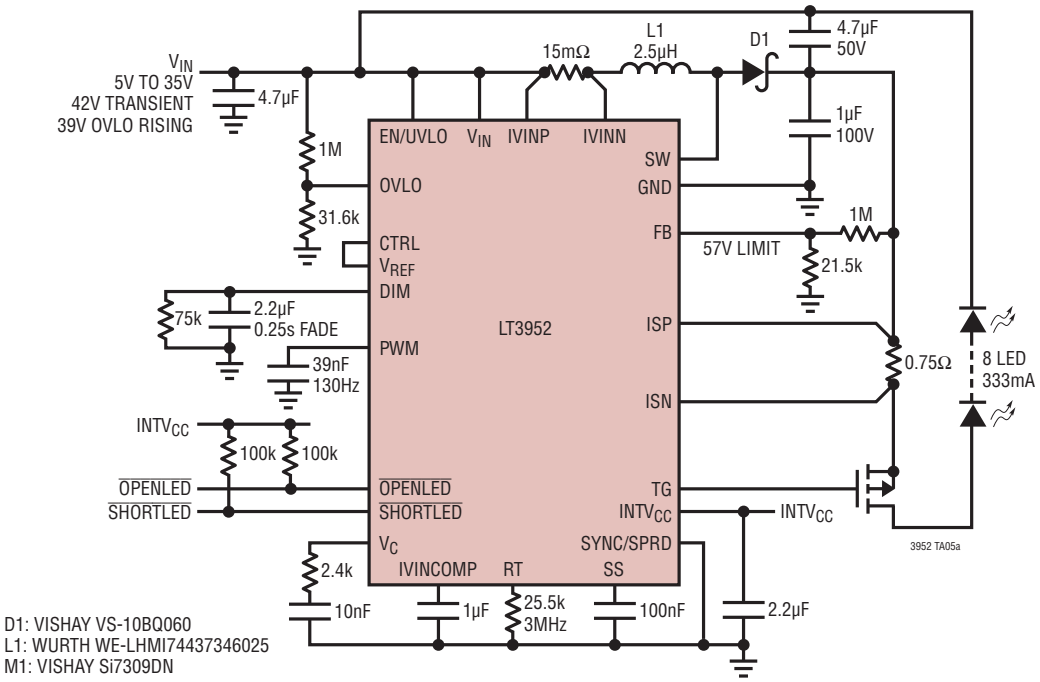


LED Dead Short Response

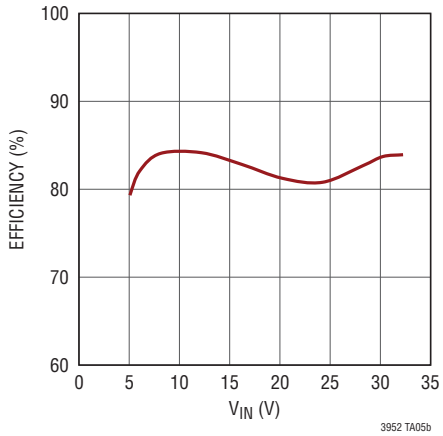


TYPICAL APPLICATIONS

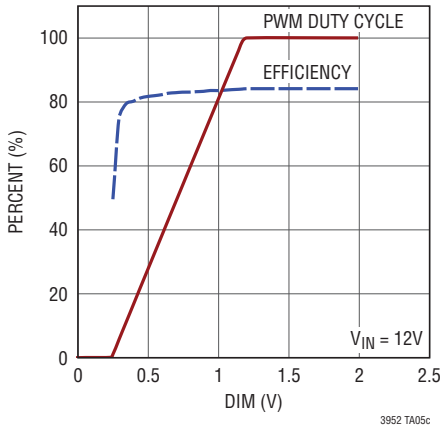
3MHz Buck-Boost LED Driver with Internal PWM Dimming and Fade Start



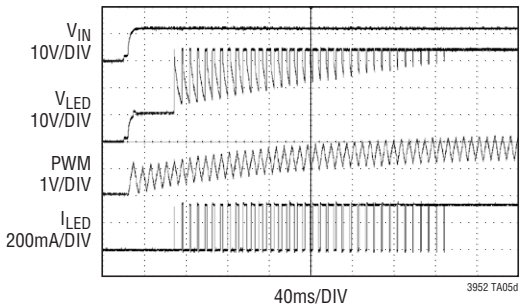
Efficiency vs Input Voltage



PWM Duty Cycle and Efficiency vs DIM Voltage



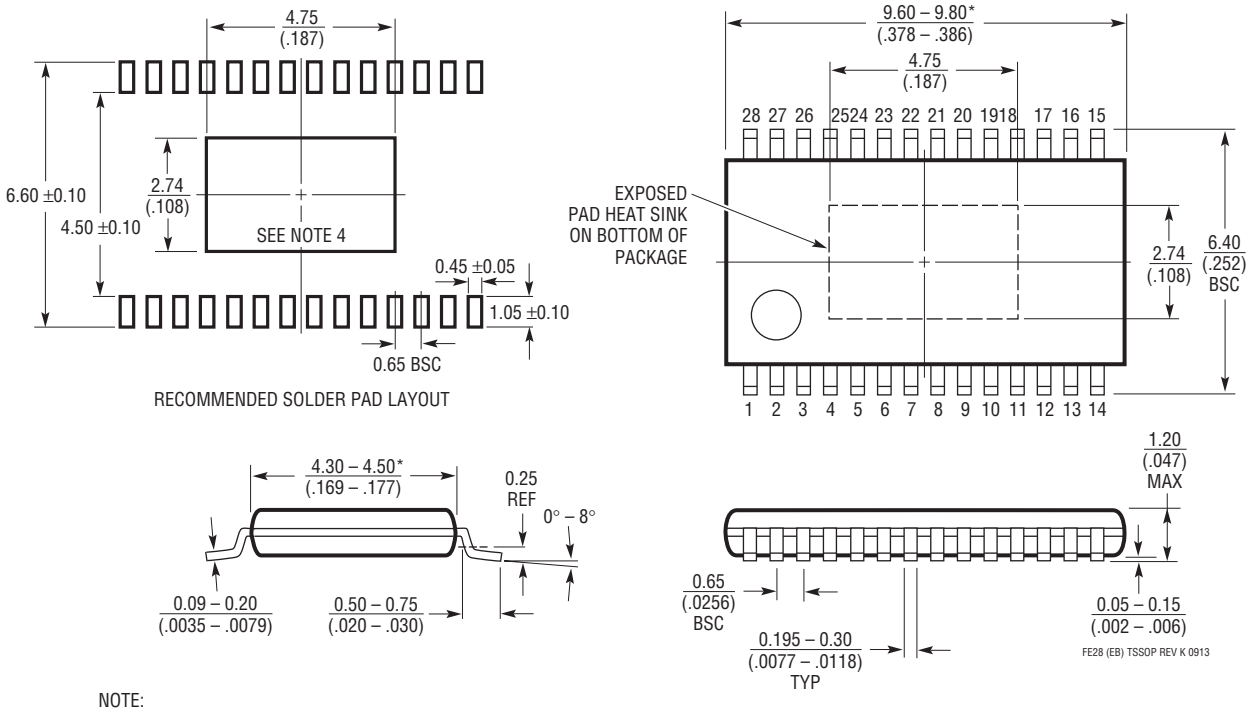
Power On – Fade Start



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3952#packaging for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation EB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

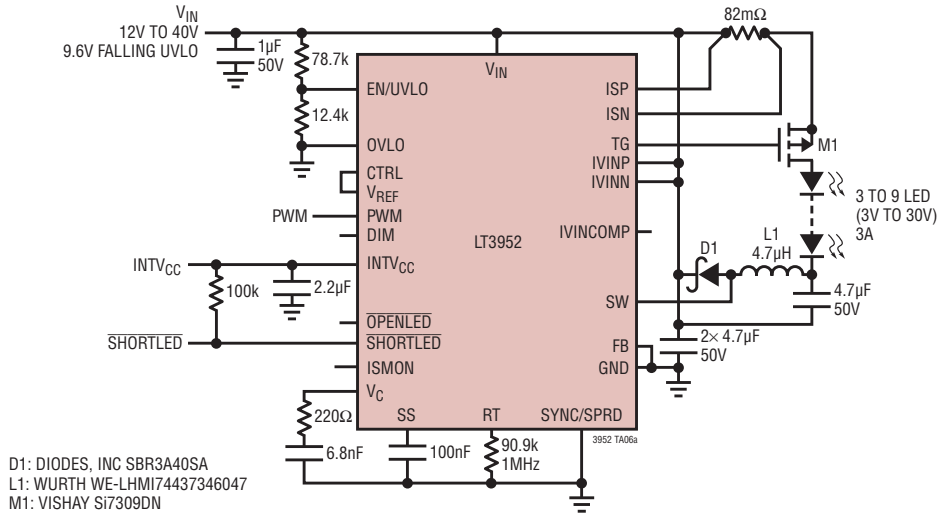
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

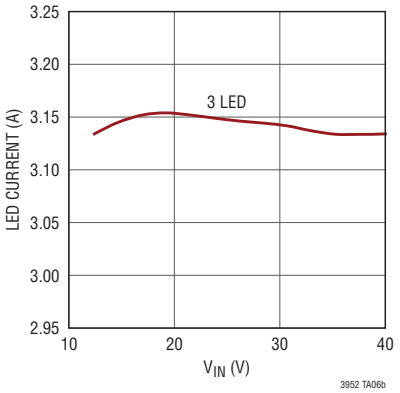
REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/16	Replaced reference to Note 5 to Note 4 in Absolute Maximum Table	2
		Removed Note 4 from $INTV_{CC}$ Dropout Voltage specification	3
		Replaced Note 5 with Note 4	5
		Clarified SS (Pin 19) description – replaced “shutdown mode” with “start-up mode”	11
		Clarified the Block Diagram pin designators	12
		Clarified Figure 11	19
		Clarified Open LED Flag and Overvoltage section 60mV becomes 65mV	20
		Clarifed LED Dead Short Response graph	28
		Clarifed Power On – Fade Start graph	29
		Clarifed Related Parts table	32

TYPICAL APPLICATION

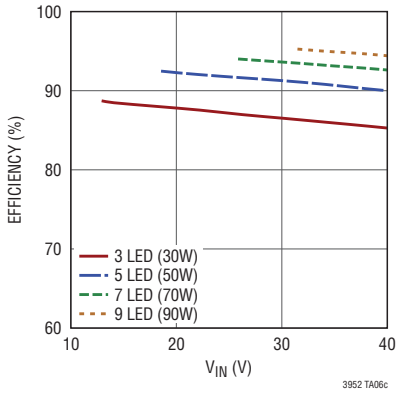
3A Buck Mode LED Driver



LED Current vs Input Voltage



Efficiency vs V_{IN}



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3795	110V High Side LED Controller with Spread Spectrum and Boost Short-Circuit Protection	V_{IN}: 4.5V to 110V, $V_{OUT(MAX)}$ = 110V, PWM Dimming = 3000:1, I_{SD} < 10mA, TSSOP-28 Package
LT3518	2.3A, 2.5MHz High Current LED Driver with 3000:1 Dimming with PMOS Disconnect FET Driver	V_{IN}: 3V to 30V, $V_{OUT(MAX)}$ = 45V, 3000:1 PWM Dimming, I_{SD} < 1µA, 4mm × 4mm QFN-16 and TSSOP-16E Packages
LT3755/LT3755-1/ LT3755-2	High Side 40V, 1MHz LED Controllers with True Color 3000:1 PWM Dimming	V_{IN}: 4.5V to 40V, $V_{OUT(MAX)}$ = 75V, 3000:1 PWM Dimming, I_{SD} < 1µA, 3mm × 3mm QFN-16 and MSOP-16E Packages
LT3956	High Side 80V, 3.3A, 1MHz LED Driver with True Color 3000:1 PWM Dimming	V_{IN}: 6V to 80V, $V_{OUT(MAX)}$ = 80V, PWM Dimming = 3000:1, I_{SD} < 1µA, 5mm × 6mm QFN-36 Package
LT3761	High Side 80V, 1MHz LED Controller with 3000:1 PWM Dimming and Internal PWM Generator	V_{IN}: 4.5V to 60V, $V_{OUT(MAX)}$ = 80V, 3000:1 True Color PWM Dimming, Analog, I_{SD} < 1µA, MSOP-16E Package
LT3478/LT3478-1	4.5A, 2MHz High Current LED Drivers with 3000:1 Dimming	V_{IN}: 2.8V to 36V, $V_{OUT(MAX)}$ = 40V, 3000:1 PWM Dimming, I_{SD} < 1µA, TSSOP-16E Package
LT3954	High Side 40V, 5A 1MHz LED Driver with 3000:1 PWM Dimming and Internal PWM Generator	V_{IN}: 4.5V to 40V, $V_{OUT(MAX)}$ = 40V, True Color PWM Dimming = 3000:1, Analog, I_{SD} < 1µA, 5mm × 6mm QFN-36 Package

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LT3952

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