Low Noise, Low Distortion Fully Differential Input/ Output Amplifier/Driver

FEATURES

- **Fully Differential Input and Output**
- **Wide Supply Range: 2.375V to 12.6V**
- **Rail-to-Rail Output Swing**
- **Low Noise: 3nV/√Hz**
- **Low Distortion, $2V_{P-P}$, 1MHz: –94dBc**
- **Adjustable Output Common Mode Voltage**
- Unity-Gain Stable
- Gain-Bandwidth: 70MHz
- Slew Rate: 65V/µs
- Large Output Current: 85mA
- DC Voltage Offset <2mV Max
- Open-Loop Gain: 100V/mV
- Low Power Shutdown
- 8-Pin MSOP or 3mm × 3mm DFN Package

APPLICATIONS

- Differential Input A/D Converter Driver
- Single-Ended to Differential Conversion
- Differential Amplification with Common Mode Translation
- Rail-to-Rail Differential Line Driver/Receiver
- Low Voltage, Low Noise, Differential Signal Processing

DESCRIPTION

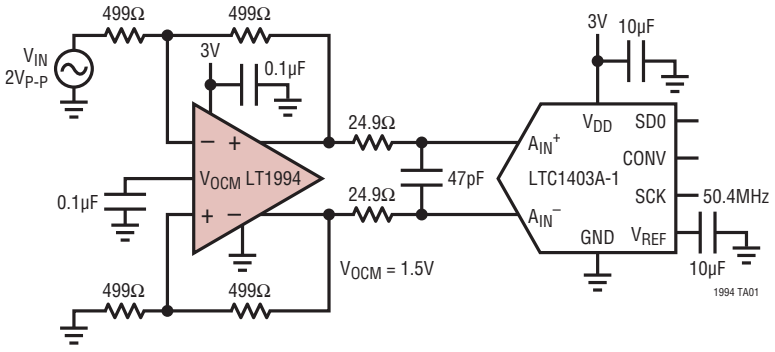
The LT®1994 is a high precision, very low noise, low distortion, fully differential input/output amplifier optimized for 3V, single-supply operation. The LT1994's output common mode voltage is independent of the input common mode voltage, and is adjustable by applying a voltage on the V_{OCM} pin. A separate internal common mode feedback path provides accurate output phase balancing and reduced even-order harmonics. This makes the LT1994 ideal for level shifting ground referenced signals for driving differential input, single-supply ADCs.

The LT1994 output can swing rail-to-rail and is capable of sourcing and sinking up to 85mA. In addition to the low distortion characteristics, the LT1994 has a low input referred voltage noise of 3nV/√Hz. This part maintains its performance for supply voltages as low as 2.375V. It draws only 13.3mA of supply current and has a hardware shutdown feature that reduces current consumption to 225µA.

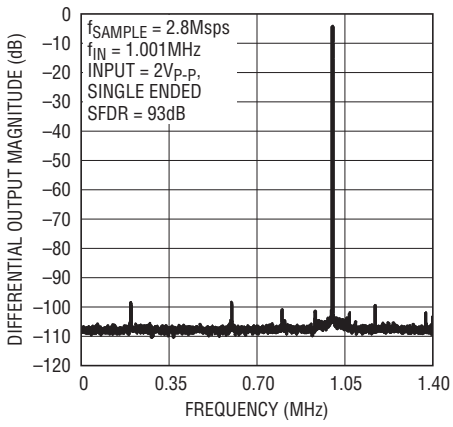
The LT1994 is available in an 8-pin MSOP or 8-pin DFN package.

TYPICAL APPLICATION

A/D Preamplifier: Single-Ended Input to Differential Output with Common Mode Level Shifting



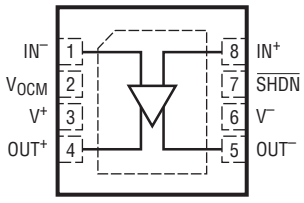
LT1994 Driving an LTC1403A-1 1MHz Sine Wave, 8192 Point FFT Plot



ABSOLUTE MAXIMUM RATINGS (Note 1)

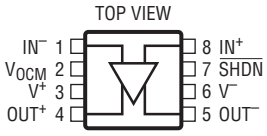
Total Supply Voltage (V^+ to V^-) 12.6V
Input Voltage (Note 2) ..... $\pm V_S$
Input Current (Note 2) ..... ±10mA
Input Current (V_{OCM}, $\overline{SHDN}$) ..... ±10mA
V_{OCM}, $\overline{SHDN}$ ..... $\pm V_S$
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4)
LT1994C ..... –40°C to 85°C
LT1994I ..... –40°C to 85°C
LT1994H ..... –40°C to 125°C
LT1994MP ..... –55°C to 125°C
Specified Temperature Range (Note 5)
LT1994C ..... 0°C to 70°C
LT1994I ..... –40°C to 85°C
LT1994H ..... –40°C to 125°C
LT1994MP ..... –55°C to 125°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO V^-



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 140°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1994CDD#PBF	LT1994CDD#TRPBF	LBQM	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT1994IDD#PBF	LT1994IDD#TRPBF	LBQM	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT1994HDD#PBF	LT1994HDD#TRPBF	LBQM	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT1994MPDD#PBF	LT1994MPDD#TRPBF	LDXQ	8-Lead (3mm × 3mm) Plastic DFN	–55°C to 125°C
LT1994CMS8#PBF	LT1994CMS8#TRPBF	LTBQN	8-Lead Plastic MSOP	0°C to 70°C
LT1994IMS8#PBF	LT1994IMS8#TRPBF	LTBQN	8-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = mid-supply, $V_{\overline{SHDN}}$ = OPEN, R_I = R_F = 499Ω, R_L = 800Ω to a mid-supply voltage (See Figure 1) unless otherwise noted. V_S is defined ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{OUT}^+ + V_{OUT}^-$)/2. V_{ICM} is defined as ($V_{IN}^+ + V_{IN}^-$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT}^+ – V_{OUT}^-$). V_{INDIFF} is defined as ($V_{IN}^+ – V_{IN}^-$).

SYMBOL	PARAMETER	CONDITIONS		C/I GRADES MIN	C/I GRADES TYP	C/I GRADES MAX	H/MP GRADES MIN	H/MP GRADES TYP	H/MP GRADES MAX	UNITS
V_{OSDIFF}	Differential Offset Voltage (Input Referred)	V_S = 2.375V, V_{ICM} = V_S/4	●			±2			±2	mV
		V_S = 3V	●			±2			±2	mV
		V_S = 5V	●			±2			±2	mV
		V_S = ±5V	●			±3			±3	mV
$\Delta V_{OSDIFF}/\Delta T$	Differential Offset Voltage Drift (Input Referred)	V_S = 2.375V, V_{ICM} = V_S/4			3					µV/°C
		V_S = 3V			3					µV/°C
		V_S = 5V			3					µV/°C
		V_S = ±5V			3					µV/°C
I_B	Input Bias Current (Note 6)	V_S = 2.375V, V_{ICM} = V_S/4	●	–45	–18	–3	–45	–18	–3	µA
		V_S = 3V	●	–45	–18	–3	–45	–18	–3	µA
		V_S = 5V	●	–45	–18	–3	–45	–18	–3	µA
		V_S = ±5V	●	–45	–18	–3	–45	–18	–3	µA
I_{OS}	Input Offset Current (Note 6)	V_S = 2.375V, V_{ICM} = V_S/4	●		±0.2	±2		±0.2	±2	µA
		V_S = 3V	●		±0.2	±2		±0.2	±2	µA
		V_S = 5V	●		±0.2	±3		±0.2	±3	µA
		V_S = ±5V	●		±0.2	±4		±0.2	±4	µA
R_{IN}	Input Resistance	Common Mode			700			700		kΩ
		Differential Mode			4.5			4.5		kΩ
C_{IN}	Input Capacitance	Differential			2			2		pF
e_n	Differential Input Referred Noise Voltage Density	f = 50kHz			3			3		nV/√Hz
i_n	Input Noise Current Density	f = 50kHz			2.5			2.5		pA/√Hz
e_{nVOCM}	Input Referred Common Mode Output Noise Voltage Density	f = 50kHz, V_{OCM} Shorted to Ground			15			15		nV/√Hz
V_{ICMR} (Note 7)	Input Signal Common Mode Range	V_S = 3V	●	0		1.75	0		1.75	V
		V_S = ±5V	●	–5		3.75	–5		3.75	V
CMRRI (Note 8)	Input Common Mode Rejection Ratio (Input Referred) $\Delta V_{ICM}/\Delta V_{OSDIFF}$	V_S = 3V, ΔV_{ICM} = 0.75V	●	55	85		55	85		dB
CMRRIO (Note 8)	Output Common Mode Rejection Ratio (Input Referred) $\Delta V_{OCM}/\Delta V_{OSDIFF}$	V_S = 5V, ΔV_{OCM} = 2V	●	65	85		65	85		dB
PSRR (Note 9)	Differential Power Supply Rejection ($\Delta V_S/\Delta V_{OSDIFF}$)	V_S = 3V to ±5V	●	69	105		69	105		dB
PSRRCM (Note 9)	Output Common Mode Power Supply Rejection ($\Delta V_S/\Delta V_{OSCM}$)	V_S = 3V to ±5V	●	45	70		45	70		dB
G_{CM}	Common Mode Gain ($\Delta V_{OUTCM}/\Delta V_{OCM}$)	V_S = ±2.5V	●		1					V/V
	Common Mode Gain Error $100 \bullet (G_{CM} – 1)$	V_S = ±2.5V	●		–0.15	±1				%
BAL	Output Balance ($\Delta V_{OUTCM}/\Delta V_{OUTDIFF}$)	$\Delta V_{OUTDIFF}$ = 2V								
		Single-Ended Input	●		–65	–46		–65	–46	dB
		Differential Input	●		–71	–50		–71	–50	dB
V_{OSCM}	Common Mode Offset Voltage ($V_{OUTCM} – V_{OCM}$)	V_S = 2.375V, V_{ICM} = V_S/4	●		±2.5	±25		±2.5	±25	mV
		V_S = 3V	●		±2.5	±25		±2.5	±25	mV
		V_S = 5V	●		±2.5	±30		±2.5	±30	mV
		V_S = ±5V	●		±2.5	±40		±2.5	±40	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = mid-supply, $V_{\overline{SHDN}}$ = OPEN, R_I = R_F = 499Ω, R_L = 800Ω to a mid-supply voltage (See Figure 1) unless otherwise noted. V_S is defined ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{OUT}^+ + V_{OUT}^-$)/2. V_{ICM} is defined as ($V_{IN}^+ + V_{IN}^-$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT}^+ - V_{OUT}^-$). V_{INDIFF} is defined as ($V_{IN}^+ - V_{IN}^-$).

SYMBOL	PARAMETER	CONDITIONS		C/I GRADES MIN	C/I GRADES TYP	C/I GRADES MAX	H/MP GRADES MIN	H/MP GRADES TYP	H/MP GRADES MAX	UNITS
$\Delta V_{OSCM}/\Delta T$	Common Mode Offset Voltage Drift	V_S = 2.375V, V_{ICM} = V_S/4			5			5		µV/°C
		V_S = 3V			5			5		µV/°C
		V_S = 5V			5			5		µV/°C
		V_S = ±5V			5			5		µV/°C
V_{OUTCMR} (Note 7)	Output Signal Common Mode Range (Voltage Range for the V_{OCM} Pin)	V_S = 3V, ±5V	●	V^- + 1.1		V^+ – 0.8	V^- + 1.1		V^+ – 0.8	V
R_{INVOCM}	Input Resistance, V_{OCM} Pin		●	30	40	60	30	40	60	kΩ
V_{MID}	Voltage at the V_{OCM} Pin	V_S = 5V	●	2.45	2.5	2.55	2.45	2.5	2.55	V
V_{OUT}	Output Voltage, High, Either Output Pin (Note 10)	V_S = 3V, No Load	●		70	140		70	140	mV
		V_S = 3V, R_L = 800Ω	●		90	175		90	175	mV
		V_S = 3V, R_L = 100Ω	●		200	400		200	400	mV
		V_S = ±5V, No Load	●		150	325		150	325	mV
		V_S = ±5V, R_L = 800Ω	●		200	450		200	450	mV
		V_S = ±5V, R_L = 100Ω	●		900	2400		900	2400	mV
	Output Voltage, Low, Either Output Pin (Note 10)	V_S = 3V, No Load	●		30	70		30	70	mV
		V_S = 3V, R_L = 800Ω	●		50	90		50	90	mV
		V_S = 3V, R_L = 100Ω	●		125	250		125	250	mV
		V_S = ±5V, No Load	●		80	180		80	180	mV
		V_S = ±5V, R_L = 800Ω	●		125	250		125	250	mV
		V_S = ±5V, R_L = 100Ω	●		900	2400		900	2400	mV
I_{SC}	Output Short-Circuit Current, Either Output Pin (Note 11)	V_S = 2.375V, R_L = 10Ω	●	±25	±35		±10	±35		mA
		V_S = 3V, R_L = 10Ω	●	±30	±40		±15	±40		mA
		V_S = 5V, R_L = 10Ω	●	±40	±65		±40	±65		mA
		V_S = ±5V, V_{CM} = 0V, R_L = 10Ω	●	±45	±85		±45	±85		mA
SR	Slew Rate	V_S = 5V, $\Delta V_{OUT}^+ = -\Delta V_{OUT}^-$ = 1V	●	50	65	85	50	65	85	V/µS
		V_S = ±5V, V_{CM} = 0V, $\Delta V_{OUT}^+ = -\Delta V_{OUT}^-$ = 1.8V	●	50	65	85	50	65	85	V/µS
GBW	Gain-Bandwidth Product (f_{TEST} = 1MHz)	V_S = 3V, T_A = 25°C	●	58	70		58	70		MHz
		V_S = ±5V, V_{CM} = 0V, T_A = 25°C	●	58	70		58	70		MHz
	Distortion	V_S = 3V, R_L = 800Ω, f_{IN} = 1MHz, $V_{OUT}^+ - V_{OUT}^-$ = $2V_{P-P}$								
		Differential Input								
		2nd Harmonic			–99			–99		dBc
		3rd Harmonic			–96			–96		dBc
		Single-Ended Input								
		2nd Harmonic			–94			–94		dBc
		3rd Harmonic			–108			–108		dBc
t_S	Settling Time	V_S = 3V, 0.01%, 2V Step			120			120		ns
		V_S = 3V, 0.1%, 2V Step			90			90		ns
A_{VOL}	Large-Signal Voltage Gain	V_S = 3V			100			100		dB
V_S	Supply Voltage Range		●	2.375		12.6	2.375		12.6	V
I_S	Supply Current	V_S = 3V	●		13.3	18.5		13.3	20.0	mA
		V_S = 5V	●		13.9	19.5		13.9	20.5	mA
		V_S = ±5V	●		14.8	20.5		14.8	21.5	mA
$I_{\overline{SHDN}}$	Supply Current in Shutdown	V_S = 3V	●		0.225	0.8		0.225	0.8	mA
		V_S = 5V	●		0.375	1.75		0.375	1.75	mA
		V_S = ±5V	●		0.7	2.5		0.7	2.5	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = mid-supply, $V_{\overline{SHDN}}$ = OPEN, R_I = R_F = 499Ω, R_L = 800Ω to a mid-supply voltage (See Figure 1) unless otherwise noted. V_S is defined ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{OUT}^+ + V_{OUT}^-$)/2. V_{ICM} is defined as ($V_{IN}^+ + V_{IN}^-$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT}^+ - V_{OUT}^-$). V_{INDIFF} is defined as ($V_{IN}^+ - V_{IN}^-$).

SYMBOL	PARAMETER	CONDITIONS		C/I GRADES MIN	C/I GRADES TYP	C/I GRADES MAX	H/MP GRADES MIN	H/MP GRADES TYP	H/MP GRADES MAX	UNITS
V_{IL}	$\overline{SHDN}$ Input Logic Low	V_S = 3V to ±5V	●			V^+ – 2.1			V^+ – 2.1	V
V_{IH}	$\overline{SHDN}$ Input Logic High	V_S = 3V to ±5V	●	V^+ – 0.6			V^+ – 0.6			V
$R_{\overline{SHDN}}$	$\overline{SHDN}$ Pull-Up Resistor	V_S = 2.375V to ±5V		40	55	75	40	55	75	kΩ
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ 0.5V to 3V			1			1		µs
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ 3V to 0.5V			1			1		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by a pair of back-to-back diodes. If the differential input voltage exceeds 1V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT1994C/LT1994I are guaranteed functional over the operating temperature range –40°C to 85°C. The LT1994H is guaranteed functional over the operating temperature range –40°C to 125°C. The LT1994MP is guaranteed functional over the operating temperature range –55°C to 125°C.

Note 5: The LT1994C is guaranteed to meet specified performance from 0°C to 70°C. The LT1994C is designed, characterized, and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1994I is guaranteed to meet specified performance from –40°C to 85°C. The LT1994H is guaranteed to meet specified performance from –40°C to 125°C. The LT1994MP is guaranteed to meet specified performance from –55°C to 125°C.

Note 6: Input bias current is defined as the average of the input currents flowing into Pin 1 and Pin 8 (IN^- and IN^+). Input Offset current is defined as the difference of the input currents flowing into Pin 8 and Pin 1 ($I_{OS} = I_B^+ - I_B^-$).

Note 7: Input Common Mode Range is tested using the Test Circuit of Figure 1 (R_F = R_I) by applying a single ended $2V_{P-P}$ 1kHz signal to V_{INP} (V_{INM} = 0), and measuring the output distortion (THD) at the common mode Voltage Range limits listed in the Electrical Characteristics table, and confirming the output THD is better than –40dB. The voltage range for the output common mode range (Pin 2) is tested using the Test Circuit of Figure 1 (R_F = R_I) by applying a 0.5V peak, 1kHz signal to the V_{OCM} Pin 2 (with V_{INP} = V_{INM} = 0) and measuring the output distortion (THD) at V_{OUTCM} with V_{OCM} biased 0.5V from the V_{OCM} pin range limits listed in the Electrical Characteristics Table, and confirming the THD is better than –40dB.

Note 8: Input CMRR is defined as the ratio of the change in the input common mode voltage at the pins IN^+ or IN^- to the change in differential input referred voltage offset. Output CMRR is defined as the ratio of the change in the voltage at the V_{OCM} pin to the change in differential input referred voltage offset.

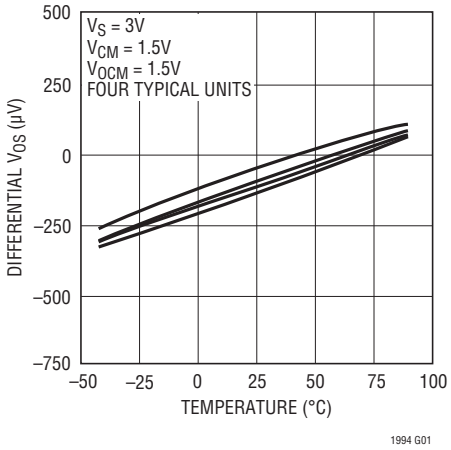
Note 9: Differential Power Supply Rejection (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred voltage offset. Common Mode Power Supply Rejection (PSRRCM) is defined as the ratio of the change in supply voltage to the change in the common mode offset, $V_{OUTCM} - V_{OCM}$.

Note 10: Output swings are measured as differences between the output and the respective power supply rail.

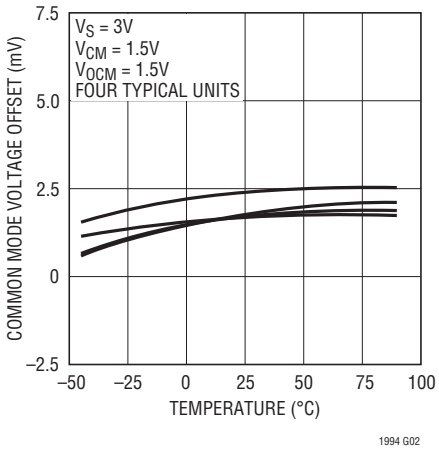
Note 11: Extended operation with the output shorted may cause junction temperatures to exceed the 150°C limit and is not recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

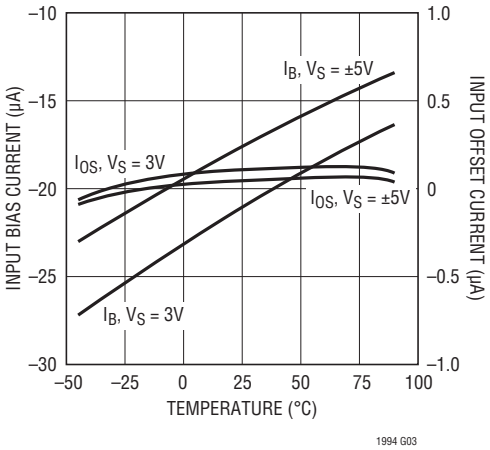
Differential Input Referred Voltage Offset vs Temperature



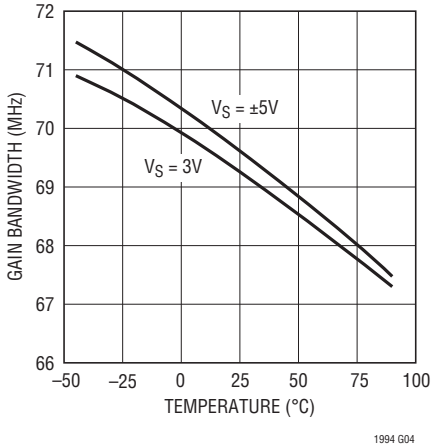
Common Mode Voltage Offset vs Temperature



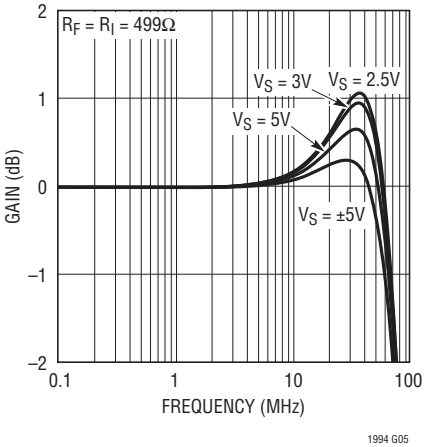
Input Bias Current and Input Offset Current vs Temperature



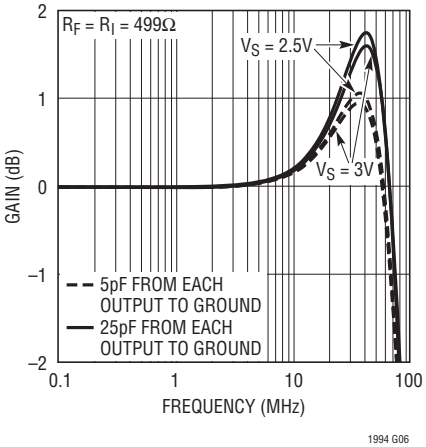
Gain Bandwidth vs Temperature



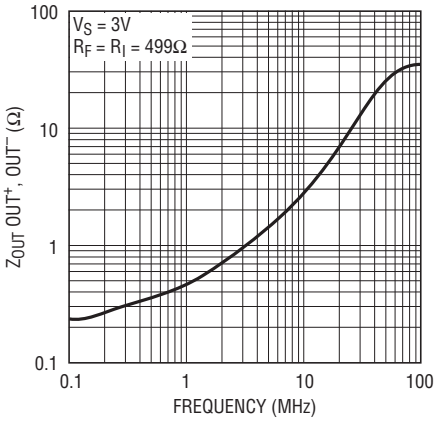
Frequency Response vs Supply Voltage



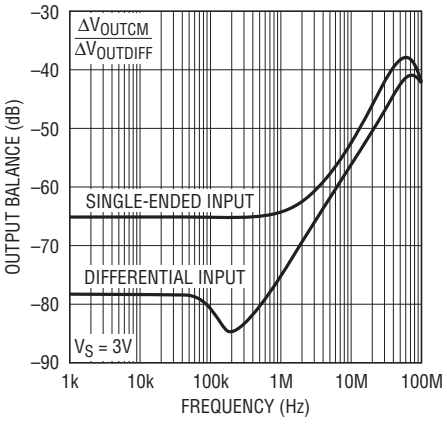
Frequency Response vs Load Capacitance



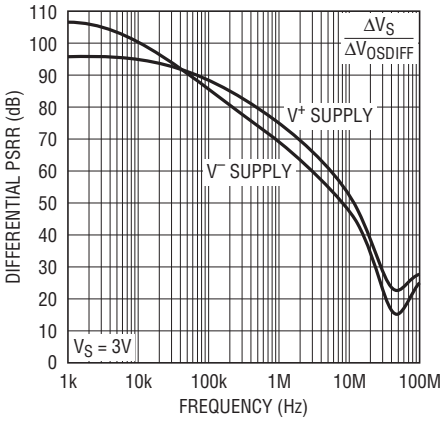
Output Impedance vs Frequency



Output Balance vs Frequency

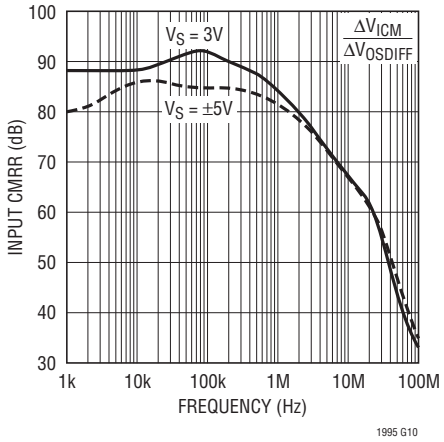


Differential Power Supply Rejection vs Frequency

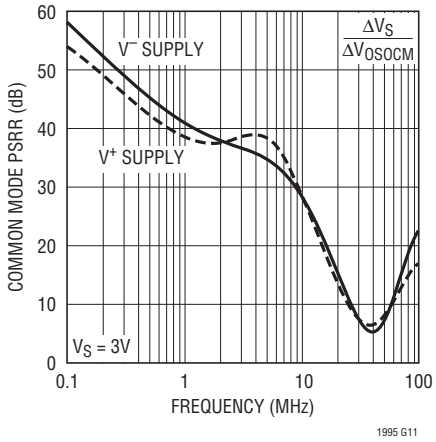


TYPICAL PERFORMANCE CHARACTERISTICS

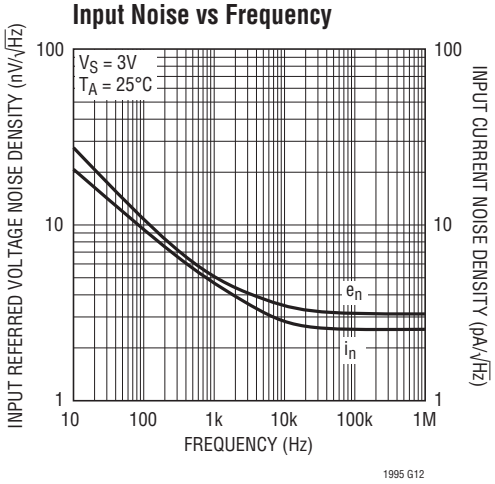
Input Common Mode Rejection vs Frequency



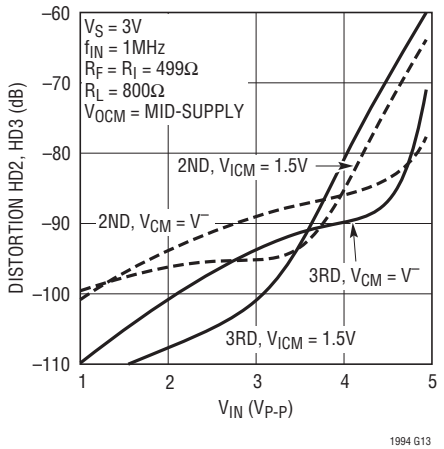
Common Mode Output Power Supply Rejection vs Frequency



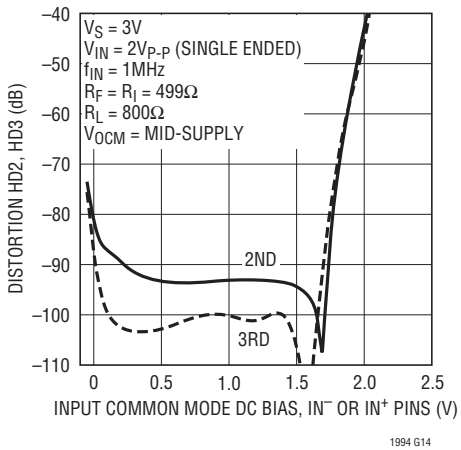
Input Noise vs Frequency



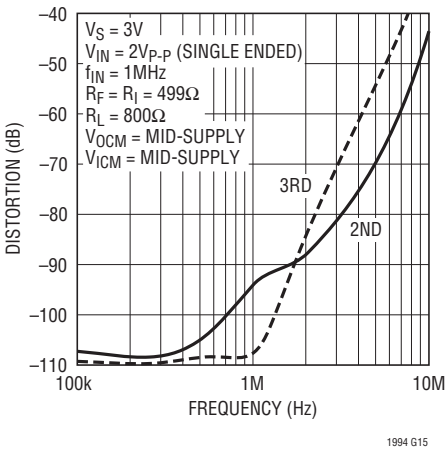
Differential Distortion vs Input Amplitude (Single-Ended Input)



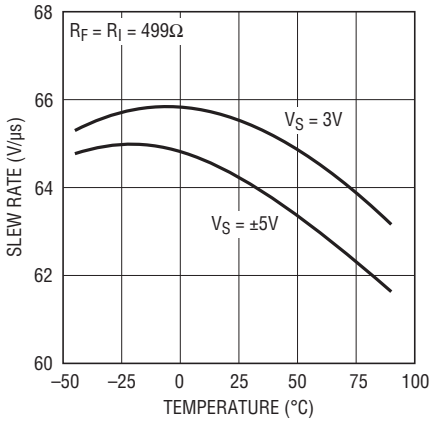
Differential Distortion vs Input Common Mode Level



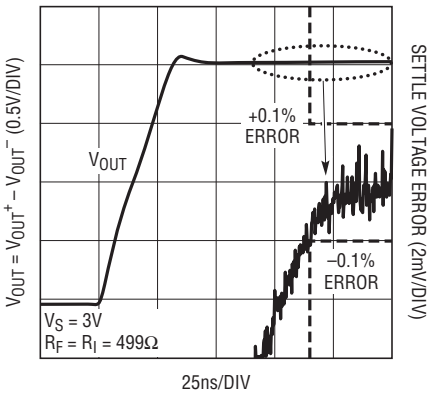
Differential Distortion vs Frequency



Slew Rate vs Temperature

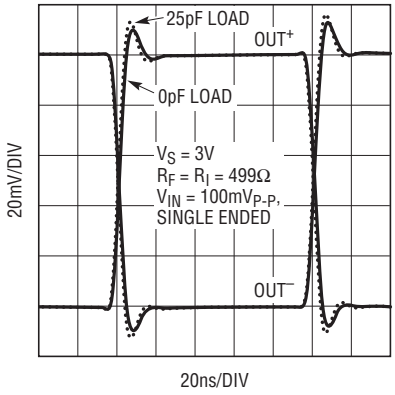


2V Step Response Settling

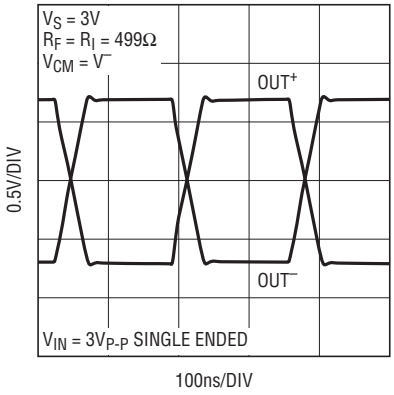


TYPICAL PERFORMANCE CHARACTERISTICS

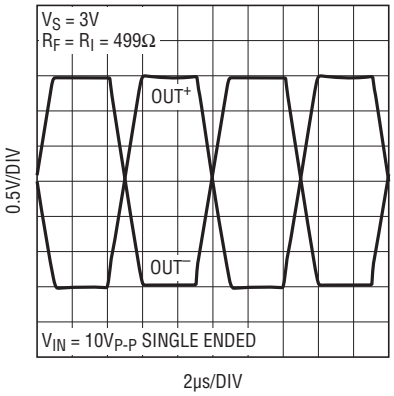
Small-Signal Step Response



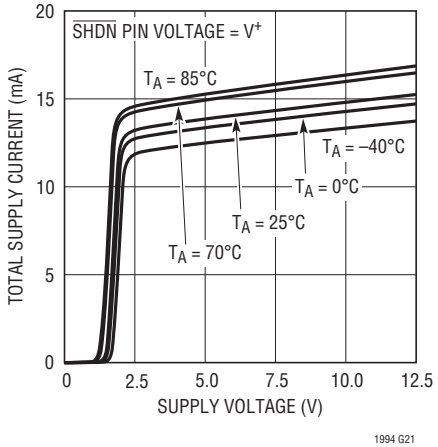
Large-Signal Step Response



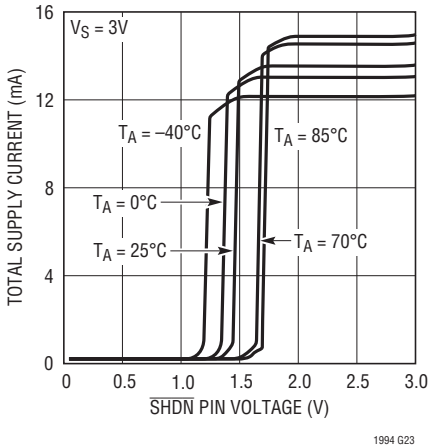
Output with Large Input Overdrive



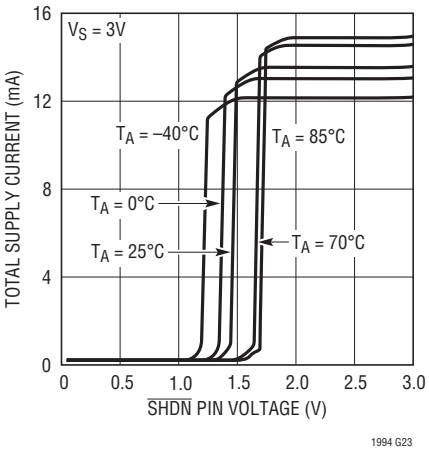
Supply Current vs Supply Voltage



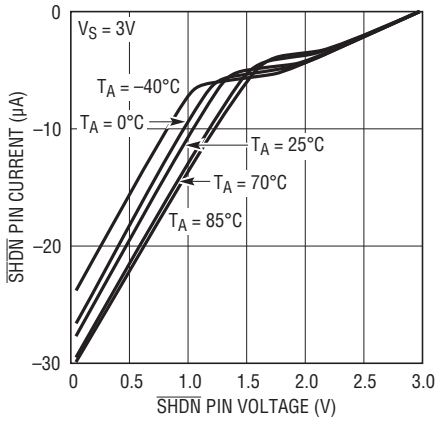
Supply Current vs $\overline{SHDN}$ Voltage



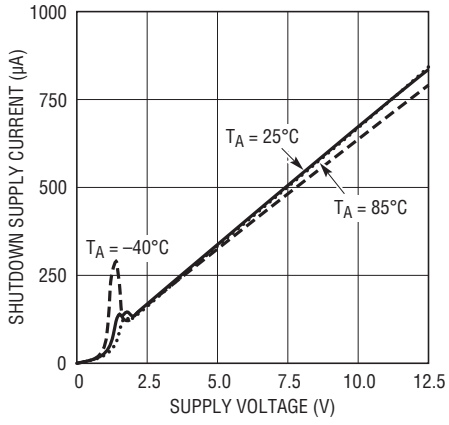
Supply Current vs $\overline{SHDN}$ Voltage



$\overline{SHDN}$ Pin Current vs $\overline{SHDN}$ Pin Voltage



Shutdown Supply Current vs Supply Voltage



PIN FUNCTIONS

IN^+, IN^- (Pins 1, 8): Noninverting and Inverting Input Pins of the Amplifier, Respectively. For best performance, it is highly recommended that stray capacitance be kept to an absolute minimum by keeping printed circuit connections as short as possible, and if necessary, stripping back nearby surrounding ground plane away from these pins.

V_{OCM} (Pin 2): Output Common Mode Reference Voltage. The V_{OCM} pin is the midpoint of an internal resistive voltage divider between the supplies, developing a (default) mid-supply voltage potential to maximize output signal swing. V_{OCM} has a Thevenin equivalent resistance of approximately 40k and can be overdriven by an external voltage reference. The voltage on V_{OCM} sets the output common mode voltage level (which is defined as the average of the voltages on the OUT^+ and OUT^- pins). V_{OCM} should be bypassed with a high quality ceramic bypass capacitor of at least 0.1µF (unless connected directly to a low impedance, low noise ground plane) to minimize common mode noise from being converted to differential noise by impedance mismatches both externally and internally to the IC.

V^+, V^- (Pins 3, 6): Power Supply Pins. For single-supply applications (Pin 6 grounded) it is recommended that high quality 1µF and 0.1µF ceramic bypass capacitors be placed from the positive supply pin (Pin 3) to the negative supply pin (Pin 6) with minimal routing. Pin 6 should be directly tied to a low impedance ground plane. For dual power supplies, it is recommended that high quality, 0.1µF ceramic capacitors are used to bypass Pin 3 to ground and Pin 6 to ground. It is also highly recommended that high quality 1µF and 0.1µF ceramic bypass capacitors be placed across the power supply pins (Pins 3 and 6) with minimal routing.

OUT^+, OUT^- (Pins 4, 5): Output Pins. Each pin can drive approximately 100Ω to ground with a short-circuit current limit of up to ±85mA. Each amplifier output is designed to drive a load capacitance of 25pF. This basically means the amplifier can drive 25pF from each output to ground or 12.5pF differentially. Larger capacitive loads should be decoupled with at least 25Ω resistors from each output.

$\overline{SHDN}$ (Pin 7): When Pin 7 ($\overline{SHDN}$) is floating or when Pin 7 is directly tied to V^+, the LT1994 is in the normal operating mode. When Pin 7 is pulled a minimum of 2.1V below V^+, the LT1994 enters into a low power shutdown state. Refer to the $\overline{SHDN}$ pin section under Applications Information for a description of the LT1994 output impedance in the shutdown state.

APPLICATIONS INFORMATION

Functional Description

The LT1994 is a small outline, wideband, low noise and low distortion fully-differential amplifier with accurate output-phase balancing. The LT1994 is optimized to drive low voltage, single-supply, differential input analog-to-digital converters (ADCs). The LT1994's output is capable of swinging rail-to-rail on supplies as low as 2.5V, which makes the amplifier ideal for converting ground referenced, single-ended signals into V_{OCM} referenced differential signals in preparation for driving low voltage, single-supply, differential input ADCs. Unlike traditional op amps which have a single output, the LT1994 has two outputs to process signals differentially. This allows for two times the signal swing in low voltage systems when compared to single-ended output amplifiers. The balanced differential nature of the amplifier also provides even-order harmonic distortion cancellation, and less susceptibility to common mode noise (like power supply noise). The LT1994 can be used as a single-ended input to differential output amplifier, or as a differential input to differential output amplifier.

The LT1994's output common mode voltage, defined as the average of the two output voltages, is independent of the input common mode voltage, and is adjusted by applying a voltage on the V_{OCM} pin. If the pin is left open, there is an internal resistive voltage divider, which develops a potential halfway between the V^+ and V^- pins. The V_{OCM} pin will have an equivalent Thevenin equivalent resistance of 40k, and a Thevenin equivalent voltage of half supply. Whenever this pin is not hard tied to a low impedance ground plane, it is recommended that a high quality ceramic capacitor is used to bypass the V_{OCM} pin to a low impedance ground plane (see Layout Considerations in this document). The LT1994's internal common mode feedback path forces accurate output phase balancing to reduce even order harmonics, and centers each individual output about the potential set by the V_{OCM} pin.

$$V_{OUTCM} = V_{OCM} = \frac{V_{OUT}^{+} + V_{OUT}^{-}}{2}$$

The outputs (OUT^+ and OUT^-) of the LT1994 are capable of swinging rail-to-rail. They can source or sink up to approximately 85mA of current. Each output is rated to drive approximately 25pF to ground (12.5pF differentially). Higher load capacitances should be decoupled with at least 25Ω of series resistance from each output.

Input Pin Protection

The LT1994's input stage is protected against differential input voltages that exceed 1V by two pairs of back-to-back diodes that protect against emitter base breakdown of the input transistors. In addition, the input pins have steering diodes to either power supply. If the input pair is overdriven, the current should be limited to under 10mA to prevent damage to the IC. The LT1994 also has steering diodes to either power supply on the V_{OCM}, and $\overline{SHDN}$ pins (Pins 2 and 7) and if exposed to voltages that exceed either supply, they too should be current limited to under 10mA.

$\overline{SHDN}$ Pin

If the $\overline{SHDN}$ pin (Pin 7) is pulled 2.1V below the positive supply, an internal current is generated that is used to power down the LT1994. The pin will have the Thevenin equivalent impedance of approximately 55kΩ to V^+. If the pin is left unconnected, an internal pull-up resistor of 120k will keep the part in normal active operation. Care should be taken to control leakage currents at this pin to under 1µA to prevent leakage currents from inadvertently putting the LT1994 into shutdown. In shutdown, all biasing current sources are shut off, and the output pins OUT^+ and OUT^- will each appear as open collectors with a nonlinear capacitor in parallel, and steering diodes to either supply. Because of the nonlinear capacitance, the outputs still have the ability to sink and source small amounts of transient current if exposed to significant voltage transients. The inputs (IN^+ and IN^-) have anti-parallel diodes that can conduct if voltage transients at the input exceed 1V. The inputs also have steering diodes to either supply. The turn-on and turn-off time between the shutdown and active states are on the order of 1µs but depends on the circuit configuration.

APPLICATIONS INFORMATION

General Amplifier Applications

As levels of integration have increased and, correspondingly, system supply voltages decreased, there has been a need for ADCs to process signals differentially in order to maintain good signal-to-noise ratios. These ADCs are typically supplied from a single-supply voltage that can be as low as 2.5V and will have an optimal common mode input range near mid-supply. The LT1994 makes interfacing to these ADCs trivial, by providing both single-ended to differential conversion as well as common mode level shifting. Figure 1 shows a general single-supply application with perfectly matched feedback networks from OUT^+ and OUT^-. The gain to $V_{OUTDIFF}$ from V_{INM} and V_{INP} is:

$$V_{OUTDIFF} = V_{OUT}^{+} - V_{OUT}^{-} \approx \frac{R_F}{R_I} \bullet (V_{INP} - V_{INM})$$

Note from the above equation that the differential output voltage ($V_{OUT}^+ - V_{OUT}^-$) is completely independent of input and output common mode voltages, or the voltage at the common mode pin. This makes the LT1994 ideally suited pre-amplification, level shifting, and conversion of single-ended signals to differential output signals in preparation for driving differential input ADCs.

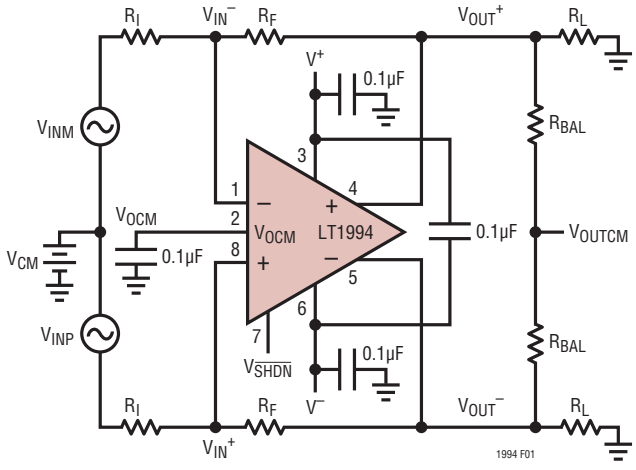


Figure 1. Test Circuit

Effects of Resistor Pair Mismatch

Figure 2 shows a circuit diagram that takes into consideration that real world resistors will not perfectly match. Assuming infinite open-loop gain, the differential output relationship is given by the equation:

$$V_{OUTDIFF} = V_{OUT}^{+} - V_{OUT}^{-} \cong \frac{R_F}{R_I} \bullet V_{INDIFF} + \frac{\Delta\beta}{\beta_{AVG}} \bullet V_{ICM} - \frac{\Delta\beta}{\beta_{AVG}} \bullet V_{OCM},$$

where:

R_F is the average of R_{F1} and R_{F2}, and R_I is the average of R_{I1} and R_{I2}.

β_{AVG} is defined as the average feedback factor (or gain) from the outputs to their respective inputs:

$$\beta_{AVG} = \frac{1}{2} \bullet \left(\frac{R_{I2}}{R_{I2} + R_{F2}} + \frac{R_{I1}}{R_{I1} + R_{F1}} \right)$$

$\Delta\beta$ is defined as the difference in feedback factors:

$$\Delta\beta = \frac{R_{I2}}{R_{I2} + R_{F2}} - \frac{R_{I1}}{R_{I1} + R_{F1}}$$

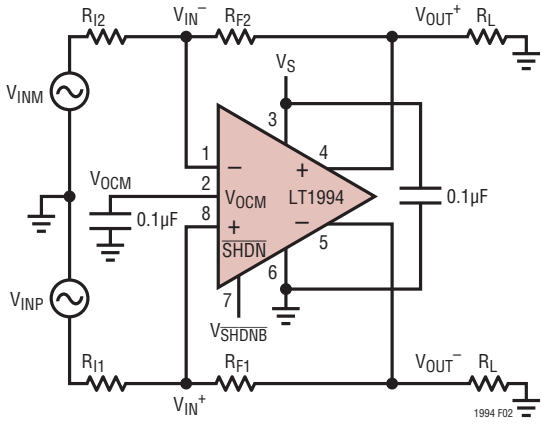


Figure 2. Real-World Application

APPLICATIONS INFORMATION

V_{ICM} is defined as the average of the two input voltages, V_{INP} and V_{INM} (also called the input common mode voltage):

$$V_{ICM} = \frac{1}{2} \bullet (V_{INP} + V_{INM})$$

and V_{INDIFF} is defined as the difference of the input voltages:

$$V_{INDIFF} = V_{INP} - V_{INM}$$

When the feedback ratios mismatch ($\Delta\beta$), common mode to differential conversion occurs.

Setting the differential input to zero ($V_{INDIFF} = 0$), the degree of common mode to differential conversion is given by the equation:

$$V_{OUTDIFF} = V_{OUT}^{+} - V_{OUT}^{-} \approx (V_{ICM} - V_{OCM}) \bullet \frac{\Delta\beta}{\beta_{AVG}} \Bigg|_{V_{INDIFF} = 0}$$

In general, the degree of feedback pair mismatch is a source of common mode to differential conversion of both signals and noise. Using 1% resistors or better will provide about 28dB of common mode rejection. Using 0.1% resistors will provide about 48dB of common mode rejection. A low impedance ground plane should be used as a reference for both the input signal source and the V_{OCM} pin. A direct short of V_{OCM} to this ground plane or bypassing the V_{OCM} with a high quality 0.1µF ceramic capacitor to this ground plane will further mitigate against common mode signals from being converted to differential.

Input Impedance and Loading Effects

The input impedance looking into the V_{INP} or V_{INM} input of Figure 1 depends on whether or not the sources V_{INP} and V_{INM} are fully differential. For balanced input sources ($V_{INP} = -V_{INM}$), the input impedance seen at either input is simply:

$$R_{INP} = R_{INM} = R_I$$

For single-ended inputs, because of the signal imbalance at the input, the input impedance actually increases over the balanced differential case. The input impedance looking into either input is:

$$R_{INP} = R_{INM} = \frac{R_I}{\left(1 - \frac{1}{2} \bullet \left[\frac{R_F}{R_I + R_F}\right]\right)}$$

Input signal sources with non-zero output impedances can also cause feedback imbalance between the pair of feedback networks. For the best performance, it is recommended that the source's output impedance be compensated for. If input impedance matching is required by the source, R1 should be chosen (see Figure 3):

$$R1 = \frac{R_{INM} \bullet R_S}{R_{INM} - R_S}$$

According to Figure 3, the input impedance looking into the differential amp (R_{INM}) reflects the single-ended source case, thus:

$$R_{INM} = \frac{R_I}{\left(1 - \frac{1}{2} \bullet \left[\frac{R_F}{R_I + R_F}\right]\right)}$$

R2 is chosen to balance $R1 || R_S$:

$$R2 = \frac{R1 \bullet R_S}{R1 + R_S}$$

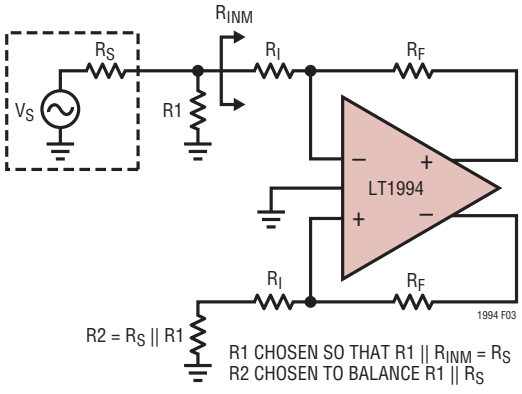


Figure 3. Optimal Compensation for Signal-Source Impedance

APPLICATIONS INFORMATION

Input Common Mode Voltage Range

The LT1994's input common mode voltage (V_{ICM}) is defined as the average of the two input voltages, V_{IN}^+, and V_{IN}^-. It extends from V^- to approximately 1.25V below V^+. The input common mode range depends on the circuit configuration (gain), V_{OCM} and V_{CM} (refer to Figure 4). For fully differential input applications, where $V_{INP} = -V_{INM}$, the common mode input is approximately:

$$V_{ICM} = \frac{V_{IN}^+ + V_{IN}^-}{2} \approx V_{OCM} \bullet \left(\frac{R_I}{R_I + R_F}\right) + V_{CM} \bullet \left(\frac{R_F}{R_F + R_I}\right)$$

With singled-ended inputs, there is an input signal component to the input common mode voltage. Applying only V_{INP} (setting V_{INM} to zero), the input common voltage is approximately:

$$V_{ICM} = \frac{V_{IN}^+ + V_{IN}^-}{2} \approx V_{OCM} \bullet \left(\frac{R_I}{R_I + R_F}\right) + V_{CM} \bullet \left(\frac{R_F}{R_F + R_I}\right) + \frac{V_{INP}}{2} \bullet \left(\frac{R_F}{R_F + R_I}\right)$$

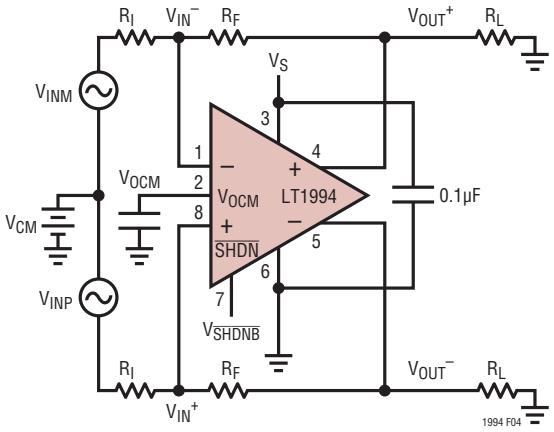


Figure 4. Circuit for Common Mode Range

Output Common Mode Voltage Range

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = V_{OCM} = \frac{V_{OUT}^+ + V_{OUT}^-}{2}$$

The V_{OCM} sets this average by an internal common mode feedback loop which internally forces $V_{OUT}^+ = -V_{OUT}^-$. The output common mode range extends from approximately 1.1V above V^- to approximately 0.8V below V^+. The V_{OCM} pin sits in the middle of an 80kΩ to 80kΩ voltage divider that sets the default mid-supply open-circuit potential.

In single-supply applications, where the LT1994 is used to interface to an ADC, the optimal common mode input range to the ADC is often determined by the ADC's reference. If the ADC makes a reference available for setting the input common mode voltage, it can be directly tied to the V_{OCM} pin, but must be capable of driving a 40k equivalent resistance that is tied to a mid-supply potential. If an external reference drives the V_{OCM} pin, it should still be bypassed with a high quality 0.1µF capacitor to a low impedance ground plane to filter any thermal noise and to prevent common mode signals on this pin from being inadvertently converted to differential signals.

Noise Considerations

The LT1994's input referred voltage noise is on the order of 3nV/√Hz. Its input referred current noise is on the order of 2.5pA/√Hz. In addition to the noise generated by the amplifier, the surrounding feedback resistors also contribute noise. The output noise generated by both the amplifier and the feedback components is given by the equation:

$$e_{no} = \sqrt{\left(e_{ni} \bullet \left[1 + \frac{R_F}{R_I}\right]\right)^2 + 2 \bullet \left(I_n \bullet R_F\right)^2 + 2 \bullet \left(e_{nRI} \bullet \left[\frac{R_F}{R_I}\right]\right)^2 + 2 \bullet e_{nRF}^2}$$

APPLICATIONS INFORMATION

A plot of this equation and a plot of the noise generated by the feedback components are shown in Figure 6.

The LT1994's input referred voltage noise contributes the equivalent noise of a 560Ω resistor. When the feedback network is comprised of resistors whose values are less than this, the LT1994's output noise is voltage noise dominant (See Figure 6):

$$e_{no} \approx e_{ni} \bullet \left(1 + \frac{R_F}{R_I}\right)$$

Feedback networks consisting of resistors with values greater than about 10k will result in output noise which is amplifier current noise dominant.

$$e_{no} \approx \sqrt{2} \bullet I_n \bullet R_F$$

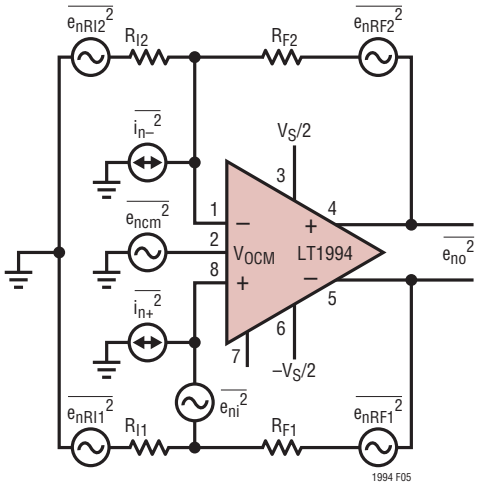


Figure 5. Noise Analysis

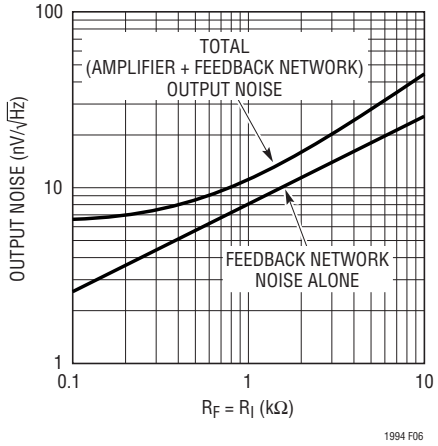


Figure 6. LT1994 Output Spot Noise vs Spot Noise Contributed by Feedback Network Alone

Lower resistor values always result in lower noise at the penalty of increased distortion due to increased loading of the feedback network on the output. Higher resistor values will result in higher output noise, but improved distortion due to less loading on the output.

Figure 6 shows the noise voltage that will appear differentially between the outputs. The common mode output noise voltage does not add to this differential noise. For optimum noise and distortion performance, use a differential output configuration.

Power Dissipation Considerations

The LT1994 is housed in either an 8-lead MSOP package (θ_{JA} = 140°C/W or an 8-lead DD package (θ_{JA} = 43°C/W). The LT1994 combines high speed and large output current with a small die and small package so there is a need to be sure the die temperature does not exceed 150°C. In the 8-lead MSOP, LT1994 has its V^- lead fused to the frame so it is possible to lower the package thermal impedance by connecting the V^- pin to a large ground plane or metal trace. Metal trace and plated through holes can be used to spread the heat generated by the device to the backside of the PC board. For example, an 8-lead MSOP on a 3/32" FR-4 board with 540mm^2 of 2oz. copper on both sides of the PC board tied to the V^- pin can drop the θ_{JA} from 140°C/W to 110°C/W (see Table 1).

The underside of the DD package has exposed metal (4mm^2) from the lead frame where the die is attached. This provides for the direct transfer of heat from the die junction to the printed circuit board to help control the maximum operating junction temperature. The dual-in-line pin arrangement allows for extended metal beyond the ends of the package on the topside (component side) of a circuit board. Table 1 summarizes for the MSOP package, the thermal resistance from the die junction-to-ambient that can be obtained using various amounts of topside, and backside metal (2oz. copper). On multilayer boards, further reductions can be obtained using additional metal on inner PCB layers connected through vias beneath the package.

APPLICATIONS INFORMATION

In general, the die temperature can be estimated from the ambient temperature T_A, and the device power dissipation P_D:

$$T_J = T_A^+ + P_D \bullet \theta_{JA}$$

The power dissipation in the IC is a function of the supply voltage, the output voltage, and the load resistance. For fully differential output amplifiers at a given supply voltage ($\pm V_{CC}$), and a given differential load (R_{LOAD}), the worst-case power dissipation $P_{D(MAX)}$ occurs at the worst-case quiescent current ($I_{Q(MAX)}$ = 20.5mA) and when the load current is given by the expression:

$$I_{LOAD} = \frac{V_{CC}}{R_{LOAD}}$$

The worst-case power dissipation in the LT1994 at

$$I_{LOAD} = \frac{V_{CC}}{R_{LOAD}} \text{ is:}$$

$$P_{D(MAX)} = 2 \bullet V_{CC} \bullet \left(I_{LOAD} + I_{Q(MAX)}\right) - {I_{LOAD}}^2 \bullet$$

$$R_{LOAD} = \frac{{V_{CC}}^2}{R_{LOAD}} + 2 \bullet V_{CC} \bullet I_{Q(MAX)}$$

Example: A LT1994 is mounted on a circuit board in a MSOP-8 package (θ_{JA} = 140°C/W), and is running off of ±5V supplies driving an equivalent load (external load plus feedback network) of 75Ω. The worst-case power that would be dissipated in the device occurs when:

$$P_{D(MAX)} = \frac{{V_{CC}}^2}{R_{LOAD}} + 2 \bullet V_{CC} \bullet I_{Q(MAX)}$$

$$= \frac{5V^2}{75\Omega} + 2 \bullet 5V \bullet 17.5MA = 0.54W$$

The maximum ambient temperature the 8-lead MSOP is allowed to operate under these conditions is:

$T_A = T_{JMAX} - P_D \bullet \theta_{JA}$ = 150°C – (0.54W) • (140°C/W) = 75°C

To operate the device at higher ambient temperature, connect more copper to the V^- pin to reduce the thermal resistance of the package as indicated in Table 1.

Table 1. LT1994 MSOP Package Thermal Resistivity

COPPER AREA TOPSIDE (mm^2)	COPPER AREA BACKSIDE (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
0	0	140
30	0	135
100	0	130
100	100	120
540	540	110

Layout Considerations

Because the LT1994 is a high speed amplifier, it is sensitive to both stray capacitance and stray inductance. Components connected to the LT1994 should be connected with as short and direct connections as possible. A low noise, low impedance ground plane is critical for the highest performance. In single-supply applications, high quality surface mount 1µF and 0.1µF ceramic bypass capacitors with minimum PCB trace should be used directly across the power supplies V^+ to V^-. In split supply applications, high quality surface mount 1µF and 0.1µF ceramic bypass capacitors should be placed across the power supplies V^+ to V^-, and individual high quality surface mount 0.1µF bypass capacitors should be used from each supply to ground with direct (short) connections.

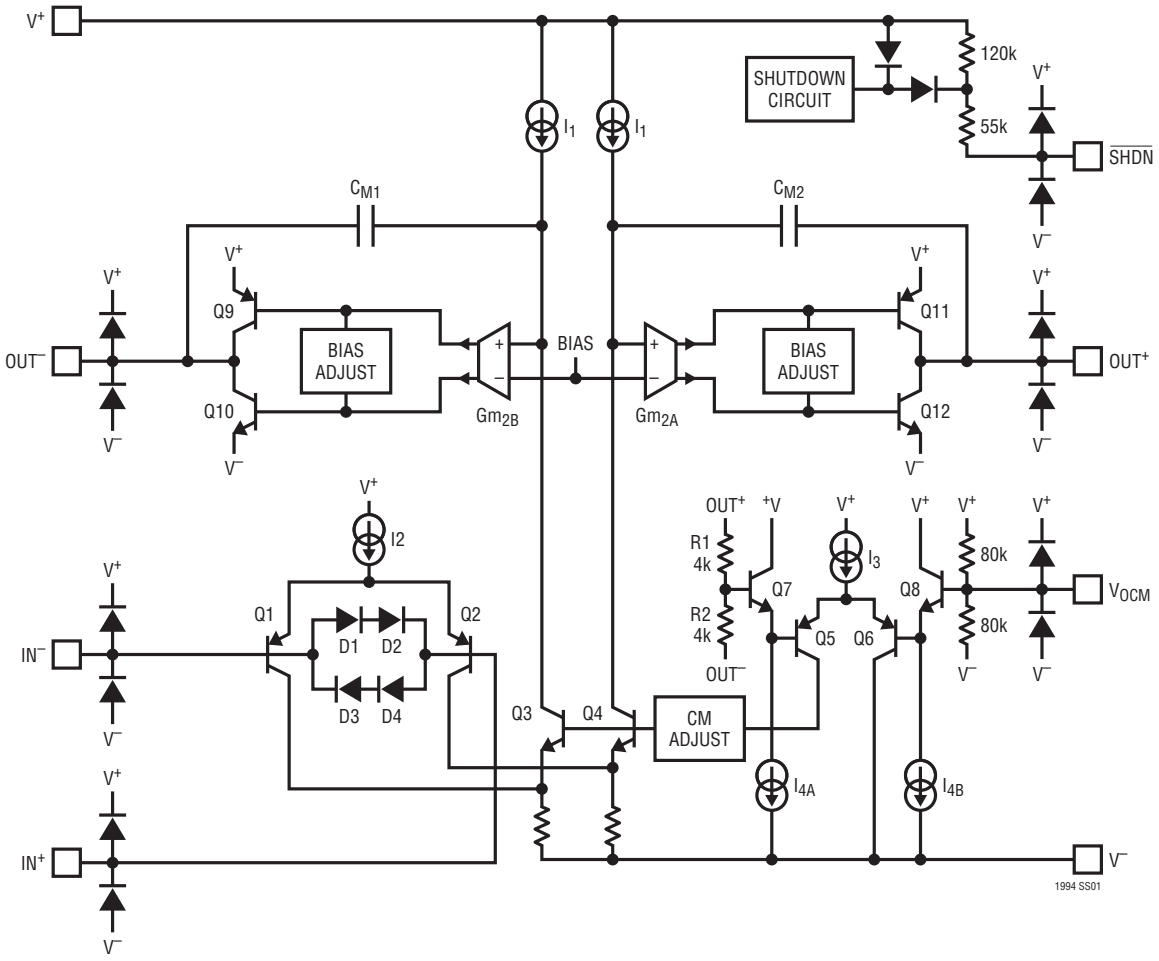
Any stray parasitic capacitance to ground at the summing junctions, IN^+ and IN^- should be kept to an absolute minimum even if it means stripping back the ground plane away from any trace attached to this node. This becomes especially true when the feedback resistor network uses resistor values >500Ω in circuits with $R_F = R_I$. Excessive peaking in the frequency response can be mitigated by adding small amounts of feedback capacitance around RF (2pF to 5pF). Always keep in mind the differential nature of the LT1994, and that it is critical that the output impedances seen by both outputs (stray or intended) should be as balanced and symmetric as possible. This will help preserve the natural balance of the LT1994, which minimizes the generation of even order harmonics, and preserves the rejection of common mode signals and noise.

It is highly recommended that the V_{OCM} pin be either hard tied to a low impedance ground plane (in split supply applications) or bypassed to ground with a high quality

APPLICATIONS INFORMATION

0.1µF ceramic capacitor in single-supply applications. This will help prevent thermal noise from the internal 80kΩ-80kΩ voltage divider (25nV/√Hz) and other external sources of noise from being converted to differential noise due to mismatches in the feedback networks. It is also recommended that the resistive feedback networks be comprised of 1% resistors (or better) to enhance the output common mode rejection. This will also prevent V_{OCM} input referred common mode noise of the common mode amplifier path (which cannot be filtered) from being converted to differential noise, degrading the differential noise performance.

SIMPLIFIED SCHEMATIC

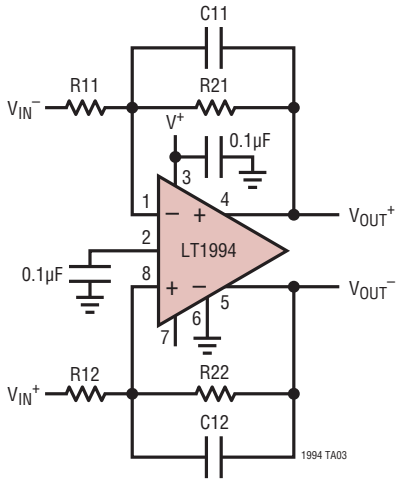


TYPICAL APPLICATIONS

Differential 1st Order Lowpass Filter

Maximum –3dB frequency (f_{3dB}) 2MHz

Stopband attenuation: –6dB at 2 • f_{3dB} and 14dB at 5 • f_{3dB}



Component Calculation:

R11 = R12, R21 = R22

$$f_{3dB} \leq 2MHz \text{ and Gain} \leq \frac{2MHz}{f_{3dB}}$$

1. Calculate an absolute value for C11 ($C11_{abs}$) using a specified –3dB frequency

$$C11_{abs} = \frac{4 \bullet 10^5}{f_{3dB}} \; (C11_{abs} \text{ in pF and } f_{3dB} \text{ in kHz})$$

2. Select a standard 5% capacitor value nearest the absolute value for C11
3. Calculate R11 and R21 using the standard 5% C11 value, f_{3dB} and desired gain

   R11 and R21 equations (C11 in pF and f_{3dB} in kHz)

$$R21 = \frac{159.2 \bullet 10^6}{C11 \bullet f_{3dB}}$$

$$R11 = \frac{R21}{Gain}$$

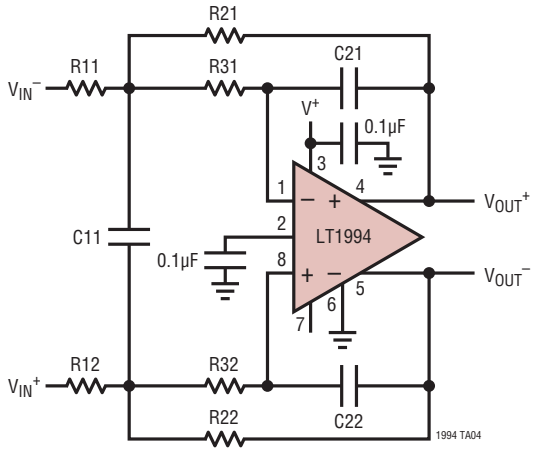
Example: The specified –3dB frequency is 1MHz Gain = 4

1. Using f_{3dB} = 1000kHz, $C11_{abs}$ = 400pF
2. Nearest standard 5% value to 400pF is 390pF and C11 = C12 = 390pF
3. Using f_{3dB} = 1000kHz, C11 = 390pF and Gain = 4, R21 = R22 = 412Ω and R11 = R12 = 102Ω (nearest 1% value)

Differential 2nd Order Butterworth Lowpass Filter

Maximum –3dB frequency (f_{3dB}) 1MHz

Stopband attenuation: –12dB at 2 • f_{3dB} and –28dB at 5 • f_{3dB}



Component Calculation:

R11 = R12, R21 = R22, R31 = R32, C21 = C22, C11 = 10 • C21, R1 = R11, R2 = R21, R3 = R31, C2 = C21 and C1 = C11

1. Calculate an absolute value for C2 ($C2_{abs}$) using a specified –3dB frequency

$$C2_{abs} = \frac{4 \bullet 10^5}{f_{3dB}} \; (C2_{abs} \text{ in pF and } f_{3dB} \text{ in kHz}) \text{ (Note 2)}$$

2. Select a standard 5% capacitor value nearest the absolute value for C2 (C1 = 10 • C2)

TYPICAL APPLICATIONS

3. Calculate R3, R2 and R1 using the standard 5% C2 value, the specified f_{3dB} and the specified passband gain (Gn)

$$f_{3dB} \le 1MHz \text{ and } Gain \le 8.8 \text{ or } Gain \le \frac{1MHz}{f_{3dB}}$$

R1, R2 and R3 equations (C2 in pF and f_{3dB} in kHz)

$$R3 = \frac{\left(1.121 - \sqrt{(1.131 - 0.127 \bullet Gn)}\right) \bullet 10^8}{(Gn+1) \bullet C2 \bullet f_{3dB}} \text{ (Note 1)}$$

$$R2 = \frac{1.266 \bullet 10^{15}}{R3 \bullet C2^2 \bullet f_{3dB}^{\ 2}}$$

$$R1 = \frac{R2}{Gn}$$

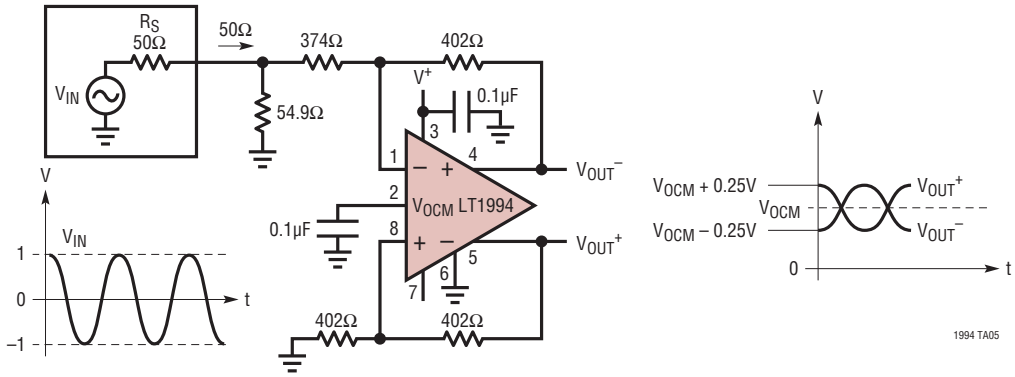
Example: The specified –3dB frequency is 1MHz Gain = 1

1. Using f_{3dB} = 1000kHz, $C2_{abs}$ = 400pF
2. Nearest standard 5% value to 400pF is 390pF and C21 = C22 = 390pF and C11 = 3900pF
3. Using f_{3dB} = 1000kHz, C2 = 390pF and Gain = 1, R1 = 549Ω, R2 = 549Ω and R3 = 15.4Ω (nearest 1% values). R11 = R21 = 549Ω, R21 = R22 = 549Ω and R31 = R32 = 15.4Ω.

Note 1: The equations for R1, R2, R3 are ideal and do not account for the finite gain bandwidth product (GBW) of the LT1994 (70MHz). The maximum gain is set by the C1/C2 ratio (which for convenience is set equal to ten).

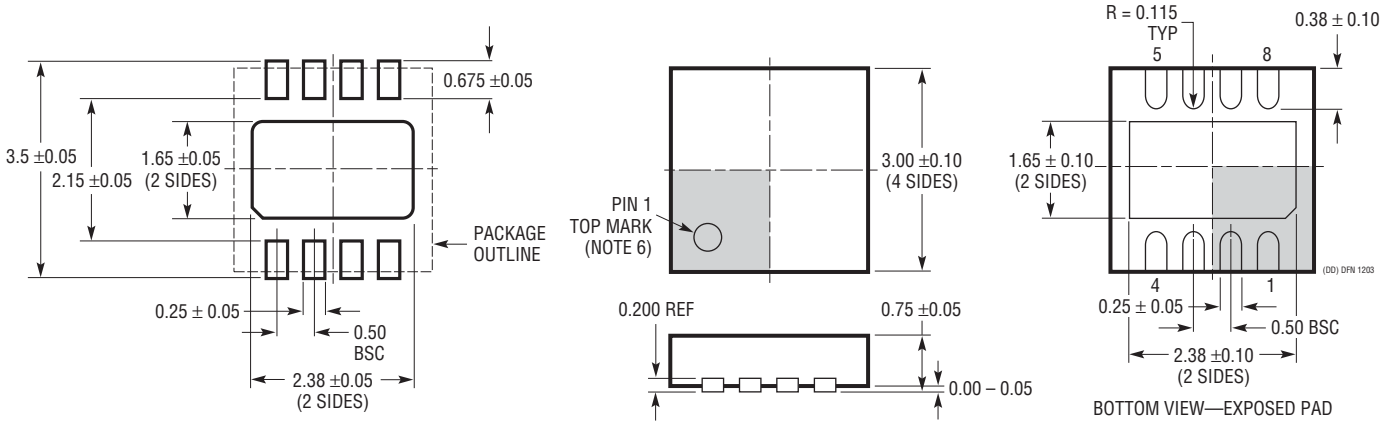
Note 2: The calculated value of a capacitor is chosen to produce input resistors less than 600Ω. If a higher value input resistance is required then multiply all resistor values and divide all capacitor values by the same number.

A Single-Ended to Differential Voltage Conversion with Source Impedance Matching and Level Shifting



PACKAGE DESCRIPTION

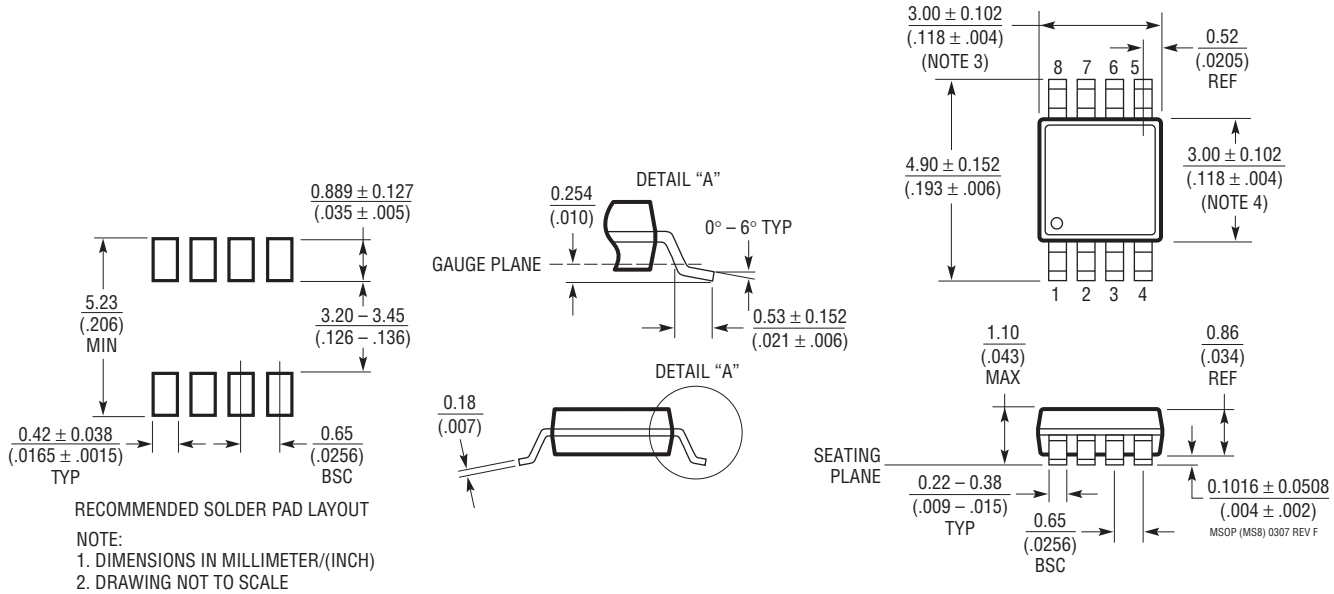
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)

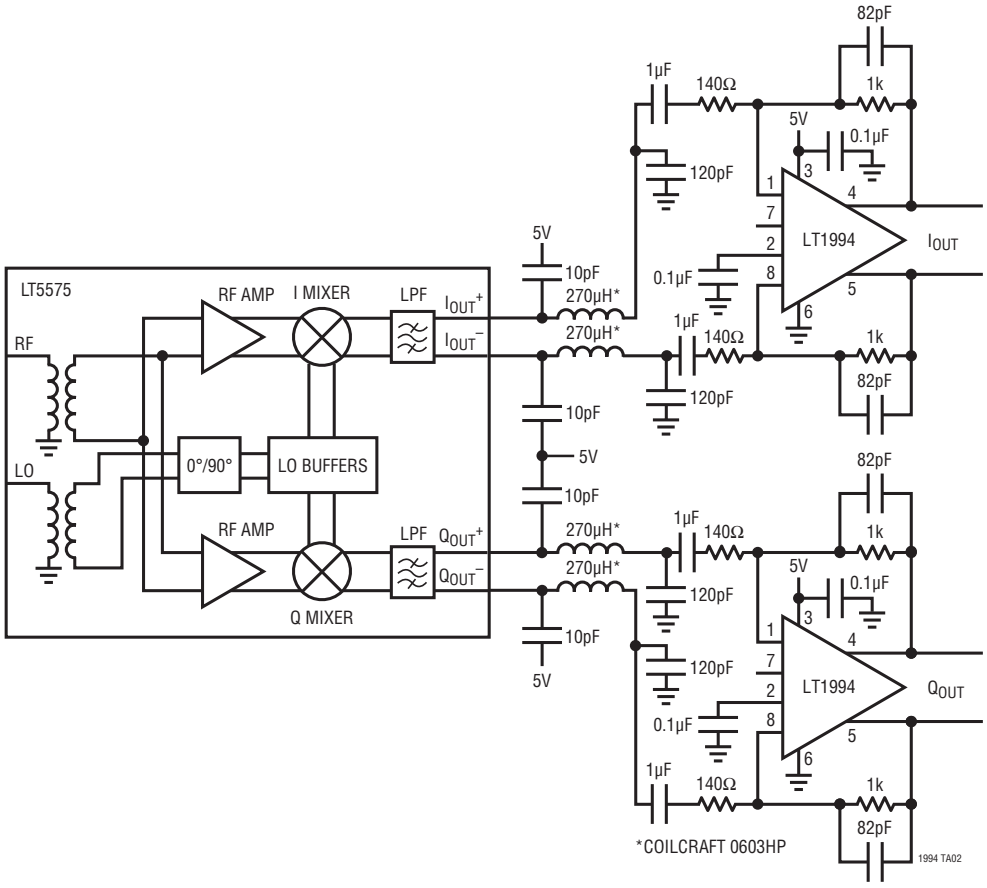


RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

RFID Receiver Front-End, 1kHz < –3dB BW < 2MHz
(Baseband Gain = 5)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1167	Precision, Instrumentation Amp	Single Gain Set Resistor: G = 1 to 10,000
LT1806/LT1807	Single/Dual Low Distortion Rail-to-Rail Amp	325MHz, 140V/µs Slew Rate, 3.5nV/√Hz Noise
LT1809/LT1810	Single/Dual Low Distortion Rail-to-Rail Amp	180MHz, 350V/µs Slew Rate, Shutdown
LT1990	High Voltage Gain Selectable Differential Amp	±250V Common Mode, Micropower, Gain = 1, 10
LT1991	Precision Gain Selectable Differential Amp	Micropower, Pin Selectable Gain = –13 to 14
LTC1992/LTC1992-x	Fully Differential Input/Output Amplifiers	Programmable Gain or Fixed Gain (G = 1, 2, 5, 10)
LT1993-2/-4/-10	Low Distortion and Noise, Differential In/Out	Fixed Gain (G = 2, 4, 10)
LT1995	High Speed Gain Selectable Differential Amp	30MHz, 1000V/µs, Pin Selectable Gain = –7 to 8
LT1996	Precision, 100µA, Gain Selectable Differential Amp	Pin Selectable Gain = 9 to 117
LTC6403	Low Noise, Low Power Fully Differential Amp	11mA Supply Current
LTC6404-1/LTC6404-2 LTC6404-4	600MHz AC Precision Fully Differential Amp	Available H-Grade (–40°C to 125°C)
LT6600-2.5/-5/-10/-15/-20	Differential Amp and Lowpass, Chebyshev Filter	Filter Cutoff = 2.5MHz, 5MHz, 10MHz, 15MHz or 20MHz

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 0309 REV B • PRINTED IN USA