70MHz, 1000V/µs Op Amp

FEATURES

- **70MHz Gain Bandwidth**
- **1000V/µs Slew Rate**
- **7.5mA Maximum Supply Current**
- 9nV/√Hz Input Noise Voltage
- Unity-Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 1.5mV Maximum Input Offset Voltage
- 2µA Maximum Input Bias Current
- 350nA Maximum Input Offset Current
- 50mA Minimum Output Current
- ±7.5V Minimum Output Swing into 150Ω
- 4.5V/mV Minimum DC Gain, R_L=1k
- 50ns Settling Time to 0.1%, 10V Step
- 0.06% Differential Gain, A_V=2, R_L=150Ω
- 0.04° Differential Phase, A_V=2, R_L=150Ω
- Specified at ±2.5V, ±5V, and ±15V

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

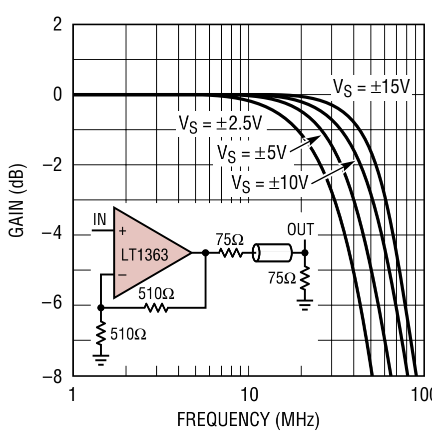
DESCRIPTION

The LT1363 is a high speed, very high slew rate operational amplifier with excellent DC performance. The LT1363 features reduced supply current, lower input offset voltage, lower input bias current and higher DC gain than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier. The amplifier is a single gain stage with outstanding settling characteristics which makes the circuit an ideal choice for data acquisition systems. The output drives a 150Ω load to ±7.5V with ±15V supplies and to ±3.4V on ±5V supplies. The amplifier is also capable of driving any capacitive load which makes it useful in buffer or cable driver applications.

The LT1363 is a member of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For dual and quad amplifier versions of the LT1363 see the LT1364/1365 data sheet. For 50MHz amplifiers with 4mA of supply current per amplifier see the LT1360 and LT1361/1362 data sheets. For lower supply current amplifiers with bandwidths of 12MHz and 25MHz see the LT1354 through LT1359 data sheets. Singles, duals, and quads of each amplifier are available.

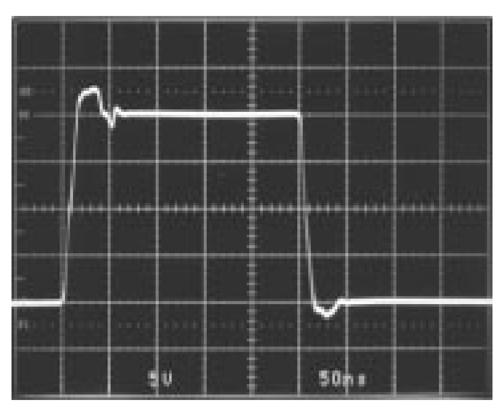
TYPICAL APPLICATION

Cable Driver Frequency Response



1363 TA01

A_V = –1 Large-Signal Response

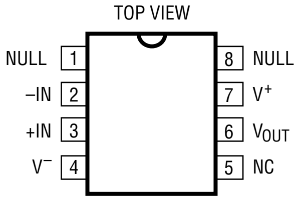


1363 TA02

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage
(Transient Only) (Note 2)................................. ±10V
Input Voltage ....$\pm V_S$
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 8) ...–40°C to 85°C
Specified Temperature Range (Note 9) ....–40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package .... 150°C
Storage Temperature Range ....–65°C to 150°C
Lead Temperature (Soldering, 10 sec).................. 300°C

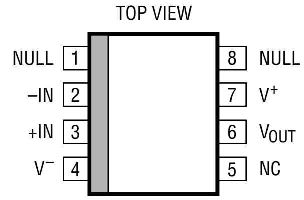
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1363CN8



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1363CS8
S8 PART MARKING
1363

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)	±15V		0.5	1.5	mV
			±5V		0.5	1.5	mV
			±2.5V		0.7	1.8	mV
I_{OS}	Input Offset Current		±2.5V to ±15V		120	350	nA
I_B	Input Bias Current		±2.5V to ±15V		0.6	2.0	µA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		9		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		1		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	12	50		MΩ
	Input Resistance	Differential	±15V		5		MΩ
C_{IN}	Input Capacitance		±15V		3		pF
	Input Voltage Range⁺		±15V	12.0	13.4		V
			±5V	2.5	3.4		V
			±2.5V	0.5	1.1		V
	Input Voltage Range⁻		±15V		–13.2	–12.0	V
			±5V		–3.2	–2.5	V
			±2.5V		–0.9	–0.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V	±15V	84	90		dB
		V_{CM} = ±2.5V	±5V	76	81		dB
		V_{CM} = ±0.5V	±2.5V	66	71		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		90	100		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k	±15V	4.5	9.0		V/mV
		V_{OUT} = ±10V, R_L = 500Ω	±15V	3.0	6.5		V/mV
		V_{OUT} = ±7.5V, R_L = 150Ω	±15V	2.0	3.8		V/mV
		V_{OUT} = ±2.5V, R_L = 500Ω	±5V	3.0	6.4		V/mV
		V_{OUT} = ±2.5V, R_L = 150Ω	±5V	2.0	5.6		V/mV
		V_{OUT} = ±1V, R_L = 500Ω	±2.5V	2.5	5.2		V/mV

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$ $R_L = 150Ω$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$	±15V ±15V ±5V ±5V ±2.5V	13.5 13.0 3.5 3.4 1.3	14.0 13.7 4.1 3.8 1.7		±V ±V ±V ±V ±V
I_{OUT}	Output Current	$V_{OUT} = ±7.5V$ $V_{OUT} = ±3.4V$	±15V ±5V	50 23	60 29		mA mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = ±3V$	±15V	70	105		mA
SR	Slew Rate	$A_V = –2$, (Note 5)	±15V ±5V	750 300	1000 450		V/µs V/µs
	Full Power Bandwidth	10V Peak, (Note 6) 3V Peak, (Note 6)	±15V ±5V		15.9 23.9		MHz MHz
GBW	Gain Bandwidth	f = 1MHz	±15V ±5V ±2.5V		70 50 40		MHz MHz MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	±15V ±5V		2.6 3.6		ns ns
	Overshoot	$A_V = 1$, 0.1V	±15V ±5V		36 23		% %
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V ±5V		4.6 5.6		ns ns
t_s	Settling Time	10V Step, 0.1%, $A_V = –1$ 10V Step, 0.01%, $A_V = –1$ 5V Step, 0.1%, $A_V = –1$	±15V ±15V ±5V		50 80 55		ns ns ns
	Differential Gain	f = 3.58MHz, $A_V = 2$, $R_L = 150Ω$ f = 3.58MHz, $A_V = 2$, $R_L = 1k$	±15V ±5V ±15V ±5V		0.03 0.06 0.01 0.01		% % % %
	Differential Phase	f = 3.58MHz, $A_V = 2$, $R_L = 150Ω$ f = 3.58MHz, $A_V = 2$, $R_L = 1k$	±15V ±5V ±15V ±5V		0.10 0.04 0.05 0.25		Deg Deg Deg Deg
R_O	Output Resistance	$A_V = 1$, f = 1MHz	±15V		0.7		Ω
I_S	Supply Current		±15V ±5V		6.3 6.0	7.5 7.2	mA mA

The ● denotes the specifications which apply over the temperature range $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)	±15V ±5V ±2.5V	● ● ●			2.0 2.0 2.2	mV mV mV
	Input V_{OS} Drift	(Note 7)	±2.5V to ±15V	●		10	13	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			500	nA
I_B	Input Bias Current		±2.5V to ±15V	●			3	µA
CMRR	Common Mode Rejection Ratio	$V_{CM} = ±12V$ $V_{CM} = ±2.5V$ $V_{CM} = ±0.5V$	±15V ±5V ±2.5V	● ● ●	82 74 64			dB dB dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $0°C \le T_A \le 70°C$, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		●	88			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k V_{OUT} = ±10V, R_L = 500Ω V_{OUT} = ±2.5V, R_L = 500Ω V_{OUT} = ±2.5V, R_L = 150Ω V_{OUT} = ±1V, R_L = 500Ω	±15V ±15V ±5V ±5V ±2.5V	● ● ● ● ●	3.6 2.4 2.4 1.5 2.0			V/mV V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV R_L = 150Ω, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV	±15V ±15V ±5V ±5V ±2.5V	● ● ● ● ●	13.4 12.8 3.4 3.3 1.2			±V ±V ±V ±V ±V
I_{OUT}	Output Current	V_{OUT} = ±12.8V V_{OUT} = ±3.3V	±15V ±5V	● ●	25 22			mA mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	●	55			mA
SR	Slew Rate	A_V = –2, (Note 5)	±15V ±5V	● ●	600 225			V/µs V/µs
I_S	Supply Current		±15V ±5V	● ●			8.7 8.4	mA mA

The ● denotes the specifications which apply over the temperature range $-40°C \le T_A \le 85°C$, V_{CM} = 0V unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)	±15V ±5V ±2.5V	● ● ●			2.5 2.5 2.7	mV mV mV
	Input V_{OS} Drift	(Note 7)	±2.5V to ±15V	●		10	13	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			600	nA
I_B	Input Bias Current		±2.5V to ±15V	●			3.6	µA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V V_{CM} = ±2.5V V_{CM} = ±0.5V	±15V ±5V ±2.5V	● ● ●	82 74 64			dB dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		●	87			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k V_{OUT} = ±10V, R_L = 500Ω V_{OUT} = ±2.5V, R_L = 500Ω V_{OUT} = ±2.5V, R_L = 150Ω V_{OUT} = ±1V, R_L = 500Ω	±15V ±15V ±5V ±5V ±2.5V	● ● ● ● ●	2.5 1.5 1.5 1.0 1.3			V/mV V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	R_L = 1kΩ, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV R_L = 150Ω, V_{IN} = ±40mV R_L = 500Ω, V_{IN} = ±40mV	±15V ±15V ±5V ±5V ±2.5V	● ● ● ● ●	13.4 12.7 3.4 3.2 1.2			±V ±V ±V ±V ±V
I_{OUT}	Output Current	V_{OUT} = ±12.7V V_{OUT} = ±3.2V	±15V ±5V	● ●	25 21			mA mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	●	50			mA
SR	Slew Rate	A_V = –2, (Note 5)	±15V ±5V	● ●	550 180			V/µs V/µs
I_S	Supply Current		±15V ±5V	● ●			9.0 8.7	mA mA

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Differential inputs of ±10V are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more details.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Input offset voltage is pulse tested and is exclusive of warm-up drift.

Note 5: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±2V on the output with ±1.75V input for ±5V supplies.

Note 6: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_P$.

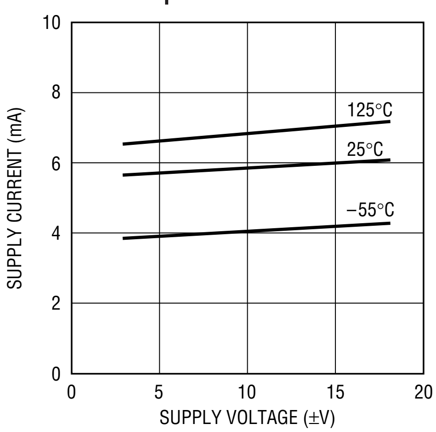
Note 7: This parameter is not 100% tested.

Note 8: The LT1363C is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 9: The LT1363C is guaranteed to meet specified performance from 0°C to 70°C. The LT1363C is designed, characterized and expected to meet specified performance from –40°C to 85°C, but is not tested or QA sampled at these temperatures. For guaranteed I-grade parts, consult the factory.

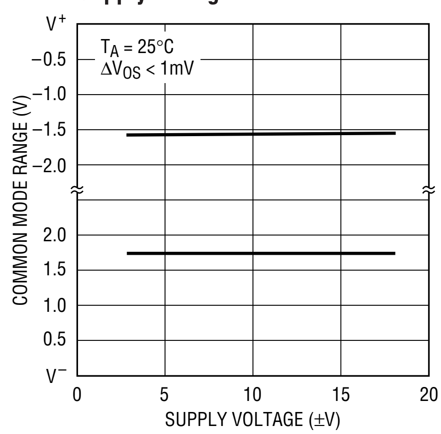
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage and Temperature



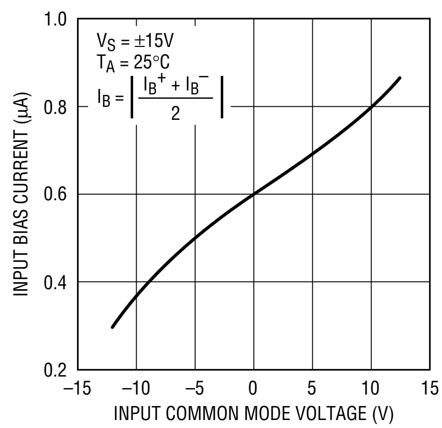
1363 G01

Input Common Mode Range vs Supply Voltage



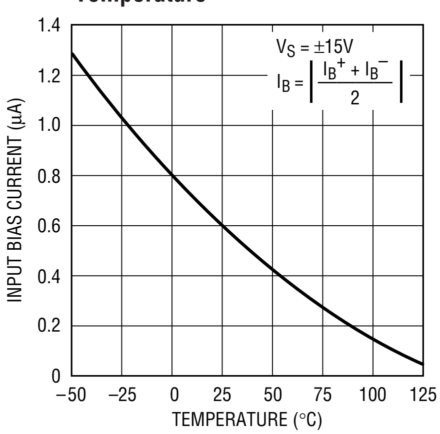
1363 G02

Input Bias Current vs Input Common Mode Voltage



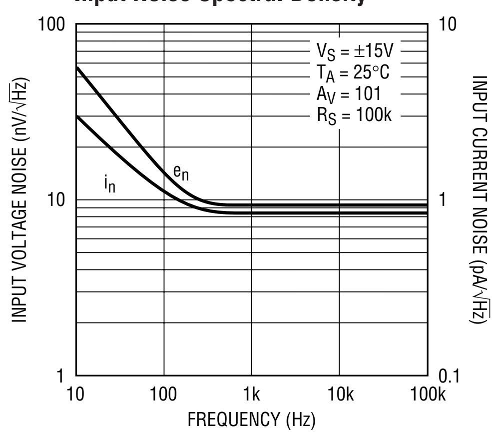
1363 G03

Input Bias Current vs Temperature



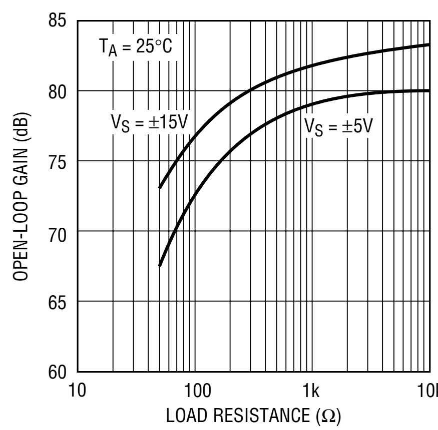
1363 G04

Input Noise Spectral Density



1363 G05

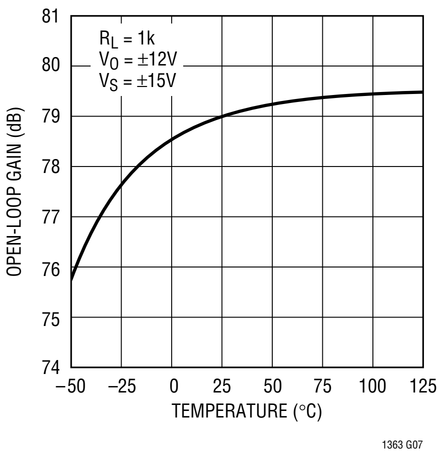
Open-Loop Gain vs Resistive Load



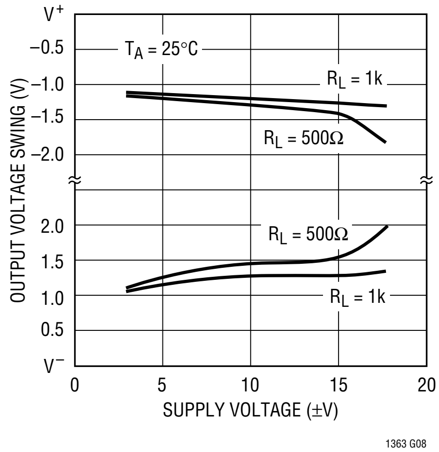
1363 G06

TYPICAL PERFORMANCE CHARACTERISTICS

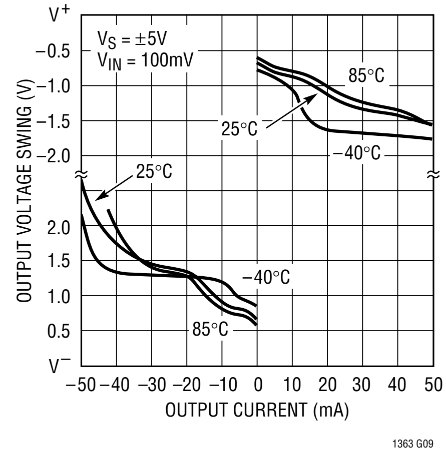
Open-Loop Gain vs Temperature



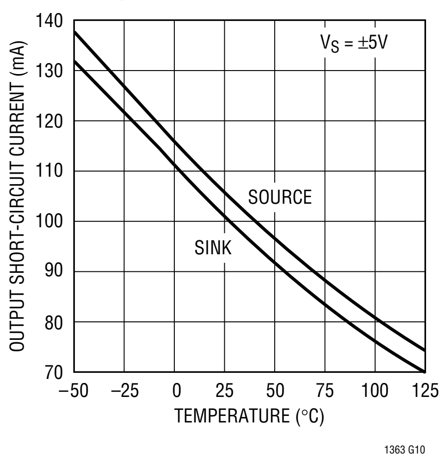
Output Voltage Swing vs Supply Voltage



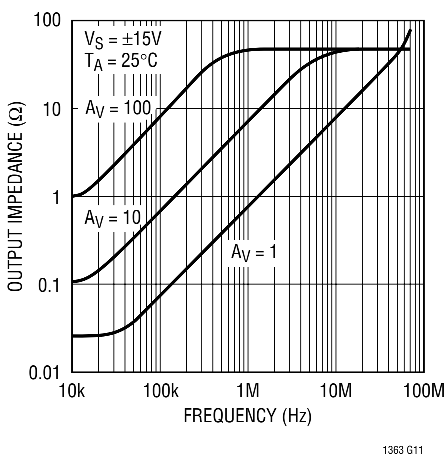
Output Voltage Swing vs Load Current



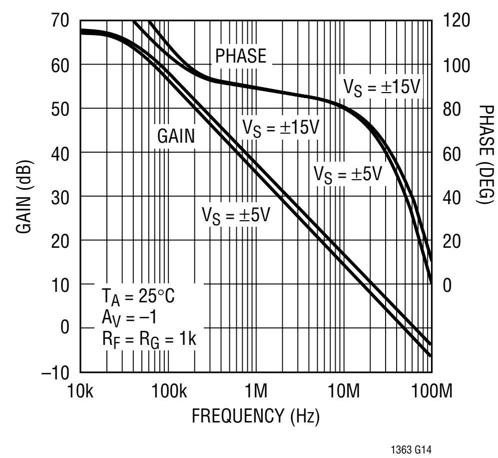
Output Short-Circuit Current vs Temperature



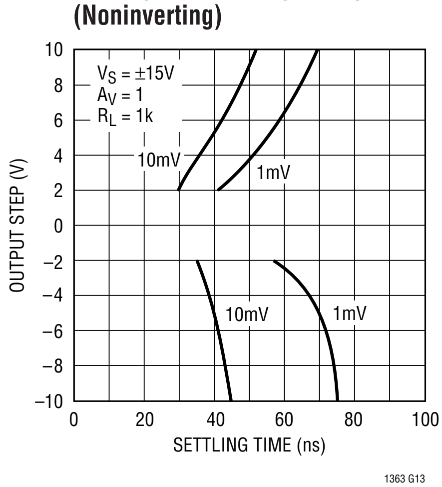
Output Impedance vs Frequency



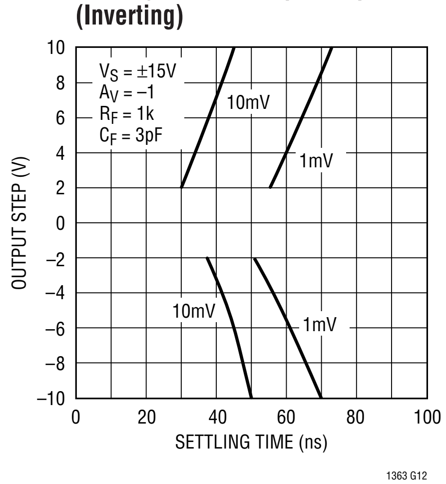
Gain and Phase vs Frequency



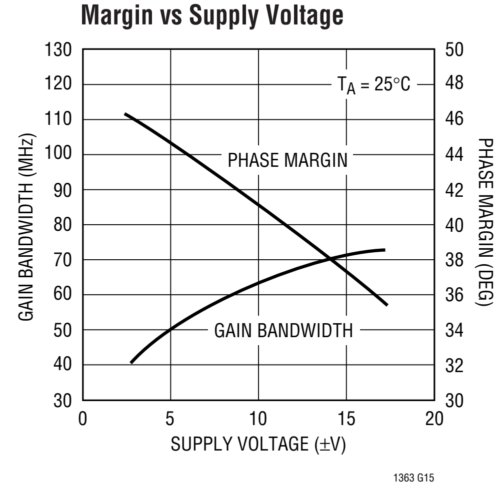
Settling Time vs Output Step (Noninverting)



Settling Time vs Output Step (Inverting)

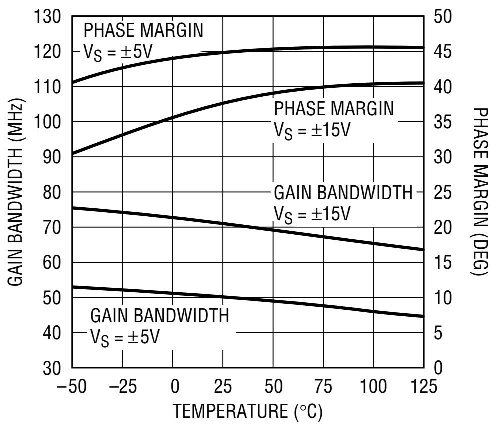


Gain Bandwidth and Phase Margin vs Supply Voltage



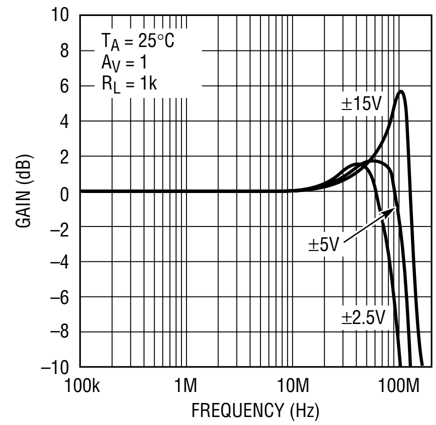
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Bandwidth and Phase Margin vs Temperature



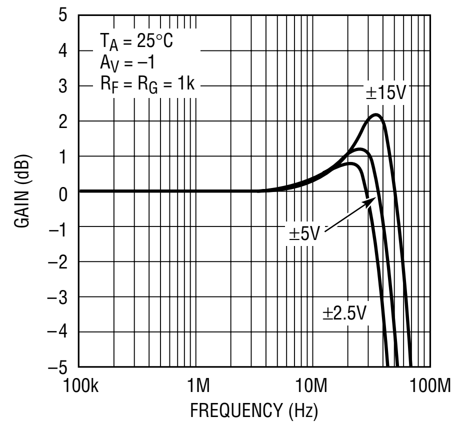
1363 G16

Frequency Response vs Supply Voltage (A_V = 1)



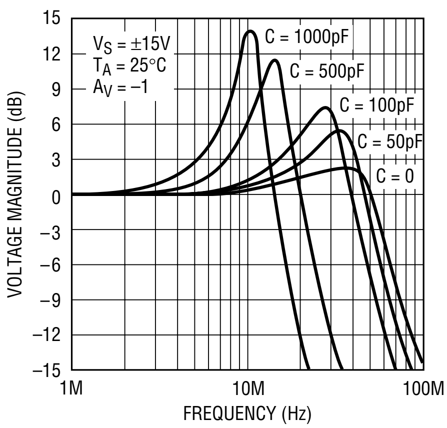
1363 G17

Frequency Response vs Supply Voltage (A_V = –1)



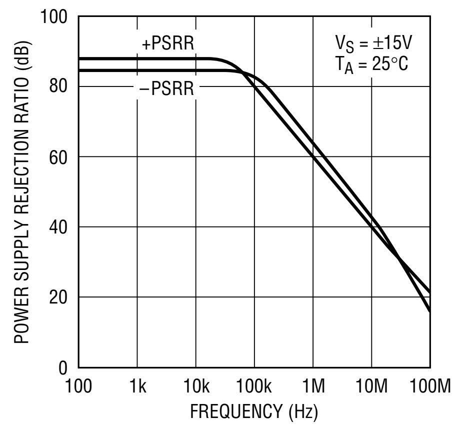
1363 G18

Frequency Response vs Capacitive Load



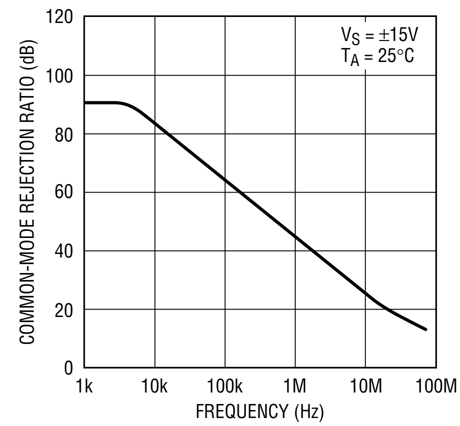
1363 G19

Power Supply Rejection Ratio vs Frequency



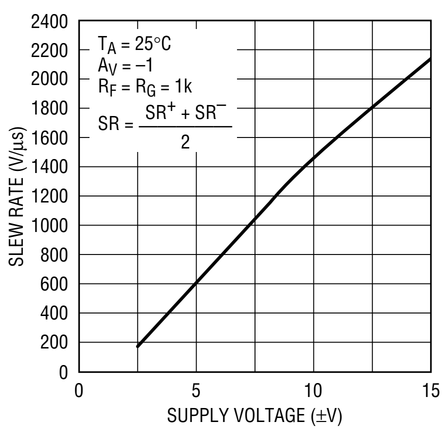
1363 G20

Common Mode Rejection Ratio vs Frequency



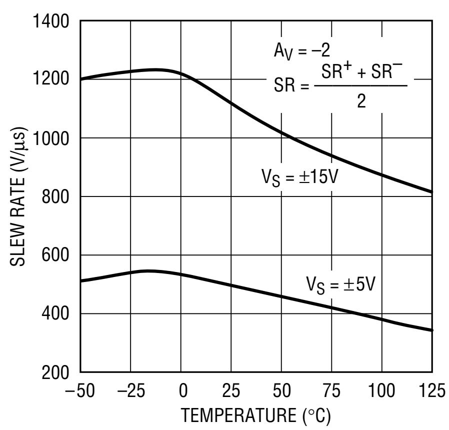
1363 G21

Slew Rate vs Supply Voltage



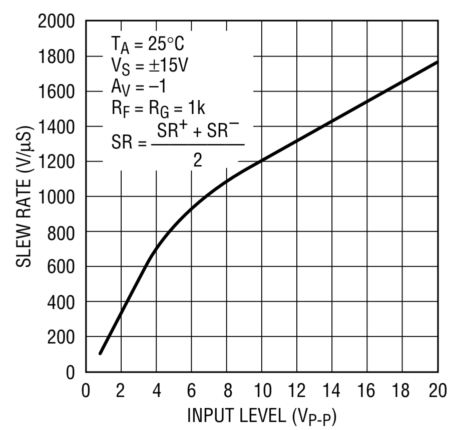
1363 G22

Slew Rate vs Temperature



1363 G23

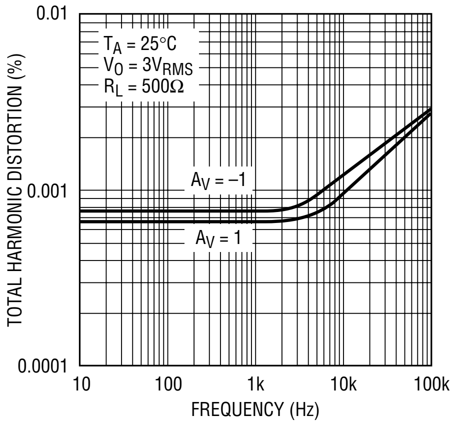
Slew Rate vs Input Level



1363 G24

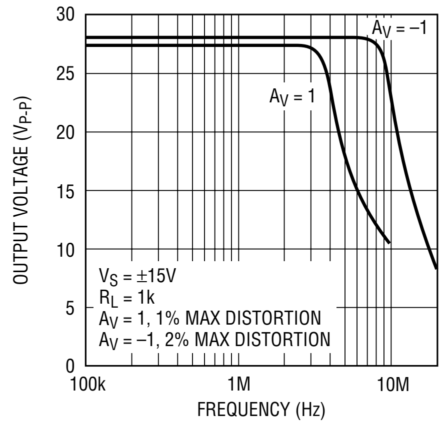
TYPICAL PERFORMANCE CHARACTERISTICS

Total Harmonic Distortion vs Frequency



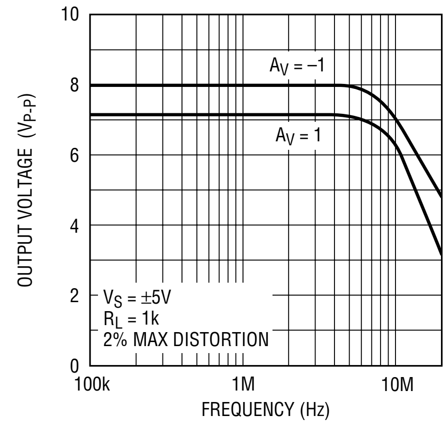
1363 G25

Undistorted Output Swing vs Frequency (±15V)



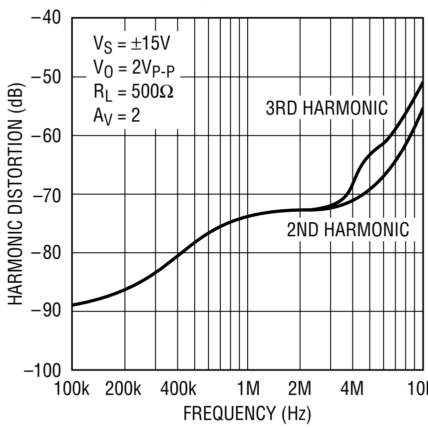
1363 G26

Undistorted Output Swing vs Frequency (±5V)



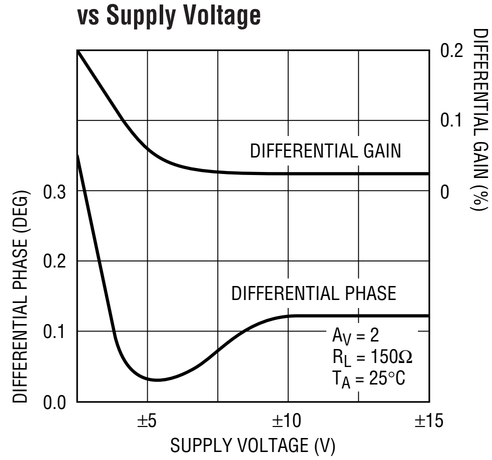
1363 G27

2nd and 3rd Harmonic Distortion vs Frequency



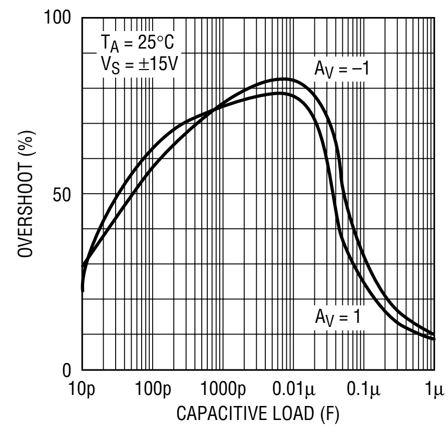
1363 G28

Differential Gain and Phase vs Supply Voltage



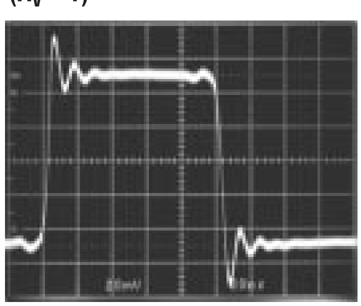
1363 G29

Capacitive Load Handling



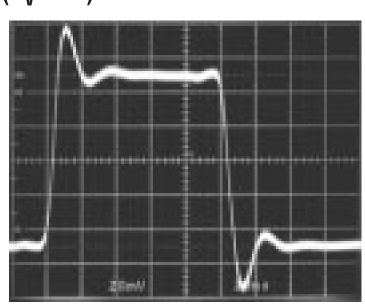
1363 G30

Small-Signal Transient ($A_V = 1$)



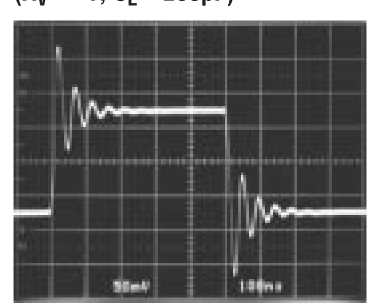
1363 TA31

Small-Signal Transient ($A_V = –1$)



1363 TA32

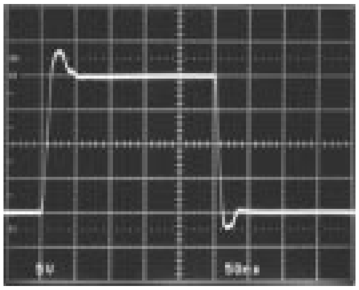
Small-Signal Transient ($A_V = –1$, $C_L = 200pF$)



1363 TA33

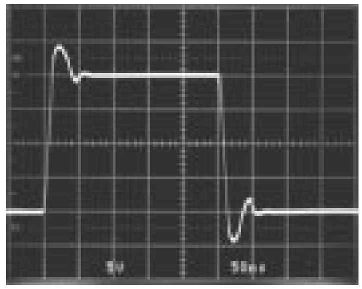
TYPICAL PERFORMANCE CHARACTERISTICS

Large-Signal Transient ($A_V = 1$)



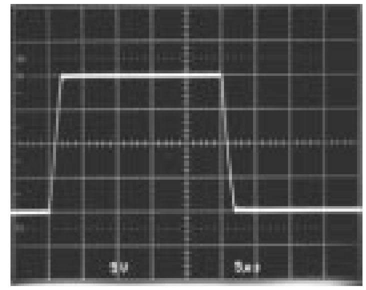
1363 TA34

Large-Signal Transient ($A_V = –1$)



1363 TA35

Large-Signal Transient ($A_V = 1$, $C_L = 10,000pF$)

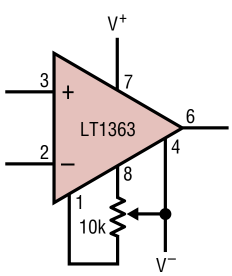


1363 TA36

APPLICATIONS INFORMATION

The LT1363 may be inserted directly into AD817, AD847, EL2020, EL2044, and LM6361 applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1363 is shown below.

Offset Nulling



1363 AI01

Layout and Passive Components

The LT1363 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or oscillations. For feedback resistors greater than 5kΩ, a parallel capacitor of value

$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1363 is stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves.The photo of the small-signal response with 200pF load shows 62% peaking. The large-signal response with a 10,000pF load shows the output slew rate being limited to 10V/µs by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground. The response of a cable driver in a gain of 2 driving a 75Ω cable is shown on the front page of the data sheet.

APPLICATIONS INFORMATION

Input Considerations

Each of the LT1363 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on NPN/PNP beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

The inputs can withstand transient differential input voltages up to 10V without damage and need no clamping or source resistance for protection. Differential inputs, however, generate large supply currents (tens of mA) as required for high slew rates. If the device is used with sustained differential inputs, the average supply current will increase, excessive power dissipation will result and the part may be damaged. **The part should not be used as a comparator, peak detector or other open-loop application with large, sustained differential inputs**. Under normal, closed-loop operation, an increase of power dissipation is only noticeable in applications with large slewing outputs and is proportional to the magnitude of the differential input voltage and the percent of the time that the inputs are apart. Measure the average supply current for the application in order to calculate the power dissipation.

Single Supply Operation

The LT1363 is specified at ±15V, ±5V, and ±2.5V supplies, but it is also well suited to single supply operation down to a single 5V supply. The symmetrical input Ccmmon mode range and output swing make the device well suited for applications with a single supply if the the input and output swing ranges are centered (i.e., a DC bias of 2.5V on the input and the output). For 5V video applications with an assymetrical swing, an offset of 2V on the input works best.

Power Dissipation

The LT1363 combines high speed and large output drive in a small package. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1363CN8: $T_J = T_A + (P_D \times 130°C/W)$
LT1363CS8: $T_J = T_A + (P_D \times 190°C/W)$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

Example: LT1363CS8 at 70°C, $V_S = \pm15V$, $R_L = 390\Omega$

$$P_{DMAX} = (30V)(8.7mA) + (7.5V)^2/390\Omega = 405mW$$

$$T_{JMAX} = 70°C + (405mW)(190°C/W) = 147°C$$

Circuit Operation

The LT1363 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1363 is tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

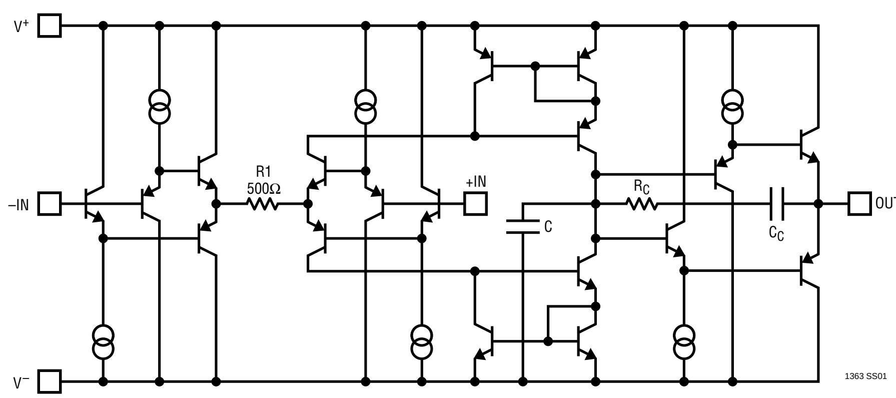
APPLICATIONS INFORMATION

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity-gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

Comparison to Current Feedback Amplifiers

The LT1363 enjoys the high slew rates of Current Feedback Amplifiers (CFAs) while maintaining the characteristics of a true voltage feedback amplifier. The primary differences are that the LT1363 has two high impedance inputs and its closed loop bandwidth decreases as the gain increases. CFAs have a low impedance inverting input and maintain relatively constant bandwidth with increasing gain. The LT1363 can be used in all traditional op amp configurations including integrators and applications such as photodiode amplifiers and I-to-V converters where there may be significant capacitance on the inverting input. The frequency compensation is internal and not dependent on the value of the feedback resistor. For CFAs, the feedback resistance is fixed for a given bandwidth and capacitance on the inverting input can cause peaking or oscillations. The slew rate of the LT1363 in noninverting gain configurations is also superior in most cases.

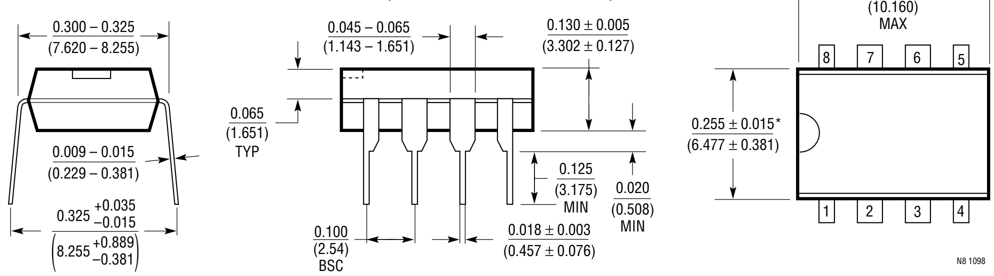
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

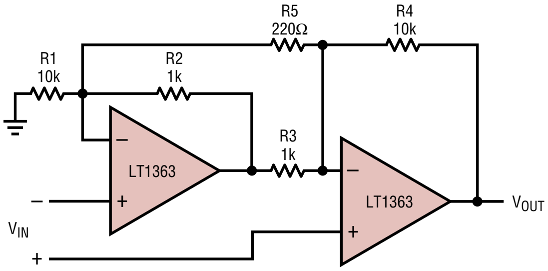
N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

TYPICAL APPLICATIONS

Two Op Amp Instrumentation Amplifier

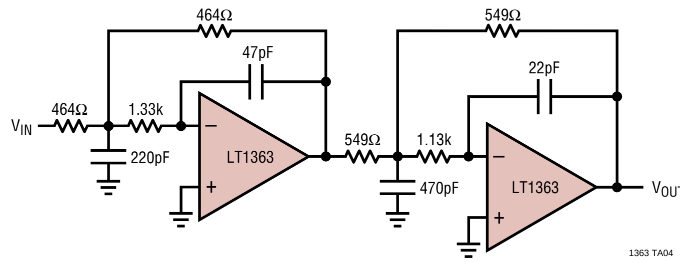


$$GAIN = \left[\frac{R4}{R3}\right]\left[1 + \left(\frac{1}{2}\right)\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{(R2 + R3)}{R5}\right] = 102$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 700kHz

1363 TA03

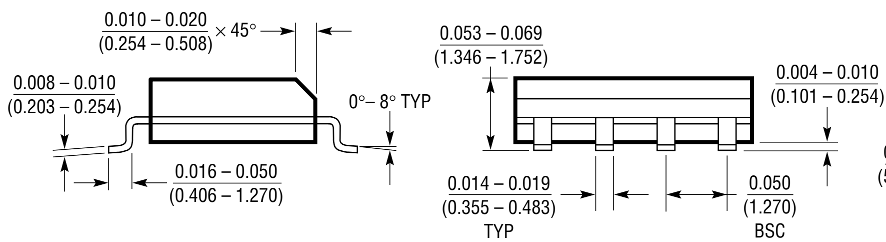
2MHz, 4th Order Butterworth Filter

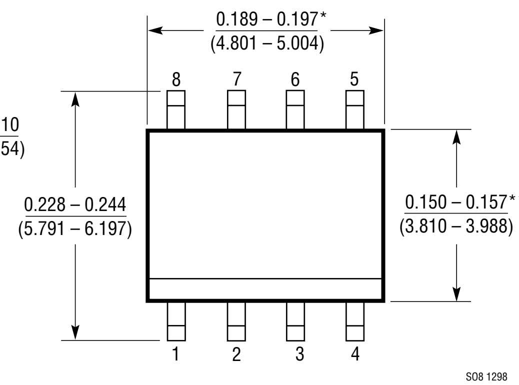


PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)





*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1364/LT1365	Dual and Quad 70MHz, 1000V/µs Op Amps	Dual and Quad Versions of LT1363
LT1360	50MHz, 800V/µs Op Amp	Lower Power Version of LT1363, V_{OS} = 1mV, I_S = 4mA
LT1357	25MHz, 600V/µs Op Amp	Lower Power Version of LT1363, V_{OS} = 0.6mV, I_S = 2mA
LT1812	100MHz, 750V/µs Op Amp	Low Voltage, Low Power LT1363, V_{OS} = 1.5mV, I_S = 3mA

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