ANALOG DEVICES | POWER BY LINEAR

LT1241 Series

High Speed Current Mode Pulse Width Modulators

FEATURES

- **Low Start-Up Current: < 250µA**
- **50ns Current Sense Delay**
- **Current Mode Operation: To 500kHz**
- **Pin Compatible with UC1842 Series**
- Undervoltage Lockout with Hysteresis
- No Cross-Conduction Current
- Trimmed Bandgap Reference
- 1A Totem Pole Output
- Trimmed Oscillator Frequency and Sink Current
- Active Pull-Down on Reference and Output During Undervoltage Lockout
- High Level Output Clamp: 18V
- Current Sense Leading Edge Blanking

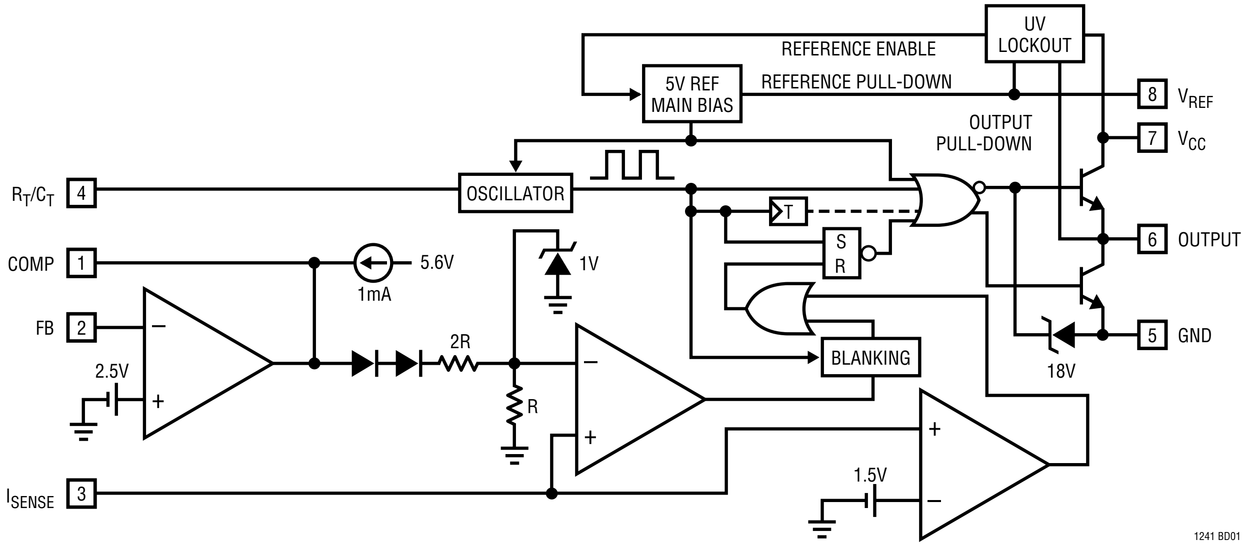
APPLICATIONS

- Off-Line Converters
- DC/DC Converters

DESCRIPTION

The LT®1241 series devices are 8-pin, fixed frequency, current mode, pulse width modulators. They are improved plug compatible versions of the industry standard UC1842 series. These devices have both improved speed and lower quiescent current. The LT1241 series is optimized for off-line and DC/DC converter applications. They contain a temperature-compensated reference, high gain error amplifier, current sensing comparator and a high current totem pole output stage ideally suited to driving power MOSFETs. Start-up current has been reduced to less than 250µA. Cross-conduction current spikes in the output stage have been eliminated, making 500kHz operation practical. Several new features have been incorporated. Leading edge blanking has been added to the current sense comparator. Trims have been added to the oscillator circuit for both frequency and sink current, and both of these parameters are tightly specified. The output stage is clamped to a maximum V_{OUT} of 18V in the on state. The output and the reference output are actively pulled low during undervoltage lockout.

BLOCK DIAGRAM



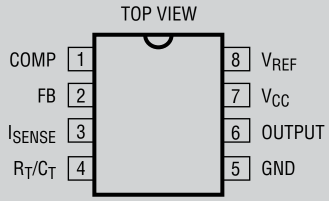
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	25V
Output Current	±1A*
Output Energy (Capacitive Load per Cycle)	5µJ
Analog Inputs (Pins 2, 3)	–0.3 to 6V
Error Amplifier Output Sink Current	10mA
Power Dissipation at $T_A \le 25°C$	1W

Operating Junction Temperature Range	
LT124XC	0°C to 100°C
LT124XI	–40°C to 100°C
LT124XM **(Obsolete)**	–55°C to 125°C
Storage Temperature Range	– 65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

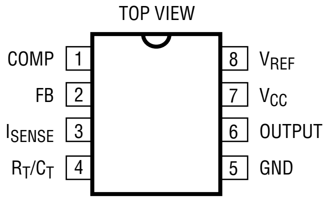
*The 1A rating for output current is based on transient switching requirements.

PIN CONFIGURATION

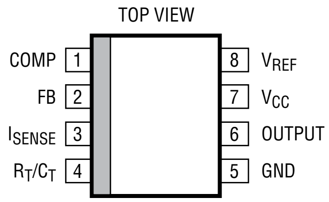


J8 PACKAGE 8-LEAD CERDIP
T_{JMAX} = 125°C, θ_{JA} = 100°C/W

OBSOLETE PACKAGE



N8 PACKAGE 8-LEAD PDIP
T_{JMAX} = 100°C, θ_{JA} = 130°C/W



S8 PACKAGE 8-LEAD PLASTIC SO
T_{JMAX} = 100°C, θ_{JA} = 150°C/W

ORDER INFORMATION http://www.linear.com/product/LT1241#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
OBSOLETE PACKAGE				
LT124XCJ8#PBF	LT124XCJ8#TRPBF	124X	8-Lead CERDIP	0°C to 100°C
LT124XCN8#PBF	LT124XCN8#TRPBF	124X	8-Lead PDIP	0°C to 100°C
LT124XCS8#PBF	LT124XCS8#TRPBF	124X	8-Lead Plastic SO	0°C to 100°C
LT124XIN8#PBF	LT124XIN8#TRPBF	124XI	8-Lead PDIP	–40°C to 125°C
LT124XIS8#PBF	LT124XIS8#TRPBF	124XI	8-Lead Plastic SO	–40°C to 125°C
OBSOLETE PACKAGE				
LT124XMJ8#PBF	LT124XMJ8#TRPBF		8-Lead CERDIP	–55°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 2 and 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Section						
Output Voltage	I_O = 1mA, T_J = 25°C		4.925	5.000	5.075	V
Line Regulation	12V < V_{CC} < 25V	●		3	20	mV
Load Regulation	1mA < I_{VREF} < 20mA	●		–6	–25	mV
Temperature Stability				0.1		mV/°C
Total Output Variation	Line, Load, Temp	●	4.87		5.13	V
Output Noise Voltage	10Hz < F < 10kHz, T_J = 25°C			50		µV
Long Term Stability	T_A = 125°C, 1000 Hrs			5	25	mV
Output Short-Circuit Current		●	–30	–90	–180	mA
Oscillator Section						
Initial Accuracy	R_T = 10k, C_T = 3.3nF, T_J = 25°C		47.5	50	52.5	kHz
	R_T = 13.0k, C_T = 500pF, T_J = 25°C		228	248	268	kHz
Voltage Stability	12V < V_{CC} < 25V, T_J = 25°C				1	%
Temperature Stability	T_{MIN} < T_J < T_{MAX}			–0.05		%/°C
Amplitude	T_J = 25°C (Pin 4)			1.7		V
Clock Ramp Reset Current	V_{OSC} (Pin 4) = 2V, T_J = 25°C		7.9	8.2	8.5	mA
Error Amplifier Section						
Feedback Pin Input Voltage	V_{PIN1} = 2.5V	●	2.42	2.50	2.58	V
Input Bias Current	V_{FB} = 2.5V	●			–2	µA
Open-Loop Voltage Gain	2 < V_O < 4V	●	65	90		dB
Unity-Gain Bandwidth	T_J = 25°C		0.7	1.3	2	MHz
Power Supply Rejection Ratio	12V < V_{CC} < 25V	●	60			dB
Output Sink Current	V_{PIN2} = 2.7V, V_{PIN1} = 1.1V	●	2	6		mA
Output Source Current	V_{PIN2} = 2.3V, V_{PIN1} = 5V	●	–0.5	–0.75		mA
Error Amplifier Section						
Output Voltage High Level	V_{PIN2} = 2.3V, R_L = 15k to GND	●	5	5.6		V
Output Voltage Low Level	V_{PIN2} = 2.7V, R_L = 15k to Pin 8	●		0.2	1.1	V
Current Sense Section						
Gain		●	2.85	3.00	3.15	V/V
Maximum Current Sense Input Threshold	V_{PIN3} < 1.1V	●	0.90	1.00	1.10	V
Power Supply Rejection Ratio		●		70		dB
Input Bias Current		●		–1	10	µA
Delay to Output		●		50	100	ns
Blanking Time				100		ns
Blanking Override Voltage				1.5		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 2 and 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Section						
Output Low Level	I_{OUT} = 20mA	●		0.25	0.4	V
	I_{OUT} = 200mA	●		0.75	2.2	V
Output High Level	I_{OUT} = 20mA	●	12.0			V
	I_{OUT} = 200mA	●	11.75			V
Rise Time	C_L = 1nF, T_J = 25°C			50	80	ns
Fall Time	C_L = 1.0nF, T_J = 25°C			30	60	ns
Output Clamp Voltage	I_O = 1mA	●		18	19.5	V
Undervoltage Lockout						
Start-Up Threshold						
LT1241		●	9.0	9.6	10.2	V
LT1242/LT1244		●	15	16	17	V
LT1243/LT1245		●	7.8	8.4	9.0	V
Minimum Operating Voltage						
LT1241/LT1243/LT1245		●	7.0	7.6	8.2	V
LT1242/LT1244		●	9.0	10	11	V
Hysteresis						
LT1241			1.6	2.0		V
LT1242/LT1244			5.5	6.0		V
LT1243/LT1245			0.4	0.8		V
PWM						
Maximum Duty Cycle						
LT1241/LT1244/LT1245	T_J = 25°C		46	48		%
LT1242/LT1243	T_J = 25°C		94	96		%
Minimum Duty Cycle		●		0		%
Total Device						
Start-Up Current		●		170	250	μA
Operating Current		●		7	10	mA

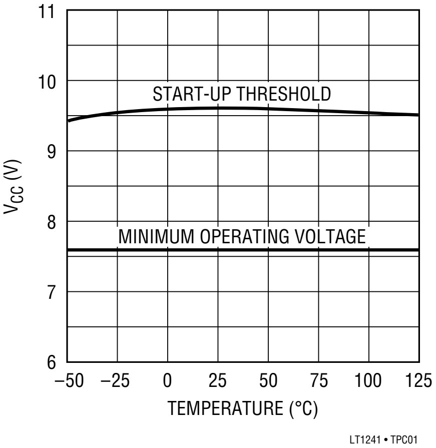
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise specified, V_{CC} = 15V, R_T = 10k, C_T = 3.3nF.

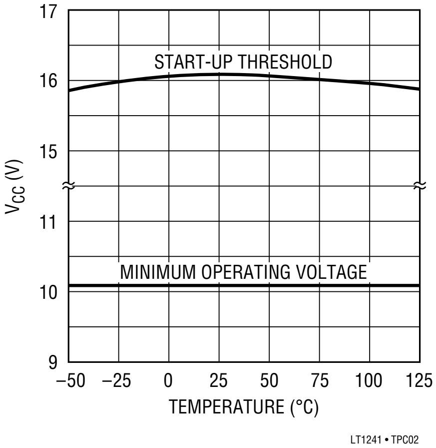
Note 3: Low duty cycle pulse techniques are used during test to maintain junction temperature close to ambient.

TYPICAL PERFORMANCE CHARACTERISTICS

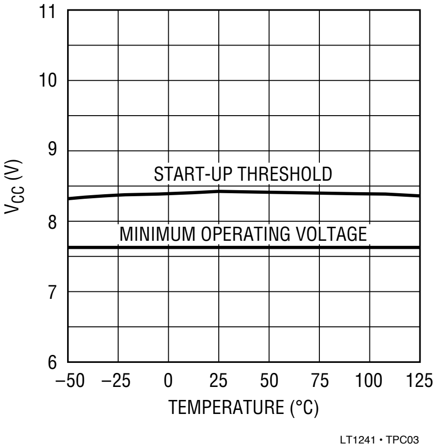
Undervoltage Lockout – LT1241



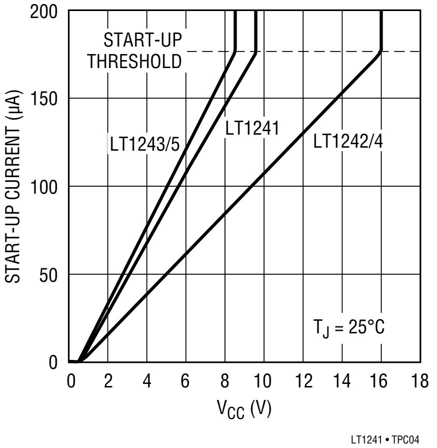
Undervoltage Lockout – LT1242, LT1244



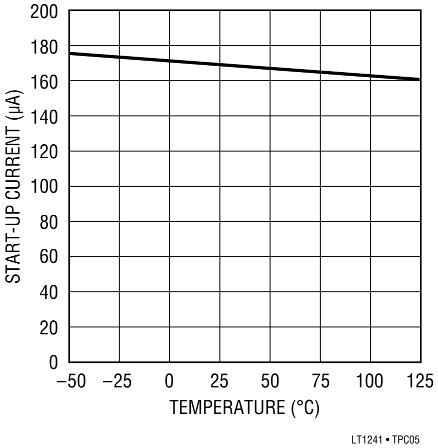
Undervoltage Lockout – LT1243, LT1245



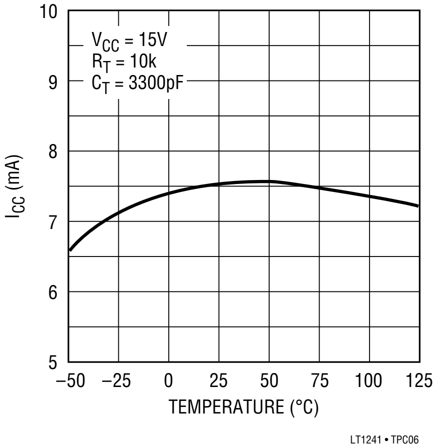
Start-Up Current



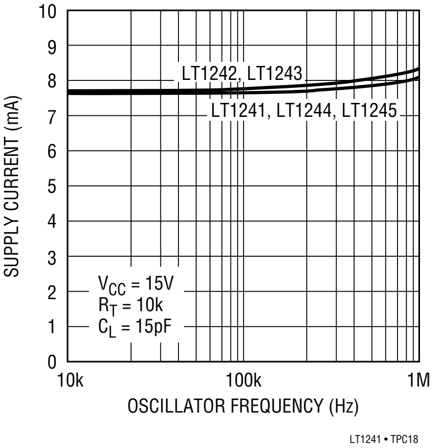
Start-Up Current



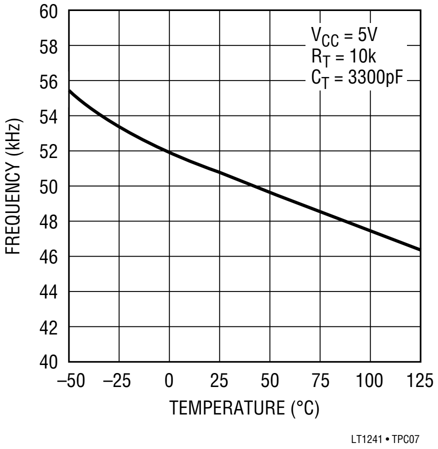
Supply Current



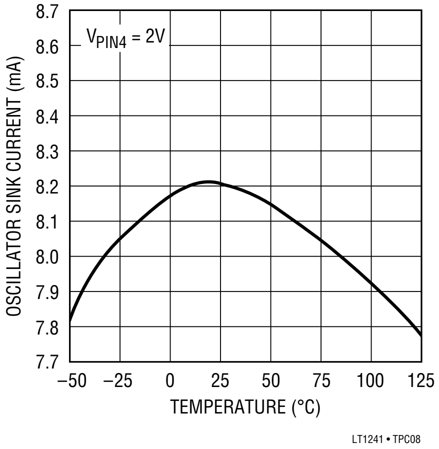
Supply Current vs Oscillator Frequency



Oscillator Frequency

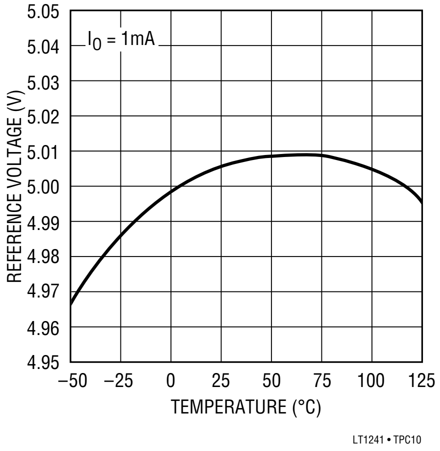


Oscillator Sink Current

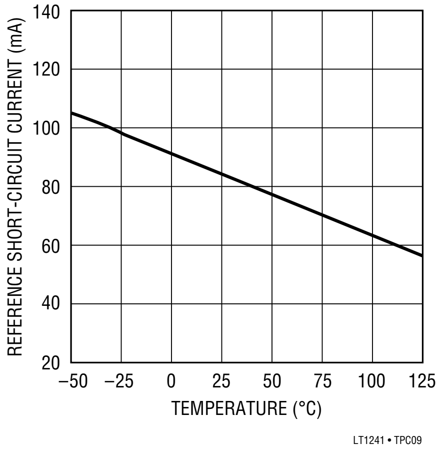


TYPICAL PERFORMANCE CHARACTERISTICS

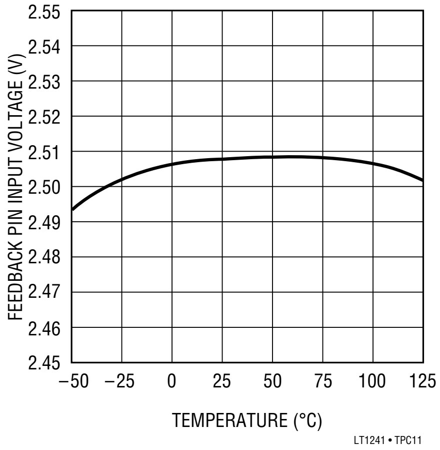
Reference Voltage



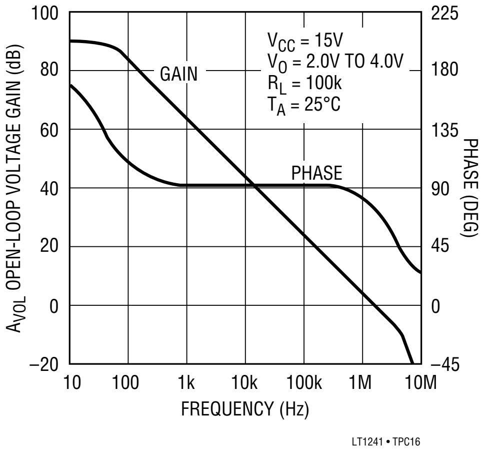
Reference Short-Circuit Current



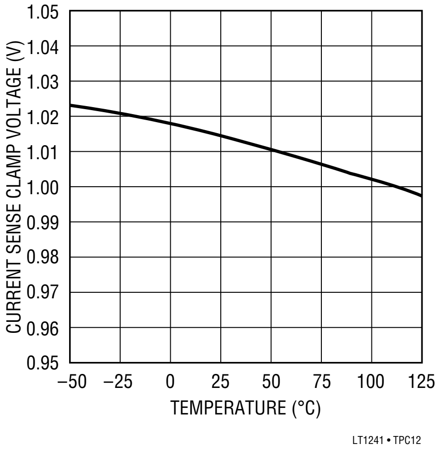
Feedback Pin Input Voltage



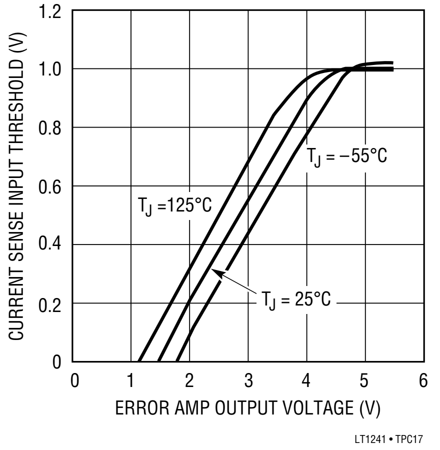
Error Amplifier Open-Loop Gain and Phase



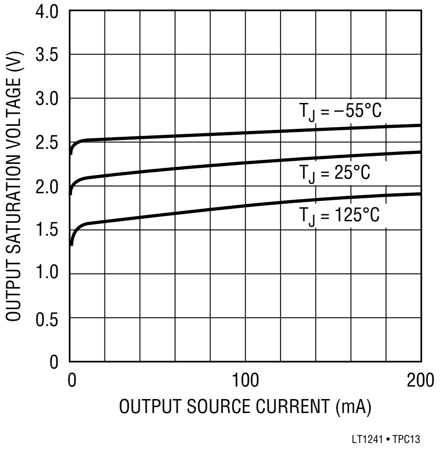
Current Sense Clamp Voltage



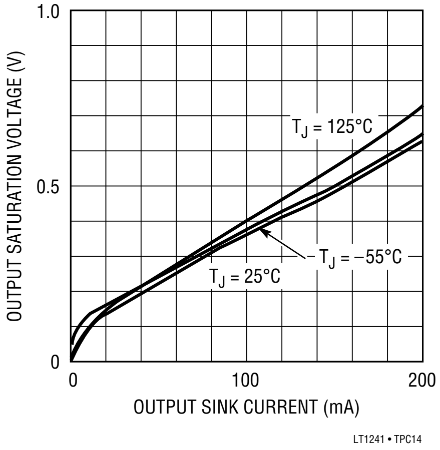
Current Sense Input Threshold



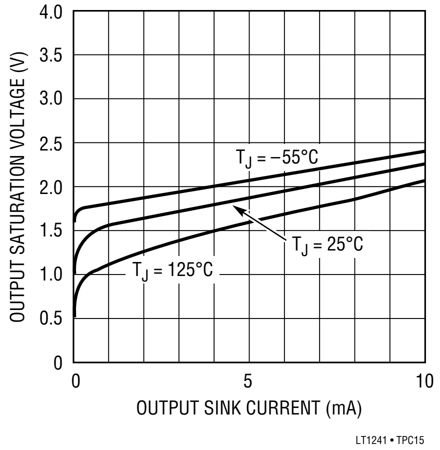
High Level Output Saturation Voltage



Low Level Output Saturation Voltage

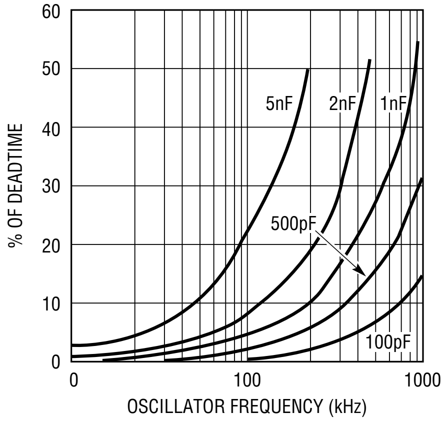


Low Level Output Saturation Voltage During Undervoltage Lockout



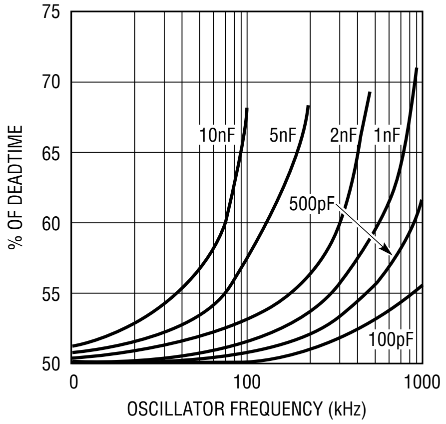
TYPICAL PERFORMANCE CHARACTERISTICS

Output Deadtime vs Oscillator Frequency – LT1242, LT1244



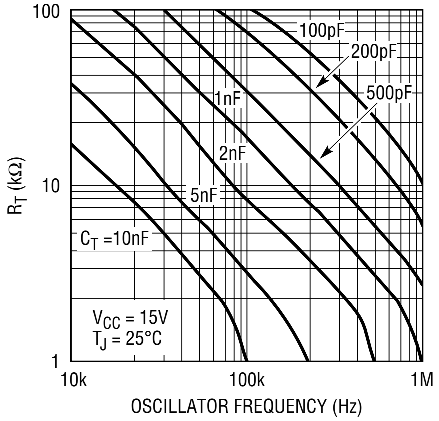
LT1241 • TPC19

Output Deadtime vs Oscillator Frequency – LT1241, LT1243, LT1245



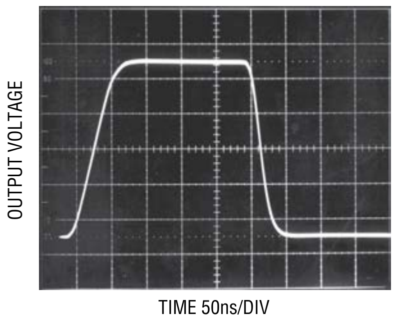
LT1241 • TPC20

Timing Resistor vs Oscillator Frequency



LT1241 • TPC21

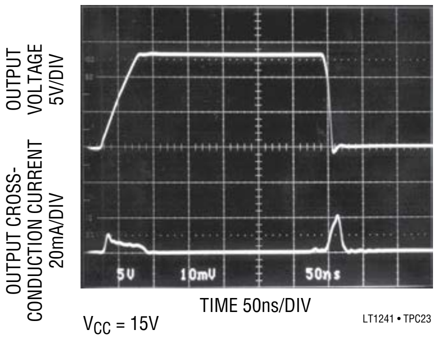
Output Rise and Fall Time



V_{CC} = 15V
C_L = 1nF

LT1241 • TPC22

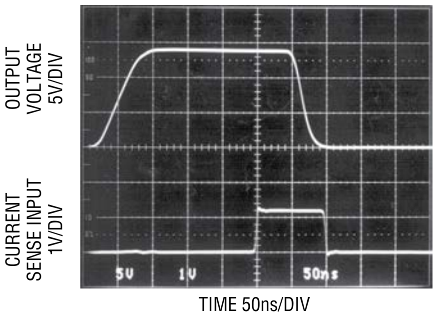
Output Cross-Conduction Current



V_{CC} = 15V
C_L = 1nF

LT1241 • TPC23

Current Sense Delay



V_{CC} = 15V
C_L = 1nF

LT1241 • TPC24

PIN FUNCTIONS

COMP (Pin 1): Compensation Pin. This pin is the output of the Error Amplifier and is made available for loop compensation. It can also be used to adjust the maximum value of the current sense clamp voltage to less than 1V. This pin can source a minimum of 0.5mA (0.8mA typ) and sink a minimum of 2mA (4mA typ)

FB (Pin 2): Voltage Feedback Pin. This pin is the inverting input of the error amplifier. The output voltage is normally fed back to this pin through a resistive divider. The non-inverting input of the error amplifier is internally committed to a 2.5V reference point.

I_{SENSE} (Pin 3): Current Sense Pin. This is the input to the current sense comparator. The trip point of the comparator is set by, and is proportional to, the output voltage of the Error Amplifier.

R_T/C_T (Pin 4): The oscillator frequency and the deadtime are set by connecting a resistor (R_T) from V_{REF} to R_T/C_T and a capacitor (C_T) from R_T/C_T to GND.

The rise time of the oscillator waveform is set by the RC time constant of R_T and C_T. The fall time, which is equal to the output deadtime, is set by a combination of the RC time constant and the oscillator sink current (8.2mA typ).

GND (Pin 5): Ground.

OUTPUT (Pin 6): This pin is the output of a high current totem pole output stage. It is capable of driving up to ±1A of current into a capacitive load such as the gate of a MOSFET.

V_{CC} (Pin 7): This pin is the positive supply of the control IC.

V_{REF} (Pin 8): Reference. This is the reference output of the IC. The reference output is used to supply charging current to the external timing resistor R_T. The reference provides biasing to a large portion of the internal circuitry, and is used to generate several internal reference levels including the V_{FB} level and the current sense clamp voltage.

APPLICATIONS INFORMATION

DEVICE	MINIMUM START-UP THRESHOLD	MINIMUM OPERATING VOLTAGE	MAXIMUM DUTY CYCLE	REPLACES
LT1241	9.6V	7.6V	50%	NONE
LT1242	16V	10V	100%	UC1842
LT1243	8.4V	7.6V	100%	UC1843
LT1244	16V	10V	50%	UC1844
LT1245	8.4V	7.6V	50%	UC1845

Oscillator

The LT1241 series devices are fixed frequency current mode pulse width modulators. The oscillator frequency and the oscillator discharge current are both trimmed and tightly specified to minimize the variations in frequency and deadtime. The oscillator frequency is set by choosing a resistor and capacitor combination, R_T and C_T. This RC combination will determine both the frequency and the maximum duty cycle. The resistor R_T is connected from V_{REF} (Pin 8) to the R_T/C_T pin (Pin 4). The capacitor C_T is connected from the R_T/C_T pin to ground. The charging current for C_T is determined by the value of R_T. The discharge current for C_T is set by the difference between the current supplied by R_T and the discharge current of the LT124X. The discharge current of the device is trimmed to 8.2mA. For large values of R_T discharge time will be determined by the discharge current of the device and the value of C_T. As the value of R_T is reduced it will have more effect on the discharge time of C_T. During an oscillator cycle capacitor C_T is charged to approximately 2.8V and discharged to approximately 1.1V. The output is enabled during the charge time of C_T and disabled, in an off state, during the discharge time of C_T. The deadtime of the circuit is equal to the discharge time of C_T. The maximum duty cycle is limited by controlling the deadtime of the oscillator. There are many combinations of R_T and C_T that will yield a given oscillator frequency, however there is only one combination that will yield a specific deadtime at that frequency. Curves of oscillator frequency and deadtime for various values of R_T and C_T appear in the Typical Performance Characteristics section. Frequency and deadtime can also be calculated using the following formulas:

Oscillator Rise Time: $t_r = 0.583 \bullet RC$

Oscillator Discharge Time: $t_d = \dfrac{3.46 \bullet RC}{(0.0164)R - 11.73}$

Oscillator Period: $T_{OSC} = t_r + t_d$

Oscillator Frequency: $f_{OSC} = \dfrac{1}{T_{OSC}}$

Maximum Duty Cycle:

LT1241, LT1244, LT1245

$$D_{MAX} = \frac{t_r}{2T_{OSC}} = \frac{T_{OSC} - t_d}{2T_{OSC}}$$

LT1242, LT1243

$$D_{MAX} = \frac{t_r}{T_{OSC}} = \frac{T_{OSC} - t_d}{T_{OSC}}$$

The above formulas will give values that will be accurate to approximately ±5%, at the oscillator, over the full operating frequency range. This is due to the fact that the oscillator trip levels are constant versus frequency and the discharge current and initial oscillator frequency are trimmed. Some fine adjustment may be required to achieve more accurate results. Once the final R_T/C_T combination is selected the oscillator characteristics will be repeatable from device to device. Note that there will be some slight differences between maximum duty cycle at the oscillator and maximum duty cycle at the output due to the finite rise and fall times of the output.

The output switching frequency will be equal to the oscillator frequency for LT1242 and LT1243. The output switching frequency will be equal to one-half the oscillator frequency for LT1241, LT1244 and LT1245. The oscillator of LT1241 series devices will run at frequencies up to 1MHz, allowing 500kHz output switching frequencies for all devices.

APPLICATIONS INFORMATION

Error Amplifier

The LT1241 series of devices contain a fully compensated error amplifier with a DC gain of 90dB and a unity-gain frequency of 1MHz. Phase margin at unity-gain is 80°. The noninverting input is internally committed to a 2.5V reference point derived from the 5V reference of Pin 8. The inverting input (Pin 2) and the output (Pin 1) are made available to the user. The output voltage in a regulator circuit is normally fed back to the inverting input of the error amplifier through a resistive divider.

The output of the error amplifier is made available for external loop compensation. The output current of the error amplifier is limited to approximately 0.8mA sourcing and approximately 6mA sinking. In a current mode PWM the peak switch current is a function of the output voltage of the error amplifier. In the LT1241 series devices the output of the error amplifier is offset by two diodes (1.4V at 25°C), divided by a factor of three, and fed to the inverting input of the current sense comparator. For error amplifier output voltages less than 1.4V the duty cycle of the output stage will be zero. The maximum offset that can appear at the current sense input is limited by a 1V clamp. This occurs when the error amplifier output reaches 4.4V at 25°C.

The output of the error amplifier can be clamped below 4.4V in order to reduce the maximum voltage allowed across the current sensing resistor to less than 1V. The supply current will increase by the value of the output source current when the output voltage of the error amplifier is clamped.

Current Sense Comparator and PWM Latch

LT1241 series devices are current mode controllers. Under normal operating conditions the output (Pin 6) is turned on at the start of every oscillator cycle, coincident with the rising edge of the oscillator waveform. The output is then turned off when the current reaches a threshold level proportional to the error voltage at the output of the error amplifier. Once the output is turned off it is latched off until the start of the next cycle. The peak current is thus proportional to the error voltage and is controlled on a cycle by cycle basis. The peak switch current is normally sensed by placing a sense resistor in the source lead of the output MOSFET. This resistor converts the switch current to a voltage that can be fed into the current sense input. For normal operating conditions the peak inductor current, which is equal to the peak switch current, will be equal to:

$$I_{PK} = \frac{(V_{PIN1} - 1.4V)}{(3R_S)}$$

During fault conditions the maximum threshold voltage at the input of the current sense comparator is limited by the internal 1V clamp at the inverting input. The peak switch current will be equal to:

$$I_{PK(MAX)} = \frac{1V}{R_S}$$

In certain applications, such as high power regulators, it may be desirable to limit the maximum threshold voltage to less than 1V in order to limit the power dissipated in the sense resistor or to limit the short-circuit current of the regulator circuit. This can be accomplished by clamping the output of the error amplifier. A voltage level of approximately 1.4V at the output of the error amplifier will give a threshold voltage of 0V. A voltage level of approximately 4.4V at the output of the error amplifier will give a threshold level of 1V. Between 1.4V and 4.4V the threshold voltage will change by a factor of one-third of the change in the error amplifier output voltage. The threshold voltage will be 0.333V for an error amplifier voltage of 2.4V. To reduce the maximum current sense threshold to less than 1V the error amplifier output should be clamped to less than 4.4V.

APPLICATIONS INFORMATION

Blanking

A unique feature of the LT1241 series devices is the built-in blanking circuit at the output of the current sense comparator. A common problem with current mode PWM circuits is erratic operation due to noise at the current sense input. The primary cause of noise problems is the leading edge current spike due to transformer interwinding capacitance and diode reverse recovery time. This current spike can prematurely trip the current sense comparator causing an instability in the regulator circuit. A filter at the current sense input is normally required to eliminate this instability.

This filter will in turn slow down the current sense loop. A slow current sense loop will increase the minimum pulse width which will increase the short-circuit current in an overload condition. The LT1241 series devices blank (lock out) the signal at the output of the current sense comparator for a fixed amount of time after the switch is turned on. This effectively prevents the PWM latch from tripping due to the leading edge current spike.

The blanking time will be a function of the voltage at the feedback pin (Pin 2). The blanking time will be 100ns for normal operating conditions (V_{FB} = 2.5V). The blanking time goes to zero as the feedback pin is pulled to 0V. This means that the blanking time will be minimized during start-up and also during an output short-circuit fault. This blanking circuit eliminates the need for an input filter at the current sense input except in extreme cases. Eliminating the filter allows the current sense loop to operate with minimum delays, reducing peak currents during fault conditions.

Undervoltage Lockout

The LT1241 series devices incorporate an undervoltage lockout comparator which prevents the internal reference circuitry and the output from starting up until the supply voltage reaches the start-up threshold voltage. The quiescent current, below the start-up threshold, has been reduced to less than 250µA (170µA typ.) to minimize the power loss due to the bleed resistor used for start-up in off-line converters. In undervoltage lockout both V_{REF} (Pin 8) and the output (Pin 6) are actively pulled low by Darlington connected PNP transistors. They are designed to sink a few milliamps of current and will pull down to about 1V. The pull-down transistor at the reference pin can be used to reset the external soft start capacitor. The pull-down transistor at the output eliminates the external pull-down resistor required, with earlier devices, to hold the external MOSFET gate low during undervoltage lockout.

Output

The LT1241 series devices incorporate a single high current totem pole output stage. This output stage is capable of driving up to ±1A of output current. Cross-conduction current spikes in the output totem pole have been eliminated. This device is primarily intended for driving MOSFET switches. Rise time is typically 40ns and fall time is typically 30ns when driving a 1.0nF load. A clamp is built into the device to prevent the output from rising above 18V in order to protect the gate of the MOSFET switch.

The output is actively pulled low during undervoltage lockout by a Darlington PNP. This PNP is designed to sink several milliamps and will pull the output down to approximately 1V. This active pull-down eliminates the need for an external resistor which was required in older designs. The output pin of the device connects directly to the emitter of the upper NPN drive transistor and the collector of the lower NPN drive transistor in the totem pole. The collector of the lower transistor, which is n-type silicon, forms a p-n junction with the substrate of the device. This junction is reverse biased during normal operation.

In some applications the parasitic LC of the external MOSFET gate can ring and pull the OUTPUT pin below ground. If the OUTPUT pin is pulled negative by more than a diode drop the parasitic diode formed by the collector

APPLICATIONS INFORMATION

of the output NPN and the substrate will turn on. This can cause erratic operation of the device. In these cases a Schottky clamp diode is recommended from the output to ground.

Reference

The internal reference of the LT1241 series devices is a 5V bandgap reference, trimmed to within ±1% initial tolerance. The reference is used to power the majority of internal logic and the oscillator circuitry. The oscillator charging current is supplied from the reference. The feedback pin voltage and the clamp level for the current sense comparator are derived from the reference voltage. The reference can supply up to 20mA of current to power external circuitry. Note that using the reference in this manner, as a voltage regulator, will significantly increase power dissipation in the device which will reduce the useful operating ambient temperature range.

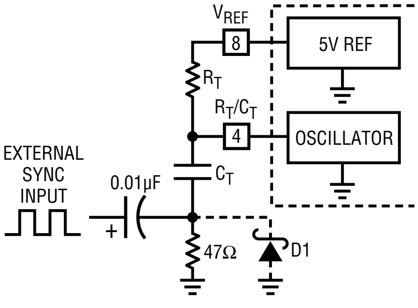
Design/Layout Considerations

LT1241 series devices are high speed circuits capable of generating pulsed output drive currents of up to 1A peak. The rise and fall time for the output drive current is in the range of 10ns to 20ns. High speed circuit techniques must be used to insure proper operation of the device. **Do not attempt to use Proto-boards or wire-wrap techniques to breadboard high speed switching regulator circuits. They will not work properly.**

Printed circuit layouts should include separate ground paths for the voltage feedback network, oscillator capacitor, and switch drive current. These ground paths should be connected together directly at the ground pin (Pin 5) of the LT124X. This will minimize noise problems due to pulsed ground pin currents. V_{CC} should be bypassed, with a minimum of 0.1μF, as close to the device as possible. High current paths should be kept short and they should be separated from the feedback voltage network with shield traces if possible.

TYPICAL APPLICATIONS

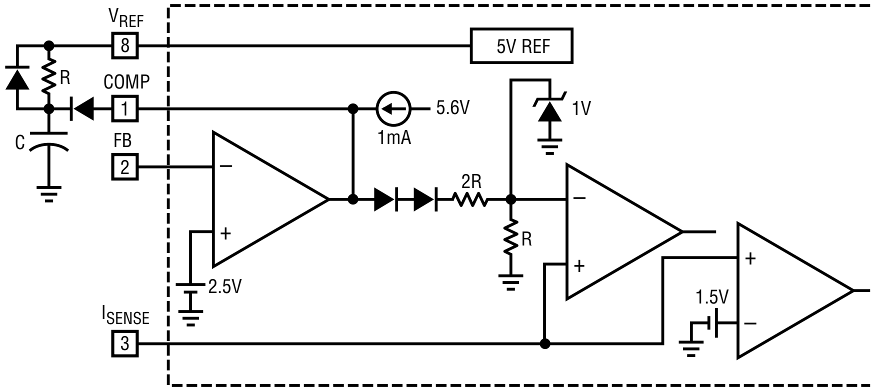
External Clock Synchronization



D1 IS REQUIRED IF THE SYNC AMPLITUDE IS LARGE ENOUGH TO PULL THE BOTTOM OF C_T MORE THAN 300mV BELOW GROUND.

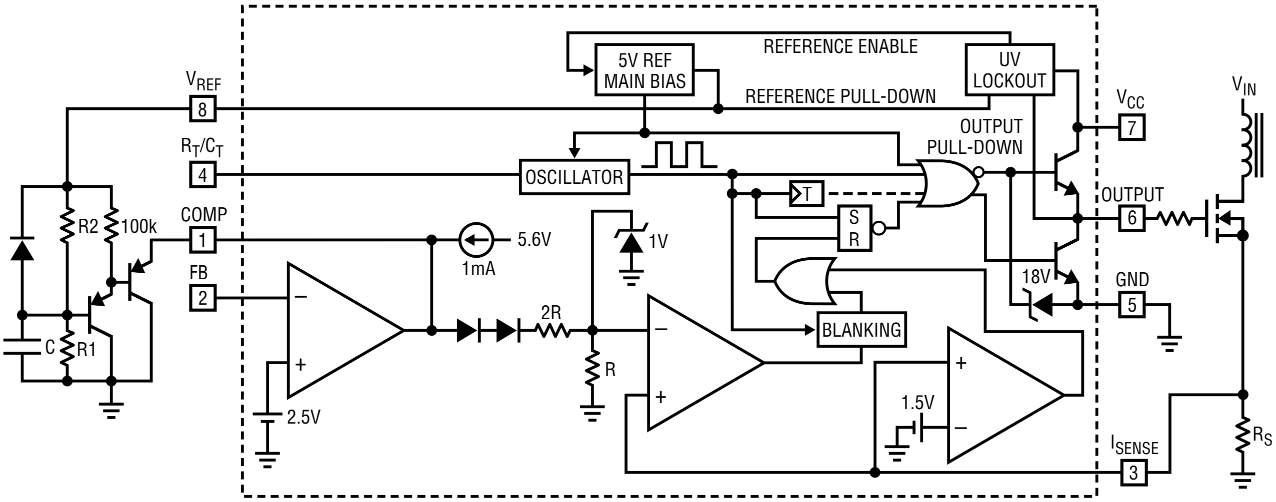
LT1241 • TA01

Soft-Start



LT1241 • TA02

Adjustable Clamp Level with Soft-Start

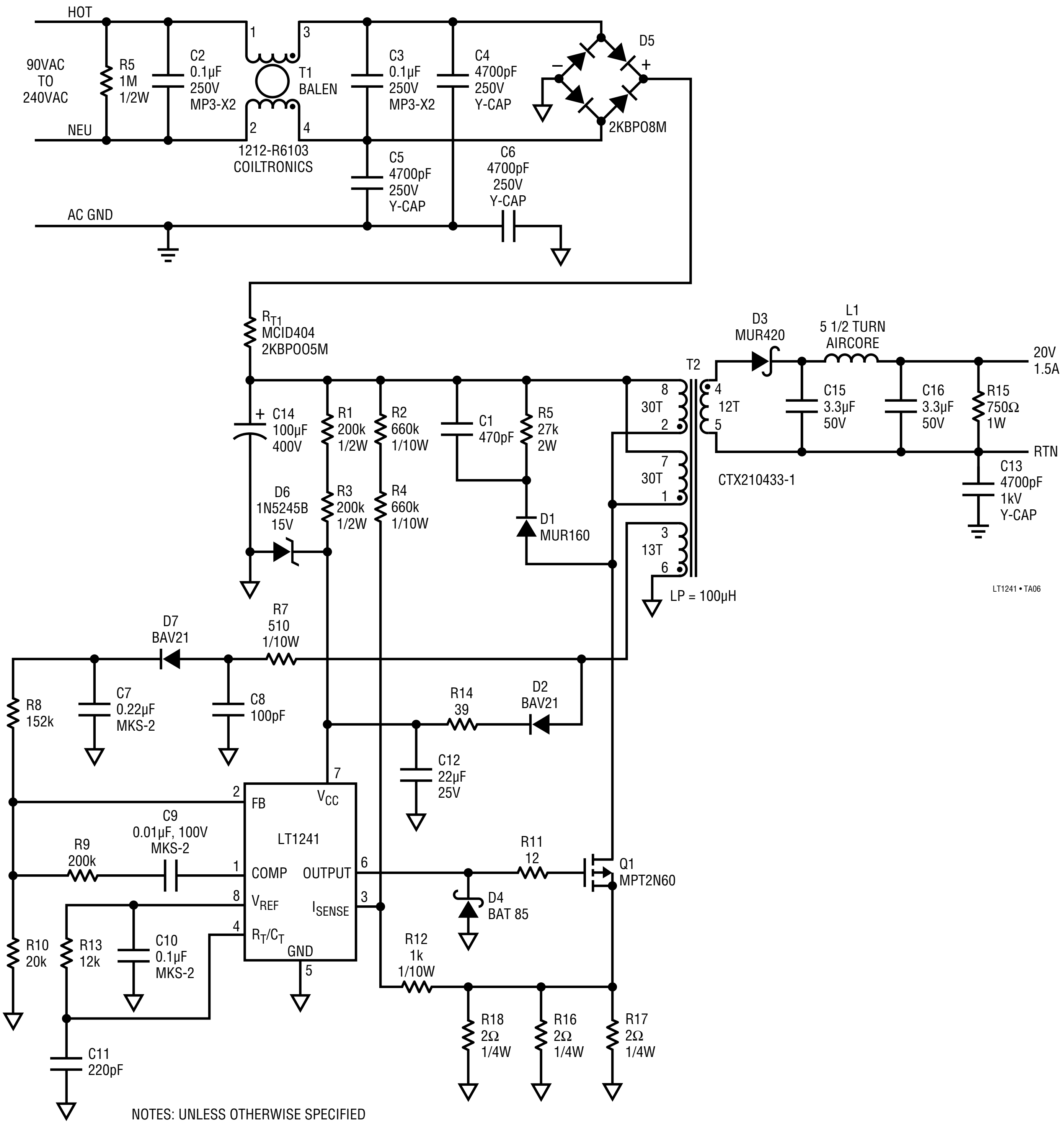


$V_{CLAMP} \approx \dfrac{1.67}{\left(\dfrac{R2}{R1} + 1\right)}$ $\quad I_{PK\,(MAX)} \approx \dfrac{V_{CLAMP}}{R_S}$ $\quad$ WHERE: $0V \le V_{CLAMP} \le 1.0V$ $\quad t_{SOFT\text{-}START} = -\ln\left[1 - \dfrac{V_C}{3 \bullet V_{CLAMP}}\right] C \dfrac{R1\,R2}{R1 + R2}$

LT1241 • TA03

TYPICAL APPLICATIONS

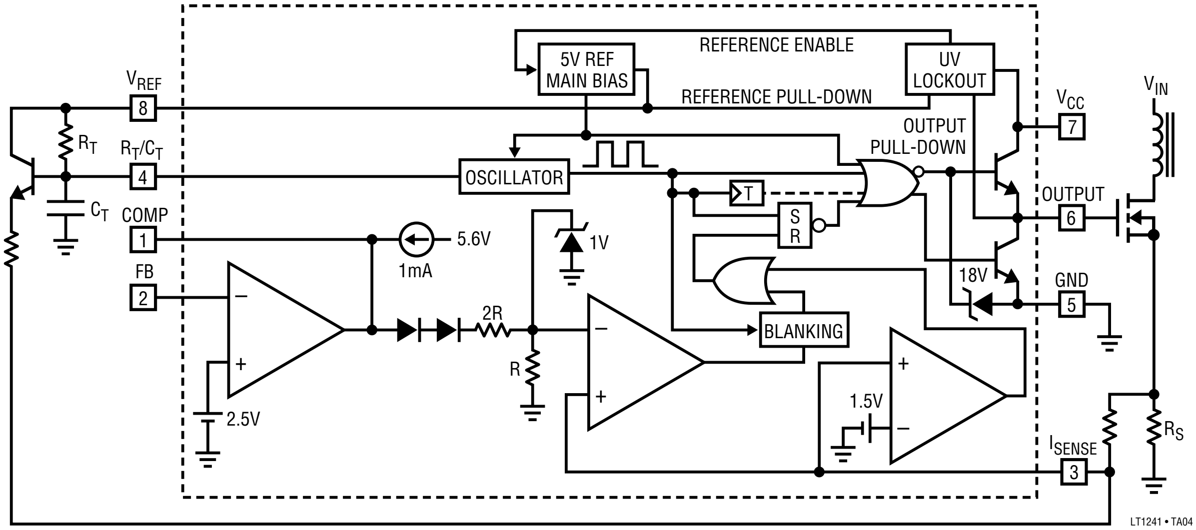
300kHz Off-Line Power Supply



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITANCES ARE IN MICROFARADS, 50V, 10%.

TYPICAL APPLICATIONS

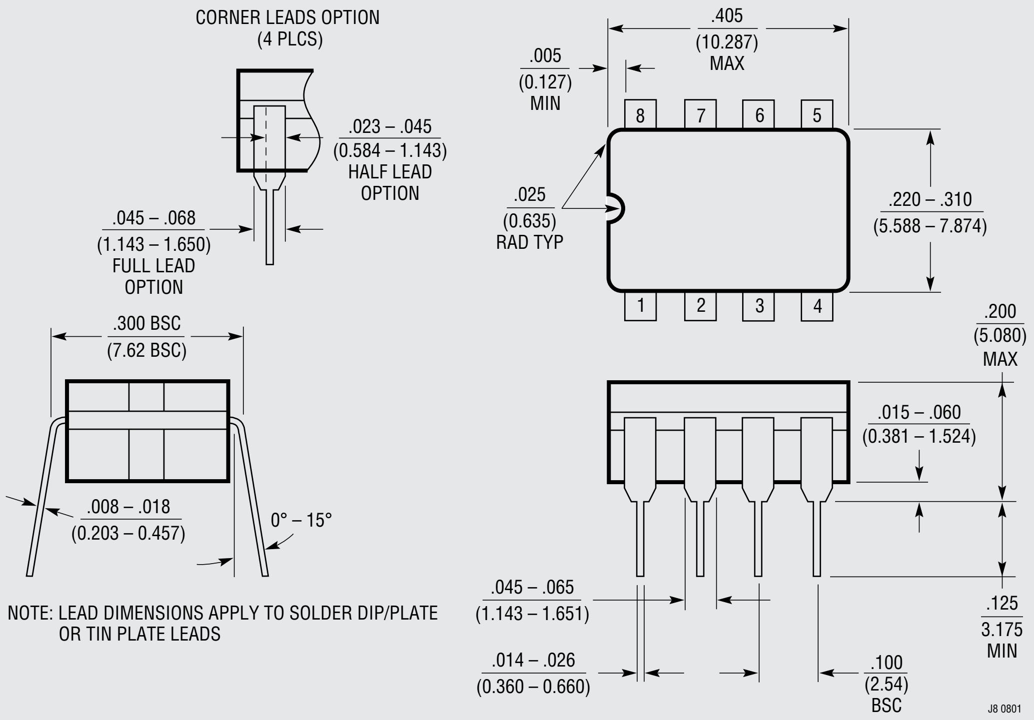
Slope Compensation at I_{SENSE} Pin



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT1241#packaging for the most recent package drawings.

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



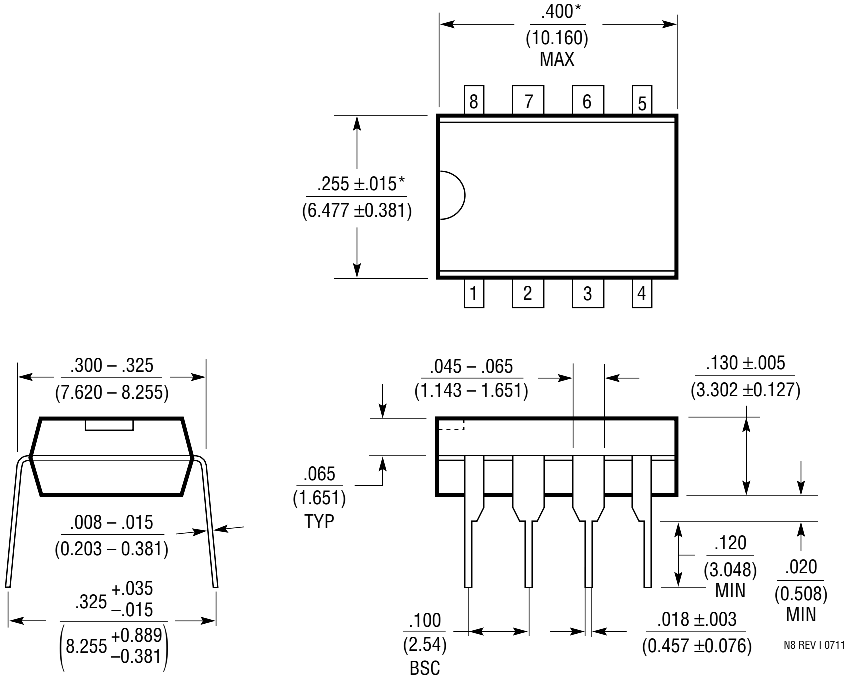
NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE
OR TIN PLATE LEADS

OBSOLETE PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT1241#packaging for the most recent package drawings.

N Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)

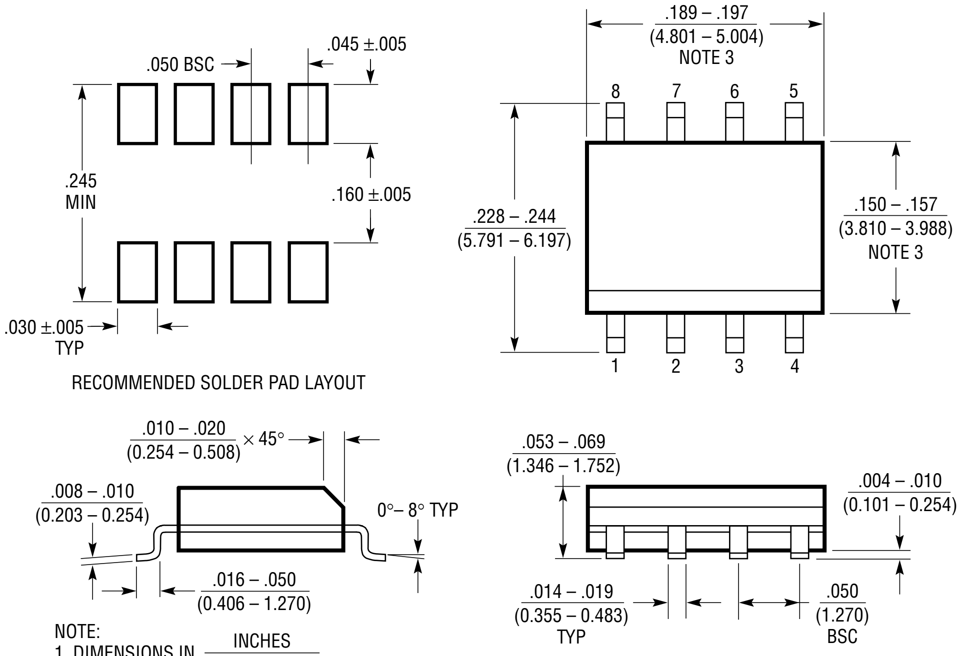


NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT1241#packaging for the most recent package drawings.

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



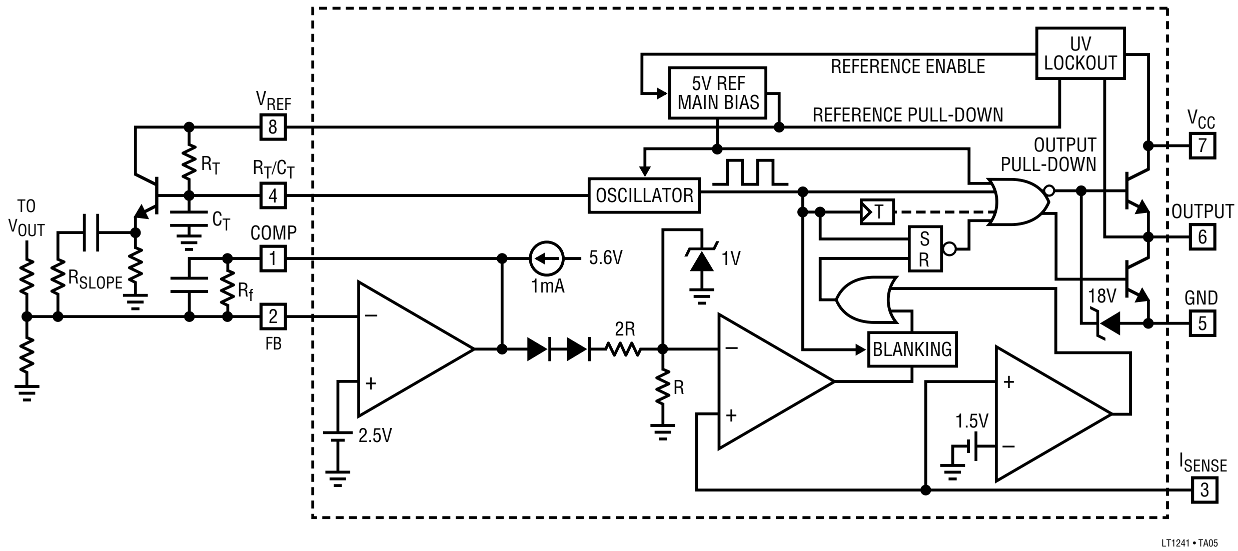
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	04/18	Deleted CERDIP J8 package	2

TYPICAL APPLICATION

Slope Compensation at Error Amp



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3895	150V Low I_Q, Synchronous Step-Down DC/DC Controller	4V ≤ V_{IN} ≤ 140V, 150V ABS Max, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50μA PLL Fixed Frequency 50kHz to 900kHz
LTC3810	100V Synchronous Step-Down DC/DC Controller	Constant On-Time Valley Current Mode 6.2V ≤ V_{IN} ≤ 100V, 0.8V ≤ V_{OUT} ≤ 0.93V_{IN}, SSOP-28
LTC3864	60V, Low I_Q, High Voltage DC/DC Controller with 100% Duty Cycle	Fixed Frequency 50kHz to 850kHz, 3.5V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ V_{IN} , I_Q = 40μA, MSOP-12E, 3mm × 4mm DFN-12
LTC3891	60V, Low I_Q, Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50μA PLL Fixed Frequency 50kHz to 900kHz
LT3840	60V, Low I_Q, Synchronous Step-Down Controller with Integrated Buck-Boost Bias Voltage Regulator	2.5V ≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 60V, I_Q = 75μA Synchronizable Fixed Frequency 100kHz to 600kHz
LTC3892/LTC3892-1	60V Low I_Q, Dual, 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 0.99V_{IN}, PLL Fixed Frequency 50kHz to 900kHz, Adjustable 5V to 10V Gate Drive, I_Q = 29μA
LTC3890/LTC3890-1 LTC3890-2/LTC3890-3	60V, Low I_Q, Dual 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50μA
LTC7813	60V Low I_Q, Synchronous Boost + Buck DC/DC Controller	4.5V(Down to 2.2V After Start-Up) ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 60V, Adjustable 5V to 10V Gate Drive, I_Q = 33μA
LTC7801	150V Low I_Q, Synchronous Step-Down DC/DC Controller	4V ≤ V_{IN} ≤ 140V, 150V ABS Max, 0.8V ≤ V_{OUT} ≤ 60V, I_Q = 40μA PLL Fixed Frequency 320kHz to 2.25MHz
LTC7103	105V, 2.3A Low EMI Synchronous Step-Down Regulator	4.4V ≤ V_{IN} ≤ 105V, 1V ≤ V_{OUT} ≤ V_{IN}, I_Q = 2μA Fixed Frequency 200kHz to 2MHz, 5mm × 6mm QFN

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