Quad Buck Regulator Integrated Power Solution

Data Sheet

ADP5054

FEATURES

- Wide input voltage range: 4.5 V to 15.5 V
- ±1.5% output accuracy over full temperature range
- 250 kHz to 2 MHz adjustable switching frequency with individual ½× frequency option
- Power regulation
  - Channel 1 and Channel 2
    - Programmable 2 A/4 A/6 A sync buck regulators with low-side FET drivers
  - Channel 3 and Channel 4: 2.5 A sync buck regulators
- Flexible parallel operation
  - Single 12 A output (Channel 1 and Channel 2 in parallel)
  - Single 5 A output (Channel 3 and Channel 4 in parallel)
- Low 1/f noise density
  - 40 µV rms at 0.8 V_{REF} for 10 Hz to 100 kHz
- Precision enable with 0.811 V accurate threshold
- Active output discharge switch
- FPWM/PSM mode selection
- Frequency synchronization input or output
- Power-good flag for Channel 1 output
- UVLO, OCP, and TSD protection
- 48-lead, 7 mm × 7 mm LFCSP
- −40°C to +125°C operational junctional temperature range

APPLICATIONS

- FPGA and processor applications
- Small cell base stations
- Security and surveillance
- Medical applications

TYPICAL APPLICATION CIRCUIT

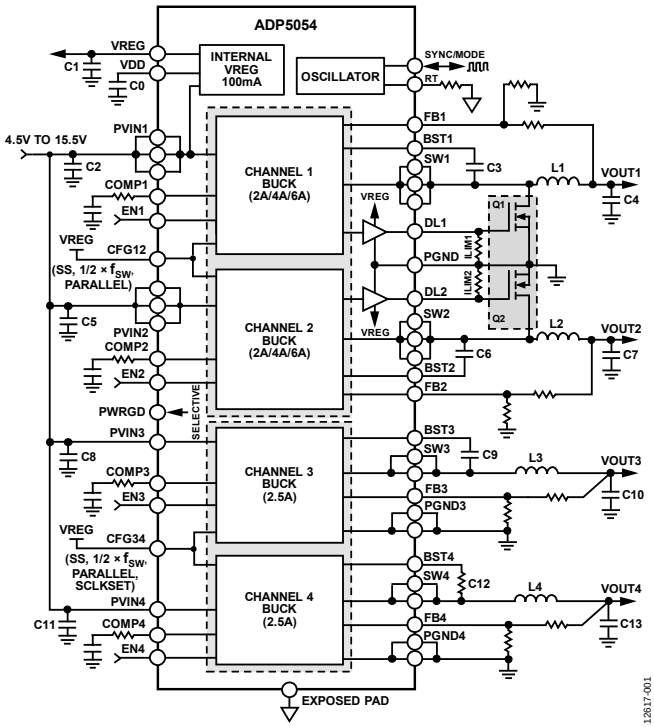

Figure 1.

GENERAL DESCRIPTION

The ADP5054 combines four high performance buck regulators in a 48-lead LFCSP package that meets demanding performance and board space requirements. The device enables direct connection to high input voltages of up to 15.5 V with no preregulators.

Channel 1 and Channel 2 integrate high-side power metal-oxide semiconductor field effect transistors (MOSFETs) and low-side MOSFET drivers. External NFETs can be used in low-side power devices to achieve an efficiency optimized solution and to deliver a programmable output current of 2 A, 4 A, or 6 A. Combining Channel 1 and Channel 2 in a parallel configuration provides a single output with up to 12 A of current.

Channel 3 and Channel 4 integrate both high-side and low-side MOSFETs to deliver an output current of 2.5 A. Combining Channel 3 and Channel 4 in a parallel configuration can provide a single output with up to 5 A of current.

The switching frequency of the ADP5054 can be programmed or synchronized to an external clock from 250 kHz to 2 MHz, and an individual ½× frequency configuration is available for each channel.

The ADP5054 contains an individual precision enable pin on each channel for easy power-up sequencing. The internal low 1/f noise reference is implemented in the ADP5054 for noise sensitive applications.

Table 1. Related Products

Model	Channels	I²C	Package
ADP5050	Four bucks, one LDO	Yes	48-Lead LFCSP
ADP5051	Four bucks, supervisory	Yes	48-Lead LFCSP
ADP5052	Four bucks, one LDO	No	48-Lead LFCSP
ADP5053	Four bucks, supervisory	No	48-Lead LFCSP
ADP5054	Four high current bucks	No	48-Lead LFCSP

Rev. G Document Feedback

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3/2019—Rev. E to Rev. F

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6/2018—Rev. D to Rev. E

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10/2017—Rev. C to Rev. D

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9/2015—Rev. A to Rev. B

Changes to Figure 1 and Table 1 1
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4/2015—Rev. 0 to Rev. A

Changes to Figure 3 8

3/2015—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

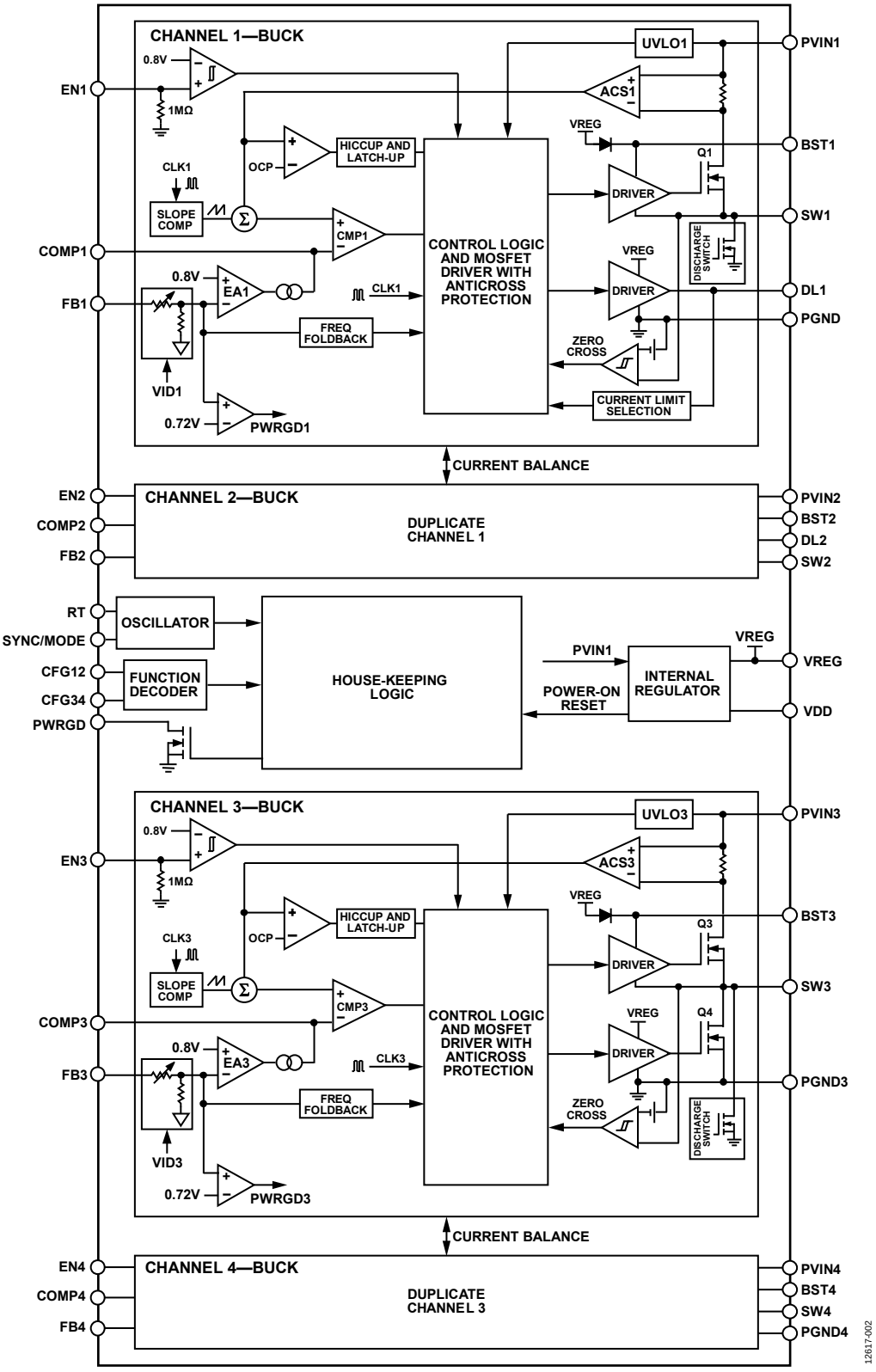


Figure 2.

SPECIFICATIONS

V_{IN} = 12 V, V_{VREG} = 5.0 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE	V_{IN}	4.5		15.5	V	PVIN1, PVIN2, PVIN3, PVIN4 pins
QUIESCENT CURRENT						PVIN1, PVIN2, PVIN3, PVIN4 pins
Operating Quiescent Current	I_Q		4.7	5.3	mA	No switching, all ENx pins high
Shutdown Current	I_{SHDN}		20	35	µA	All ENx pins low
UNDERVOLTAGE LOCKOUT	UVLO					PVIN1, PVIN2, PVIN3, PVIN4 pins
Threshold, Rising	V_{UVLO_RISING}		4.22	4.34	V	
Threshold, Falling	$V_{UVLO\_FALLING}$	3.65	3.79		V	
Hysteresis	V_{HYS}		0.43		V	
OSCILLATOR CIRCUIT						
Switching Frequency	f_{SW}	570	600	630	kHz	RT = 32.4 kΩ
Switching Frequency Range		250		2000	kHz	
SYNC Input						
Input Clock Range	f_{SYNC}	250		2000	kHz	
Input Clock Pulse Width						
Minimum On Time	$t_{SYNC\_MIN\_ON}$	100			ns	
Minimum Off Time	$t_{SYNC\_MIN\_OFF}$	100			ns	
Input Clock High Voltage	$V_{H(SYNC)}$	1.3			V	
Input Clock Low Voltage	$V_{L(SYNC)}$			0.4	V	
SYNC Output						
Clock Frequency	f_{CLK}		f_{SW}		kHz	
Positive Pulse Duty Cycle	$t_{CLK\_PULSE\_DUTY}$		50		%	
Rise or Fall Time	$t_{CLK\_RISE\_FALL}$		10		ns	
High Level Voltage	$V_{H(SYNC\_OUT)}$		V_{VREG}		V	
PRECISION ENABLING						EN1, EN2, EN3, EN4 pins
High Level Threshold	$V_{TH\_H(EN)}$		0.811	0.835	V	
Low Level Threshold	$V_{TH\_L(EN)}$	0.69	0.72		V	
Pull-Down Resistor	$R_{PULL\text{-}DOWN(EN)}$		2.0		MΩ	
POWER GOOD						
Internal Power-Good Rising Threshold	$V_{PWRGD(RISE)}$	86	91	96	%	
Internal Power-Good Hysteresis	$V_{PWRGD(HYS)}$		3.5		%	
Internal Power-Good Falling Delay	t_{PWRGD_FALL}		50		µs	
Rising Delay for PWRGD Pin	$t_{PWRGD\_PIN\_RISE}$		1		ms	
Leakage Current for PWRGD Pin	$I_{PWRGD\_LEAKAGE}$		0.1	1	µA	
Output Low Voltage for PWRGD Pin	V_{PWRGD_LOW}		50	100	mV	I_{PWRGD} = 1 mA
INTERNAL REGULATOR						
VDD Output Voltage	V_{VDD}	3.2	3.3	3.4	V	I_{VDD} = 10 mA
VDD Current Limit	I_{LIM_VDD}	30	50	70	mA	
VREG Output Voltage	V_{VREG}	4.85	5.0	5.15	V	I_{VREG} = 50 mA
Dropout Voltage	$V_{DROPOUT}$		225		mV	I_{VREG} = 50 mA
VREG Current Limit	I_{LIM_VREG}	85	160	225	mA	
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDN}		150		°C	
Thermal Shutdown Hysteresis	T_{HYS}		15		°C	

BUCK REGULATOR SPECIFICATIONS

V_{IN} = 12 V, V_{VREG} = 5.0 V, f_{SW} = 600 kHz for all channels, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 1 SYNC BUCK REGULATOR						
FB1 Pin						
Adjustable Feedback Voltage	V_{FB1}		0.800		V	
Feedback Voltage Accuracy	$V_{FB1(DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB1}			0.1	µA	Adjustable voltage
SW1 Pin						
High-Side Power FET On Resistance	$R_{DS(ON)\_1H}$		50		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH(ILIM1)}$	5.2	6.9	8.6	A	R_{ILIM1} floating
		2.6	3.8	5.0	A	R_{ILIM1} = 47 kΩ
		7.8	10.4	12.4	A	R_{ILIM1} = 22 kΩ
Minimum On Time	t_{MIN_ON1}		115	150	ns	f_{SW} = 250 kHz to 2.0 MHz
Minimum Off Time	t_{MIN_OFF1}		1/9 × t_{SW}		ns	f_{SW} = 250 kHz to 2.0 MHz
Low-Side Driver, DL1 Pin						
Rising Time	$t_{RISING1}$		20		ns	C_{ISS} = 1.2 nF
Falling Time	$t_{FALLING1}$		3.4		ns	C_{ISS} = 1.2 nF
Sourcing Resistor	$t_{SOURCING1}$		8		Ω	
Sinking Resistor	$t_{SINKING1}$		1.2		Ω	
Error Amplifier (EA), COMP1 Pin						
EA Transconductance	g_{m1}	310	465	620	µS	
Soft Start						
Soft Start Time	t_{SS1}		2.0		ms	CFG12 connected to ground
Programmable Soft Start Range		2.0		16.0	ms	
Hiccup Time	$t_{HICCUP1}$		7 × t_{SS1}		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS1}		250		Ω	
CHANNEL 2 SYNC BUCK REGULATOR						
FB2 Pin						
Adjustable Feedback Voltage	V_{FB2}		0.800		V	
Feedback Voltage Accuracy	$V_{FB2(DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ +85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB2}			0.1	µA	Adjustable voltage
SW2 Pin						
High-Side Power FET On Resistance	$R_{DS(ON)\_2H}$		50		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH(ILIM2)}$	5.2	6.9	8.6	A	R_{ILIM2} = floating
		2.6	3.8	5.0	A	R_{ILIM2} = 47 kΩ
		7.8	10.4	12.4	A	R_{ILIM2} = 22 kΩ
Minimum On Time	t_{MIN_ON2}		115	150	ns	f_{SW} = 250 kHz to 2.0 MHz
Minimum Off Time	t_{MIN_OFF2}		1/9 × t_{SW}		ns	f_{SW} = 250 kHz to 2.0 MHz
Low-Side Driver, DL2 Pin						
Rising Time	$t_{RISING2}$		20		ns	C_{ISS} = 1.2 nF
Falling Time	$t_{FALLING2}$		3.4		ns	C_{ISS} = 1.2 nF
Sourcing Resistor	$t_{SOURCING2}$		8		Ω	
Sinking Resistor	$t_{SINKING2}$		1.2		Ω	
Error Amplifier (EA), COMP2 Pin						
EA Transconductance	g_{m2}	310	465	620	µS	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Soft Start						
Soft Start Time	t_{SS2}		2.0		ms	CFG12 connected to ground
Programmable Soft Start Range		2.0		16.0	ms	
Hiccup Time	$t_{HICCUP2}$		$7 \times t_{SS1}$		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS2}		250		Ω	
CHANNEL 3 SYNC BUCK REGULATOR						
FB3 Pin						
Adjustable Feedback Voltage	V_{FB3}		0.800		V	
Feedback Voltage Accuracy	$V_{FB3(DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB3}			0.1	µA	Adjustable voltage
SW3 Pin						
High-Side Power FET On Resistance	$R_{DS(ON)\_3H}$		125		mΩ	Pin-to-pin measurement
Low-Side Power FET On Resistance	$R_{DS(ON)\_3L}$		80		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH(ILIM3)}$	3.5	4.66	5.5	A	
Minimum On Time	t_{MIN_ON3}		95	125	ns	f_{SW} = 250 kHz to 2.0 MHz
Minimum Off Time	t_{MIN_OFF3}		$1/9 \times t_{SW}$		ns	f_{SW} = 250 kHz to 2.0 MHz
Error Amplifier (EA), COMP3 Pin						
EA Transconductance	g_{m3}	310	465	620	µS	
Soft Start						
Soft Start Time	t_{SS3}		2.0		ms	CFG34 connected to ground
Programmable Soft Start Range		2.0		16.0	ms	
Hiccup Time	$t_{HICCUP3}$		$7 \times t_{SS3}$		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS3}		250		Ω	
CHANNEL 4 SYNC BUCK REGULATOR						
FB4 Pin						
Adjustable Feedback Voltage	V_{FB4}		0.800		V	
Feedback Voltage Accuracy	$V_{FB4(DEFAULT)}$	−0.55		+0.55	%	T_J = 25°C
		−1.25		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB4}			0.1	µA	
SW4 Pin						
High-Side Power FET On Resistance	$R_{DS(ON)\_4H}$		125		mΩ	Pin-to-pin measurement
Low-Side Power FET On Resistance	$R_{DS(ON)\_4L}$		80		mΩ	Pin-to-pin measurement
Current-Limit Threshold	$I_{TH(ILIM4)}$	3.5	4.66	5.5	A	
Minimum On Time	t_{MIN_ON4}		95	125	ns	f_{SW} = 250 kHz to 2.0 MHz
Minimum Off Time	t_{MIN_OFF4}		$1/9 \times t_{SW}$		ns	f_{SW} = 250 kHz to 2.0 MHz
Error Amplifier (EA), COMP4 Pin						
EA Transconductance	g_{m4}	310	465	620	µS	
Soft Start						
Soft Start Time	t_{SS4}		2.0		ms	CFG34 connected to ground
Programmable Soft Start Range		2.0		16.0	ms	
Hiccup Time	$t_{HICCUP4}$		$7 \times t_{SS3}$		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS4}		250		Ω	

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter[1]	Rating
PVIN1 to PGND	−0.3 V to +18 V
PVIN2 to PGND	−0.3 V to +18 V
PVIN3 to PGND3	−0.3 V to +18 V
PVIN4 to PGND4	−0.3 V to +18 V
SW1 to PGND	−0.3 V to +18 V
SW2 to PGND	−0.3 V to +18 V
SW3 to PGND3	−0.3 V to +18 V
SW4 to PGND4	−0.3 V to +18 V
PGND to Ground	−0.3 V to +0.3 V
PGND3 to Ground	−0.3 V to +0.3 V
PGND4 to Ground	−0.3 V to +0.3 V
BST1 to SW1	−0.3 V to +6.5 V
BST2 to SW2	−0.3 V to +6.5 V
BST3 to SW3	−0.3 V to +6.5 V
BST4 to SW4	−0.3 V to +6.5 V
DL1 to PGND	−0.3 V to +6.5 V
DL2 to PGND	−0.3 V to +6.5 V
CFG12, CFG34 to Ground	−0.3 V to +6.5 V
EN1, EN2, EN3, EN4 to Ground	−0.3 V to +6.5 V
VREG to Ground	−0.3 V to +6.5 V
SYNC/MODE to Ground	−0.3 V to +6.5 V
RT to Ground	−0.3 V to +3.6 V
PWRGD to Ground	−0.3 V to +6.5 V
FB1, FB2, FB3, FB4 to Ground[2]	−0.3 V to +3.6 V
COMP1, COMP2, COMP3, COMP4 to Ground	−0.3 V to +3.6 V
Storage Temperate Range	−65°C to +150°C
Operational Junction Temperature Range	−40°C to +125°C

[1] The exposed pad is the analog ground for the ADP5054. See Table 6.
[2] The rating for the FB1, FB2, FB3, and FB4 pins applies to the adjustable output voltage models of the ADP5054.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-Lead LFCSP	28.4	10.1	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

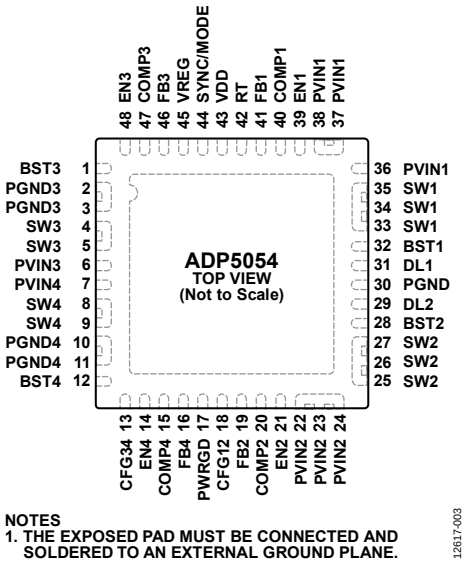


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BST3	High-Side FET Driver Power Supply for Channel 3.
2, 3	PGND3	Power Ground for Channel 3.
4, 5	SW3	Switching Node Output for Channel 3.
6	PVIN3	Power Input for Channel 3. Connect a bypass capacitor between this pin and ground.
7	PVIN4	Power Input for Channel 4. Connect a bypass capacitor between this pin and ground.
8, 9	SW4	Switching Node Output for Channel 4.
10, 11	PGND4	Power Ground for Channel 4.
12	BST4	High-Side FET Driver Power Supply for Channel 4.
13	CFG34	Connect a resistor divider from this pin to VREG and ground to configure the different functionalities for Channel 3 and Channel 4, including the soft start timer, ½× frequency, parallel operation, and SYNC clock output features.
14	EN4	Enable Input for Channel 4. Use an external resistor divider to set the turn-on threshold.
15	COMP4	Error Amplifier Output for Channel 4. Connect an RC network from this pin to ground.
16	FB4	Feedback Sensing Input for Channel 4.
17	PWRGD	Power-Good Signal Output. This open-drain output is the power-good signal for the selected channels.
18	CFG12	Connect a resistor divider from this pin to VREG and ground to configure the different functionalities for Channel 1 and Channel 2, including the soft start timer, ½× frequency, and parallel operation features.
19	FB2	Feedback Sensing Input for Channel 2.
20	COMP2	Error Amplifier Output for Channel 2. Connect an RC network from this pin to ground.
21	EN2	Enable Input for Channel 2. Use an external resistor divider to set the turn-on threshold.
22, 23, 24	PVIN2	Power Input for Channel 2. Connect a bypass capacitor between this pin and ground.
25, 26, 27	SW2	Switching Node Output for Channel 2.
28	BST2	High-Side FET Driver Power Supply for Channel 2.
29	DL2	Low-Side FET Gate Driver for Channel 2. Connect a resistor from this pin to ground to program the current-limit threshold for Channel 2.
30	PGND	Power Ground for Channel 1 and Channel 2.
31	DL1	Low-Side FET Gate Driver for Channel 1. Connect a resistor from this pin to ground to program the current-limit threshold for Channel 1.
32	BST1	High-Side FET Driver Power Supply for Channel 1.
33, 34, 35	SW1	Switching Node Output for Channel 1.
36, 37, 38	PVIN1	Power Input for the Internal Linear Regulator and the Channel 1 Buck Regulator. Connect a bypass capacitor between this pin and ground.

Pin No.	Mnemonic	Description
39	EN1	Enable Input for Channel 1. Use an external resistor divider to set the turn-on threshold.
40	COMP1	Error Amplifier Output for Channel 1. Connect an RC network from this pin to ground.
41	FB1	Feedback Sensing Input for Channel 1.
42	RT	Connect a resistor from RT to ground to program the switching frequency from 250 kHz to 2 MHz.
43	VDD	Output of the Internal 3.3 V Linear Regulator. Connect a 1.0 µF ceramic capacitor between this pin and ground.
44	SYNC/MODE	Synchronization Input/Output (SYNC). To synchronize the switching frequency of the device to an external clock, connect this pin to an external clock with a frequency from 250 kHz to 2.0 MHz. This pin can also be configured as a synchronization output via the CFG34 pin configuration. Forced PWM or Automatic PWM/PSM Selection Pin (MODE). When this pin is logic high, each channel works in forced PWM or automatic PWM/PSM mode. When this pin is logic low, all channels operate in automatic PWM/PSM mode.
45	VREG	Output of the Internal 5.0 V Linear Regulator. Connect a 1.0 µF ceramic capacitor between this pin and ground.
46	FB3	Feedback Sensing Input for Channel 3.
47	COMP3	Error Amplifier Output for Channel 3. Connect an RC network from this pin to ground.
48	EN3	Enable Input for Channel 3. Use an external resistor divider to set the turn-on threshold.
	EPAD	Exposed Pad (Analog Ground). The exposed pad must be connected and soldered to an external ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

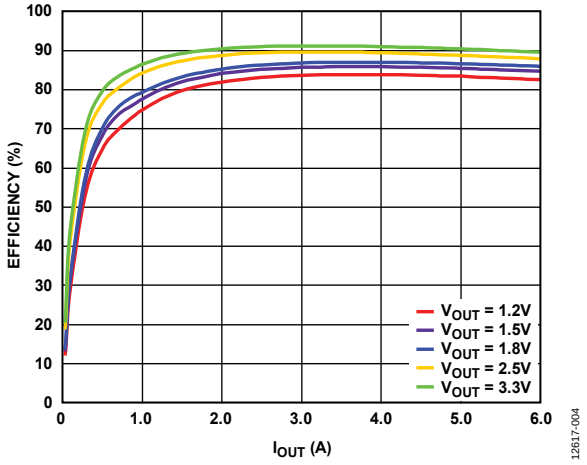


Figure 4. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, MOSFET = SI4204DY, FPWM Mode

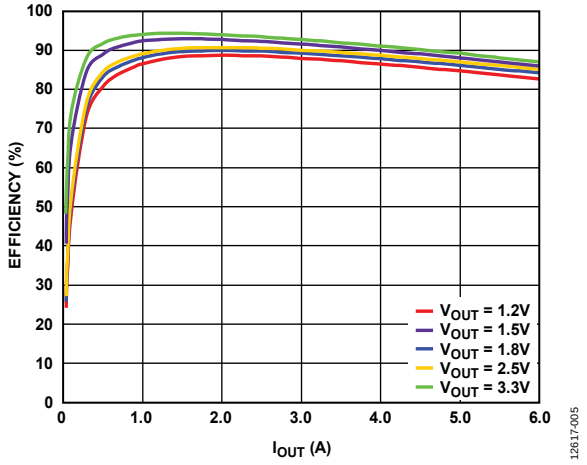


Figure 5. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 5 V, f_{SW} = 600 kHz, MOSFET = SI4204DY, FPWM Mode

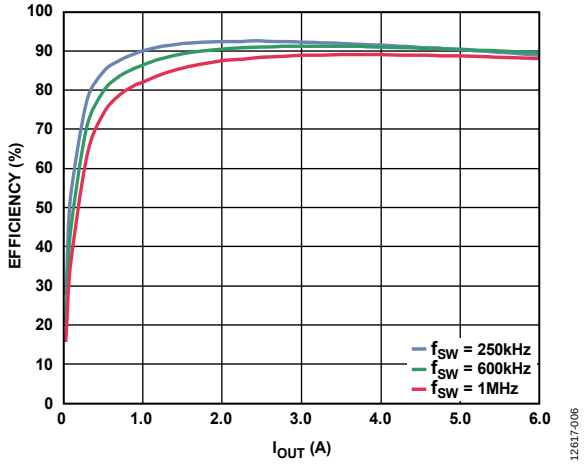


Figure 6. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, V_{OUT} = 3.3 V, MOSFET = SI4204DY, FPWM Mode

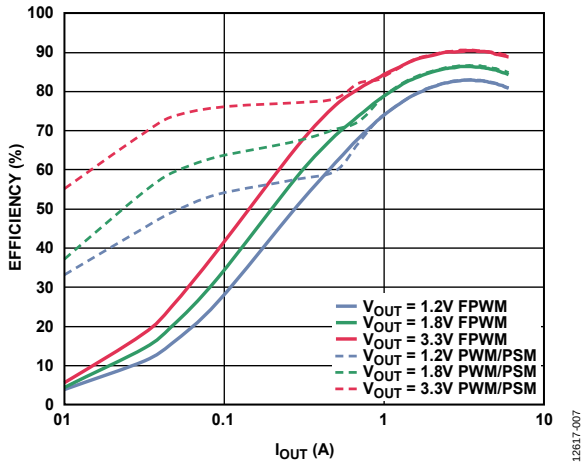


Figure 7. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM and Automatic PWM/PSM Modes

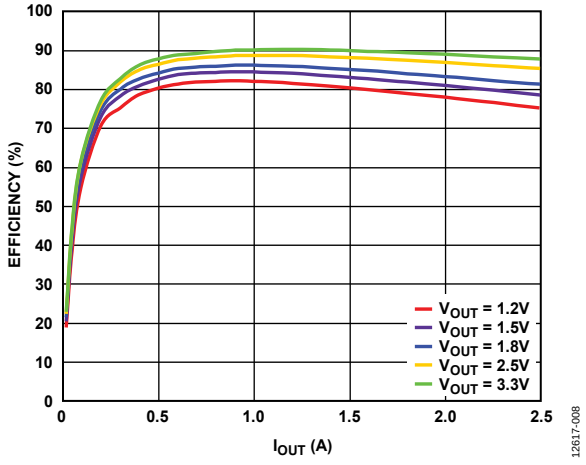


Figure 8. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode

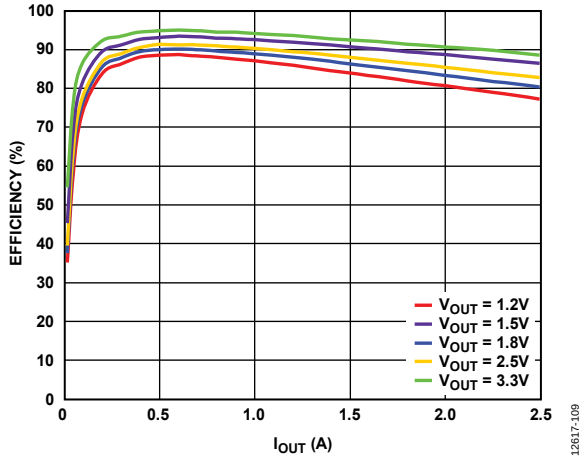


Figure 9. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 5.0 V, f_{SW} = 600 kHz, FPWM Mode

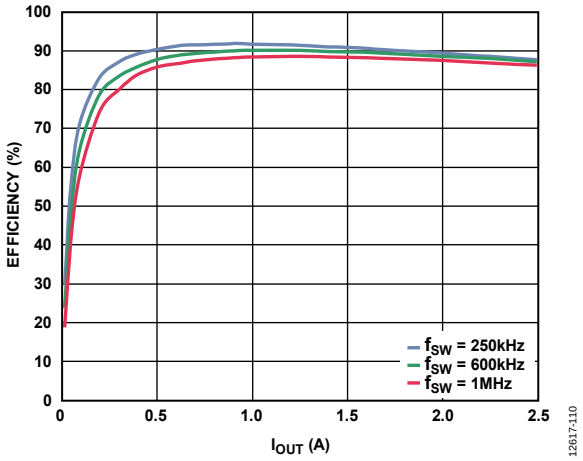


Figure 10. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 12 V, V_{OUT} = 1.8 V, FPWM Mode

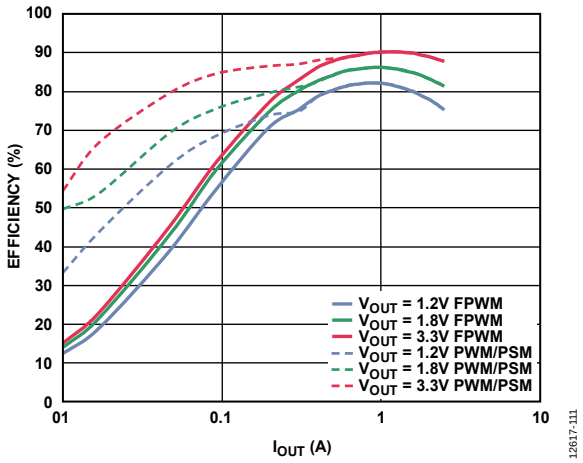


Figure 11. Channel 3/Channel 4 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM and Automatic PWM/PSM Modes

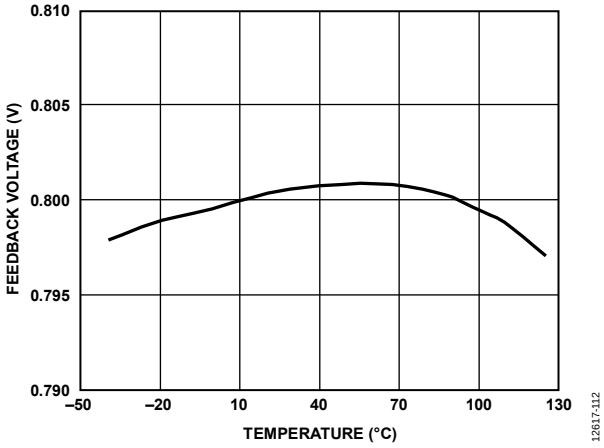


Figure 12. 0.8 V Feedback Voltage Accuracy vs. Temperature for Channel 1, Adjustable Output Model

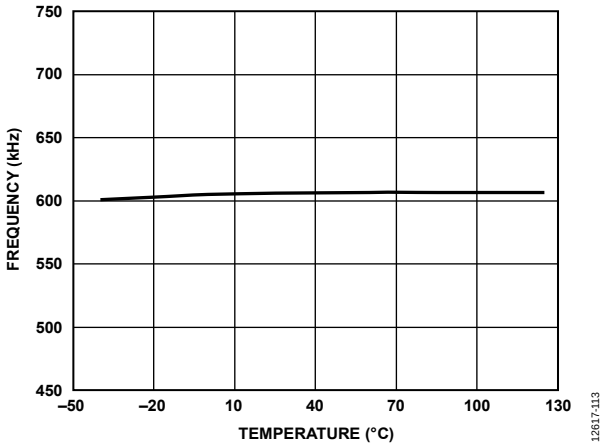


Figure 13. Frequency vs. Temperature, V_{IN} = 12 V, f_{SW} = 600 kHz

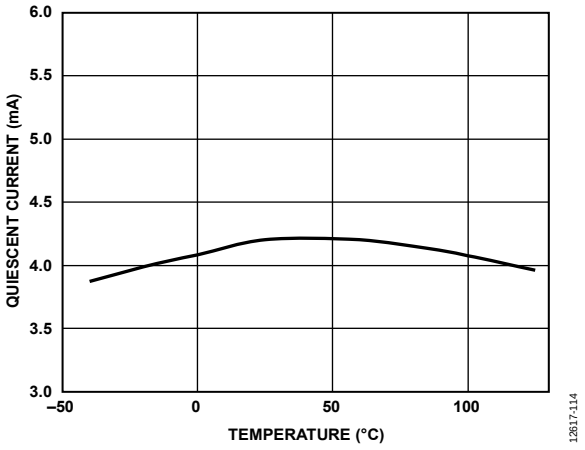


Figure 14. Quiescent Current vs. Temperature (Includes PVIN1, PVIN2, PVIN3, and PVIN4)

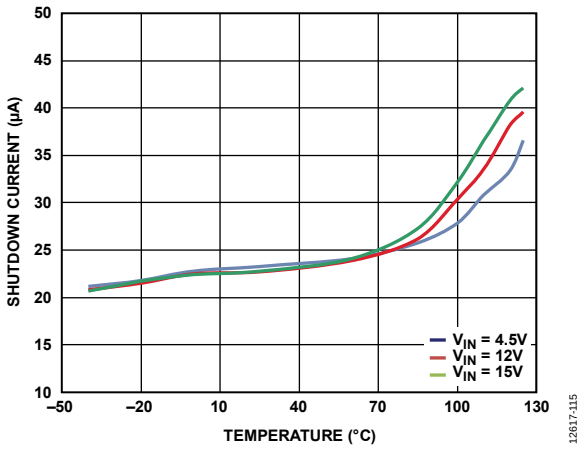


Figure 15. Shutdown Current vs. Temperature (EN1, EN2, EN3, and EN4 Low)

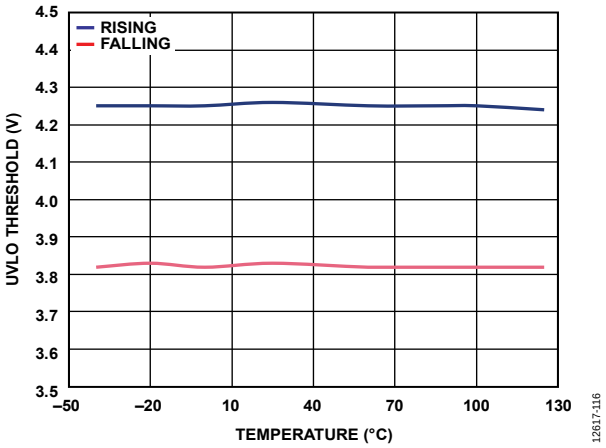


Figure 16. UVLO Threshold vs. Temperature

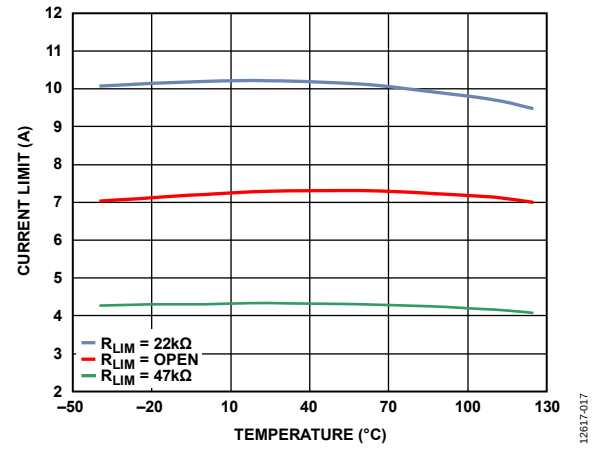


Figure 17. Channel 1/Channel 2 Current Limit vs. Temperature

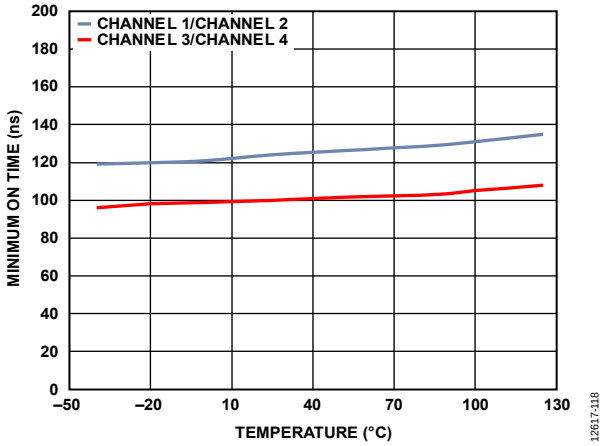


Figure 18. Minimum On Time vs. Temperature

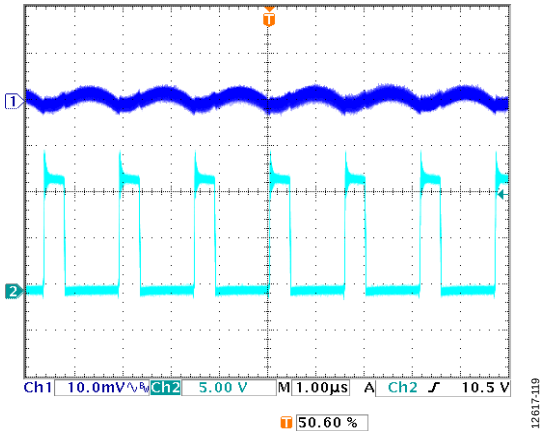


Figure 19. Steady State Waveform at Heavy Load, V_{IN} = 12 V, V_{OUT} = 3.3 V, Output Load Current (I_{OUT}) = 3 A, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 2, FPWM Mode, Channel 1 = V_{OUTX}, Channel 2 = SWx

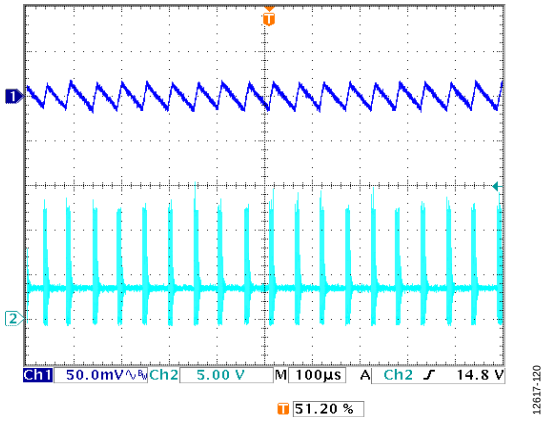


Figure 20. Steady State Waveform at Light Load, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 30 mA, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 2, Automatic PWM/PSM Mode, Channel 1 = V_{OUTX}, Channel 2 = SWx

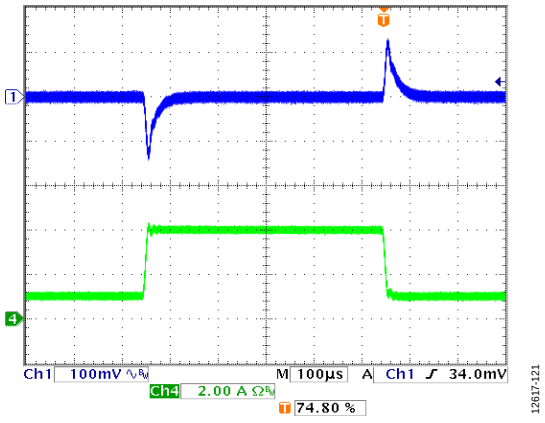


Figure 21. Channel 1/Channel 2 Load Transient, 1 A to 4 A, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, L = 2.2 µH, C_{OUT} = 47 µF × 2, Channel 1 = V_{OUTX}, Channel 4 = I_{OUTX}

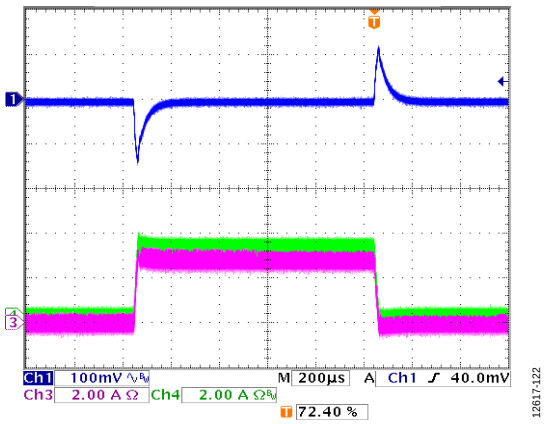


Figure 22. Load Transient, Channel 1/Channel 2 Parallel Output, 0 A to 6 A, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, L = 4.7 µH, C_{OUT} = 47 µF × 4, Channel 1 = V_{OUT}, Channel 3 = I_{L1}, Channel 4 = I_{L2}

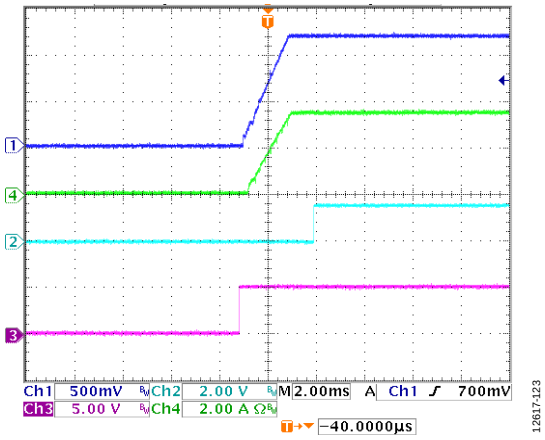


Figure 23. Channel 1 Soft Start with 4 A Resistance Load, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2, Channel 1 = V_{OUT1}, Channel 2 = PWRGD, Channel 3 = EN1, Channel 4 = I_{OUT1}

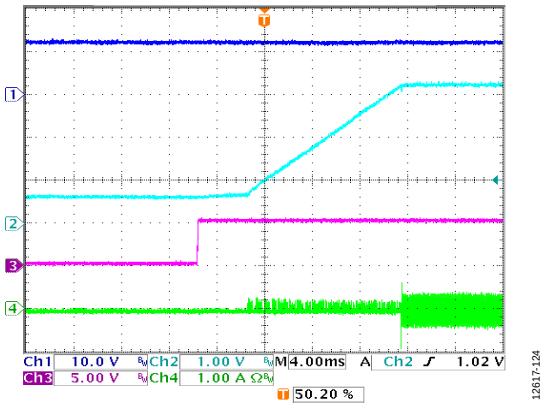


Figure 24. Channel 1 Startup with Precharged Output, V_{IN} = 12 V, V_{OUT} = 3.3 V, Channel 1 = V_{IN}, Channel 2 = V_{OUT1}, Channel 3 = EN1, Channel 4 = I_{L1}

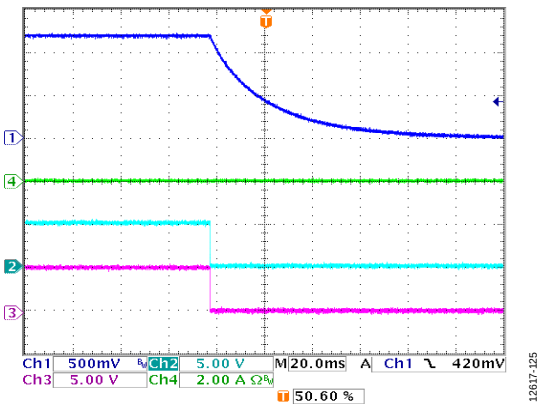


Figure 25. Channel 1 Shutdown with Active Output Discharge, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2, Channel 1 = V_{OUT1}, Channel 2 = EN1, Channel 3 = PWRGD, Channel 4 = I_{OUT1}

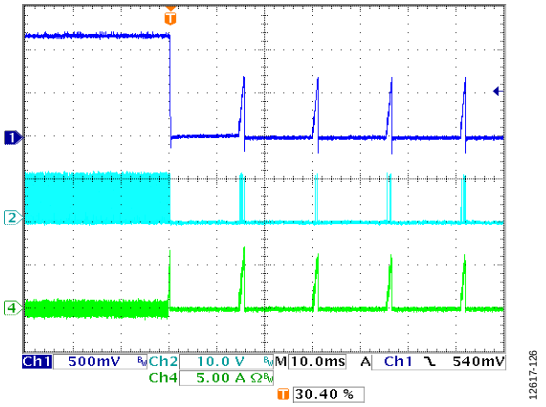


Figure 26. Short-Circuit Protection Entry, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2, Channel 1 = V_{OUTX}, Channel 2 = SWx, Channel 4 = I_{LX}

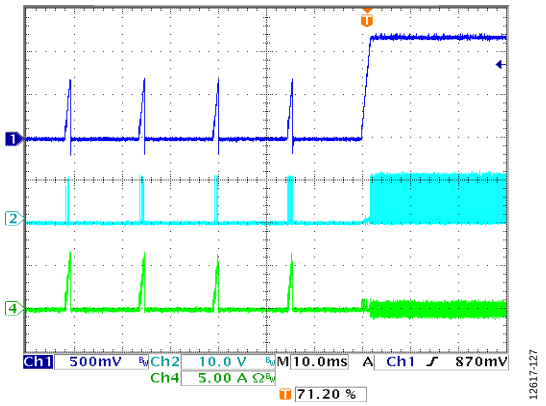


Figure 27. Short-Circuit Protection Recovery, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 2, Channel 1 = V_{OUTX}, Channel 2 = SWx, Channel 4 = I_{LX}

THEORY OF OPERATION

The ADP5054 is a micropower management unit that combines four high performance buck regulators in a 48-lead LFCSP package to meet demanding performance and board space requirements. The device enables direct connection to high input voltages of up to 15.5 V with no preregulators to make applications simpler and more efficient.

BUCK REGULATOR OPERATIONAL MODES

PWM Mode

In pulse width modulation (PWM) mode, the buck regulators in the ADP5054 operate at a fixed frequency; this frequency is set by an internal oscillator that is programmed by the RT pin. At the start of each oscillator cycle, the high-side MOSFET switch turns on and sends a positive voltage across the inductor. The inductor current increases until the current-sense signal exceeds the peak inductor current threshold that turns off the high-side MOSFET switch; this threshold is set by the error amplifier output. During the high-side MOSFET off time, the inductor current decreases through the low-side MOSFET switch until the next oscillator clock pulse starts a new cycle. The buck regulators in the ADP5054 regulate the output voltage by adjusting the peak inductor current threshold.

PSM Mode

To achieve higher efficiency, the buck regulators in the ADP5054 smoothly transition to variable frequency, power savings mode (PSM) operation when the output load falls below the PSM current threshold. When the output voltage falls below regulation, the buck regulator enters PWM mode for a few oscillator cycles until the voltage increases to within regulation. During the idle time between bursts, the MOSFET switch turns off, and the output capacitor supplies all the output current.

The PSM mode comparator monitors the internal compensation node, which represents the peak inductor current information. The average PSM mode current threshold depends on the input voltage (V_{IN}), the output voltage (V_{OUT}), the inductor, and the output capacitor. Because the output voltage occasionally falls below regulation and then recovers, the output voltage ripple in PSM mode is larger than the ripple in forced PWM (FPWM) mode under light load conditions.

Forced PWM and Automatic PWM/PSM Modes

The buck regulators can be configured to always operate in forced PWM (FPWM) mode using the SYNC/MODE pin. In FPWM mode, the regulator continues to operate at a fixed frequency even when the output current is below the PWM/PSM threshold. In PWM mode, efficiency is lower compared to PSM mode under light load conditions. The low-side MOSFET remains on when the inductor current falls to less than 0 A, causing the ADP5054 to enter continuous conduction mode (CCM).

The buck regulators can be configured to operate in automatic PWM/PSM mode using the SYNC/MODE pin. In automatic PWM/PSM mode, the buck regulators operate in either PWM mode or PSM mode, depending on the output current. When the average output current falls below the PWM/PSM threshold, the buck regulator enters PSM mode; in PSM mode, the regulator operates with a reduced switching frequency to maintain high efficiency. The low-side MOSFET turns off when the output current reaches 0 A, causing the regulator to operate in discontinuous mode (DCM).

The user can alternate between FPWM mode and automatic PWM/PSM mode during operation. The flexible configuration capability during device operation enables efficient power management.

When a logic high level is applied to the SYNC/MODE pin (or when SYNC/MODE is configured as a clock input or output), the operational mode of all four buck regulators is set for forced PWM mode. When a logic low level is applied to the SYNC/MODE pin, the operational mode of all four buck regulators is automatic PWM/PSM mode.

Table 7 describes the function of the SYNC/MODE pin in setting the operational mode of the device.

Table 7. Configuring the Mode of Operation Using the SYNC/MODE Pin

SYNC/MODE Pin	Mode of Operation for All Channels
High	Forced PWM mode
Clock In/Out	Forced PWM mode
Low	Automatic PWM/PSM mode

ADJUSTABLE AND FIXED OUTPUT VOLTAGE

The ADP5054 provides adjustable and fixed output voltage settings via the factory fuse. For the adjustable output settings, use an external resistor divider to set the desired output voltage via the feedback reference voltage (0.8 V for Channel 1 to Channel 4).

For the fixed output settings, the feedback resistor divider is built into the ADP5054, and the feedback pin (FBx) must be tied directly to the output. Each buck regulator channel can be programmed for a specific output voltage.

If a different output voltage range is required, contact your local Analog Devices, Inc., sales or distribution representative.

INTERNAL REGULATORS (VREG AND VDD)

The internal VREG regulator in the ADP5054 provides a stable 5.0 V power supply for the bias voltage of the MOSFET drivers. The internal VDD regulator in the ADP5054 provides a stable 3.3 V power supply for the internal control circuits. One 1.0 µF ceramic capacitor must be connected between VREG and ground, and another 1.0 µF ceramic capacitor must be connected between VDD and ground.

The internal VREG and VDD regulators are active as long as PVIN1 is available. The internal VREG regulator can provide a total load of 150 mA, including the MOSFET driving current. The current-limit circuit is included in the VREG regulator to protect the circuit when the device is heavily loaded.

Note that the VDD regulator is for internal circuit use and is not recommended for other purposes.

SEPARATE SUPPLY APPLICATIONS

The ADP5054 supports separate input voltages for the four buck regulators, meaning the input voltages for the four buck regulators can be connected to different supply voltages. The PVIN1 voltage provides the power supply for the internal regulators and the control circuitry. Therefore, if the user plans to use separate supply voltages for the buck regulators, the PVIN1 voltage must be above the UVLO threshold before the other channels begin to operate.

Note that precision enabling can be used to monitor the PVIN1 voltage and to delay the startup of the outputs to ensure that PVIN1 is high enough to support the outputs in regulation (see the Precision Enabling section).

The ADP5054 supports cascading supply operations for the four buck regulators. As shown in Figure 28, PVIN2, PVIN3, and PVIN4 are powered from the Channel 1 output. In this configuration, the Channel 1 output voltage must be higher than the UVLO threshold for PVIN2, PVIN3, and PVIN4.

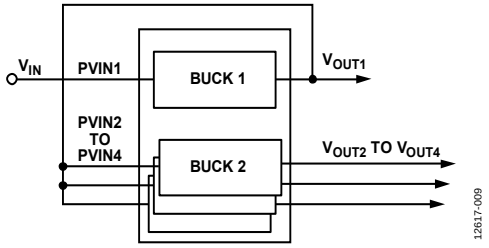


Figure 28. Cascading Supply Application

LOW-SIDE DEVICE SELECTION

The buck regulators in Channel 1 and Channel 2 integrate 6 A high-side power MOSFETs and low-side MOSFET drivers. The N-channel MOSFETs selected for use with the ADP5054 must be able to work with the synchronized buck regulators. In general, use a low $R_{DS(ON)}$ N-channel MOSFET to achieve higher efficiency; dual MOSFETs in one package (for both Channel 1 and Channel 2) are recommended to save space on the printed circuit board (PCB). For more information, see the Low-Side Power Device Selection section.

BOOTSTRAP CIRCUITRY

Each buck regulator in the ADP5054 has an integrated boot regulator. The boot regulator requires a 0.1 µF ceramic capacitor (X5R or X7R) between the BSTx and SWx pins to provide the gate drive voltage for the high-side MOSFET.

ACTIVE OUTPUT DISCHARGE SWITCH

Each buck regulator in the ADP5054 integrates a discharge switch from the switching node to ground. This switch is turned on when its associated regulator is disabled, which helps to discharge the output capacitor quickly. The typical value of the discharge switch is 120 Ω for Channel 1 to Channel 4.

PRECISION ENABLING

The ADP5054 has an enable control pin for each regulator, including the LDO regulator. Each enable control pin (ENx) features a precision enable circuit with a 0.811 V reference voltage. When the voltage at the ENx pin is greater than 0.811 V, the regulator is enabled. When the ENx pin voltage falls below 0.72 V, the regulator is disabled. An internal 1 MΩ pull-down resistor prevents errors if the ENx pin is left floating.

The precision enable threshold voltage allows easy sequencing of channels within the device, as well as sequencing between the ADP5054 and other input/output supplies. The ENx pin can also be used as a programmable UVLO input using a resistor divider (see Figure 29).

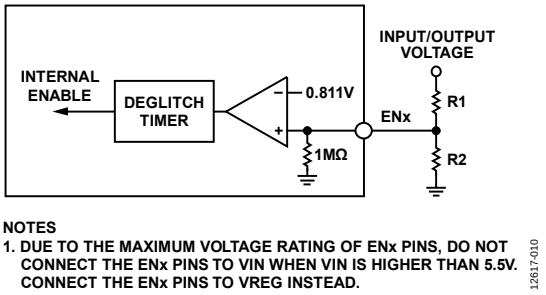


Figure 29. Precision Enable Diagram for One Channel

The ENx pin voltage must be lower than 5.5V. Do not connect ENx pin to PVINx pin in high input voltage applications. For automatic startup when input supply is available, connect ENx pin to the internal VREG regulator. If some channels are unused, pull down the corresponding PVINx and ENx pin to ground and leave the SWx, BSTx, COMPx and FBx pins floating.

OSCILLATOR

The switching frequency (f_{SW}) of the ADP5054 can be set to a value from 250 kHz to 2.0 MHz by connecting a resistor from the RT pin to ground. The value of the RT resistor can be calculated as follows:

$$R_{RT}\,(\text{k}\Omega) = [14{,}822/f_{SW}\,(\text{kHz})]^{1.081}$$

Figure 30 shows the typical relationship between f_{SW} and the RT resistor. The adjustable frequency allows users to make decisions based on the trade-off between efficiency and the size of the solution.

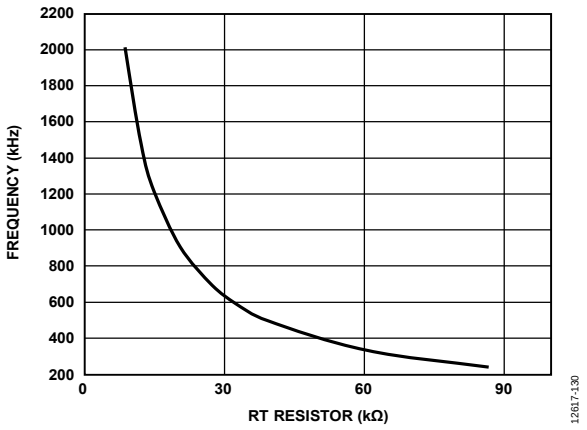


Figure 30. Switching Frequency vs. RT Resistor

The frequency in each channel can be set to half the master switching frequency set by the RT pin. This setting is configured using the CFG12 and CFG34 pins (see Table 8 and Table 9). This halving of the frequency is not recommended if the switching frequency is less than 250 kHz.

Phase Shift

By default, the phase shift between Channel 1 and Channel 2 and between Channel 3 and Channel 4 is 180° (see Figure 31). This value provides the benefits of out-of-phase operation by reducing the input ripple current and lowering the grounding noise.

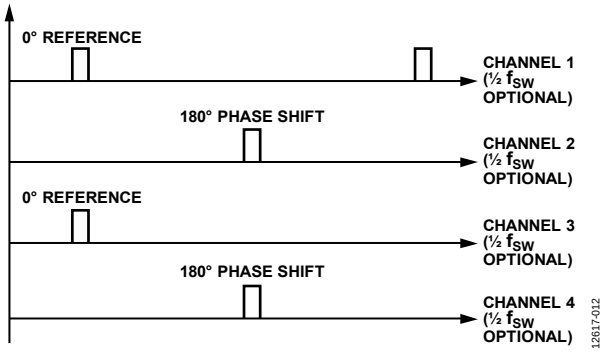


Figure 31. Phase Shift Diagram, Four Buck Regulators

SYNCHRONIZATION INPUT/OUTPUT

The switching frequency of the ADP5054 can be synchronized to an external clock with a frequency range from 250 kHz to 2.0 MHz. The ADP5054 automatically detects the presence of an external clock applied to the SYNC/MODE pin, and the switching frequency transitions smoothly to the frequency of the external clock. When the external clock signal stops, the device automatically switches back to the internal clock and continues to operate.

Note that the internal switching frequency set by the RT pin must be programmed to a value that is close to the external clock value for successful synchronization; the suggested frequency difference is less than ±15% in typical applications.

The SYNC/MODE pin can be configured as a synchronization clock output using CFG34 (see Table 9). A positive clock pulse with a 50% duty cycle is generated at the SYNC/MODE pin with a frequency equal to the internal switching frequency set by the RT pin. There is a short delay time (approximately 15% of t_{SW}) from the generated synchronization clock to the Channel 1 switching node.

Figure 32 shows two ADP5054 devices configured for frequency synchronization mode: one ADP5054 device is configured as the clock output to synchronize another ADP5054 device. It is recommended that a 100 kΩ pull-up resistor be used to prevent logic errors when the SYNC/MODE pin is left floating.

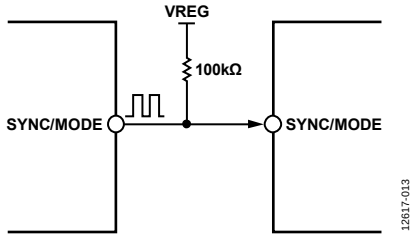


Figure 32. Two ADP5054 Devices Configured for Synchronization Mode

In the configuration shown in Figure 32, the phase shift between Channel 1 of the first ADP5054 device and Channel 1 of the second ADP5054 device is 0° (see Figure 33).

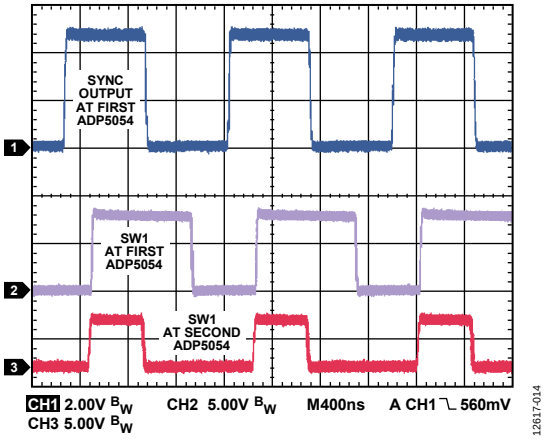


Figure 33. Waveforms of Two ADP5054 Devices Operating in Synchronization Mode

Table 8. CFG12 Configuration (Channel 1 and Channel 2)[1]

		Channel 1		Channel 2		
R_{TOP} (kΩ)	R_{BOT} (kΩ)	Soft Start (ms)	Frequency (kHz)	Soft Start (ms)	Frequency (kHz)	Parallel or Individual Operation
0	N/A	16	1 × f_{SW}	16	1 × f_{SW}	Individual
100	600	16	½ × f_{SW}	16	½ × f_{SW}	Individual
200	500	2	1 × f_{SW}	2	½ × f_{SW}	Individual
300	400	2	½ × f_{SW}	2	1 × f_{SW}	Individual
400	300	16	½ × f_{SW}	N/A	N/A	Parallel
500	200	16	1 × f_{SW}	N/A	N/A	Parallel
600	100	2	1 × f_{SW}	N/A	N/A	Parallel
N/A	0	2	1 × f_{SW}	2	1 × f_{SW}	Individual

[1] N/A means not applicable.

Table 9. CFG34 Configuration (Channel 3, Channel 4, and SYNC/MODE)[1]

		Channel 3		Channel 4			
R_{TOP} (kΩ)	R_{BOT} (kΩ)	Soft Start (ms)	Frequency (kHz)	Soft Start (ms)	Frequency (kHz)	Parallel or Individual Operation	SYNC/MODE or Clock Out
0	N/A	16	1 × f_{SW}	16	1 × f_{SW}	Individual	SYNC/MODE
100	600	16	½ × f_{SW}	16	½ × f_{SW}	Individual	SYNC/MODE
200	500	2	½ × f_{SW}	2	1 × f_{SW}	Individual	SYNC/MODE
300	400	16	½ × f_{SW}	N/A	N/A	Parallel	SYNC/MODE
400	300	2	1 × f_{SW}	N/A	N/A	Parallel	SYNC/MODE
500	200	16	1 × f_{SW}	N/A	N/A	Parallel	Clock out (FPWM)
600	100	2	1 × f_{SW}	2	1 × f_{SW}	Individual	Clock out (FPWM)
N/A	0	2	1 × f_{SW}	2	1 × f_{SW}	Individual	SYNC/MODE

[1] N/A means not applicable.

SOFT START

The buck regulators in the ADP5054 include soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. The soft start time is typically fixed at 2 ms for each buck regulator when the CFG12 and CFG34 pins are tied to ground.

To set the soft start time to a value of 2 ms or 16 ms, connect a resistor divider from the CFG12 pin or the CFG34 pin to the VREG pin and ground (see Figure 34). This configuration may be required to accommodate a specific start-up sequence or an application with a large output capacitor.

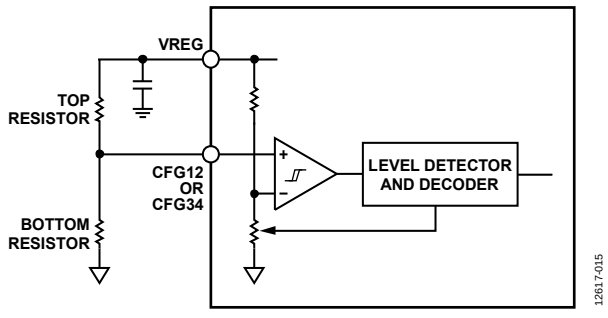


Figure 34. Level Detector Circuit for Soft Start

The CFG12 pin can be used to program the soft start time, ½× frequency setting, and parallel operation for Channel 1 and Channel 2. The CFG34 pin can be used to program the soft start time, ½× frequency setting, parallel operation, and clock output feature for Channel 3 and Channel 4. Table 8 and Table 9 provide the values of the resistors needed to set the soft start time.

PARALLEL OPERATION

The ADP5054 supports two-phase parallel operation of Channel 1 and Channel 2 to provide a single output with up to 12 A of current, and two-phase parallel operation of Channel 3 and Channel 4 to provide a single output with up to 5 A of current.

To configure a two-phase single output in parallel operation, take the following steps (see Figure 35):

- Use the CFG12 pin (or CFG34 pin) to select parallel operation as specified in Table 8 and Table 9.
- Leave the COMP2 pin (or COMP4 pin) open.
- Use the FB1 pin (or FB3 pin) to set the output voltage.
- Connect the FB2 pin (or FB4 pin) to ground (FB2 or FB4 is ignored).
- Connect the EN2 pin (or EN4 pin) to ground (EN2 or EN4 is ignored).

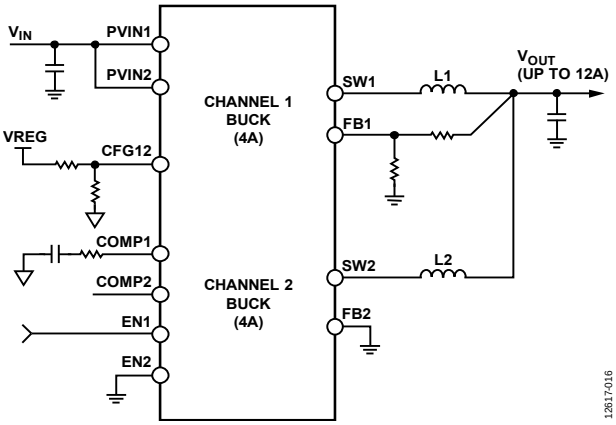


Figure 35. Parallel Operation for Channel 1 and Channel 2

The following considerations apply when two channels are operated in parallel configuration.

- The input voltages and current-limit settings for both channels must be the same.
- Both channels must be operated in FPWM mode.

Current balance in parallel configuration is well regulated by the internal control loop. Figure 36 shows the Channel 1 and Channel 2 typical current balance matching in parallel output configuration. Figure 37 shows the Channel 3 and Channel 4 current balance matching in parallel output configuration.

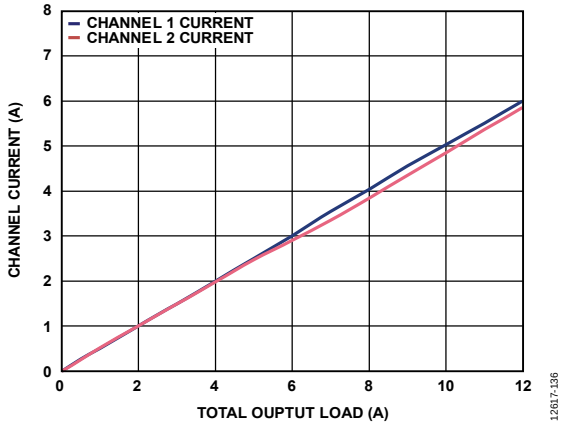


Figure 36. Channel 1 and Channel 2 Current Balance in Parallel Output Configuration, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode

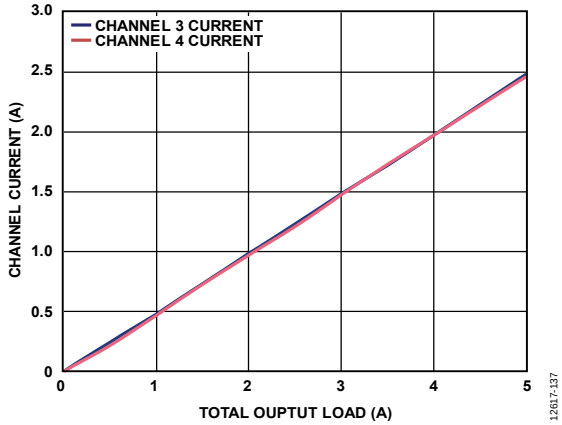


Figure 37. Channel 3 and Channel 4 Current Balance in Parallel Output Configuration, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode

STARTUP WITH PRECHARGED OUTPUT

The buck regulators in the ADP5054 include a precharged start-up feature to protect the low-side FETs from damage during startup. If the output voltage is precharged before the regulator is turned on, the regulator prevents reverse inductor current—which would discharge the output capacitor—until the internal soft start reference voltage exceeds the precharged voltage on the feedback (FBx) pin.

CURRENT-LIMIT PROTECTION

The buck regulators in the ADP5054 include peak current-limit protection circuitry to limit the amount of positive current flowing through the high-side MOSFET switch. The peak current limit on the power switch limits the amount of current that can flow from the input to the output. The programmable current-limit threshold feature allows the use of small size inductors for low current applications.

To configure the current-limit threshold for Channel 1, connect a resistor from the DL1 pin to ground; to configure the current-limit threshold for Channel 2, connect another resistor from the DL2 pin to ground. Table 10 lists the peak current-limit threshold settings for Channel 1 and Channel 2.

Table 10. Peak Current-Limit Threshold Settings for Channel 1 and Channel 2

R_{ILIM1} or R_{ILIM2}	Typical Peak Current-Limit Threshold (A)
Floating	6.9
47 kΩ	3.8
22 kΩ	10.4

The buck regulators in the ADP5054 include negative current-limit protection circuitry to limit certain amounts of negative current flowing through the low-side MOSFET switch.

FREQUENCY FOLDBACK

The buck regulators in the ADP5054 include frequency foldback to prevent output current runaway when a hard short occurs on the output. Frequency foldback is implemented as follows:

- If the voltage at the FBx pin falls below half of the target output voltage, the switching frequency is reduced by half.
- If the voltage at the FBx pin falls again to below one-fourth of the target output voltage, the switching frequency is reduced by half of its current value again, as one-fourth of f_{SW}.

The reduced switching frequency allows more time for the inductor current to decrease but also increases the ripple current during peak current regulation. This results in a reduction in average current and prevents output current runaway.

PULSE SKIP IN MAXIMUM DUTY

Under maximum duty cycle conditions, frequency foldback maintains the output in regulation. If the maximum duty cycle is reached—for example, when the input voltage decreases—the PWM modulator skips every other PWM pulse, resulting in a switching frequency foldback of one-half of the switching

frequency. If the maximum duty cycle increases further, the PWM modulator skips two of every three PWM pulses, resulting in a switching frequency foldback that is one-third of the switching frequency. Frequency foldback increases the effective maximum duty cycle, thereby decreasing the dropout voltage between the input and output voltages.

SHORT-CIRCUIT PROTECTION (SCP)

The buck regulators in the ADP5054 include a hiccup mode for overcurrent protection (OCP). When the peak inductor current reaches the current-limit threshold, the high-side MOSFET turns off, and the low-side MOSFET turns on until the next cycle.

When hiccup mode is active, the overcurrent fault counter is incremented. If the overcurrent fault counter reaches 15 and overflows (indicating a short-circuit condition), both the high-side and low-side MOSFETs are turned off. The buck regulator remains in hiccup mode for a period equal to seven soft start cycles and then attempts to restart from soft start. If the short-circuit fault clears, the regulator resumes normal operation; otherwise, it reenters hiccup mode after the soft start.

Hiccup protection is masked during the initial soft start cycle to enable startup of the buck regulator under heavy load conditions. Note that careful design and proper component selection are required to ensure that the buck regulator recovers from hiccup mode under heavy loads. The hiccup protection can be disabled by the factory fuse for each buck regulator. When hiccup protection is disabled, the frequency foldback feature is still used for overcurrent protection.

LATCH-OFF PROTECTION

The buck regulators in the ADP5054 have an optional latch-off mode to protect the device from serious problems such as short-circuit conditions. Latch-off mode can be enabled via the factory fuse.

Short-Circuit Latch-Off Mode

Short-circuit latch-off mode is enabled by the factory fuse. When short-circuit latch-off mode is enabled and the protection circuit detects an overcurrent status after a soft start, the buck regulator enters hiccup mode and attempts to start up again. If seven continuous retry attempts are made and the regulator remains in the fault condition, the regulator is shut down. This shutdown (latch-off) condition is cleared only by reenabling the channel or by resetting the channel power supply.

The operation of short-circuit latch-off protection is shown in Figure 38.

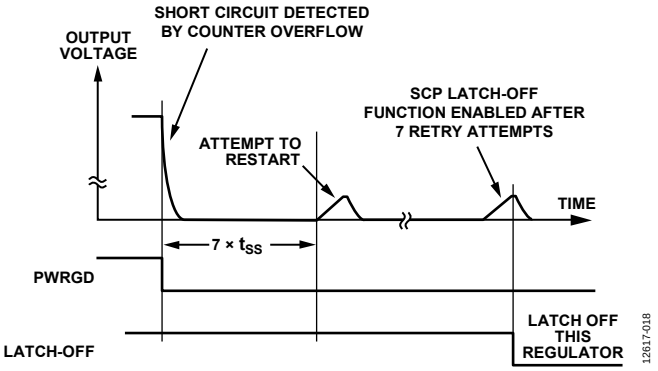


Figure 38. Short-Circuit Latch-Off Detection

Note that short-circuit latch-off mode does not work if hiccup protection is disabled.

UNDERVOLTAGE LOCKOUT (UVLO)

Undervoltage lockout circuitry monitors the input voltage level of each buck regulator in the ADP5054. If any input voltage (PVINx pin) falls below 3.79 V (typical), the corresponding channel is turned off. After the input voltage rises above 4.22 V (typical), the soft start period is initiated, and the corresponding channel is enabled when the ENx pin is high.

Note that a UVLO condition on Channel 1 (PVIN1 pin) has a higher priority than a UVLO condition on other channels, which means that the PVIN1 supply must be available before other channels can be operated.

POWER-GOOD FUNCTION

The ADP5054 includes an open-drain power-good output (PWRGD pin) that becomes active high when the Channel 1 buck regulators are operating normally.

A high status on the PWRGD pin indicates that the regulated output voltage of the buck regulator is above 90.5% (typical) of its nominal output. When the regulated output voltage of the buck regulator falls below 87.2% (typical) of its nominal output for a delay time greater than approximately 50 µs, the status of the PWRGD pin is set low.

The PWRGD pin can be programmed by the factory fuse to indicate the outputs of other specific channels.

THERMAL SHUTDOWN

If the ADP5054 junction temperature exceeds 150°C, the thermal shutdown (TSD) circuit turns off the IC except for the internal linear regulator. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that the ADP5054 does not return to operation after thermal shutdown until the on-chip temperature falls below 135°C. When the device exits thermal shutdown, a soft start is initiated for each enabled channel.

APPLICATIONS INFORMATION

ADIsimPOWER DESIGN TOOL

The ADP5054 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produces complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic and bill of materials and to calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and part count while taking into consideration the operating conditions and limitations of the IC and all real external components. The ADIsimPower tool can be found at www.analog.com/ADIsimPower; the user can request an unpopulated board through the tool.

PROGRAMMING THE OUTPUT VOLTAGE

The output voltage of the ADP5054 is externally set by a resistive voltage divider from the output voltage to the FBx pin. To limit the degradation of the output voltage accuracy due to FBx bias current, ensure that the bottom resistor in the divider is not too large; a value of less than 200 kΩ is recommended.

The equation for the output voltage setting is

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

where:
V_{OUT} is the output voltage.
V_{REF} is the 0.8 V feedback reference voltage.
R_{TOP} is the feedback resistor from V_{OUT} to FBx.
R_{BOT} is the feedback resistor from FBx to ground.

No resistor divider is required in the fixed output options. Each channel can be programmed to have a specific output voltage over a specific range. If a different fixed output voltage is required, contact your local Analog Devices sales or distribution representative.

VOLTAGE CONVERSION LIMITATIONS

For a given input voltage, upper and lower limitations on the output voltage exist due to the minimum on time and the minimum off time.

The minimum output voltage for a given input voltage and switching frequency is limited by the minimum on time. The minimum on time for Channel 1 and Channel 2 is 115 ns (typical); the minimum on time for Channel 3 and Channel 4 is 95 ns (typical). The minimum on time increases at higher junction temperatures.

Note that in forced PWM mode, Channel 1 and Channel 2 can potentially exceed the nominal output voltage when the minimum on time limit is exceeded. Careful switching frequency selection is required to avoid this problem.

The minimum output voltage in FPWM mode for a given input voltage and switching frequency can be calculated using the following equation:

$$V_{OUT\_MIN} = V_{IN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON1} - R_{DSON2}) \times I_{OUT\_MIN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON2} + R_L) \times I_{OUT\_MIN} \quad (1)$$

where:
V_{OUT_MIN} is the minimum output voltage.
t_{MIN_ON} is the minimum on time.
f_{SW} is the switching frequency.
R_{DSON1} is the high-side MOSFET on resistance.
R_{DSON2} is the low-side MOSFET on resistance.
I_{OUT_MIN} is the minimum output current.
R_L is the resistance of the output inductor.

The maximum output voltage for a given input voltage and switching frequency is limited by the minimum off time and the maximum duty cycle. Note that the frequency foldback feature helps to increase the effective maximum duty cycle by lowering the switching frequency, thereby decreasing the dropout voltage between the input and output voltages (see the Frequency Foldback section).

The maximum output voltage for a given input voltage and switching frequency can be calculated using the following equation:

$$V_{OUT\_MAX} = V_{IN} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON1} - R_{DSON2}) \times I_{OUT\_MAX} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON2} + R_L) \times I_{OUT\_MAX} \quad (2)$$

where:
V_{OUT_MAX} is the maximum output voltage.
t_{MIN_OFF} is the minimum off time.
f_{SW} is the switching frequency.
R_{DSON1} is the high-side MOSFET on resistance.
R_{DSON2} is the low-side MOSFET on resistance.
I_{OUT_MAX} is the maximum output current.
R_L is the resistance of the output inductor.

As shown in Equation 1 and Equation 2, reducing the switching frequency eases the minimum on time and minimum off time limitations.

CURRENT-LIMIT SETTING

The ADP5054 has three selectable current-limit thresholds for Channel 1 and Channel 2. Ensure that the selected current-limit value is larger than the peak current of the inductor, I_{PEAK}. See Table 10 for the current-limit configurations for Channel 1 and Channel 2.

SOFT START SETTING

The buck regulators in the ADP5054 include soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. To set the soft start time to a value of 2 ms or 16 ms, connect a resistor divider from the CFG12 pin or the CFG34 pin to the VREG pin and ground (see the Soft Start section).

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor yields faster transient response but degrades efficiency due to the larger inductor ripple current. Using a large inductor value yields a smaller ripple current and better efficiency but results in slower transient response. Thus, a trade-off must be made between transient response and efficiency. As a guideline, the inductor ripple current, ΔI_L, is typically set to a value from 30% to 40% of the maximum load current. The inductor value can be calculated using the following equation:

$$L = ((V_{IN} - V_{OUT}) \times D)/(\Delta I_L \times f_{SW})$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).
ΔI_L is the inductor ripple current.
f_{SW} is the switching frequency.

The ADP5054 has internal slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is greater than 50%.

The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{OUT} + (\Delta I_L/2)$$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a fast saturation characteristic, the saturation current rating of the inductor must be higher than the current-limit threshold of the buck regulator to prevent the inductor from becoming saturated.

The rms current of the inductor can be calculated using the following equation:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low electromagnetic interference (EMI). Table 11 lists the recommended inductors.

Table 11. Recommended Inductors

Vendor	Part No.	Value (µH)	I_{SAT} (A)	I_{RMS} (A)	DCR (mΩ)	Size (mm)
Coilcraft	XFL4030-332	3.3	5.5	6.6	26	4 × 4
	XFL4030-472	4.7	4.5	5.1	40.1	4 × 4
	XFL4030-682	6.8	3.6	3.9	67.4	4 × 4
	XFL5030-801	0.8	18.5	13	5.14	5 × 5
	XAL5030-122	1.2	12.5	11.1	8.5	5 ×5
	XAL5030-222	2.2	9.2	9.7	13.2	5× 5
	XAL5030-332	3.3	8.7	8.1	21.2	5 × 5
	XAL5030-472	4.7	6.7	5.9	36	5 × 5
TOKO	FDV0530-1R0	1.0	11.2	9.1	9.4	6.2 × 5.8
	FDV0530-2R2	2.2	7.1	7.0	17.3	6.2 × 5.8
	FDV0530-3R3	3.3	5.5	5.3	29.6	6.2 × 5.8
	FDV0530-4R7	4.7	4.6	4.2	46.6	6.2 × 5.8
WE-HCI	744314076	0.76	15	15.5	2.25	7 × 7
	744314110	1.1	13	15	3.15	7 × 7
	744314200	2.0	9	11.5	5.85	7 × 7
	744311330	3.3	8	9.0	9.0	7 × 7

OUTPUT CAPACITOR SELECTION

The selected output capacitor affects both the output voltage ripple and the loop dynamics of the regulator. For example, during load step transients on the output, when the load is suddenly increased, the output capacitor supplies the load until the control loop can ramp up the inductor current, causing an undershoot of the output voltage.

The output capacitance required to meet the voltage drop. requirement can be calculated using the following equation:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
K_{UV} is a factor (typically set to 2).
ΔI_{STEP} is the load step.
L is the output inductor.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.

Another example of the effect of the output capacitor on the loop dynamics of the regulator is when the load is suddenly removed from the output and the energy stored in the inductor rushes into the output capacitor, causing an overshoot of the output voltage.

The output capacitance required to meet the overshoot requirement can be calculated using the following equation:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - V_{OUT}^2}$$

where:
K_{OV} is a factor (typically set to 2).
ΔI_{STEP} is the load step.
ΔV_{OUT_OV} is the allowable overshoot on the output voltage.

The output voltage ripple is determined by the effective series resistance (ESR) of the output capacitor and its capacitance value. Use the following equations to select a capacitor that can meet the output ripple requirements:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

where:
ΔV_{OUT_RIPPLE} is the allowable output voltage ripple.
R_{ESR} is the equivalent series resistance of the output capacitor.

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and C_{OUT_RIPPLE} to meet both load transient and output ripple requirements.

The selected output capacitor voltage rating must be greater than the output voltage. The minimum rms current rating of the output capacitor is determined by the following equation:

$$I_{C_{OUT\_RMS}} = \frac{\Delta I_L}{\sqrt{12}}$$

INPUT CAPACITOR SELECTION

The input decoupling capacitor attenuates high frequency noise on the input and acts as an energy reservoir. This capacitor must be a ceramic capacitor and must be placed close to the PVINx pins. The loop composed of the input capacitor, the high-side NFET, and the low-side NFET must be kept as small as possible. The voltage rating of the input capacitor must be greater than the maximum input voltage. The rms current rating of the input capacitor must be larger than the following equation:

$$I_{C_{IN\_RMS}} = I_{OUT} \times \sqrt{D \times (1-D)}$$

where D is the duty cycle ($D = V_{OUT}/V_{IN}$).

LOW-SIDE POWER DEVICE SELECTION

Channel 1 and Channel 2 have integrated low-side MOSFET drivers that can drive the low-side N-channel MOSFETs (NFETs). The selection of the low-side NFET affects the buck regulator performance.

The selected NFET must meet the following requirements:

- The drain source voltage (V_{DS}) must be higher than $1.2 \times V_{IN}$.
- The drain current (I_D) must be greater than $1.2 \times I_{LIMIT\_MAX}$, where I_{LIMIT_MAX} is the selected maximum current-limit threshold.
- The selected NFET can be fully turned on at $V_{GS} = 4.5$ V, where V_{GS} is the gate to source voltage.
- Total gate charge (gate charge (Q_G) at $V_{GS} = 4.5$ V) must be less than 35 nC. Lower Q_G characteristics provide higher efficiency.

When the high-side NFET is turned off, the low-side NFET supplies the inductor current. For low duty cycle applications, the low-side NFET supplies the current for most of the period. To achieve higher efficiency, it is important to select a NFET with low turn on resistance. The power conduction loss for the low-side NFET (P_{FET_LOW}) can be calculated using the following equation:

$$P_{FET\_LOW} = I_{OUT}^2 \times R_{DSON} \times (1 - D)$$

where:
R_{DSON} is the on resistance of the low-side NFET.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).

Table 12 lists recommended dual NFETs for various current-limit settings. Ensure that the NFET can handle thermal dissipation due to power loss.

Table 12. Recommended Dual NFETs

Vendor	Part No.	V_{DS} (V)	I_D (A)	R_{DSON} (mΩ)	V_{GS} (V)	Q_G (nC)	Size (mm)
Infineon	BSC072N0-3LD[1]	30	20	7.2	1.0 to 2.2	15	5 × 6
	BSO220N-03MD	30	7.7	27	1.0 to 2.1	3.8	5 × 6
Vishay	Si4204DY[1]	20	20	6	1.0 to 2.4	14.5	5 × 6
	Si7232DN[2]	20	25	16.4	0.4 to 1.0	12	3 × 3
	SiA906EDJ[2]	20	4.5	46	0.6 to 1.5	3.5	2 × 2
Fairchild	FDMA1024[2]	20	5.0	54	0.4	5.2	2 × 2
	FDMB3900	25	7.0	33	1	11	3 × 2

[1] This dual NFET is fully evaluated and recommend for high input voltage (12 V) and high output current applications.
[2] This dual NFET is recommend for solution size compact application, and is sensitive to layout in high input voltage and output current applications.

To avoid an unexpected short circuit of the high-side and low-side NFETs, select the lower charge of gate and drain (Q_{GD}) of the dual external NFETs and keep the gate driver traces as short as possible in PCB design. It is important to select a higher V_{GS} NFET to immune the miller spike and reduce the risk of short circuit through the high-side and low-side NFET.

PROGRAMMING THE UVLO INPUT

The precision enable input can be used to program the UVLO threshold of the input voltage, as shown in Figure 29. To limit the degradation of the input voltage accuracy due to the internal 1 mΩ pull-down resistor tolerance, ensure that the bottom resistor in the divider is not too large; a value of less than 50 kΩ is recommended.

The precision turn-on threshold is 0.811 V. The resistive voltage divider for the programmable V_{IN} start-up voltage is calculated as follows:

$$V_{IN\_STARTUP} = (0.8\ nA + (0.811\ V/R_{BOT\_EN})) \times (R_{TOP\_EN} + R_{BOT\_EN})$$

where:
R_{TOP_EN} is the resistor from V_{IN} to ENx.
R_{BOT_EN} is the resistor from ENx to ground.

COMPENSATION COMPONENTS DESIGN

For the peak current-mode control architecture, the power stage can be simplified as a voltage controlled current source that supplies current to the output capacitor and load resistor. The simplified loop is composed of one domain pole and a zero contributed by the output capacitor ESR. The control-to-output transfer function is shown in the following equations:

$$G_{vd}(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_z}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_p}\right)}$$

$$f_z = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$f_p = \frac{1}{2 \times \pi \times (R + R_{ESR}) \times C_{OUT}}$$

where:
A_{VI} = 20 A/V for Channel 1 or Channel 2, and 6.66 A/V for Channel 3 or Channel 4.
R is the load resistance.
R_{ESR} is the equivalent series resistance of the output capacitor.
C_{OUT} is the output capacitance.

The ADP5054 uses a transconductance amplifier as the error amplifier to compensate the system. Figure 39 shows the simplified, peak current-mode control, small signal circuit.

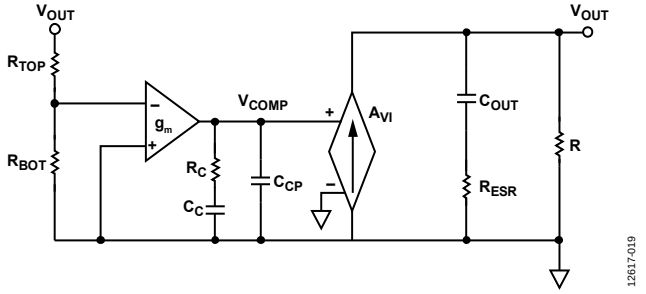


Figure 39. Simplified, Peak Current-Mode Control, Small Signal Circuit

The compensation components, R_C and C_C, contribute a zero, and the optional C_{CP} and R_C contribute an optional pole.

The closed-loop transfer equation is as follows:

$$T_V(s) = \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \times \frac{-g_m}{C_C + C_{CP}} \times \frac{1 + R_C \times C_C \times s}{s \times \left(1 + \frac{R_C \times C_C \times C_{CP}}{C_C + C_{CP}} \times s\right)} \times G_{vd}(s)$$

The following guidelines show how to select the compensation components (R_C, C_C, and C_{CP}) for ceramic output capacitor applications.

1. Determine the cross frequency (f_C). Generally, f_C is between $f_{SW}/12$ and $f_{SW}/6$.
2. R_C can be calculated using the following equation:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{0.8\ V \times g_m \times A_{VI}}$$

3. Place the compensation zero at the domain pole (f_P). C_C can be determined as follows:

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C}$$

4. C_{CP} is optional. It can be used to cancel the zero caused by the ESR of the output capacitor.

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

POWER DISSIPATION

The total power dissipation in the ADP5054 simplifies to

$$P_D = P_{BUCK1} + P_{BUCK2} + P_{BUCK3} + P_{BUCK4}$$

Buck Regulator Power Dissipation

The power dissipation (P_{LOSS}) for each buck regulator includes power switch conductive losses (P_{COND}), switching losses (P_{SW}), and transition losses (P_{TRAN}). Other sources of power dissipation exist, but these sources are generally less significant at the high output currents of the application thermal limit.

Use the following equation to estimate the power dissipation of the buck regulator:

$$P_{LOSS} = P_{COND} + P_{SW} + P_{TRAN}$$

Power Switch Conduction Loss (P_{COND})

Power switch conduction losses are caused by the flow of output current through both the high-side and low-side power switches, each of which has its own internal on resistance ($R_{DS(ON)}$).

Use the following equation to estimate the power switch conduction loss:

$$P_{COND} = (R_{DS(ON)\_HS} \times D + R_{DS(ON)\_LS} \times (1 - D)) \times I_{OUT}^2$$

where:
$R_{DS(ON)\_HS}$ is the high-side MOSFET on resistance.
$R_{DS(ON)\_LS}$ is the low-side MOSFET on resistance.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).

Switching Loss (P_{SW})

Switching losses are associated with the current drawn by the driver to turn the power devices on and off at the switching frequency. Each time a power device gate is turned on or off, the driver transfers a charge from the input supply to the gate, and then from the gate to ground. Use the following equation to estimate the switching loss:

$$P_{SW} = (C_{GATE\_HS} + C_{GATE\_LS}) \times V_{IN}^2 \times f_{SW}$$

where:
C_{GATE_HS} is the gate capacitance of the high-side switch.
C_{GATE_LS} is the gate capacitance of the low-side switch.
f_{SW} is the switching frequency.

Transition Loss (P_{TRAN})

Transition losses occur because the high-side switch cannot turn on or off instantaneously. During a switch node transition, the power switch provides all the inductor current. The source-to-drain voltage of the power switch is half the input voltage, resulting in power loss. Transition losses increase with both load and input voltage and occur twice for each switching cycle. Use the following equation to estimate the transition loss:

$$P_{TRAN} = 0.5 \times V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:
t_R is the rise time of the switch node.
t_F is the fall time of the switch node.

Thermal Shutdown

Channel 1 and Channel 2 store the value of the inductor current only during the on time of the internal high-side MOSFET. Therefore, a small amount of power (as well as a small amount of input rms current) is dissipated inside the ADP5054, which reduces thermal constraints.

However, when Channel 1 and Channel 2 are operating under maximum load with high ambient temperature and high duty cycle, the input rms current can become very large and cause the junction temperature to exceed the absolute maximum rating of 125°C. If the junction temperature exceeds 150°C, the regulator enters thermal shutdown and recovers when the junction temperature falls below 135°C.

JUNCTION TEMPERATURE

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as shown in the following equation:

$$T_J = T_A + T_R$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
T_R is the rise in temperature of the package due to power dissipation.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:
θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package (see Table 5).
P_D is the power dissipation in the package.

An important factor to consider is that the thermal resistance value is based on a 4-layer, 4 inch × 3 inch PCB with 2.5 oz of copper, as specified in the JEDEC standard, whereas real-world applications may use PCBs with different dimensions and a different number of layers.

It is important to maximize the amount of copper used to remove heat from the device. Copper exposed to air dissipates heat better than copper used in the inner layers. The exposed pad must be connected to the ground plane with several vias.

DESIGN EXAMPLES

This section provides an example of the step-by-step design procedures and the external components required for Channel 1. Table 13 lists the design requirements for this example.

Table 13. Example Design Requirements for Channel 1

Parameter	Specification
Input Voltage	V_{PVIN1} = 12 V ± 5%
Output Voltage	V_{OUT1} = 1.2 V
Output Current	I_{OUT1} = 4 A
Output Ripple	ΔV_{OUT1_RIPPLE} = 12 mV in CCM mode
Load Transient	±5%, at 20% to 80% load transient, 1 A/µs

Although this example shows step-by-step design procedures for Channel 1, the procedures also apply to all other buck regulator channels (Channel 2 to Channel 4).

SETTING THE SWITCHING FREQUENCY

The first step is to determine the switching frequency for the ADP5054 design. In general, higher switching frequencies produce a smaller solution size due to the lower component values required, whereas lower switching frequencies result in higher conversion efficiency due to lower switching losses.

The switching frequency of the ADP5054 can be set to a value from 250 kHz to 2 MHz by connecting a resistor from the RT pin to ground. The selected resistor allows users to make decisions based on the trade-off between efficiency and solution size. (For more information, see the Oscillator section.) However, the highest supported switching frequency must be assessed by checking the voltage conversion limitations enforced by the minimum on time and the minimum off time (see the Voltage Conversion Limitations section).

In this design example, a switching frequency of 600 kHz is used to achieve a good combination of small solution size and high conversion efficiency. To set the switching frequency to 600 kHz, use the following equation to calculate the resistor value, R_{RT}:

$$R_{RT}\ (\text{k}\Omega) = [14{,}822/f_{SW}\ (\text{kHz})]^{1.081}$$

Therefore, select standard resistor R_{RT} = 31.6 kΩ.

SETTING THE OUTPUT VOLTAGE

Select a 10 kΩ bottom resistor (R_{BOT}) and then calculate the top feedback resistor using the following equation:

$$R_{BOT} = R_{TOP} \times (V_{REF}/(V_{OUT} - V_{REF}))$$

where:
V_{OUT} is the output voltage.
V_{REF} is 0.8 V for Channel 1 to Channel 4, and 0.5 V for Channel 5.

To set the output voltage to 1.2 V, choose the following resistor values: R_{TOP1} = 4.99 kΩ, R_{BOT1} = 10 kΩ.

SETTING THE CURRENT LIMIT

For 4 A output current operation, the typical peak current limit is 6.9 A. For this example, choose R_{ILIM1} = floating (see Table 10). For more information, see the Current-Limit Protection section.

SELECTING THE INDUCTOR

The peak-to-peak inductor ripple current, ΔI_L, is set to 35% of the maximum output current. Use the following equation to estimate the value of the inductor:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} = 12 V.
V_{OUT} = 1.2 V.
D is the duty cycle ($D = V_{OUT}/V_{IN}$ = 0.1).
ΔI_L = 35% × 4 A = 1.4 A.
f_{SW} = 600 kHz.

The resulting value for L1 is 1.28 µH. The closest standard inductor value is 1.5 µH; therefore, the inductor ripple current, ΔI_{L1}, is 1.2 A.

The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{OUT} + (\Delta I_L/2)$$

The calculated peak current for the inductor is 4.6 A.

The rms current of the inductor can be calculated using the following equation:

$$I_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}}$$

The rms current of the inductor is approximately 4.02 A.

Therefore, an inductor with a minimum rms current rating of 4.02 A and a minimum saturation current rating of 4.6 A is required. However, to prevent the inductor from reaching its saturation point in current-limit conditions, it is recommended that the inductor saturation current be higher than the maximum peak current limit, typically 6 A, for reliable operation.

Based on these requirements and recommendations, the Coilcraft XAL5030-122, with a DCR of 8.5 mΩ, is selected for this design.

SELECTING THE OUTPUT CAPACITOR

The output capacitor must meet the output voltage ripple and load transient requirements. To meet the output voltage ripple requirement, use the following equations to calculate the ESR and capacitance:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

The calculated capacitance, C_{OUT_RIPPLE}, is 20.8 µF, and the calculated ESR, R_{ESR}, is 10 mΩ.

To meet the ±5% overshoot and undershoot requirements, use the following equations to calculate the capacitance:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - V_{OUT}{}^2}$$

For estimation purposes, use $K_{OV} = K_{UV} = 2$; therefore, $C_{OUT\_OV} = 117$ µF and $C_{OUT\_UV} = 13.3$ µF.

The ESR of the output capacitor must be less than 13.3 mΩ, and the output capacitance must be greater than 117 µF. It is recommended that three ceramic capacitors be used (47 µF, X5R, 6.3 V), such as the GRM21BR60J476ME15 from Murata with an ESR of 2 mΩ.

SELECTING THE LOW-SIDE MOSFET

A low $R_{DS(ON)}$ N-channel MOSFET must be selected for high efficiency solutions. The MOSFET breakdown voltage must be greater than 1.2 × V_{IN}, and the drain current must be greater than 1.2 × I_{LIMIT}.

It is recommended that a 20 V, dual N-channel MOSFET (such as the Si4204DY from Vishay) be used for both Channel 1 and Channel 2. The $R_{DS(ON)}$ of the Si4204DY at a 4.5 V driver voltage is 6 mΩ, and the total gate charge is 14.5 nC.

DESIGNING THE COMPENSATION NETWORK

For better load transient and stability performance, set the cross frequency, f_C, to $f_{SW}/10$. In this example, f_{SW} is set to 600 kHz; therefore, f_C is set to 60 kHz.

For the 1.2 V output rail, the 47 µF ceramic output capacitor has a derated value of 32 µF.

$$R_C = \frac{2 \times \pi \times 1.2\ \text{V} \times 3 \times 32\ \mu\text{F} \times 60\ \text{kHz}}{0.8\ \text{V} \times 470\ \mu\text{s} \times 20\ \text{A/V}} = 5.77\ \text{k}\Omega$$

$$C_C = \frac{(0.3\ \Omega + 0.001\ \Omega) \times 3 \times 32\ \mu\text{F}}{5.77\ \text{k}\Omega} = 5.01\ \text{nF}$$

$$C_{CP} = \frac{0.001\ \Omega \times 3 \times 32\ \mu\text{F}}{5.77\ \text{k}\Omega} = 16.6\ \text{pF}$$

Choose standard components: $R_C = 5.6$ kΩ and $C_C = 4.7$ nF. C_{CP} is optional.

Figure 40 shows the bode plot for the 1.2 V output rail. The cross frequency is 64 kHz, and the phase margin is 65°.

Figure 41 shows the load transient waveform.

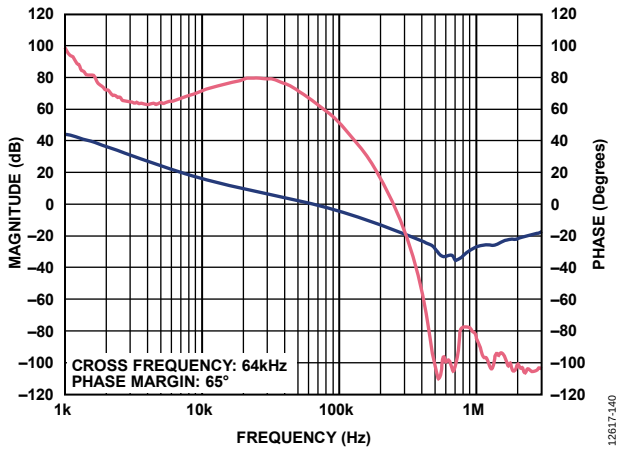


Figure 40. Bode Plot for 1.2 V Output

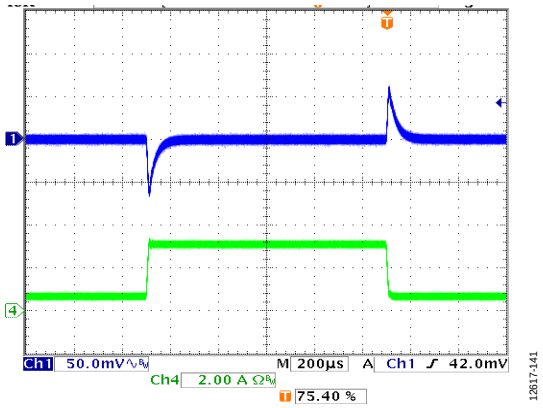


Figure 41. 0.8 A to 3.2 A Load Transient Waveform for 1.2 V Output

SELECTING THE SOFT START TIME

The soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during soft start and limiting the inrush current.

The CFG12 pin can be used to program a soft start time of 2 ms or 16 ms and can also be used to configure parallel operation of Channel 1 and Channel 2. For more information, see the Soft Start section and Table 8.

SELECTING THE INPUT CAPACITOR

For the input capacitor, select a ceramic capacitor with a minimum value of 10 µF; place the input capacitor close to the PVINx pin. In this example, one ceramic capacitor of 10 µF, X5R, 25 V is recommended.

PRINTED CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Optimal circuit board layout is essential to obtain the best performance from the ADP5054 (see Figure 43). Poor layout can affect the regulation and stability of the device, as well as the EMI and electromagnetic compatibility (EMC) performance. For a optimal PCB layout, refer to the following guidelines:

- Place the input capacitor, inductor, MOSFET, output capacitor, and bootstrap capacitor close to the IC.
- Use short, thick traces to connect the input capacitors to the PVINx pins, and use a dedicated power ground to connect the input and output capacitor grounds to minimize the connection length.
- Use several high current vias, if required, to connect PVINx, PGNDx, or SWx to other power planes.
- Use short, thick traces to connect the inductors to the SWx pins and the output capacitors.
- Ensure that the high current loop traces are as short and wide as possible. The high current path is shown in Figure 42.
- Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Place the decoupling capacitors close to the VREG and VDD pins.
- Place the frequency setting resistor close to the RT pin.
- Place the feedback resistor divider close to the FBx pin. In addition, keep the FBx traces away from the high current traces and the switch node to avoid noise pickup.
- Use 0402 or 0603 size resistors and capacitors to achieve the smallest possible footprint solution on boards where space is limited.

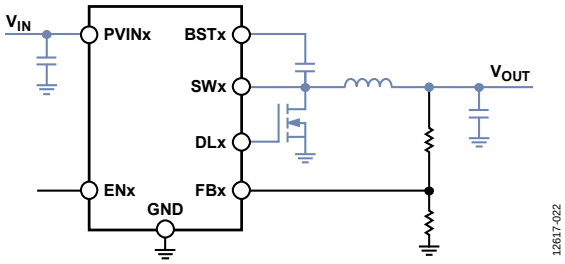


Figure 42. Typical Circuit with High Current Traces Shown in Blue

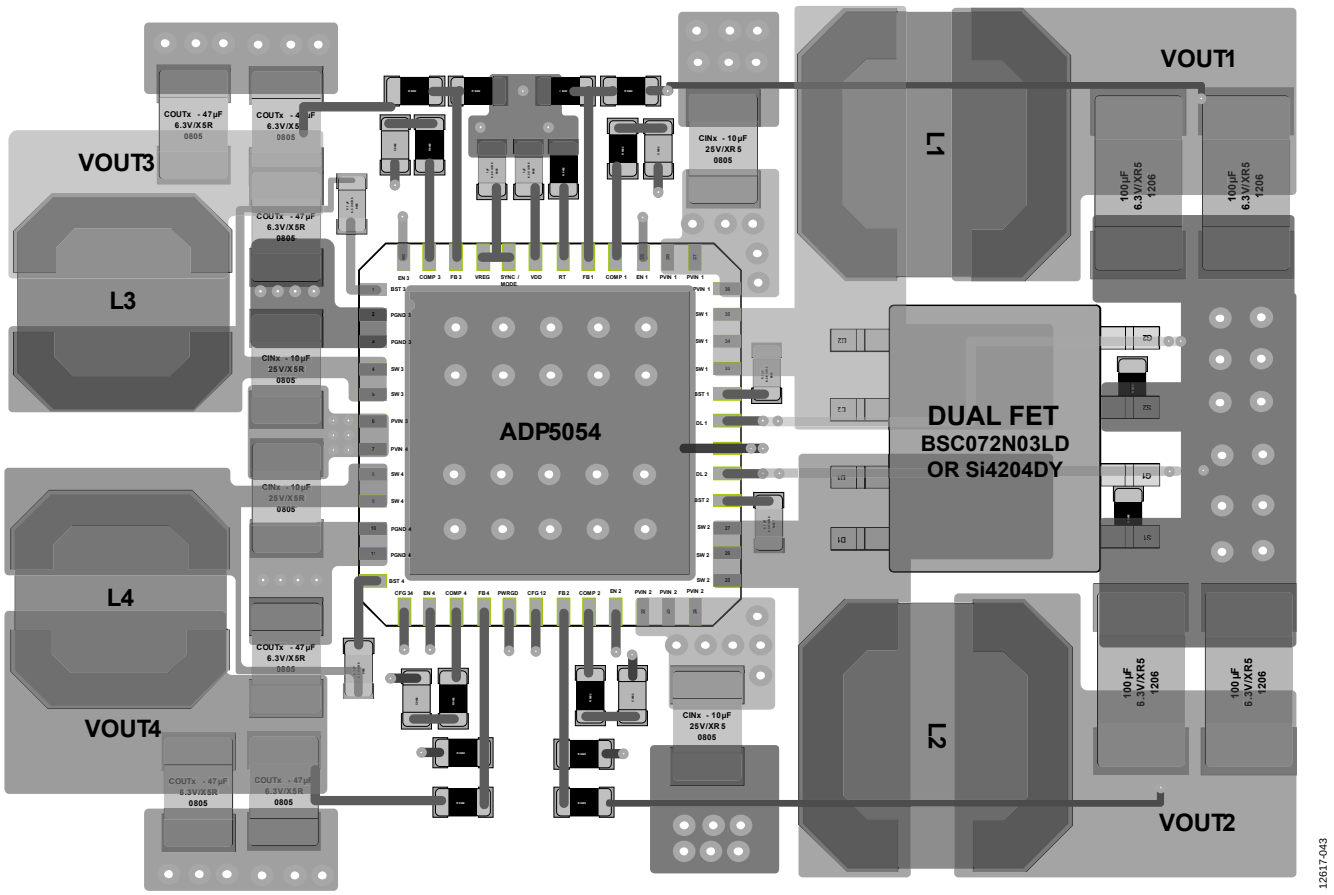


Figure 43. Typical PCB Layout for the ADP5054

TYPICAL APPLICATION CIRCUIT

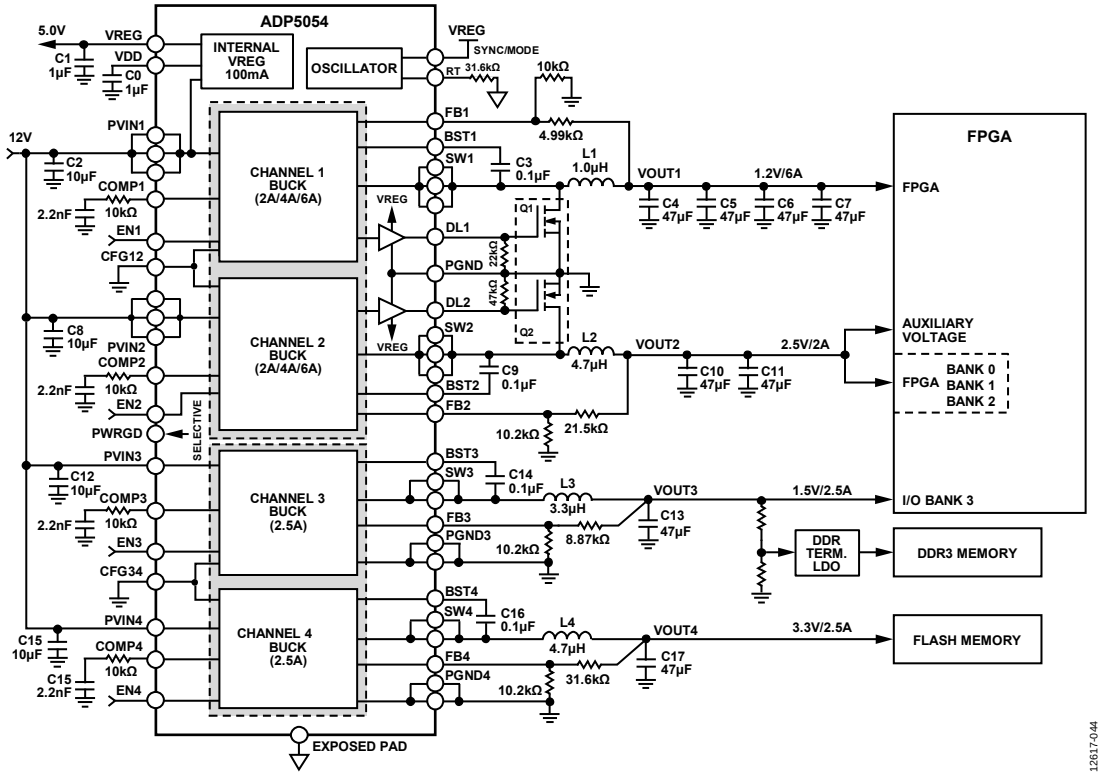


Figure 44. Typical Field Programmable Gate Array (FPGA) Application, 600 kHz Switching Frequency, Adjustable Output Model

FACTORY DEFAULT OPTIONS

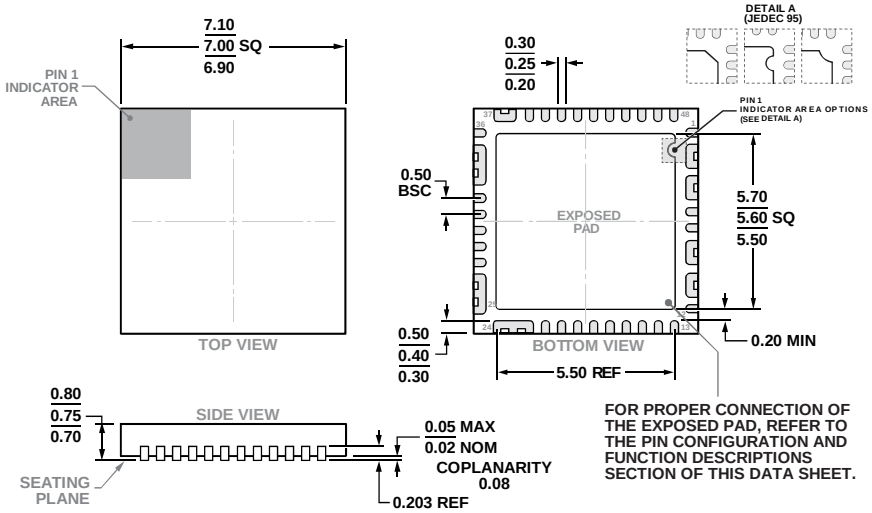
Table 14 lists the factory default options programmed into the ADP5054 when the device is ordered (see the Ordering Guide). To order the device with options other than the default options, contact your local Analog Devices sales or distribution representative.

Table 14. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8 V adjustable output
Channel 2 Output Voltage	0.8 V adjustable output
Channel 3 Output Voltage	0.8 V adjustable output
Channel 4 Output Voltage	0.8 V adjustable output
PWRGD Pin (Pin 17) Output[1]	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Hiccup Protection	Hiccup protection disabled for overcurrent events
Short-Circuit Latch-Off	Disabled for all four buck regulators

[1] Other PWRGD factory options include Monitor Channel 1, Channel 2, Channel 3, and Channel 4 outputs.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220

Figure 45. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height with Fused Leads
(CP-48-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
ADP5054ACPZ-R7	−40°C to +125°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-16
ADP5054-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] Table 14 lists the factory default options for the device. To order a device with options other than the default values, contact your local Analog Devices sales or distribution representative.

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