Data Sheet

ADL5308

Fast Response 188 dB Range (10 pA to 25 mA) Logarithmic Converter

FEATURES

- Fast transient response (I_{PD} stepped from 220 µA to 10 nA)
  - Rise/fall time: <2.4 µs
  - 2 dB Electrical (1 dB optical) settling time: <3.5 µs
- Flat Frequency Response/No Undershoot
- Bandwidth: 970 kHz at I_{INP} = 10 nA
- Accurately trimmed logarithmic response
  - Logarithmic slope: 200 mV/dec
  - Logarithmic conformance error: ±0.2 dB at 25°C (I_{INP} from 10 nA to 1 mA)
- Ratio input for direct optical gain measurements
- Comparator with adjustable hysteresis and latch enable
- I^2C adjustable
  - Adaptive photodiode bias
  - Comparator reference level
- Minimal external components are required
- 34 dB PSRR at 20 kHz and I_{INP} = 10 nA
- 2 mm × 3 mm, 14-terminal LGA package

APPLICATIONS

- Optical power monitoring
- Erbium-doped fiber amplifiers (EDFA)

GENERAL DESCRIPTION

The ADL5308 is a logarithmic transimpedance amplifier optimized for wide dynamic range signal level monitoring in fiber optic systems.

It produces an accurate, temperature-compensated output voltage proportional to the logarithm of the ratio between the input current at pin INP, and a reference current. The reference current can either be generated internally or externally provided through the IREF interface (LOG-ratio detection). The logarithmic slope and intercept are both accurately trimmed to a nominal value of 200 mV/decade and 10 pA respectively.

The low-impedance VLOG logarithmic output has enough drive capability to drive a wide range of analog-to-digital converters (ADCs) and other circuits and its gain can be adjusted by adding a resistor-divider driving the FB pin.

A built-in fast comparator provides a compact solution to compare the logarithmic output to an external reference level, either programmed through I^2C or supplied through the CREF interface. The comparator has adjustable hysteresis and an optional output latch function using the HYST pin.

Adaptive photodiode (PD) biasing is supported through the PDB pin. At a low diode current, the reverse PD bias is kept small to minimize the dark current. At higher input currents, the bias voltage scales linearly with the current to avoid nonlinearity due to PD saturation. The starting bias level as well as the scale factor at higher currents are configurable through I^2C.

The ADL5308 is specified for operation from −40°C to +105°C ambient temperature and is offered in a small 2 mm × 3 mm, 14-terminal LGA package.

FUNCTIONAL BLOCK DIAGRAM

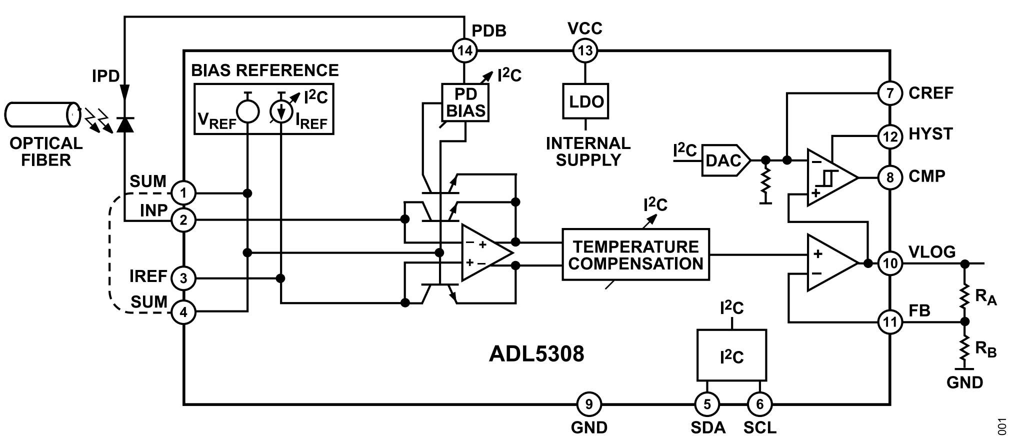


Figure 1. Functional Block Diagram

TABLE OF CONTENTS

REVISION HISTORY

8/2023—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 5.0 V, T_A = 25°C, Input current (I_{INP}) = 10 nA, default register settings, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT INTERFACES					
INP Current Range (INP)	Current into INP (Pin 2)	10			pA
				25	mA
IREF Current Range (IREF)	Current into IREF (Pin 3)	5			nA
				1	mA
Input Node Voltage	Over input current range	1.3	1.5 to 2.2	2.4	V
SUM Voltage (SUM)			1.53		V
Absolute Offset Voltage	$\|V_{PDB} − V_{INP}\|$, I_{INP} = 1 nA		1	6	mV
	$\|V_{PDB} − V_{SUM}\|$		1		mV
Temperature Drift			−12		µV/°C
PHOTODIODE BIAS (PDB)					
Output Voltage	V_{PDB}, I_{PDB} = 1 µA		1.53		V
	V_{PDB}, I_{PDB} = 10 mA	3.3	4.4	5	V
Transresistance (R_T)	$(V_{PDB} − V_{INP})/I_{PD}$	180	282	380	Ω
I_{PD} Threshold (I_{TH})	Constant PDB voltage below I_{TH}		160		µA
LOGARITHMIC OUTPUT					
Logarithmic Slope		198	200	202	mV/dec
Logarithmic Intercept		8	10	12	pA
Logarithmic Conformance Error	10 nA ≤ I_{INP} ≤ 1 mA	−0.7	±0.2	0.8	dB
Output Voltage	I_{INP} = 10 mA		1.805		V
	I_{INP} = 1 nA		406		mV
Small Signal Bandwidth	I_{INP} = 10 nA		970		kHz
Fall, Rise Times	I_{INP} from 220 µA to 10 nA, measure at 90% and 10% points		<2.4		µs
Settling Time	I_{INP} from 220 µA to 10 nA, VLOG settles within 2 dB of final value, using 220 Ω/1.2 nF VLOG low-pass filter		<3.5		µs
Output Current	I_{INP} = 1 nA, V_{VLOG} = 0.6 V, sinking		49		mA
	I_{INP} = 10 mA, V_{VLOG} = 1.6 V, sourcing		17		mA
Output Impedance			1		Ω
COMPARATOR					
Output High Voltage	CREF = 0 V, I_{INP} = 10 mA		3.3		V
Output Low Voltage	CREF = 1 V, I_{INP} = 1 nA		0		V
Short-Circuit Output Current	CMP = 2.8 V, CREF = 1 V, I_{INP} = 10 mA, sourcing		9.2		mA
	CMP = 0.2 V, CREF = 1 V, I_{INP} = 1 nA, sinking		8.8		mA
Hysteresis	HYST = 1 V, CREF_DAC (0x40) = 1.27 V		109		mV
Latch Enable Voltage	Voltage on HYST pin		1.6		V
POWER SUPPLY					
Positive Supply Voltage		4.75	5.0	5.25	V
Quiescent Current	I_{INP} = 1 µA		32		mA
Power-Supply Rejection Ratio	I_{INP} = 10 nA, measured at 20 kHz		34		dB
I^2C INTERFACE					
Logic Low Input Voltage				0.9	V
Logic High Input Voltage		2.1		3.3	V
Current Into SCL, SDA				±50	µA
Input Hysteresis Voltage, V_{HYST}			250		mV

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Capacitance			1		pF
Glitch Rejection				50	ns

SERIAL-INTERFACE TIMING SPECIFICATIONS

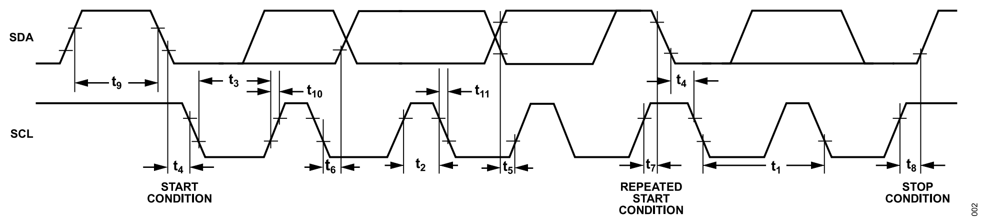


Figure 2. I²C Timing Diagram

Table 2. I²C Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
$f_{SCL(MAX)} = 1/t_1$	Maximum SCL clock frequency	400			kHz
t_3	Minimum SCL low period		0.65	1.3	µs
t_2	Minimum SCL high period		50	600	ns
t_9	Minimum bus free time between STOP/START condition		0.12	1.3	µs
t_4	Minimum hold time after (repeated) START condition		140	600	ns
t_7	Minimum repeated START condition setup-time		30	600	ns
t_8	Minimum STOP condition setup-time		30	600	ns
t_6	Minimum data-hold time input		−100	0	ns
t_6	Minimum data-hold time output	300	600	900	ns
t_5	Minimum data setup-time input		30	100	ns
$t_{SP(MAX)}$	Maximum suppressed spike pulse width	50	110	250	ns
t_{RST}	Stuck bus reset time (condition: SCL or SDA held low)	25	66		ms
C_X	SCL, SDA input capacitance		5	10	pF

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{CC})	5.5 V
Current into INP	100 mA
Current into IREF	25 mA
DC Voltage	
SUM, INP, IREF, SDA, SCL	−0.3 V to 3.6 V
CREF, CMP, VLOG, HYST	−0.3 V to 3.6 V
PDB	−0.3 V to V_{CC} + 0.3 V
Output Short-Circuit Current Duration	
VLOG, CMP, PDB	Indefinite
Temperature	
Ambient Operating Range	−40°C to +105°C
Storage Range	−65°C to +150°C
Lead (Soldering, 60 sec)	300°C
Maximum Junction (T_J)	135°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}[2]	θ_{JB}[3]	θ_{JC}[4]	Unit
CC-14-4	86	45	32	°C/W

1 Test Condition 1: thermal impedance simulated values are based upon use of 2S2P JEDEC PCB. For more information, see the Ordering Guide section.

2 θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

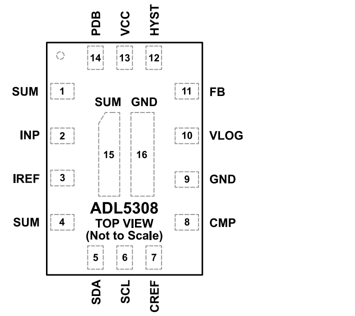
3 θ_{JB} is the junction-to-board thermal resistance.

4 θ_{JC} is the junction-to-case bottom thermal resistance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD 1. ONE OF THE EXPOSED PADS ON THE UNDERSIDE OF THE DEVICE, PIN 15, IS INTERNALLY CONNECTED TO SUM FOR IMPROVED SHIELDING OF THE INPUT PINS. CONNECT ALL SUM PINS TOGETHER AND LEAVE FLOATING.
2. EXPOSED PAD 2. ONE OF THE EXPOSED PADS ON THE UNDERSIDE OF THE DEVICE, PIN 16, IS INTERNALLY CONNECTED TO GROUND AND REQUIRES GOOD THERMAL AND ELECTRICAL CONNECTION TO THE GROUND OF THE PCB. CONNECT ALL GROUND PINS TO A LOW IMPEDANCE GROUND PLANE.

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin Number	Mnemonic	Description
1, 4	SUM	Guard Pins. The SUM pins are used to shield the input current lines to INP and IREF.
2	INP	Photocurrent Input. INP is connected to the PD anode (current flows into INP).
3	IREF	Reference Current Input. IREF can optionally be connected to a reference current or a second PD for log ratio measurements (optical gain).
5	SDA	I^2C Interface Data Input/Output.
6	SCL	I^2C Interface Clock Input.
7	CREF	Comparator Reference Level. Comparator output is high when the VLOG voltage exceeds the voltage applied to this pin. When left open, the reference level is set by an internal I^2C programmable digital-to-analog converter (DAC) if the CREF register content is not zero.
8	CMP	Comparator Output Voltage.
9	GND	Analog Ground.
10	VLOG	Logarithmic Output. The voltage at this pin changes logarithmically with the current applied to INP and IREF.
11	FB	Feedback Pin of Output Amplifier. Can be used to change the logarithmic slope with two external resistors.
12	HYST	Hysteresis. The voltage at the pin controls the amount of hysteresis in the comparator output. A voltage greater than 2.0 V applied to this pin enables the latch function.
13	VCC	Positive Power Supply. Decoupling with 1 nF and 4.7 μF capacitors to ground is recommended at this pin.
14	PDB	PD Bias. PDB can be connected to the PD cathode to provide adaptive bias control. A series network of 10 Ω and 220 pF to ground is recommended at this pin if the PD capacitance is higher than 3 pF. For lowest PD cathode to anode offset at low input currents, avoid resistive loading at this pin.
15	SUM	One of the exposed pads on the underside of the device, Pin 15, is internally connected to SUM for improved shielding of the input pins. Connect all SUM pins together and leave floating.
16	GND	One of the exposed pads on the underside of the device, Pin 16, is internally connected to ground and requires good thermal and electrical connection to the ground of the PCB. Connect all ground pins to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C, Input current (I_{INP}) = 10 nA, default register settings, unless otherwise noted.

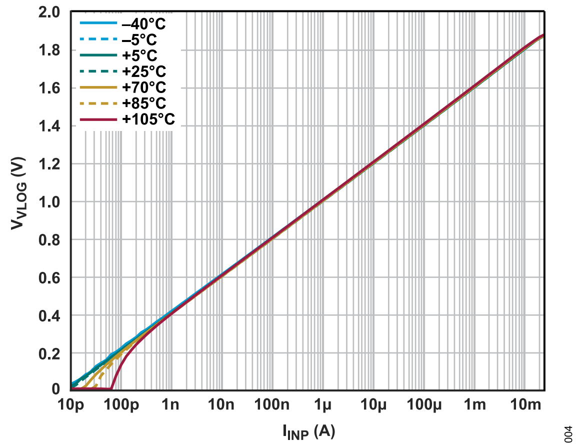


Figure 4. V_{VLOG} vs. I_{INP} at Various Temperatures with Internal Trimmed I_{IREF} Value

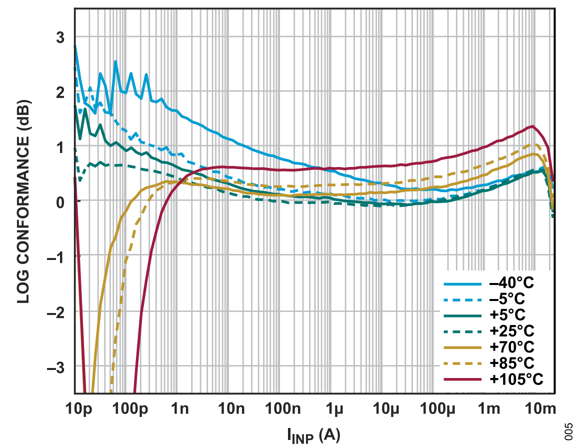


Figure 7. Log Conformance Error vs. I_{INP} at Various Temperatures, Normalized to 25°C

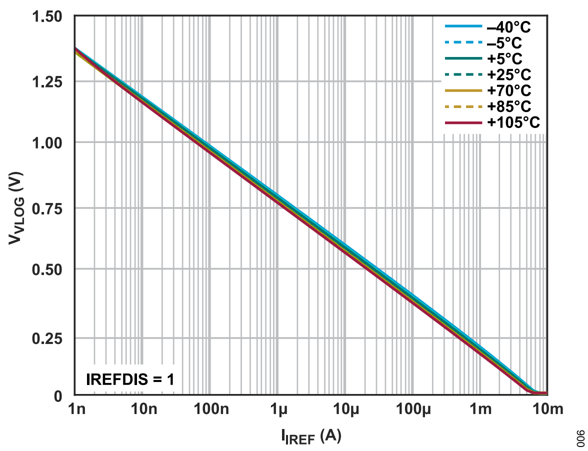


Figure 5. V_{VLOG} vs. I_{IREF} at Various Temperatures for I_{INP} = 10 nA

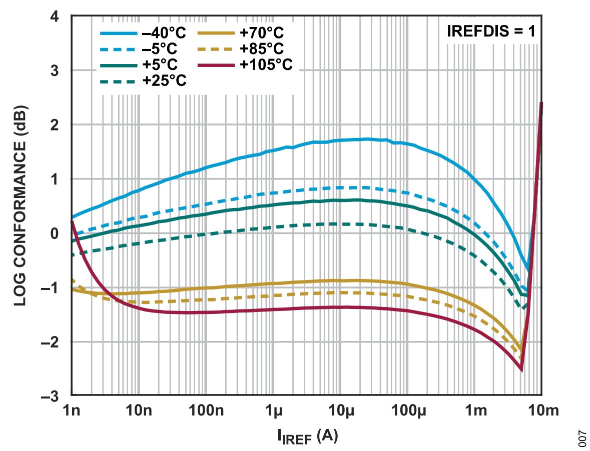


Figure 8. Log Conformance Error vs. I_{IREF} at Various Temperatures for I_{INP} = 10 nA, Normalized to 25°C

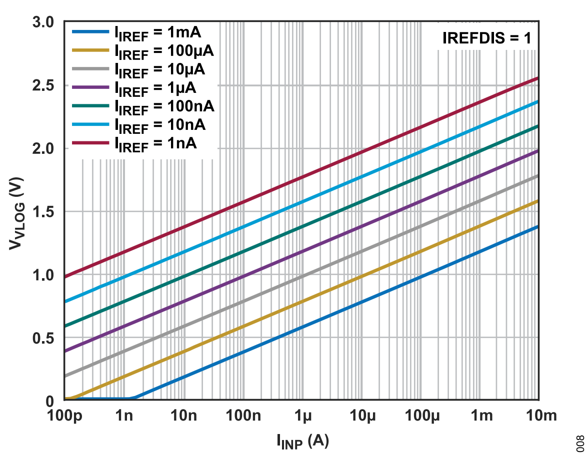


Figure 6. V_{VLOG} vs. I_{INP} at Various I_{IREF} Values in Decades Steps

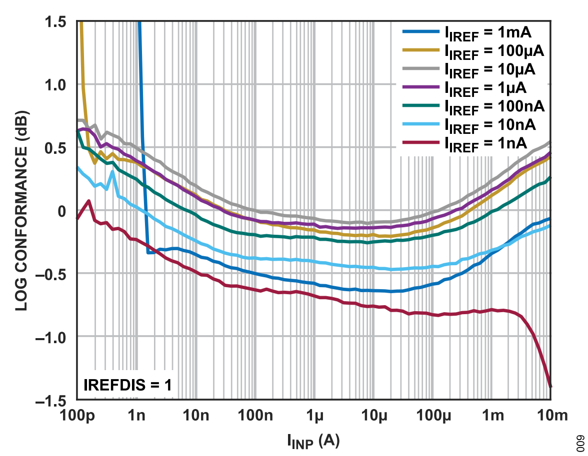


Figure 9. Log Conformance Error vs. I_{INP} at Various I_{IREF} Values in Decade Steps

TYPICAL PERFORMANCE CHARACTERISTICS

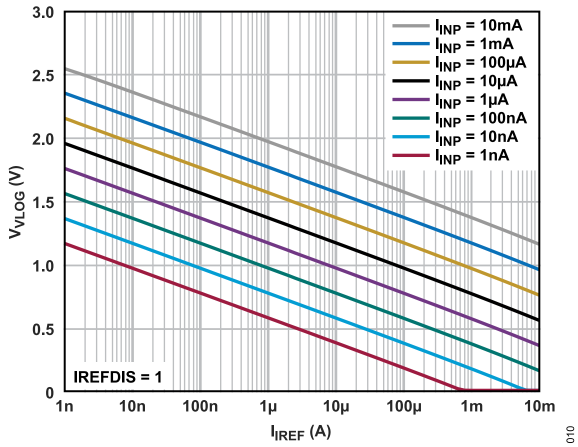


Figure 10. V_{VLOG} vs. I_{IREF} at Various I_{INP} Values in Decade Steps

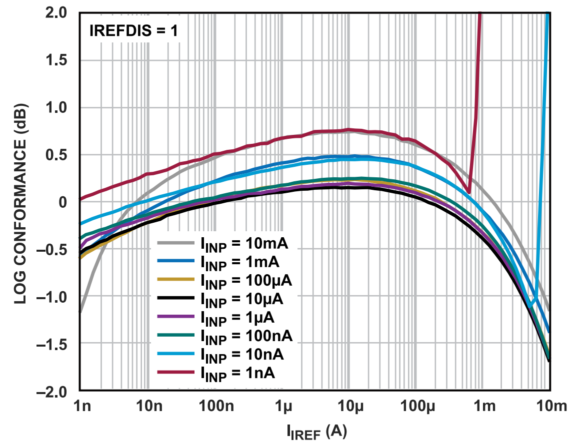


Figure 13. Log Conformance Error vs. I_{IREF} at Various I_{INP} Value in Decade Steps

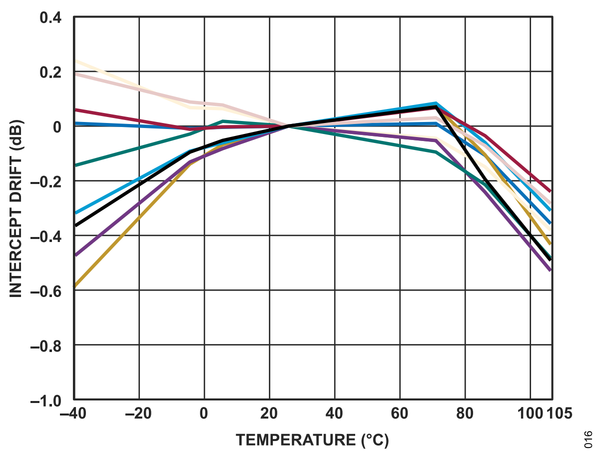


Figure 11. V_{VLOG} − 1.1 V Intercept Drift vs. Temperature Over 10 Samples

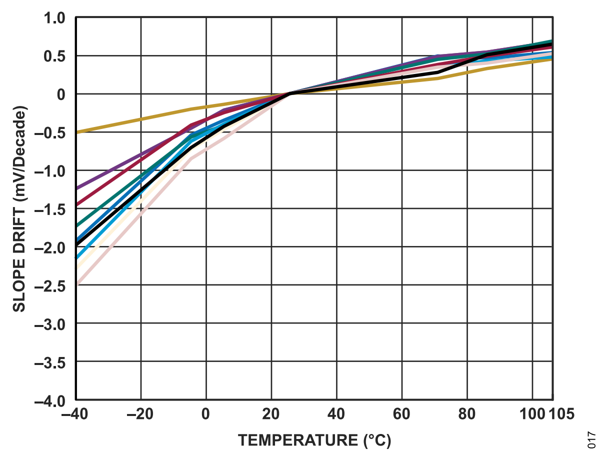


Figure 14. Slope Drift vs. Temperature Over 10 Samples

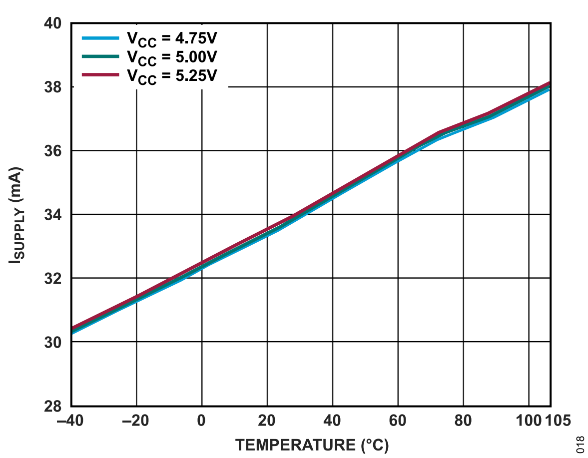


Figure 12. Supply Current vs. Temperature at Various V_{CC} Values for I_{INP} = 10 nA

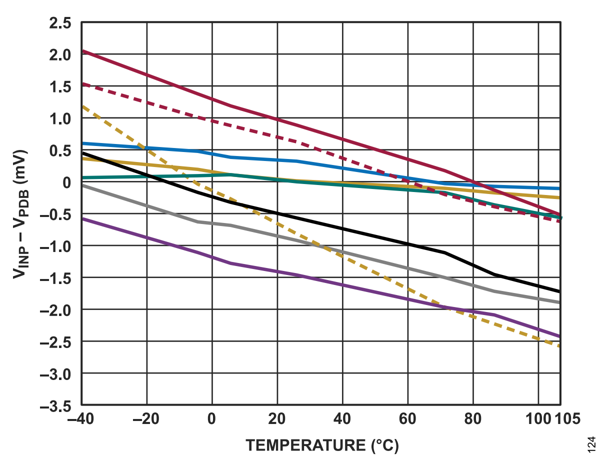


Figure 15. Offset Voltage at 10 nA vs. Temperature Over 10 Samples

TYPICAL PERFORMANCE CHARACTERISTICS

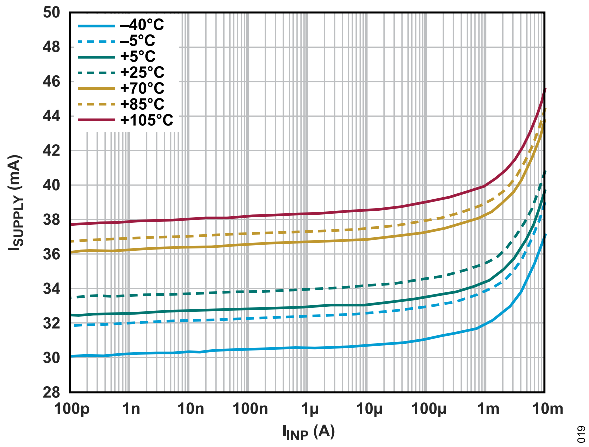


Figure 16. Supply Current vs. I_{INP} at Various Temperatures

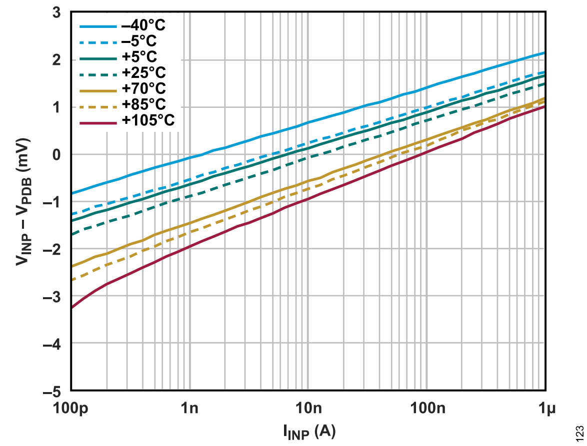


Figure 19. Offset Voltage $V_{INP} - V_{PDB}$ vs. I_{INP} Over Temperature

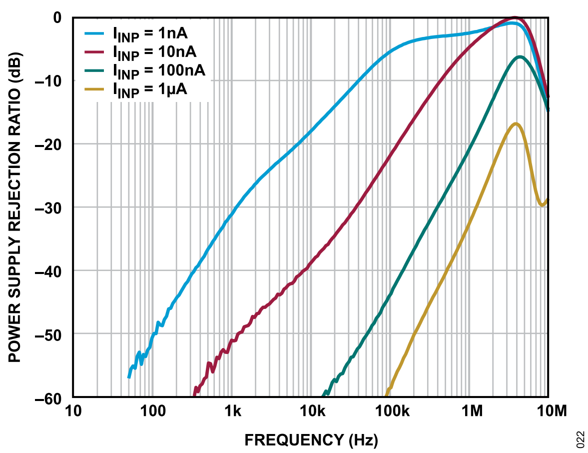


Figure 17. Power-Supply Rejection Ratio (PSRR)

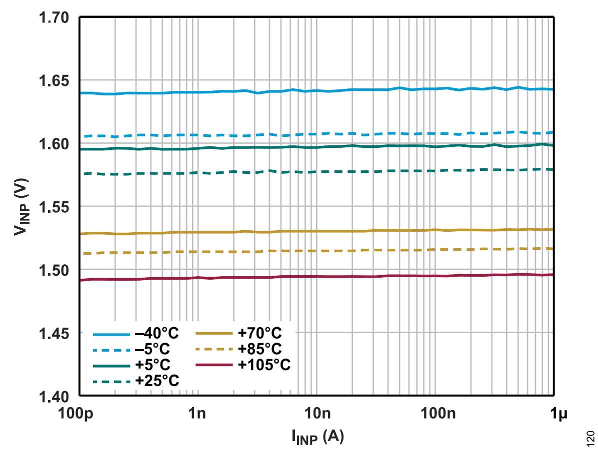


Figure 20. V_{INP} vs. I_{INP} Over Temperature

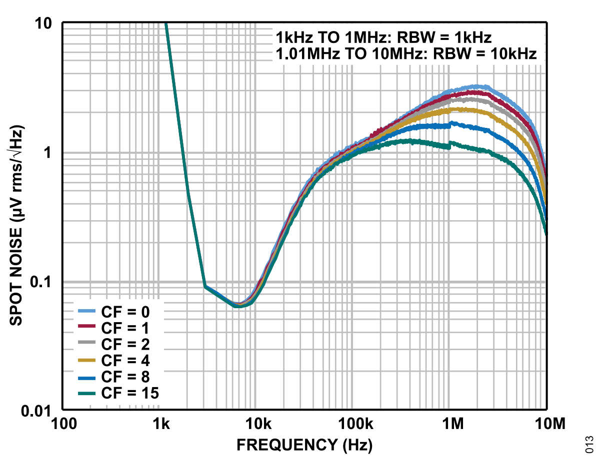


Figure 18. Spot Noise Spectral Density at V_{VLOG} vs. (CF) Register for 10 nA Input Current

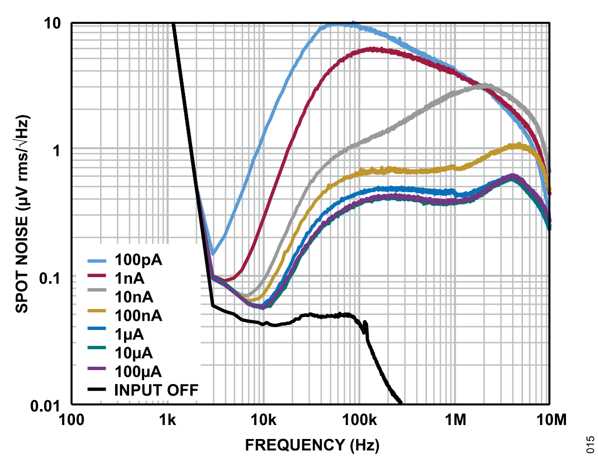


Figure 21. V_{VLOG} Spot Noise Spectral Density vs. Input Current

TYPICAL PERFORMANCE CHARACTERISTICS

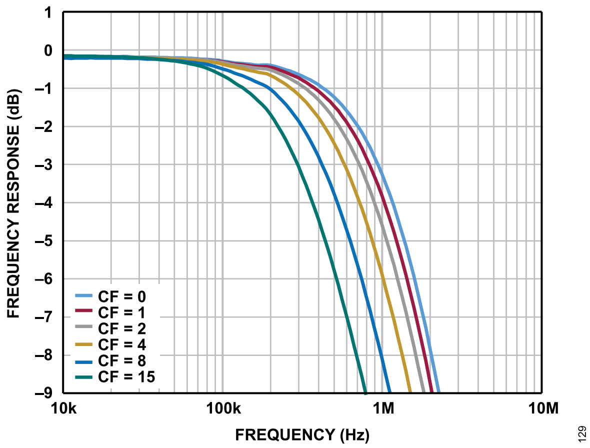


Figure 22. Small Signal AC Response from I_{INP} to V_{VLOG} vs. CF Register for I_{INP} = 10 nA

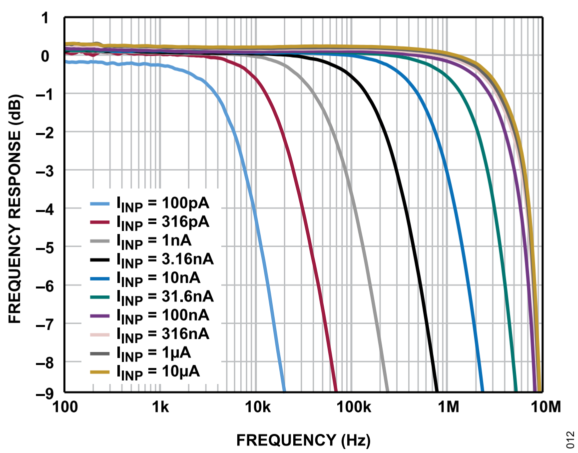


Figure 23. Small Signal AC Response from I_{INP} to V_{VLOG} at Various I_{INP} Value in Half-Decade Steps

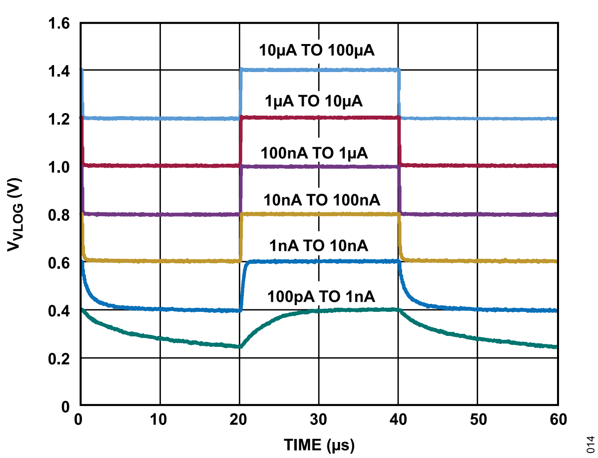


Figure 24. Pulse Response for I_{INP} in Decade Steps

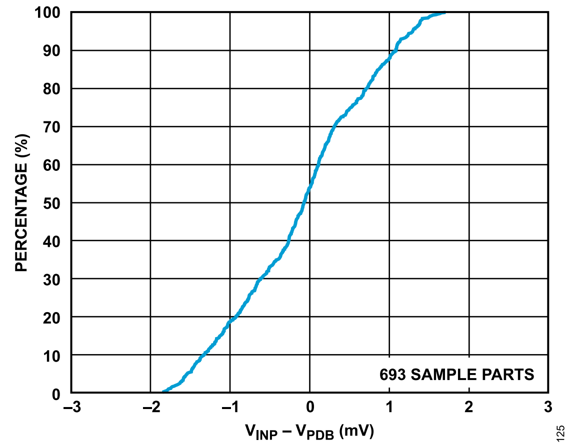


Figure 25. Offset Voltage Distribution

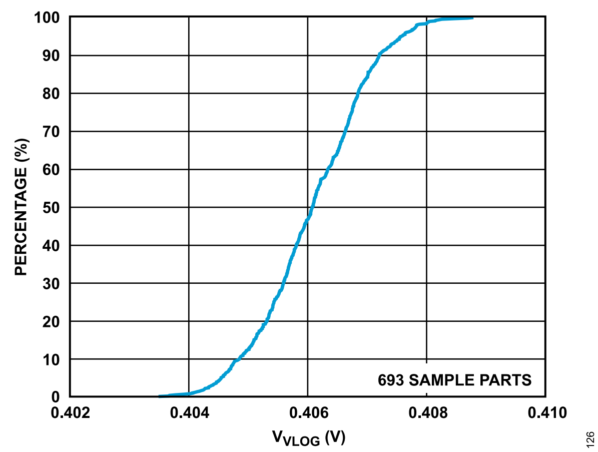


Figure 26. V_{VLOG} at I_{INP} = 1 nA Distribution

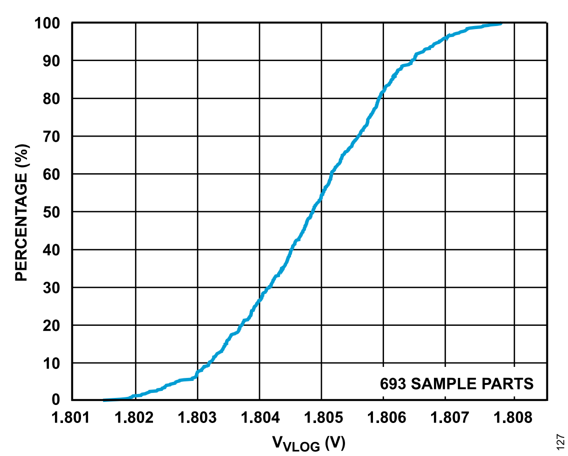


Figure 27. V_{VLOG} at I_{INP} = 10 mA Distribution

TYPICAL PERFORMANCE CHARACTERISTICS

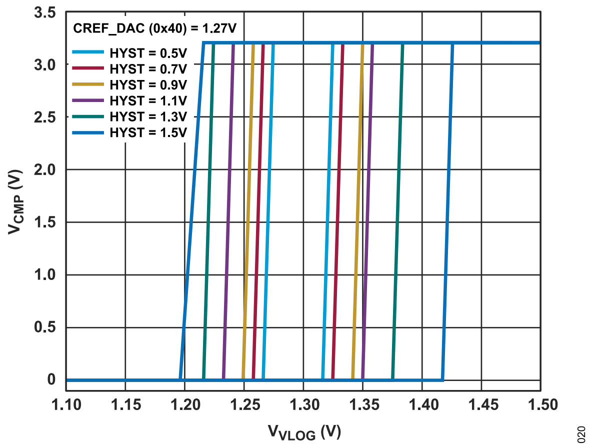


Figure 28. Comparator Hysteresis vs. V_{VLOG} at Various HYPST Pin Value

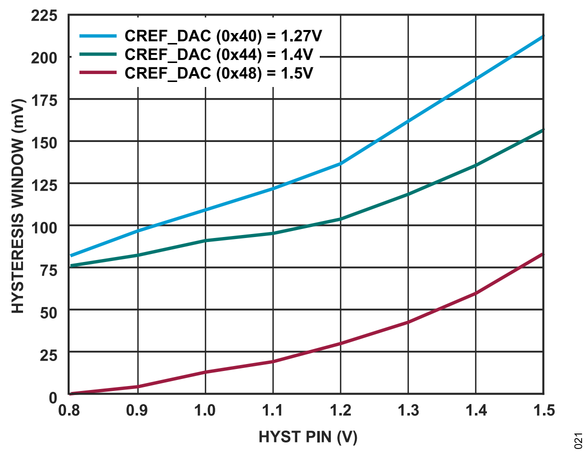


Figure 29. Calculated Comparator Hysteresis at Various CREF_DAC Value

THEORY OF OPERATION

LOGARITHMIC TRANSFER

The logarithmic transimpedance amplifiers (TIA) produce an output voltage that is (approximately) linearly related to the logarithm of the input current I_{PD}:

$$VLOG = SLOPE \times \log_{10}\left(\frac{I_{PD}}{I_Z}\right) \quad (1)$$

The logarithmic slope (SLOPE) shows the amount by which the output voltage VLOG changes for each factor of 10 (decade) change in input current I_{PD}, while the logarithmic intercept I_Z shows the (extrapolated) input current for which the output voltage becomes zero. The actual device output voltage never reaches zero, but saturates to the starting voltage of 17 mV for input currents below 10 pA. Both SLOPE and I_Z can be obtained by linear regression of the measured amplifier output voltage vs. a range of input current levels. The ADL5308 logarithmic slope and intercept of the VLOG − 1.1 V curve are accurately factory trimmed to 200 mV/dec and 3.16 µA respectively. The reason 1.1 V is subtracted from VLOG curve (the ideal value of VLOG at 3.16 µA) is to place the x-intercept in the geometric middle of the specified input current range. That way, the residual slope differences have a minimum impact on the x-intercept and its equation can be written as:

$$VLOG - 1.1 = SLOPE \times \log_{10}\left(\frac{I_{PD}}{I_{Z_{1P1}}}\right) \quad (2)$$

Expressed in dB of input current, Equation 2 can be written as:

$$VLOG - 1.1 = \frac{SLOPE}{20} \times \left(I_{PD,\ dB} - I_{Z_{1P1},\ dB}\right) \quad (3)$$

Where $I_{PD,\ dB}$ is the input current in dBA and $I_{Z1P1,dB}$ is the intercept current in dBA (−110 dBA in this case).

The measurement accuracy obtained with a logarithmic amplifier is determined by the following two factors:

- The logarithmic conformance error
- The temperature drift error

The logarithmic conformance error describes the deviation of the actual TIA transfer from the ideal log-linear relationship of Equation 3, and is expressed in dB of input current:

$$E_{LC} = \frac{20 \times VLOG(T)}{SLOPE} + I_{Z_{1P1},\ dB} - I_{PD,\ dB} \quad (4)$$

Thus E_{LC} shows the resulting measurement error when VLOG of a logarithmic TIA is measured and Equation 3 is used to determine the input current that the device is sensing. Since SLOPE and I_Z are usually determined at room temperature only, E_{LC} typically also contains a contribution due to drift of the TIA transfer over temperature.

The temperature drift error E_{drift} describes the measurement error introduced solely due to the temperature drift of the TIA transfer, excluding discrepancies of the actual TIA transfer to the ideal log-linear relationship (logarithmic conformance).

$$E_{drift}(T) = \frac{20}{SLOPE} \times [VLOG(T) - VLOG(T_o)] \quad (5)$$

The error, the difference between the output voltage measured at the operating temperature T and the actual output voltage measured at the reference temperature T_o, usually 25°C, is input referred and expressed in dB (of input current) using the logarithmic SLOPE. This is accurate as long as the error is relatively small and the TIA transfer is approximately logarithmic (linear in dB).

OPTICAL MEASUREMENTS

A high-dynamic range optical power monitor can be constructed by connecting the anode of a reverse biased PD to the input of the logarithmic TIA, such that the TIA senses the photon-generated diode current. Therefore, it is important to understand the transducer aspects of a PD, that is, how to interpret the PD current relative to the incident optical power. In the electrical circuits, the power dissipated in a resistive load is proportional to the square of the current, or, vice versa, the current through the load is proportional to the square root of the dissipated power:

$$I_R = \sqrt{P_{DISS}/R} \quad (6)$$

In a reverse biased PD, however, the photon-generated PD current (I_{PD}) itself is directly proportional to the optical power (P_{OPT}) absorbed in the detector:

$$I_{PD} = \rho \times P_{OPT} \quad (7)$$

The proportionality constant ρ shows the conversion gain from optical power to electrical current, is called the responsivity of the PD. Using the same responsivity, the logarithmic intercept current I_Z of the TIA can be related to an optical intercept power level P_Z for which the ideal log-linear transfer produces an output voltage equal to zero. The transfer from measured optical power to amplifier output voltage can therefore be expressed as:

$$VLOG = SLOPE \times \log_{10}\left(\frac{P_{OPT}}{P_Z}\right) \quad (8)$$

For incident optical power expressed in dB, that is,

$$P_{dB,\ OPT} = 10 \times \log_{10}(P_{OPT}) \quad (9)$$

This becomes:

$$VLOG = \frac{SLOPE}{10} \times \left(P_{dB,\ OPT} - P_{dB,\ Z}\right) \quad (10)$$

Thus the logarithmic slope in mV/dB optical power equals twice the logarithmic slope in mV/dB of input current I_{PD} (see Equation 3). Similarly, the optical dynamic range of the TIA in dB equals half the electrical dynamic range in dB, that is, 70 dB optical vs. 140 dB electrical.

THEORY OF OPERATION

PHOTODIODE BIAS (PDB)

The PDB function maximizes the dynamic range of optical power measurements by minimizing the impact of dark current and series resistance on the measurement accuracy.

Dark current is a small leakage current through the diode that does not change proportionally to the incident optical power, and therefore limits the sensitivity of an optical power measurement. Since it generally increases with the reverse bias voltage, a low reverse bias voltage minimizes the dark current and maximizes the sensitivity of the optical power measurement.

Series resistance introduces measurement errors at high current levels through the PD. The voltage drop across this resistance reduces the reverse bias voltage across the PD junction itself, which may lead to saturation or even forward bias of the junction. A sufficiently high reverse bias voltage, preferably proportional to the diode current to maintain constant reverse bias across the junction, is needed to minimize the impact of the PD series resistance.

The PDB function of the ADL5308 adjusts the reverse bias across the PD as a function of the current through the PD, as shown in Figure 30. At low PD currents, the reverse bias is kept at a specified low-level V_{OS} to minimize the impact of the dark current. As the PD current increases, the reverse bias increases accordingly to minimize the impact of the series resistance. To use this function, the cathode of the PD should be connected to the PDB pin.

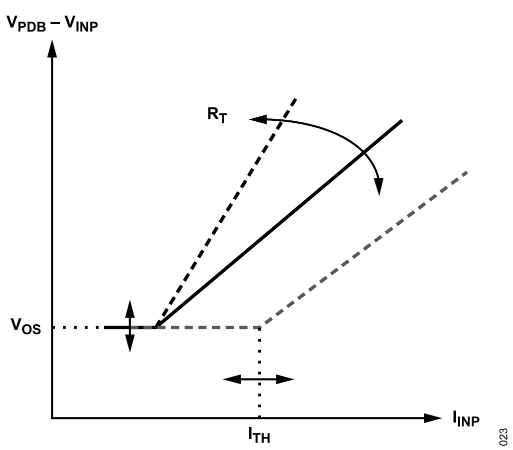


Figure 30. Adaptive PDB Principle of Operation

The ADL5308 PDB can be optimized for specific PDs through the I²C interface. The reverse bias level at low input currents V_{OS}, the transresistance R_T, that is, the change in bias voltage for a given change in bias current, and the threshold current I_{TH} above which the transresistance takes effect can all be adjusted through the I²C interface.

For input currents above I_{TH}, ringing could be observed on the PDB pin due to the positive feedback of the adaptive PD bias via the PD capacitance. Typically, the frequency of the ringing is around 100MHz and doesn't propagate noticeably to the VLOG output because it is attenuated strongly since its bandwidth is much lower. For PD's with capacitance below 3 pF, no sustained ringing (oscillation) is observed even at cold temperatures. It is possible however that for PD's with larger capacitance sustained ringing could occur. In that case, it is recommended to connect a snubber network consisting of a 10 Ω resistor in series with a 220 pF capacitor between the PDB pin and ground to reduce ringing. Since the ringing depends on the PD's capacitance vs. its reverse voltage, series resistance and PCB layout, it is good practice to measure the ringing on the PDB pin using a pulsed optical source that generates an input current well above I_{TH} to make sure the ringing is not excessive. If needed, the 220 pF capacitor can be scaled up or the PDBG register contents, which sets the transresistance, be scaled down.

R_T can be enabled or disabled, that is, effectively set to zero, through the PDBG_FIX flag in REG_14 (see Table 6). When disabled (PDBG_FIX=1), the reverse bias voltage across the diode does not change with the diode current but remains constant over the entire input current range. When enabled (PDBG_FIX=1), the PDBG bit field adjusts the transresistance value in 11.72 Ω steps. An expression for R_T in terms of the REG_14 register bit fields is given in Equation 11. Note that setting either PDBG_FIX = 1 or PDBG = 0 disables the transresistance.

$$R_T = 11.72 \times (1 - PDBG\_FIX) \times PDBG \quad (11)$$

The threshold current I_{TH} above which the transresistance R_T becomes effective is controlled by PDBG and IDZ (dead-zone current) in REG_15. It can be expressed as:

$$I_{TH} = 51\mu\text{A} \times \left(\frac{79 \times IDZ \quad - 1}{PDBG \times (1 - PDBG\_FIX)}\right) \quad (12)$$

The smallest, (minimum functional value for IDZ is 1) value for I_{TH} is obtained for IDZ = 1 and PDBG = 63, resulting in I_{TH} = 63 μA and goes infinite for PDBG_FIX = 1.

The initial bias voltage, or offset voltage between the PDB pin and INP pin below I_{TH} can be adjusted using registers REG_15 and REG_19. Additionally, it is dependent on PDBG and PDBG_FIX. Bit field IPDB in register REG_15 provides a coarse adjustment in 30 mV steps. Adding to this is a fine adjustment in 3 mV steps OS in REG_19. The contribution of PDBG in REG_14 is dependent on the state of the PDBG_FIX flag. The total nominal reverse PDB voltage in (mV) can be expressed as:

$$V_{PDB} - V_{INP} \quad = 30 \times IPDB + 3 \times (OS - 8) + 93.75 \times PDBG \times PDBG\_FIX \quad (13)$$

Note that $|V_{PDB} - V_{INP}|$ is minimized in the factory at low input current for IPDB = 0 and PDBG_FIX = 0 by trimming OS register and is therefore not necessarily 0 mV for OS = 8.

THEORY OF OPERATION

BANDWIDTH

The bandwidth of logarithmic TIAs changes with the input current I_{PD}, which results in low bandwidth at low input currents, and gradually increases to high bandwidth at high current levels. In general, bandwidth and gain have an inverse relationship to each other, such that increasing the gain of an amplifier typically reduces its bandwidth and vice versa. Logarithmic TIAs are no exception to this rule. Using Equation 1, the small-signal gain (transimpedance) of a TIA, that is, the change in output voltage due to a (small) change in input current I_{INP} can be expressed as:

$$Z_t = \frac{\mathrm{d}\,VLOG}{\mathrm{d}\,I_{PD}} = \frac{SLOPE}{\ln(10)I_{INP}} \quad (14)$$

Due to the inherent dynamic range compression by the logarithm, the TIA gain at low input levels is very high, and thus low bandwidth is to be expected. Similarly, the transimpedance at high input currents is much lower, expected to result in higher bandwidth. Further insight into this relationship between bandwidth and input current can be obtained from Figure 1, which shows a simplified schematic of a logarithmic TIA.

The overall topology is usually a negative feedback amplifier using a diode or the base-emitter junction of a bipolar transistor to establish the logarithmic transfer from input current to output voltage. Without feedback, that is, if the gain of the operational amplifier (Op Amp) is zero, the impedance (to ground) at the input node is high, most current from the source should flow into the diode, such that a small parasitic capacitance of the PD and circuit board has a major impact on the (open-loop) bandwidth of the circuit. The loop gain in the amplifier reduces the impedance at the input node by a factor approximately equal to the loop gain, which is roughly the product of op amp gain, input impedance, and the feedback diode transconductance. If the loop gain is infinite, the closed-loop input impedance of the TIA becomes zero, that is, a virtual ground, and the current through the feedback diode precisely equal to the source current I_S.

In a practical amplifier, where the op amp has high but finite gain, an increase of the transimpedance gain Z_t corresponds to a decrease of the diode transconductance (which ideally equals the inverse of Z_t) and thus a decrease of the amplifier loop gain. In turn, a decrease of the loop gain increases the closed-loop input impedance of the amplifier and given that the input capacitance is roughly fixed, decreases the amplifier bandwidth. To maintain as wide as possible bandwidth, it is thus critical to minimize capacitive loading of the TIA input pins.

NOISE

The noise level produced by a logarithmic TIA is also dependent on the input current I_{INP}. The output voltage noise is highest at low input currents (corresponding to the highest small-signal gain), and lowest at high input current levels. Figure 21 shows the spot noise spectral density vs. I_{INP} graph. For low input currents, one of the most dominant noise sources is the 1/f noise of the input NMOS, shown in Figure 31, which produces a 1/f noise voltage at the input node.

With a capacitive load at the input, this noise voltage causes an input 1/f noise current and can produce a hill-shaped spot noise spectral density curve. Therefore, it is important to minimize the source capacitance by choosing a PD with as low as possible equivalent parallel capacitance and as short as possible trace to the input node. A trade-off between noise density and bandwidth at low I_{INP} can be made by setting register CF as shown in Figure 18 and Figure 22 with maximum bandwidth and highest noise density for CF = 0 (default) and minimum bandwidth and lowest noise density for CF = 15.

APPLICATIONS INFORMATION

INTERFACES DESCRIPTION

INP and IREF Interface

The photocurrent input flows into the INP pin connected to the anode of the PD, which can operate at a maximum current of 25 mA. An internal reference current input sets the IREF through an I^2C. An external reference current is also an option to connect to the IREF pin, which requires disabling the internal IREF. The IREF can operate at a maximum current of 5 mA.

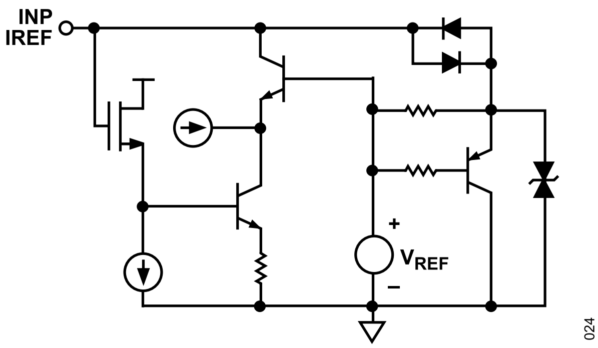


Figure 31. Simplified INP and IREF Interface

SUM Interface

A large voltage difference between nodes can cause a significant leakage current, even if the impedance between the nodes is relatively high. Guarding reduces the errors due to leakages. The concept of guarding is to surround the high-impedance conductor with another conductor (guard) driven to the same voltage potential. If there is no voltage across the insulation resistance (between the high-impedance conductor and guard), there cannot be any current flowing through it.

Reducing errors from external sources in a current-sensing circuit requires a different approach than the voltage sensing input of the typical high-impedance op amp circuit. Leakage can be a significant source of error for highly sensitive log amps, especially at the low end of their range. For example, a 1 GΩ leakage path to the ground from the current lines INP and IREF with a V_{SUM} set to the default 1.53 V generates a 1.53 nA offset.

The ADL5308 uses SUM node as guard pins, which shield the input current lines INP and IREF. It has an internal 1 kΩ resistor connected from a voltage reference buffer (V_{REF}) to the SUM node.

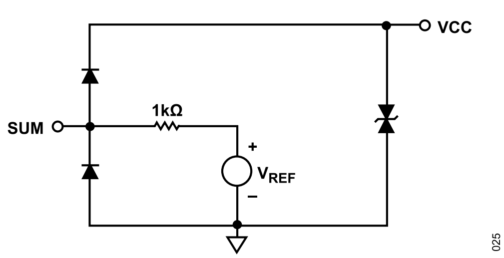


Figure 32. Simplified SUM Interface

VLOG and FB Interface

The Logarithmic voltage-output (VLOG) changes logarithmically with the current applied to INP and IREF. The output can be buffered using the log output amplifier as the VLOG pin shorted to the feedback (FB) pin. The nominal slope is 200 mV/dec in the range of 1 nA to 10 mA of the current input over the entire operating temperature with an internal trimmed IREF value as shown in Figure 4.

The logarithmic slope can be changed by connecting external gain resistors R_A and R_B as shown in Figure 33. For example, for equal resistors between FB and VLOG and FB to ground, the gain is 2.

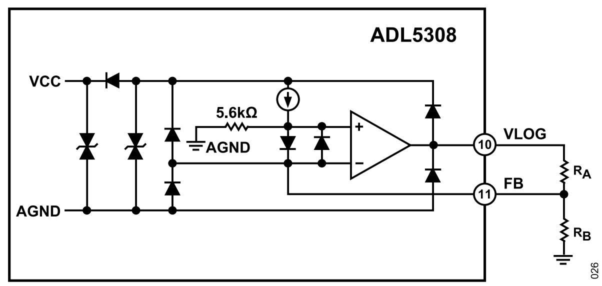


Figure 33. Simplified Schematic of VLOG and FB Interface

Figure 35 shows the logarithmic output response for a 220 μA to 10 nA input current transition (an 87 dB step in magnitude). Two curves are shown: one without any low-pass filter at the VLOG output and one with a 220 Ω/1.2 nF low-pass filter network at the VLOG output. As can be seen, the variation due to noise is lower with the low-pass filter network but its response is slightly slower.

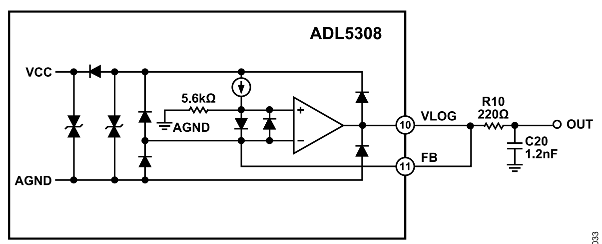


Figure 34. Simplified Schematic of the Low-Pass Filter Network at the VLOG

APPLICATIONS INFORMATION

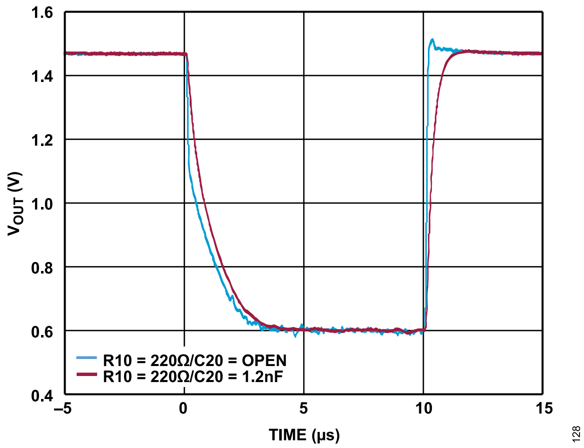


Figure 35. Logarithmic Output Response vs. Time for I_{INP} = 220 µA to 10 nA Transition

A proprietary PD is used as an input current source for this measurement, and it is believed that the response time for the high-to-low current transition is limited by the PD itself, not by the ADL5308. The 10% to 90% fall-time response time is about 2.4 µs and the settling time within 2 dB (1 dB optical power) is about 3.5 µs.

CMP, CREF, and HYST Interface

The logarithmic output VLOG is compared to a voltage reference level using a built-in comparator. The reference voltage, CREF_DAC, is controlled by an internal 7-bit DAC through I²C (range 30.6 mV to 1.93 V in 7.4 mV step). When the VLOG exceeds the CREF_DAC voltage, the comparator output (CMP) goes to logic low.

The HYST pin voltage sets the hysteresis window, which also depends on the internal CREF_DAC value, see Figure 29.

Note that the CREF pin is a monitor point to measure the CREF_DAC output, use a 10 MΩ digital multimeter (DMM). If the comparator is not used, then disable the COMP_EN register.

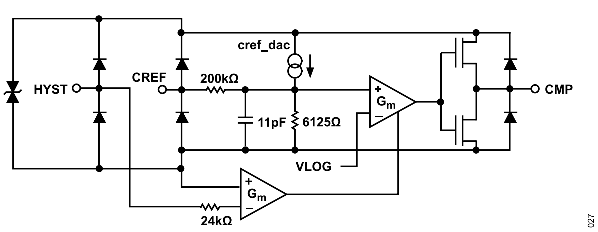


Figure 36. Simplified Comparator Interface for CREF_DAC > 0

PDB Interface

The PDB interface pin is shown in Figure 37. The purpose of this pin is to generate a bias voltage to be used with PDs.

In an optical system, the PD produces an output current proportional to the optical input power. This results in an output dynamic range that is twice (in dB) the optical input power dynamic range, and can be quite high. At low input power, the input current can be very small, on the order of pA. Here it is necessary to minimize the dark current leakage of the PD by keeping the voltage drop across the diode as small as possible. At higher input powers, the PD current can be relatively large (up to 10s of mA). This photocurrent, impressed on the internal series resistance of the diode, results in an increasing voltage drop for increasing optical power.

To address the dark current issue, the ADL5308 provides a PDB that keeps the PD's cathode-to-anode voltage close to zero for low input current, therefore reducing any dark currents. For higher current operation, the PDB Interface tracks the input current and produces an output voltage directly proportional to the input current, with the gain adjustable by the PDBG register. The transresistance can be disabled by asserting the PDBG_FIX bit or setting PDBG = 0. The PDB output voltage is limited by the power supply voltage, VCC.

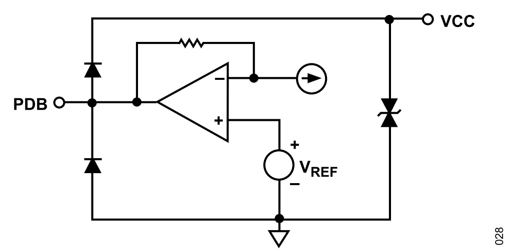


Figure 37. Simplified Schematic of PDB Interface

APPLICATIONS INFORMATION

SDA and SCL Interface

Figure 38 shows the bidirectional SDA interface. The SDA output driver is open-drain and requires an off-chip pull-up resistor at the receiver. The pull-up resistor can be connected to a maximum positive supply of 3.6 V. During a register write operation, the SDA output driver is high-impedance and the SDA input receiver should be driven by a driver capable driving the input pin capacitance of 0.8 pF at the 200 kHz maximum SDA frequency. A driver output impedance less than 20 kΩ is recommended.

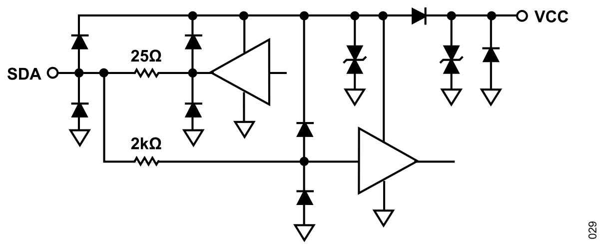


Figure 38. Simplified SDA Interface

Figure 39 shows the SCL interface for the serial clock input to the I^2C controller. This input is high impedance and should be driven by a driver capable of driving the input pin capacitance of 0.8 pF at the 400 kHz maximum SCL frequency. A driver output impedance less than 10 kΩ is recommended.

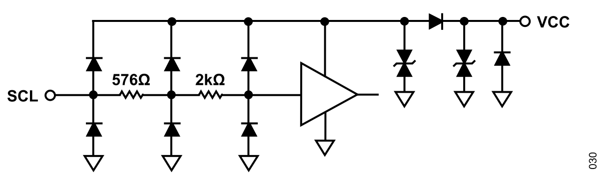


Figure 39. Simplified SCL Interface

SERIAL-PORT INTERFACE

PROTOCOL

The ADL5308 can be connected to an I²C bus interface as a target device to control and monitor several of its internal (analog) functions. For detailed timing requirements, see Serial-Interface Timing Specifications. Data is sent one byte at a time, with the most significant bit (MSB) first. Each instruction consists of one address byte, followed by one or more data bytes. The ADL5308 supports single-byte read and write, as well as autoincrement read/write methods.

ADDRESS

The ADL5308 I²C device read and write addresses consist of a fixed 7-bit device address equal to 0x6C, followed by one read-write least significant bit (LSB) address bit. The LSB address bit equals 0 for a write instruction and 1 for a read instruction. The device write address thus equals 0x6C left-shifted by one bit position (multiply-by-two), which equals 0xD8. The device read address equals the write address with the LSB changed from 0 to 1, equal to 0xD9.

SUPPORTED READ AND WRITE METHODS

The ADL5308 supports several I²C read and write methods:

- Read/write a single register
- Read/write multiple registers at once through autoincrement

Figure 40 summarizes the procedure for each method. Each transaction on the I²C bus is initiated by the controller, and starts with sending a START condition, an HIGH-LOW transition on the SDA line while SCL is high. Subsequently, the 8-bit device write address (of the selected target) is transmitted, one bit per SCL clock pulse. All addresses and data are transmitted over the bus with the MSB first.

The ninth clock pulse is reserved to transmit the ACK (acknowledge) signal from the target to the controller, to indicate that the address is received. To send an ACK, the target pulls the SDA line low. A NACK (not acknowledge) results if the SDA line remains high. Depending on the transaction, a series of byte read/write transfers follows, each ending with an ACK or NACK bit. The transaction ends with a STOP condition sent by the controller, a LOW-HIGH transition on the SDA line while SCK is high.

The autoincrement feature provides read/write access to multiple consecutive registers in a single transaction. Each data byte is read from/written to the next register with address one higher than the previous, and followed by an ACK. The last byte read/written is followed by a NACK for a read, ACK for a write, and a STOP condition.

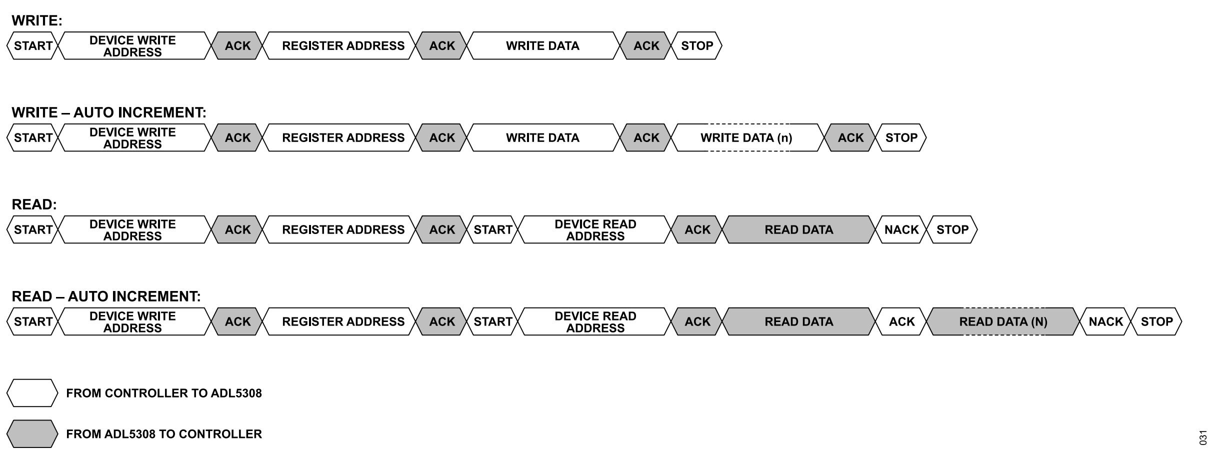


Figure 40. ADL5308 Serial Bus Read/Write Sequences

SERIAL-PORT INTERFACE

REGISTER SUMMARY

Table 6. ADL5308 I^2C Register Details[1]

Address	Name	Bits	Field Name	Description	Default	Access
0x00	REG_00	0	SOFTRESET	Writing 1 to this bit resets all registers to their default values.	0x00	R/W
0x01	REG_01	[7:0]	CHIP_ID	ID for the ADL5308.	0x6D	R
0x10	REG_10	[3:0]	IMAX	Maximum PDB output current.	0x06	R/W
0x11	REG_11	[6:0]	IPT	IREF PTAT current.	0x37	R/W
0x12	REG_12	[6:0]	ICT	IREF CTAT current.	0x49	R/W
0x13	REG_13	4	IREFDIS	Reference current disable (used for ratio measurements).	0x0A	R/W
		[3:0]	IREF	Reference current adjust.		
0x14	REG_14	6	PDBG_FIX	PDB transresistance is disabled (effectively set to zero) if this bit is set, making the PDB voltage constant vs. input current.	0x18	R/W
		[5:0]	PDBG	PDB transresistance control when PDBG_FIX is not set, PDB voltage control in 93.75 mV steps when PDBG_FIX is set.		
0x15	REG_15	[7:4]	IDZ	PDB transresistance threshold control.	0x70	R/W
		[3:0]	IPDB	Controls the PDB voltage at in 30 mV steps.		
0x18	REG_18	[5:0]	MTEMP	Slope temperature drift control.	0x00	R/W
0x19	REG_19	[7:4]	OS	$V_{PDB} - V_{INP}$ offset control in 3 mV steps.	0x74	R/W
		[3:0]	CF	Low input current bandwidth (CF = capacitor feedback).		
0x1A	REG_1A	[5:3]	PT	Band-gap PTAT control.	0x51	R/W
		[2:0]	ZT	Band-gap ZTAT control.		
0x1B	REG_1B	[7:0]	LG	Logarithmic slope adjust.	0x07	R/W
0x1C	REG_1C	[2:0]	VPED	Starting voltage adjust.	0x03	R/W
0x1D	REG_1D	[5:0]	CREF_DAC	Comparator reference level generated by internal DAC if CREF_DAC is not 0 and the external reference level for CREF_DAC = 0.	0x00	R/W
0x20	REG_20	0	COMP_EN	Comparator enable. Enabled when COMP_EN = 1, disabled when COMP_EN = 0.	0x01	R/W
0x48	REG_48	0	NVM_BYPASS[2]	Nonvolatile memory (NVM) bypass.	0x00	R
0x70	REG_70_TRIMMED_10	[3:0]	IMAX_RDBK	Readback register for the trimmed IMAX value of REG_10.	0x0X	R
0x71	REG_71_TRIMMED_11	[6:0]	IPT_RDBK	Readback register for the trimmed IPT value of REG_11.	0xXX	R
0x72	REG_72_TRIMMED_12	[6:0]	ICT_RDBK	Readback register for the trimmed ICT value of REG_12.	0xXX	R
0x73	REG_73_TRIMMED_13	4	IREFDIS_RDBK	Readback register for the trimmed IREFDIS value of REG_13.	0x0X	R
		[3:0]	IREF_RDBK	Readback register for the trimmed IREF value of REG_13.		
0x74	REG_74_TRIMMED_14	6	PDBG_FIX_RDBK	Readback register for the trimmed PDBG_FIX value of REG_14.	0x18	R
		[5:0]	PDBG_RDBK	Readback register for the trimmed PDBG value of REG_14.		
0x75	REG_75_TRIMMED_15	[7:4]	IDZ_RDBK	Readback register for the trimmed IDZ value of REG_15.	0x10	R

SERIAL-PORT INTERFACE

Table 6. ADL5308 I²C Register Details[1] (Continued)

Address	Name	Bits	Field Name	Description	Default	Access
		[3:0]	IPDB_RDBK	Readback register for the trimmed IPDB value of REG_15.		
0x78	REG_78_TRIMMED_18	[5:0]	MTEMP_RDBK	Readback register for the trimmed MTEMP value of REG_18.	0xXX	R
0x79	REG_79_TRIMMED_19	[7:4]	OS_RDBK	Readback register for the trimmed OS value of REG_19.	0xX0	R
		[3:0]	CF_RDBK	Readback register for the trimmed CF value of REG_19.		
0x7A	REG_7A_TRIMMED_1A	[5:3]	PT_RDBK	Readback register for the trimmed PT value of REG_1A.	0x51	R
		[2:0]	ZT_RDBK	Readback register for the trimmed ZT value of REG_1A.		
0x7B	REG_7B_TRIMMED_1B	[7:0]	LG_RDBK	Readback register for the trimmed LG value of REG_1B.	0xXX	R
0x7C	REG_7C_TRIMMED_1C	[2:0]	VPED_RDBK	Readback register for the trimmed VPED value of REG_1C.	0x0X	R

[1] Note that all other registers and undocumented bits are reserved.

[2] To preserve the default power-up settings of the ADL5308 prior to changing register values using NVM_BYPASS = 1, the user must first read registers 0x70 to 0x7C and then write these values to the corresponding registers 0x10 to 0x1C.

EVALUATION BOARD SCHEMATIC

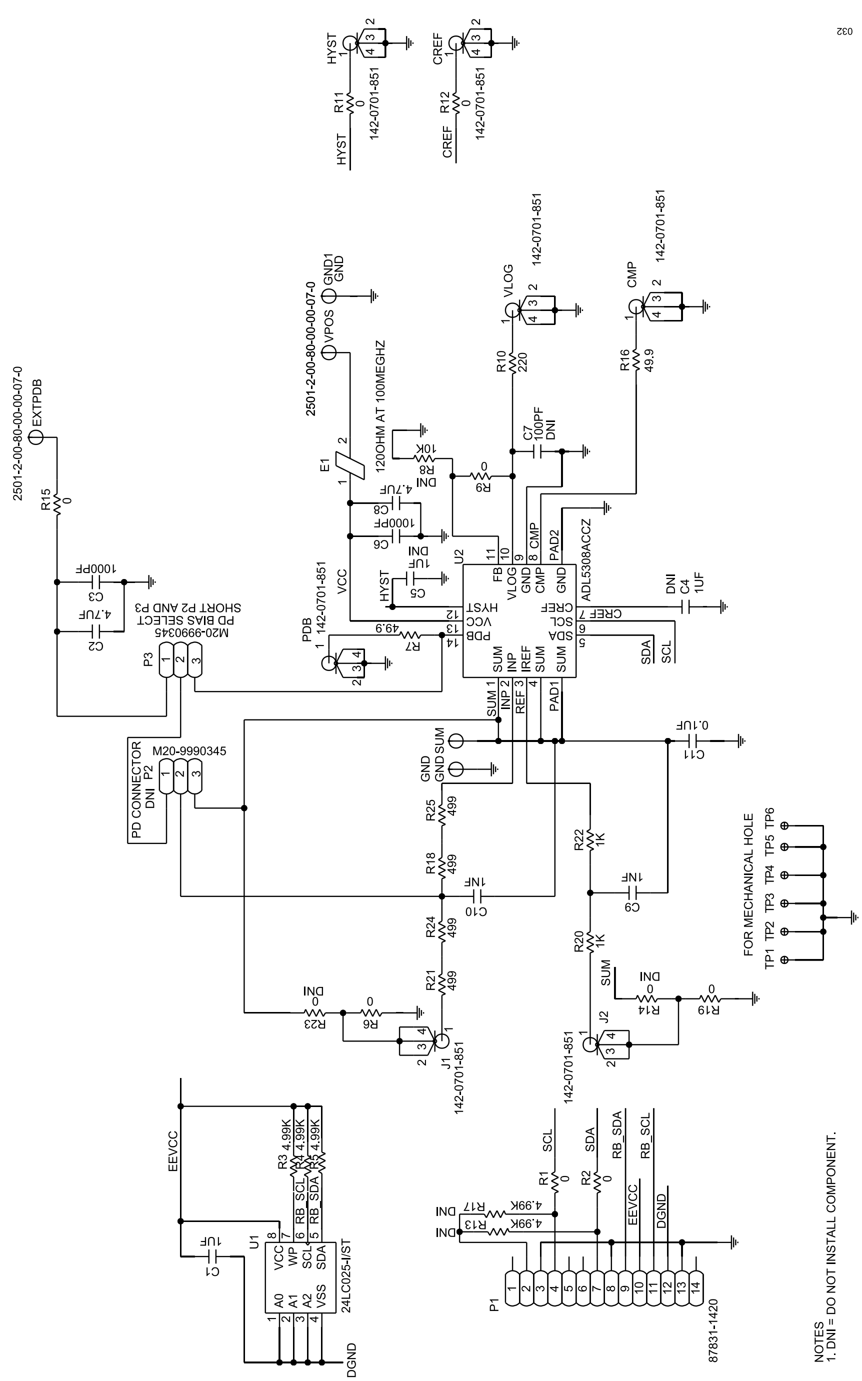


Figure 41. Evaluation Board Schematic

OUTLINE DIMENSIONS

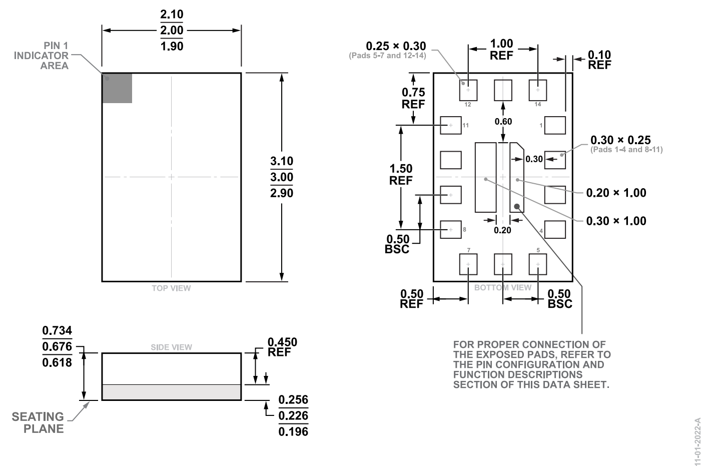


Figure 42. 14-Terminal Land Grid Array [LGA]
(CC-14-4)
Dimensions Shown in millimeters

Updated: August 16, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL5308ACCZ	−40°C to +105°C	LGA/CASON/CH ARRY SO NO LD	Reel, 3000	CC-14-4
ADL5308ACCZ-R7	−40°C to +105°C	LGA/CASON/CH ARRY SO NO LD	Reel, 3000	CC-14-4

1 Z = RoHS-Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADL5308-EVALZ[2]	Evaluation Board
ADL5308-KIT-EVALZ[3]	Evaluation Board Kit

1 Z = RoHS-Compliant Part.
2 The ADL5308-EVALZ package includes the board only.
3 A DC2026C Linduino One controller board is included with the ADL5308-KIT-EVALZ.