Zero-Drift, Single-Supply, Rail-to-Rail Input/Output Operational Amplifiers

Data Sheet **AD8551**

FEATURES

Low offset voltage: 1 µV
Input offset drift: 0.005 µV/°C
Rail-to-rail input and output swing
5 V/2.7 V single-supply operation
High gain, CMRR, PSRR: 130 dB
Ultralow input bias current: 20 pA
Low supply current: 700 µA/op amp
Overload recovery time: 50 µs
No external capacitors required

APPLICATIONS

Temperature sensors
Pressure sensors
Precision current sensing
Strain gage amplifiers
Medical instrumentation
Thermocouple amplifiers

GENERAL DESCRIPTION

This family of amplifiers has ultralow offset, drift, and bias current. The AD8551, AD8552, and AD8554 are single, dual, and quad amplifiers featuring rail-to-rail input and output swings. All are guaranteed to operate from 2.7 V to 5 V with a single supply.

The AD8551/AD8552/AD8554 provide the benefits previously found only in expensive auto-zeroing or chopper-stabilized amplifiers. Using Analog Devices, Inc. topology, these new zero-drift amplifiers combine low cost with high accuracy. No external capacitors are required.

With an offset voltage of only 1 µV and drift of 0.005 µV/°C, the AD8551/AD8552/AD8554 are perfectly suited for applications in which error sources cannot be tolerated. Temperature, position and pressure sensors, medical equipment, and strain gage amplifiers benefit greatly from nearly zero drift over their operating temperature range. The rail-to-rail input and output swings provided by the AD8551/AD8552/AD8554 make both high-side and low-side sensing easy.

The AD8551/AD8552/AD8554 are specified for the extended industrial/automotive temperature range (−40°C to +125°C). The AD8551 single amplifier is available in 8-lead MSOP and 8-lead narrow SOIC packages. The AD8552 dual amplifier is available in 8-lead narrow SOIC and 8-lead TSSOP surface-mount packages. The AD8554 quad is available in 14-lead narrow SOIC and 14-lead TSSOP packages.

PIN CONFIGURATIONS

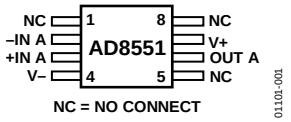

Figure 1. 8-Lead MSOP (RM Suffix)

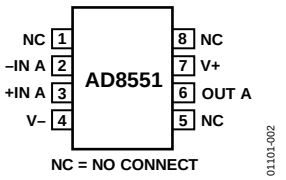

Figure 2. 8-Lead SOIC (R Suffix)

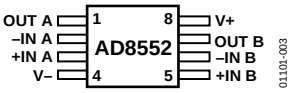

Figure 3. 8-Lead TSSOP (RU Suffix)

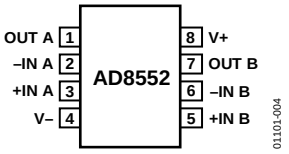

Figure 4. 8-Lead SOIC (R Suffix)

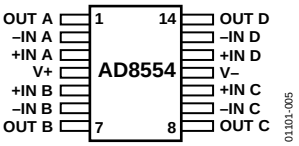

Figure 5. 14-Lead TSSOP (RU Suffix)

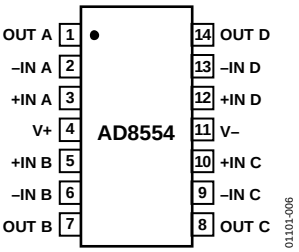

Figure 6. 14-Lead SOIC (R Suffix)

Rev. F **Document Feedback**
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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = 5 V, V_{CM} = 2.5 V, V_O = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	5	µV
		−40°C ≤ T_A ≤ +125°C			10	µV
Input Bias Current	I_B			10	50	pA
AD8551/AD8554		−40°C ≤ T_A ≤ +125°C		1.0	1.5	nA
AD8552		−40°C ≤ T_A ≤ +85°C		160	300	pA
AD8552		−40°C ≤ T_A ≤ +125°C		2.5	4	nA
Input Offset Current	I_{OS}			20	70	pA
AD8551/AD8554		−40°C ≤ T_A ≤ +125°C		150	200	pA
AD8552		−40°C ≤ T_A ≤ +85°C		30	150	pA
AD8552		−40°C ≤ T_A ≤ +125°C		150	400	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to +5 V	120	140		dB
		−40°C ≤ T_A ≤ +125°C	115	130		dB
Large Signal Voltage Gain[1]	A_{VO}	R_L = 10 kΩ, V_O = 0.3 V to 4.7 V	125	145		dB
		−40°C ≤ T_A ≤ +125°C	120	135		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.005	0.04	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	4.99	4.998		V
		R_L = 100 kΩ to GND @ −40°C to +125°C	4.99	4.997		V
		R_L = 10 kΩ to GND	4.95	4.98		V
		R_L = 10 kΩ to GND @ −40°C to +125°C	4.95	4.975		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		1	10	mV
		R_L = 100 kΩ to V+ @ −40°C to +125°C		2	10	mV
		R_L = 10 kΩ to V+		10	30	mV
		R_L = 10 kΩ to V+ @ −40°C to +125°C		15	30	mV
Output Short-Circuit Limit Current	I_{SC}		±25	±50		mA
		−40°C to +125°C		±40		mA
Output Current	I_O			±30		mA
		−40°C to +125°C		±15		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V	120	130		dB
		−40°C ≤ T_A ≤ +125°C	115	130		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		850	975	µA
		−40°C ≤ T_A ≤ +125°C		1000	1075	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.4		V/µs
Overload Recovery Time				0.05	0.3	ms
Gain Bandwidth Product	GBP			1.5		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0 Hz to 10 Hz		1.0		µV p-p
	e_n p-p	0 Hz to 1 Hz		0.32		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		42		nV/√Hz
Current Noise Density	i_n	f = 10 Hz		2		fA/√Hz

[1] Gain testing is dependent upon test bandwidth.

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V_S = 2.7 V, V_{CM} = 1.35 V, V_O = 1.35 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	5	µV
		−40°C ≤ T_A ≤ +125°C			10	µV
Input Bias Current	I_B			10	50	pA
AD8551/AD8554		−40°C ≤ T_A ≤ +125°C		1.0	1.5	nA
AD8552		−40°C ≤ T_A ≤ +85°C		160	300	pA
AD8552		−40°C ≤ T_A ≤ +125°C		2.5	4	nA
Input Offset Current	I_{OS}			10	50	pA
AD8551/AD8554		−40°C ≤ T_A ≤ +125°C		150	200	pA
AD8552		−40°C ≤ T_A ≤ +85°C		30	150	pA
AD8552		−40°C ≤ T_A ≤ +125°C		150	400	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	115	130		dB
		−40°C ≤ T_A ≤ +125°C	110	130		dB
Large Signal Voltage Gain[1]	A_{VO}	R_L = 10 kΩ, V_O = 0.3 V to 2.4 V	110	140		dB
		−40°C ≤ T_A ≤ +125°C	105	130		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.005	0.04	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	2.685	2.697		V
		R_L = 100 kΩ to GND @ −40°C to +125°C	2.685	2.696		V
		R_L = 10 kΩ to GND	2.67	2.68		V
		R_L = 10 kΩ to GND @ −40°C to +125°C	2.67	2.675		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		1	10	mV
		R_L = 100 kΩ to V+ @ −40°C to +125°C		2	10	mV
		R_L = 10 kΩ to V+		10	20	mV
		R_L = 10 kΩ to V+ @ −40°C to +125°C		15	20	mV
Short-Circuit Limit	I_{SC}		±10	±15		mA
		−40°C to +125°C		±10		mA
Output Current	I_O			±10		mA
		−40°C to +125°C		±5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V	120	130		dB
		−40°C ≤ T_A ≤ +125°C	115	130		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		750	900	µA
		−40°C ≤ T_A ≤ +125°C		950	1000	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.5		V/µs
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			1		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0 Hz to 10 Hz		1.6		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		75		nV/√Hz
Current Noise Density	i_n	f = 10 Hz		2		fA/√Hz

[1] Gain testing is dependent upon test bandwidth.

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ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND −0.3 V to V_S + 0.3 V
Differential Input Voltage[1]	±5.0 V
ESD (Human Body Model)	2000 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

[1] Differential input voltage is limited to ±5.0 V or the supply voltage, whichever is less.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM)	190	44	°C/W
8-Lead TSSOP (RU)	240	43	°C/W
8-Lead SOIC (R)	158	43	°C/W
14-Lead TSSOP (RU)	180	36	°C/W
14-Lead SOIC (R)	120	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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TYPICAL PERFORMANCE CHARACTERISTICS

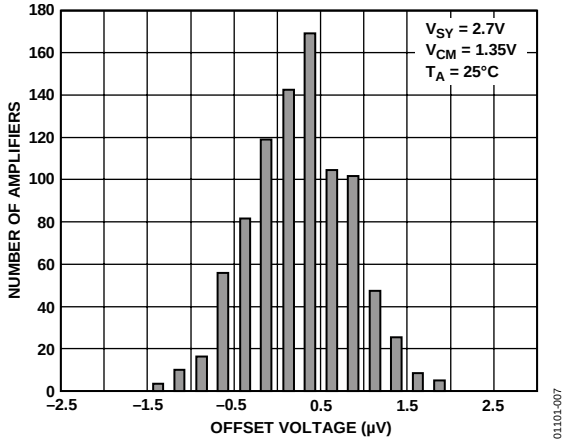

Figure 7. Input Offset Voltage Distribution at 2.7 V

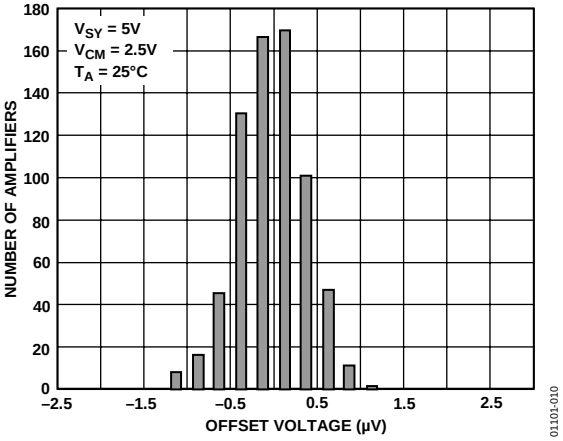

Figure 10. Input Offset Voltage Distribution at 5 V

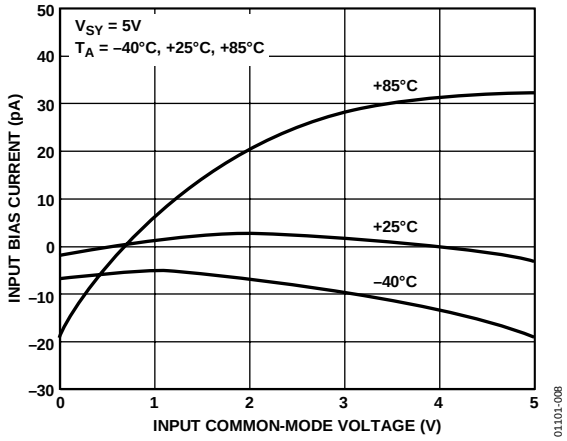

Figure 8. Input Bias Current vs. Common-Mode Voltage

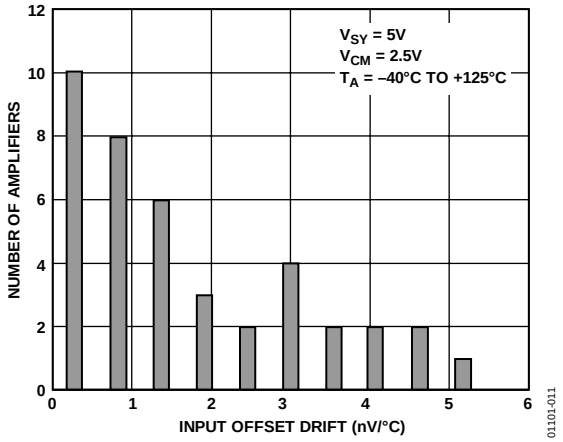

Figure 11. Input Offset Voltage Drift Distribution at 5 V

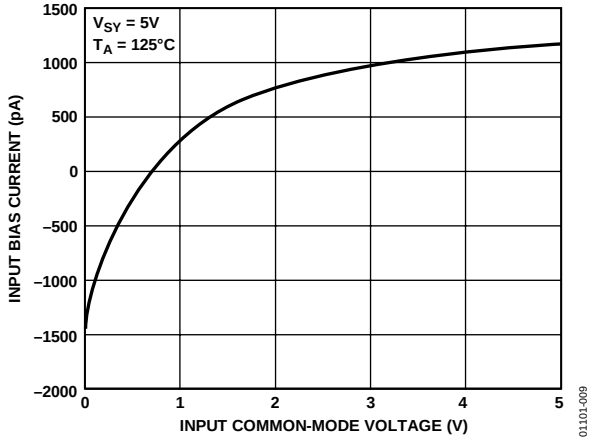

Figure 9. Input Bias Current vs. Common-Mode Voltage

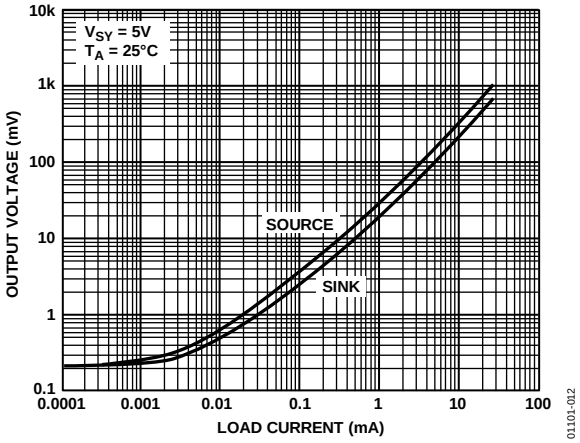

Figure 12. Output Voltage to Supply Rail vs. Load Current at 5 V

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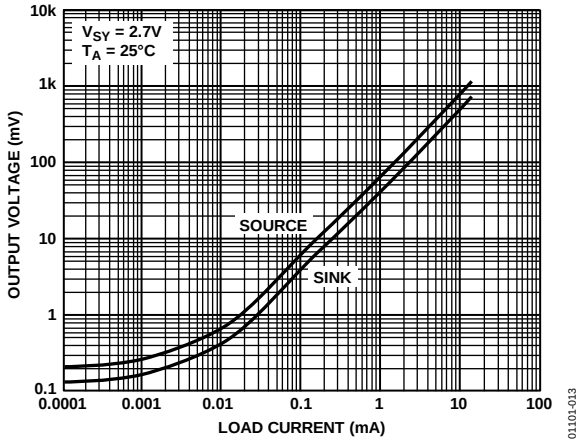


Figure 13. Output Voltage to Supply Rail vs. Load Current at 2.7 V

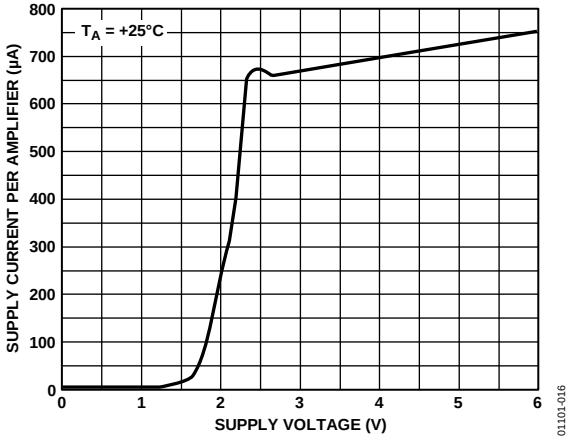


Figure 16. Supply Current per Amplifier vs. Supply Voltage

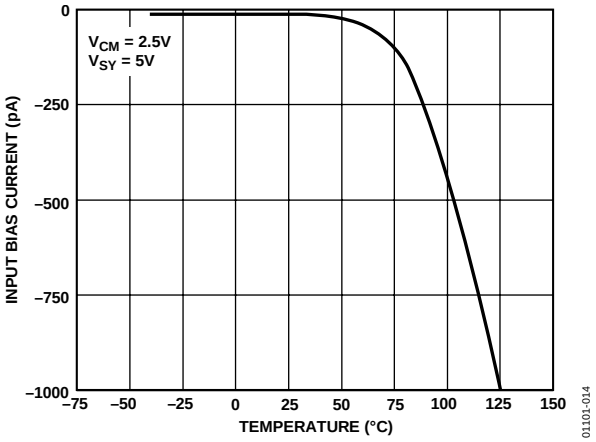


Figure 14. Input Bias Current vs. Temperature

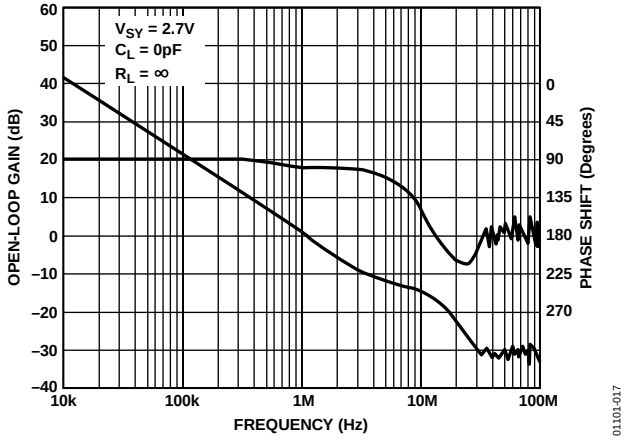


Figure 17. Open-Loop Gain and Phase Shift vs. Frequency at 2.7 V

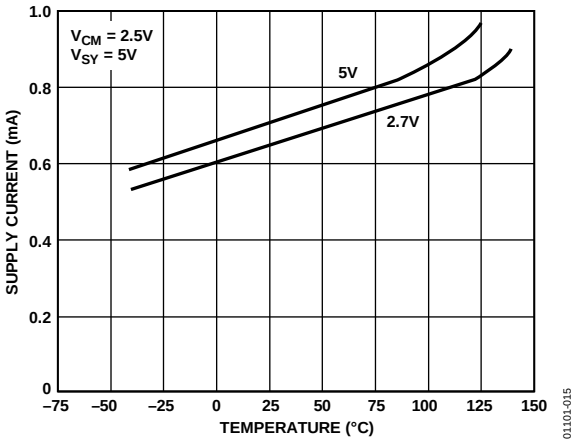


Figure 15. Supply Current vs. Temperature

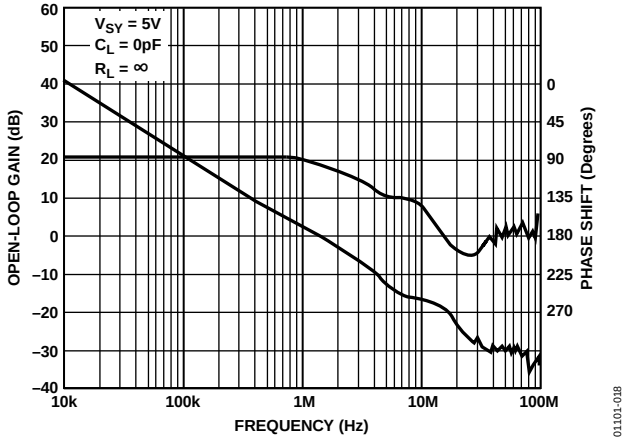


Figure 18. Open-Loop Gain and Phase Shift vs. Frequency at 5 V

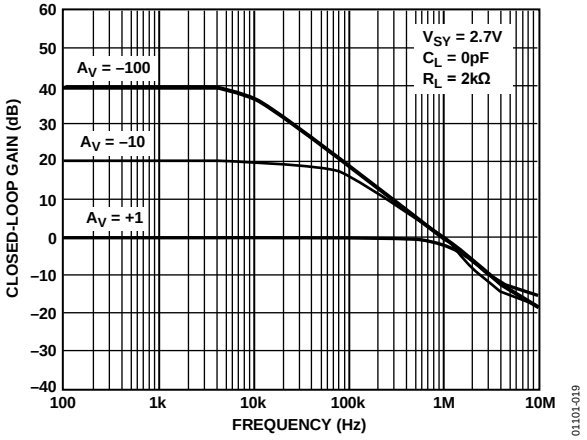


Figure 19. Closed-Loop Gain vs. Frequency at 2.7 V

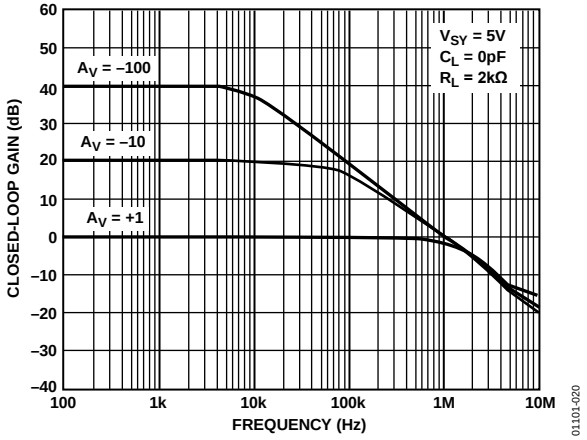


Figure 20. Closed-Loop Gain vs. Frequency at 5 V

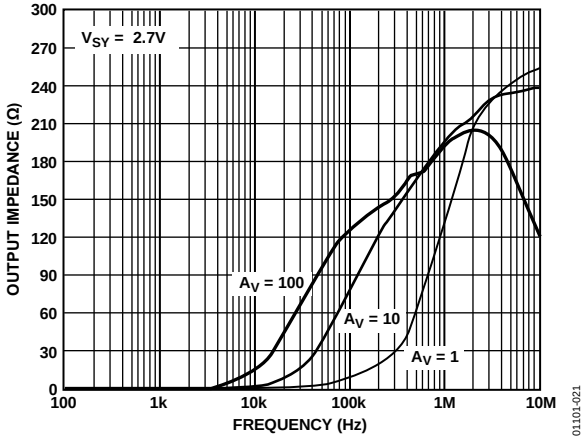


Figure 21. Output Impedance vs. Frequency at 2.7 V

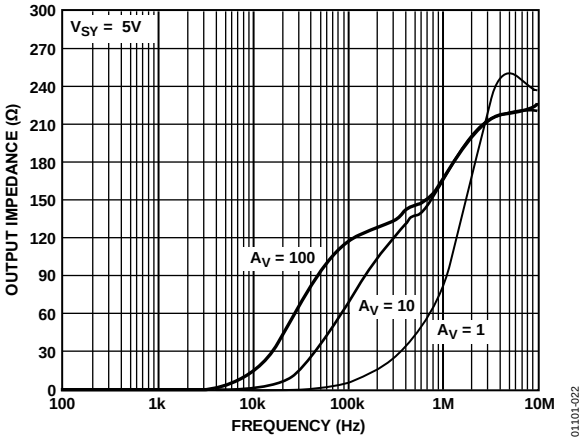


Figure 22. Output Impedance vs. Frequency at 5 V

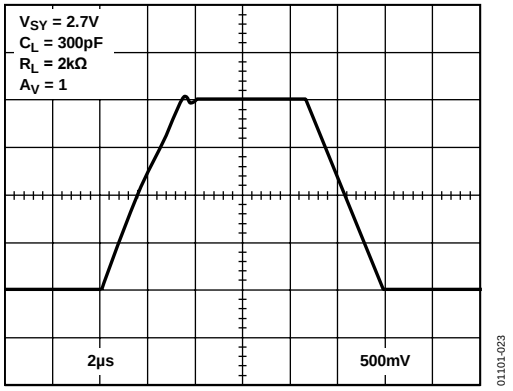


Figure 23. Large Signal Transient Response at 2.7 V

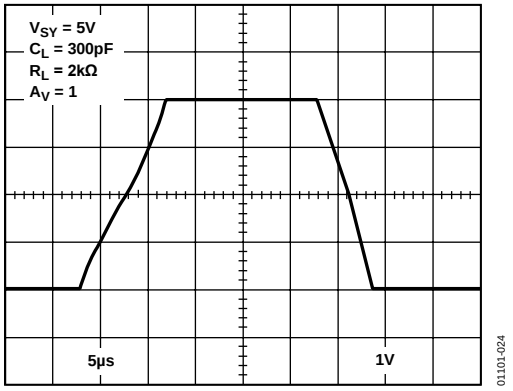


Figure 24. Large Signal Transient Response at 5 V

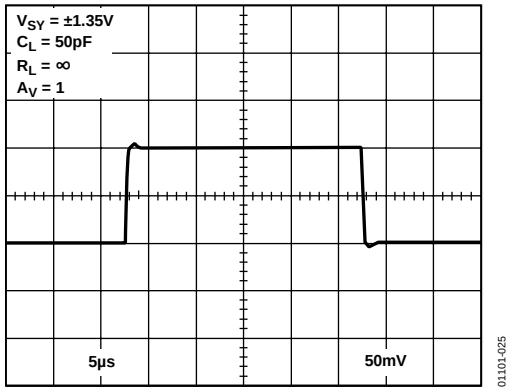


Figure 25. Small Signal Transient Response at 2.7 V

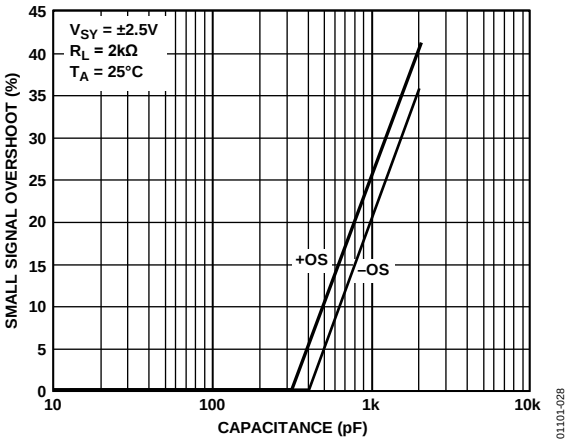


Figure 28. Small Signal Overshoot vs. Load Capacitance at 5 V

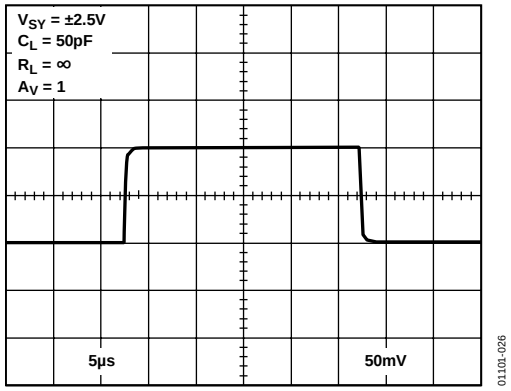


Figure 26. Small Signal Transient Response at 5 V

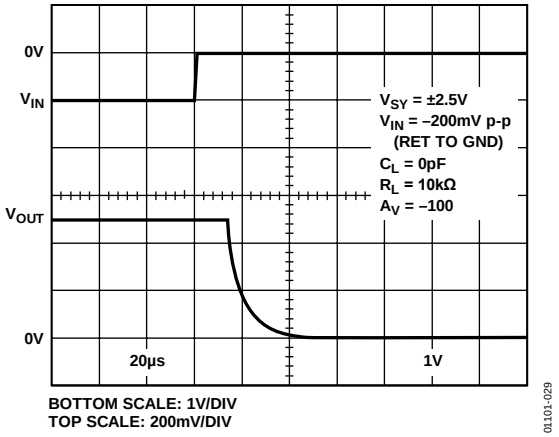


Figure 29. Positive Overvoltage Recovery

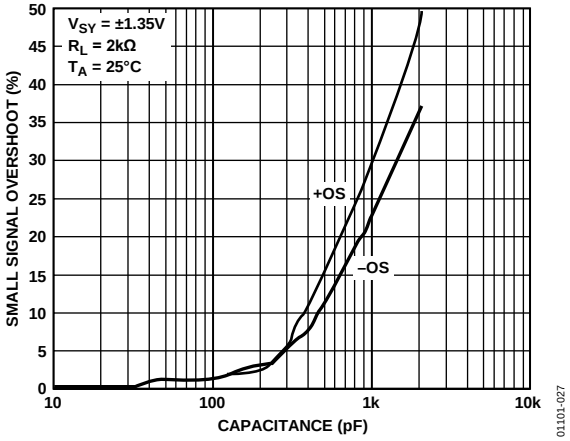


Figure 27. Small Signal Overshoot vs. Load Capacitance at 2.7 V

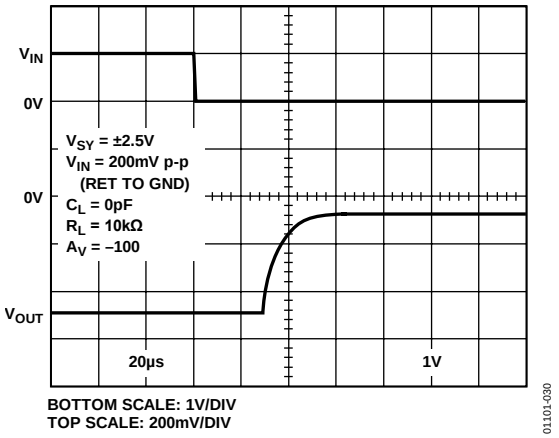


Figure 30. Negative Overvoltage Recovery

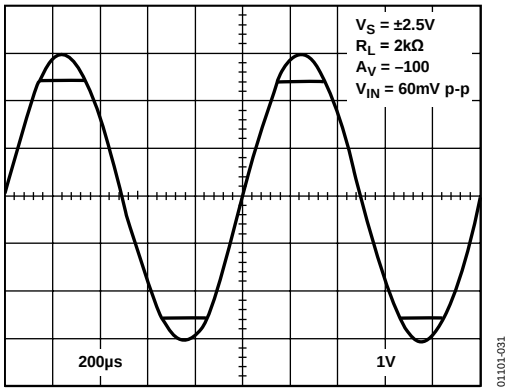


Figure 31. No Phase Reversal

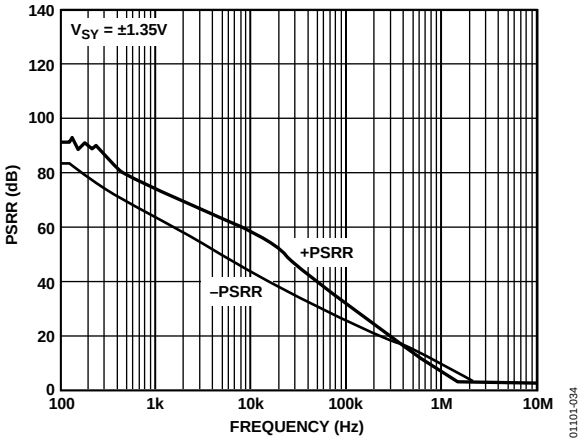


Figure 34. PSRR vs. Frequency at ±1.35 V

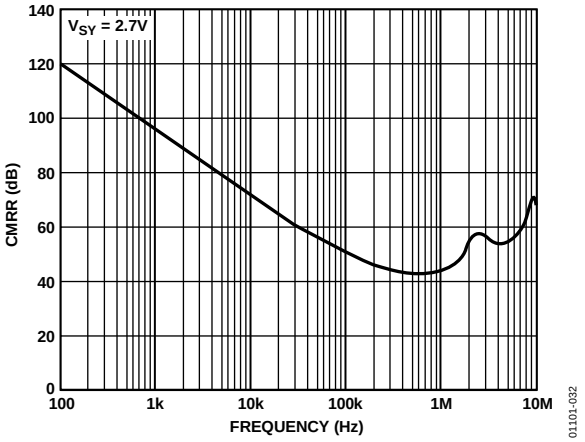


Figure 32. CMRR vs. Frequency at 2.7 V

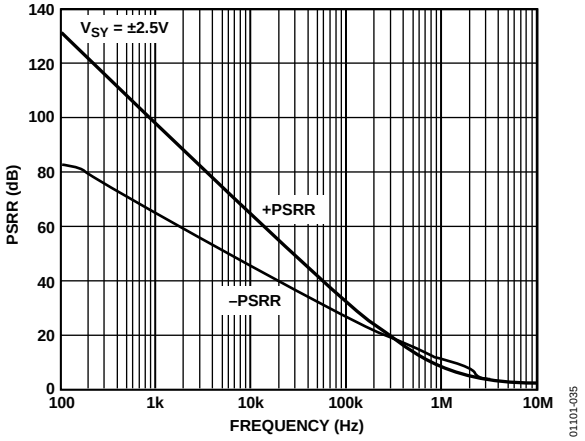


Figure 35. PSRR vs. Frequency at ±2.5 V

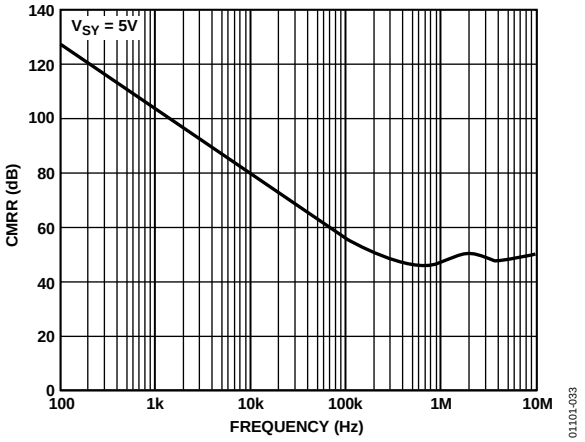


Figure 33. CMRR vs. Frequency at 5 V

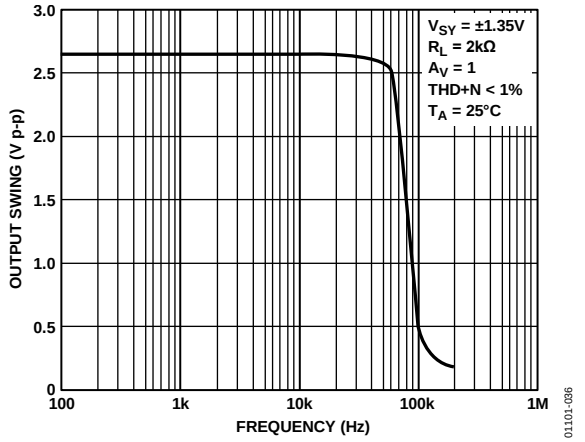


Figure 36. Maximum Output Swing vs. Frequency at 2.7 V

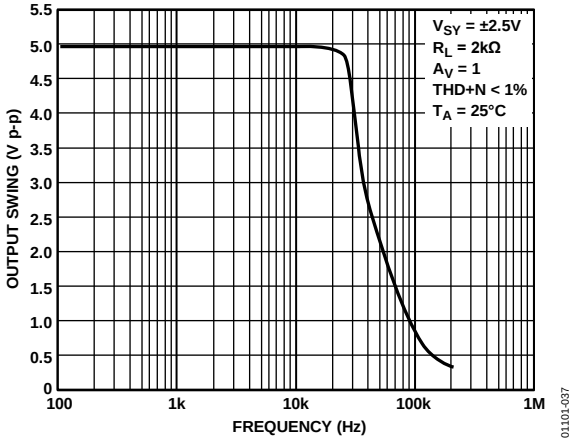


Figure 37. Maximum Output Swing vs. Frequency at 5 V

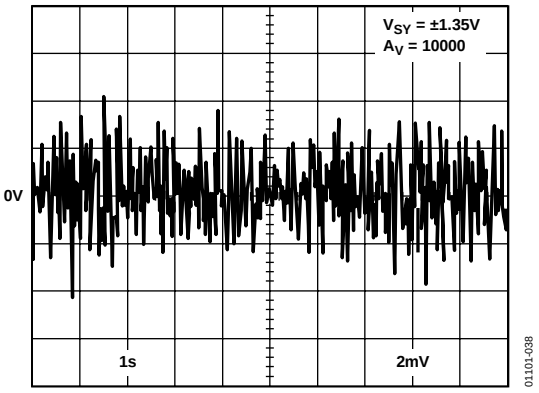


Figure 38. 0.1 Hz to 10 Hz Noise at 2.7 V

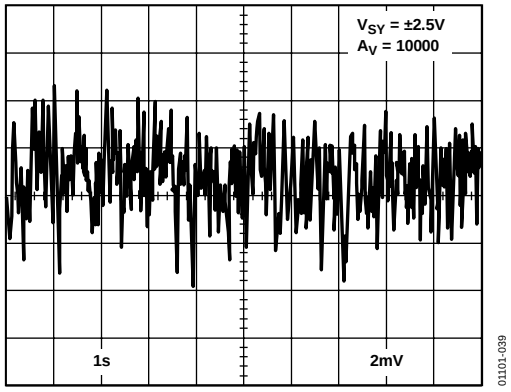


Figure 39. 0.1 Hz to 10 Hz Noise at 5 V

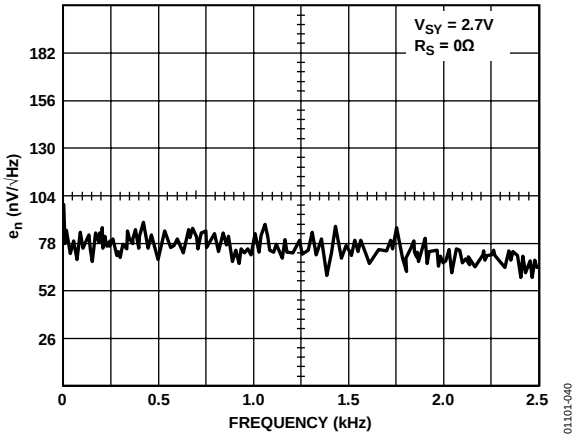


Figure 40. Voltage Noise Density at 2.7 V from 0 Hz to 2.5 kHz

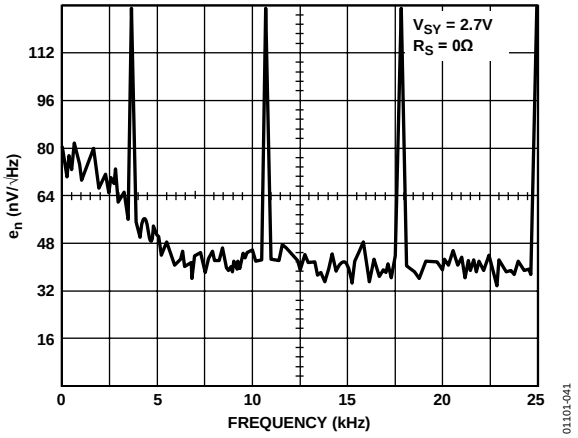


Figure 41. Voltage Noise Density at 2.7 V from 0 Hz to 25 kHz

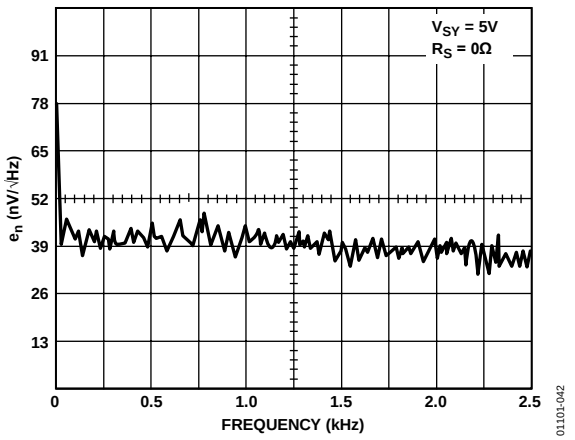


Figure 42. Voltage Noise Density at 5 V from 0 Hz to 2.5 kHz

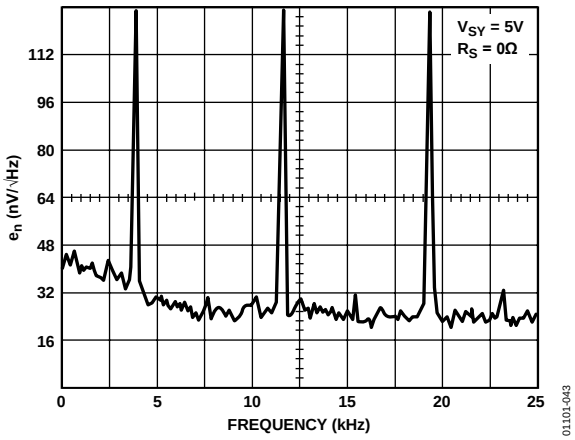


Figure 43. Voltage Noise Density at 5 V from 0 Hz to 25 kHz

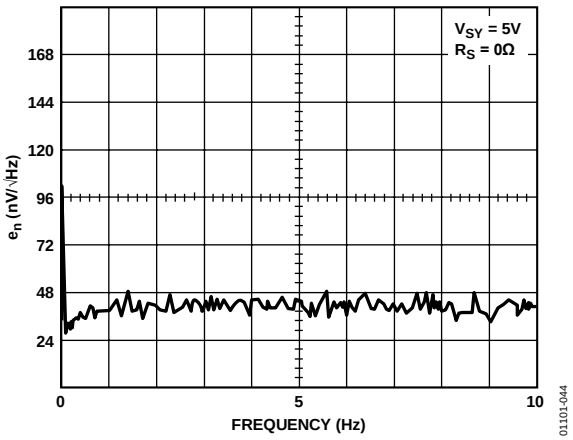


Figure 44. Voltage Noise Density at 5 V from 0 Hz to 10 Hz

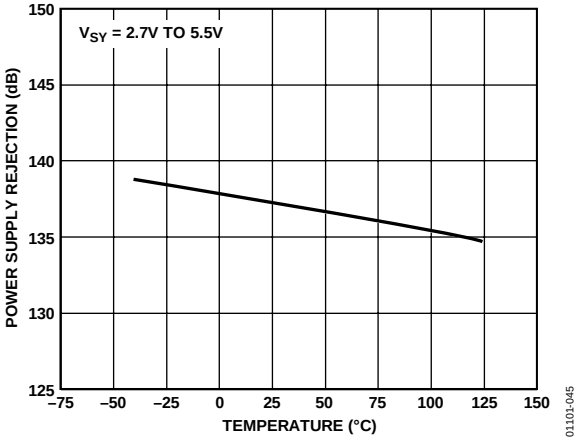


Figure 45. Power Supply Rejection vs. Temperature

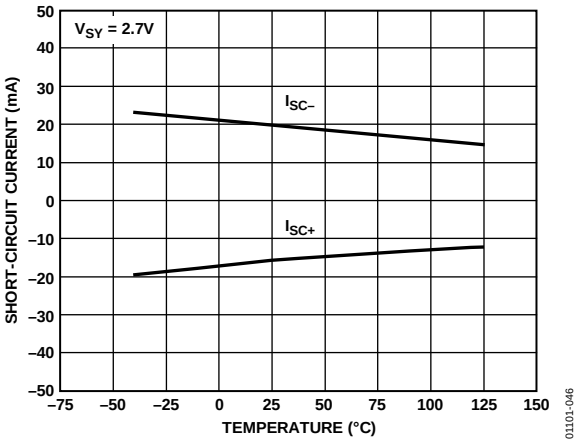


Figure 46. Output Short-Circuit Current vs. Temperature

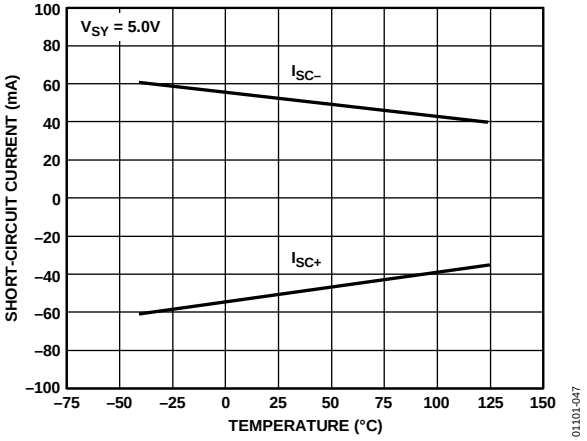


Figure 47. Output Short-Circuit Current vs. Temperature

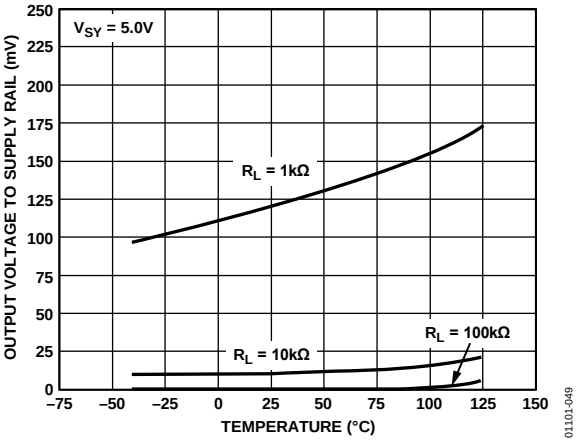


Figure 49. Output Voltage to Supply Rail vs. Temperature

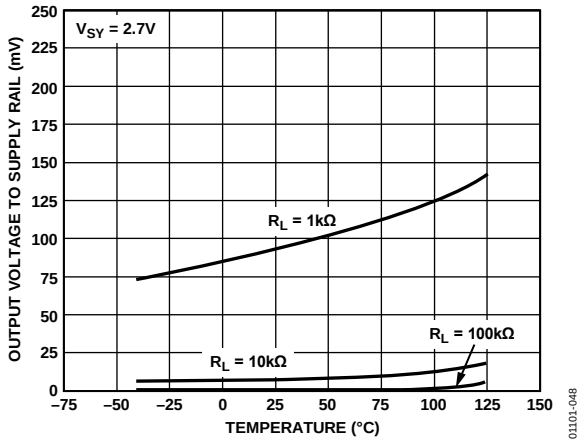


Figure 48. Output Voltage to Supply Rail vs. Temperature

FUNCTIONAL DESCRIPTION

The AD8551/AD8552/AD8554 are high precision, rail-to-rail operational amplifiers that can be run from a single-supply voltage. Their typical offset voltage of less than 1 μV allows these amplifiers to be easily configured for high gains without risk of excessive output voltage errors. The extremely small temperature drift of 5 nV/°C ensures a minimum of offset voltage error over its entire temperature range of −40°C to +125°C, making the AD8551/AD8552/AD8554 amplifiers ideal for a variety of sensitive measurement applications in harsh operating environments, such as underhood and braking/suspension systems in automobiles.

The AD8551/AD8552/AD8554 are CMOS amplifiers and achieve their high degree of precision through auto-zero stabilization. This autocorrection topology allows the AD8551/AD8552/AD8554 to maintain its low offset voltage over a wide temperature range and over its operating lifetime.

AMPLIFIER ARCHITECTURE

Each AD8551/AD8552/AD8554 op amps consist of two amplifiers, a main amplifier and a secondary amplifier, used to correct the offset voltage of the main amplifier. Both consist of a rail-to-rail input stage, allowing the input common-mode voltage range to reach both supply rails. The input stage consists of an NMOS differential pair operating concurrently with a parallel PMOS differential pair. The outputs from the differential input stages are combined in another gain stage whose output is used to drive a rail-to-rail output stage.

The wide voltage swing of the amplifier is achieved by using two output transistors in a common-source configuration. The output voltage range is limited by the drain-to-source resistance of these transistors. As the amplifier is required to source or sink more output current, the r_{DS} of these transistors increases, raising the voltage drop across these transistors. Simply put, the output voltage does not swing as close to the rail under heavy output current conditions as it does with light output current. This is a characteristic of all rail-to-rail output amplifiers. Figure 12 and Figure 13 show how close the output voltage can get to the rails with a given output current. The output of the AD8551/AD8552/AD8554 is short-circuit protected to approximately 50 mA of current.

The AD8551/AD8552/AD8554 amplifiers have exceptional gain, yielding greater than 120 dB of open-loop gain with a load of 2 kΩ. Because the output transistors are configured in a common-source configuration, the gain of the output stage, and thus the open-loop gain of the amplifier, is dependent on the load resistance. Open-loop gain decreases with smaller load resistances. This is another characteristic of rail-to-rail output amplifiers.

BASIC AUTO-ZERO AMPLIFIER THEORY

Autocorrection amplifiers are not a new technology. Various IC implementations have been available for more than 15 years with some improvements made over time. The AD8551/AD8552/AD8554 design offers a number of significant performance improvements over previous versions while attaining a very substantial reduction in device cost. This section offers a simplified explanation of how the AD8551/AD8552/AD8554 are able to offer extremely low offset voltages and high open-loop gains.

As noted in the Amplifier Architecture section, each AD8551/AD8552/AD8554 op amp contains two internal amplifiers. One is used as the primary amplifier, the other as an autocorrection, or nulling, amplifier. Each amplifier has an associated input offset voltage that can be modeled as a dc voltage source in series with the noninverting input. In Figure 50 and Figure 51 these are labeled as V_{OSX}, where x denotes the amplifier associated with the offset: A for the nulling amplifier and B for the primary amplifier. The open-loop gain for the +IN and −IN inputs of each amplifier is given as A_X. Both amplifiers also have a third voltage input with an associated open-loop gain of B_X.

There are two modes of operation determined by the action of two sets of switches in the amplifier: an auto-zero phase and an amplification phase.

Auto-Zero Phase

In this phase, all φA switches are closed and all φB switches are opened. Here, the nulling amplifier is taken out of the gain loop by shorting its two inputs together. Of course, there is a degree of offset voltage, shown as V_{OSA}, inherent in the nulling amplifier which maintains a potential difference between the +IN and −IN inputs. The nulling amplifier feedback loop is closed through φB_2 and V_{OSA} appears at the output of the nulling amp and on C_{M1}, an internal capacitor in the AD8551/AD8552/AD8554. Mathematically, this is expressed in the time domain as

$$V_{OA}[t] = A_A V_{OSA}[t] - B_A V_{OA}[t] \quad (1)$$

which can be expressed as

$$V_{OA}[t] = \frac{A_A V_{OSA}[t]}{1 + B_A} \quad (2)$$

This demonstrates that the offset voltage of the nulling amplifier times a gain factor appears at the output of the nulling amplifier and, thus, on the C_{M1} capacitor.

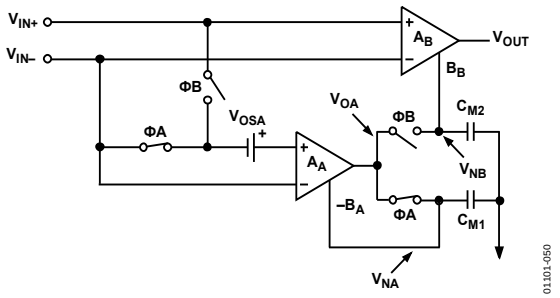


Figure 50. Auto-Zero Phase of the AD8551/AD8552/AD8554

Amplification Phase

When the φB switches close and the φA switches open for the amplification phase, this offset voltage remains on C_{M1} and, essentially, corrects any error from the nulling amplifier. The voltage across C_{M1} is designated as V_{NA}. Furthermore, V_{IN} is designated as the potential difference between the two inputs to the primary amplifier, or $V_{IN} = (V_{IN+} - V_{IN-})$. Thus, the nulling amplifier can be expressed as

$$V_{OA}[t] = A_A\left(V_{IN}[t] - V_{OSA}[t]\right) - B_A V_{NA}[t] \quad (3)$$

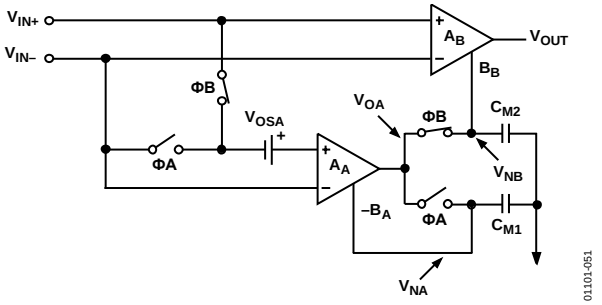


Figure 51. Output Phase of the Amplifier

Because φA is now open and there is no place for C_{M1} to discharge, the voltage (V_{NA}), at the present time (t), is equal to the voltage at the output of the nulling amp (V_{OA}) at the time when φA was closed. If the period of the autocorrection switching frequency is labeled t_S, then the amplifier switches between phases every $0.5 \times t_S$. Therefore, in the amplification phase

$$V_{NA}[t] = V_{NA}\left[t - \frac{1}{2}t_S\right] \quad (4)$$

Substituting Equation 4 and Equation 2 into Equation 3 yields

$$V_{OA}[t] = A_A V_{IN}[t] + A_A V_{OSA}[t] - \frac{A_A B_A V_{OSA}\left[t - \frac{1}{2}t_S\right]}{1 + B_A} \quad (5)$$

For the sake of simplification, assume that the autocorrection frequency is much faster than any potential change in V_{OSA} or V_{OSB}. This is a valid assumption because changes in offset voltage are a function of temperature variation or long-term wear time, both of which are much slower than the auto-zero clock frequency of the AD8551/AD8552/AD8554. This effectively renders V_{OS}

time invariant; therefore, Equation 5 can be rearranged and rewritten as

$$V_{OA}[t] = A_A V_{IN}[t] + \frac{A_A(1 + B_A)V_{OSA} - A_A B_A V_{OSA}}{1 + B_A} \quad (6)$$

or

$$V_{OA}[t] = A_A\left(V_{IN}[t] + \frac{V_{OSA}}{1 + B_A}\right) \quad (7)$$

From these equations, the auto-zeroing action becomes evident. Note the V_{OS} term is reduced by a $1 + B_A$ factor. This shows how the nulling amplifier has greatly reduced its own offset voltage error even before correcting the primary amplifier. This results in the primary amplifier output voltage becoming the voltage at the output of the AD8551/AD8552/AD8554 amplifiers. It is equal to

$$V_{OUT}[t] = A_B\left(V_{IN}[t] + V_{OSB}\right) + B_B V_{NB} \quad (8)$$

In the amplification phase, $V_{OA} = V_{NB}$, so this can be rewritten as

$$V_{OUT}[t] = A_B V_{IN}[t] + A_B V_{OSB} + B_B\left[A_A\left(V_{IN}[t] + \frac{V_{OSB}}{1 + B_A}\right)\right] \quad (9)$$

Combining terms,

$$V_{OUT}[t] = V_{IN}[t]\left(A_B + A_B B_B\right) + \frac{A_A B_A V_{OSA}}{1 + B_A} + A_B V_{OSA} \quad (10)$$

The AD8551/AD8552/AD8554 architecture is optimized in such a way that

$$A_A = A_B \text{ and } B_A = B_B \text{ and } B_A >> 1$$

Also, the gain product of $A_A B_B$ is much greater than A_B. These allow Equation 10 to be simplified to

$$V_{OUT}[t] \approx V_{IN}[t] A_A B_A + A_A\left(V_{OSA} + V_{OSB}\right) \quad (11)$$

Most obvious is the gain product of both the primary and nulling amplifiers. This $A_A B_A$ term is what gives the AD8551/AD8552/AD8554 its extremely high open-loop gain. To understand how V_{OSA} and V_{OSB} relate to the overall effective input offset voltage of the complete amplifier, establish the generic amplifier equation of

$$V_{OUT} = k \times \left(V_{IN} + V_{OS,EFF}\right) \quad (12)$$

where k is the open-loop gain of an amplifier and $V_{OS,EFF}$ is its effective offset voltage.

Putting Equation 12 into the form of Equation 11 gives

$$V_{OUT}[t] \approx V_{IN}[t] A_A B_A + V_{OS,EFF} A_A B_A \quad (13)$$

Thus, it is evident that

$$V_{OS,EFF} \approx \frac{V_{OSA} + V_{OSB}}{B_A} \quad (14)$$

The offset voltages of both the primary and nulling amplifiers are reduced by the Gain Factor B_A. This takes a typical input offset voltage from several millivolts down to an effective input offset voltage of submicrovolts. This autocorrection scheme is the outstanding feature of the AD8551/AD8552/AD8554 series that continues to earn the reputation of being among the most precise amplifiers available on the market.

HIGH GAIN, CMRR, PSRR

Common-mode and power supply rejection are indications of the amount of offset voltage an amplifier has as a result of a change in its input common-mode or power supply voltages. As shown in the previous section, the autocorrection architecture of the

AD8551/AD8552/AD8554 allows it to quite effectively minimize offset voltages. The technique also corrects for offset errors caused by common-mode voltage swings and power supply variations. This results in superb CMRR and PSRR figures in excess of 130 dB. Because the autocorrection occurs continuously, these figures can be maintained across the entire temperature range of the device, from −40°C to +125°C.

MAXIMIZING PERFORMANCE THROUGH PROPER LAYOUT

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the AD8551/AD8552/AD8554, care is needed in laying out the circuit board. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure 52 shows proper guard ring configuration, and Figure 53 shows the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the noninverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

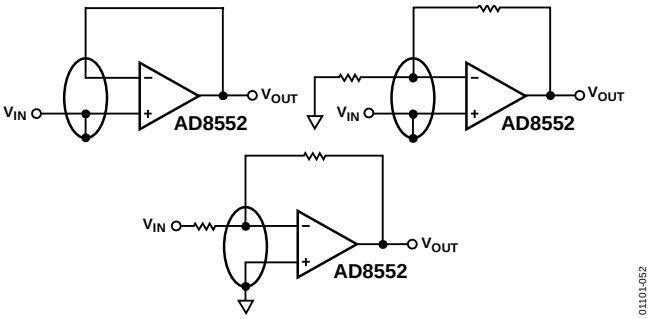


Figure 52. Guard Ring Layout and Connections to Reduce PC Board Leakage Currents

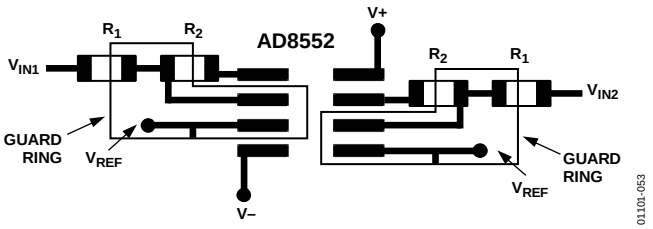


Figure 53. Top View of AD8552 SOIC Layout with Guard Rings

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. Figure 54 shows a cross-section of the thermal voltage error sources. If the temperature of the PC board at one end of the component (T_{A1}) is different from the temperature at the other end (T_{A2}), the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

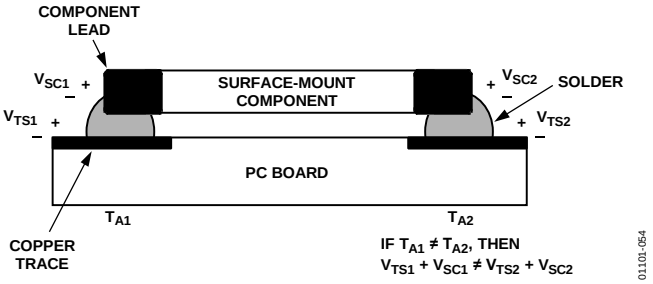


Figure 54. Mismatch in Seebeck Voltages Causes Thermoelectric Voltage Error

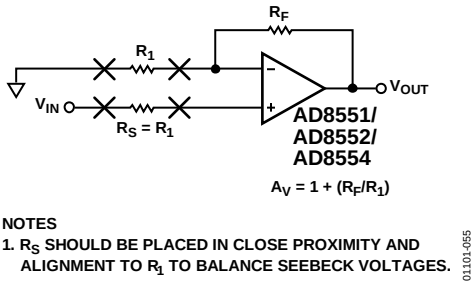


Figure 55. Using Dummy Components to Cancel Thermoelectric Voltage Errors

1/f NOISE CHARACTERISTICS

Another advantage of auto-zero amplifiers is their ability to cancel flicker noise. Flicker noise, also known as 1/f noise, is noise inherent in the physics of semiconductor devices, and it increases 3 dB for every octave decrease in frequency. The 1/f corner frequency of an amplifier is the frequency at which the flicker noise is equal to the broadband noise of the amplifier. At lower frequencies, flicker noise dominates, causing higher degrees of error for sub-Hertz frequencies or dc precision applications.

Because the AD8551/AD8552/AD8554 amplifiers are self-correcting op amps, they do not have increasing flicker noise at lower frequencies. In essence, low frequency noise is treated as a slowly varying offset error and is greatly reduced as a result of autocorrection. The correction becomes more effective as the noise frequency approaches dc, offsetting the tendency of the noise to increase exponentially as frequency decreases. This allows the AD8551/AD8552/AD8554 to have lower noise near dc than standard low noise amplifiers that are susceptible to 1/f noise.

INTERMODULATION DISTORTION

The AD8551/AD8552/AD8554 can be used as a conventional op amp for gain/ bandwidth combinations up to 1.5 MHz. The auto-zero correction frequency of the device is fixed at 4 kHz. Although a trace amount of this frequency feeds through to the output, the amplifier can be used at much higher frequencies. Figure 56 shows the spectral output of the AD8552 with the amplifier configured for unity gain and the input grounded.

The 4 kHz auto-zero clock frequency appears at the output with less than 2 µV of amplitude. Harmonics are also present, but at reduced levels from the fundamental auto-zero clock frequency. The amplitude of the clock frequency feedthrough is proportional to the closed-loop gain of the amplifier. Like other autocorrection amplifiers, at higher gains there is more clock frequency feedthrough. Figure 57 shows the spectral output with the amplifier configured for a gain of 60 dB.

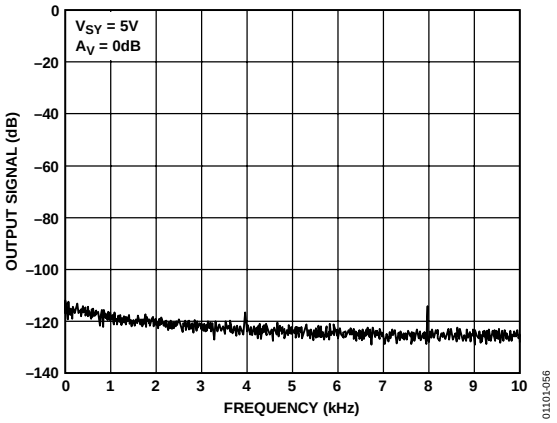


Figure 56. Spectral Analysis of AD8552 Output in Unity Gain Configuration

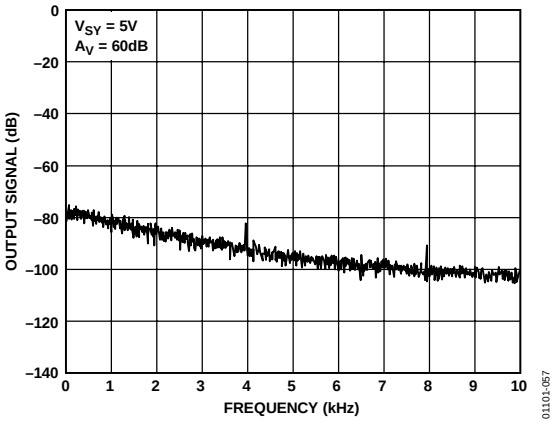


Figure 57. Spectral Analysis of AD8551/AD8552/AD8554 Output with +60 dB Gain

When an input signal is applied, the output contains some degree of intermodulation distortion (IMD). This is another characteristic feature of all autocorrection amplifiers. IMD appears as sum and difference frequencies between the input signal and the 4 kHz clock frequency (and its harmonics) and is at a level similar to, or less than, the clock feedthrough at the output. The IMD is also proportional to the closed-loop gain of the amplifier. Figure 58 shows the spectral output of an AD8552 configured as a high gain stage (+60 dB) with a 1 mV input signal applied. The relative levels of all IMD products and harmonic distortion add up to produce an output error of −60 dB relative to the input signal. At unity gain, these add up to only −120 dB relative to the input signal.

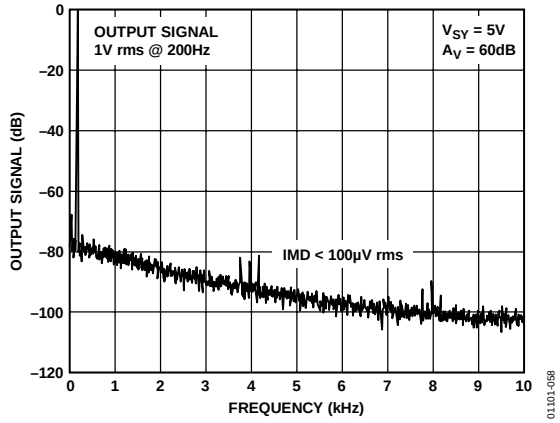


Figure 58. Spectral Analysis of AD8552 in High Gain with a 1 mV Input Signal

For most low frequency applications, the small amount of auto-zero clock frequency feedthrough does not affect the precision of the measurement system. If it is desired, the clock frequency feedthrough can be reduced through the use of a feedback capacitor around the amplifier. However, this reduces the bandwidth of the amplifier. Figure 59 and Figure 60 show a configuration for reducing the clock feedthrough and the corresponding spectral analysis at the output. The −3 dB bandwidth of this configuration is 480 Hz.

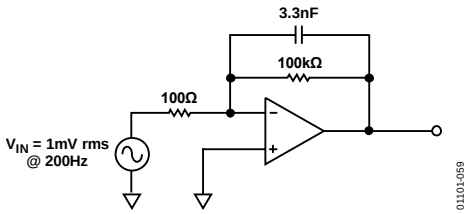


Figure 59. Reducing Autocorrection Clock Noise Using a Feedback Capacitor

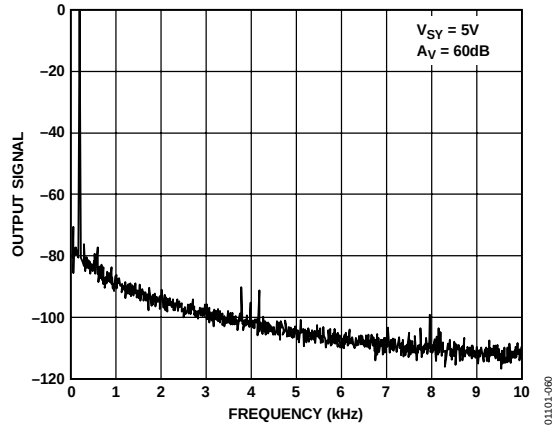


Figure 60. Spectral Analysis Using a Feedback Capacitor

BROADBAND AND EXTERNAL RESISTOR NOISE CONSIDERATIONS

The total broadband noise output from any amplifier is primarily a function of three types of noise: input voltage noise from the amplifier, input current noise from the amplifier, and Johnson noise from the external resistors used around the amplifier. Input voltage noise, or e_n, is strictly a function of the amplifier used. The Johnson noise from a resistor is a function of the resistance and the temperature. Input current noise, or i_n, creates an equivalent voltage noise proportional to the resistors used around the amplifier. These noise sources are not correlated with each other and their combined noise sums in a root-squared-sum fashion. The full equation is given as

$$e_{n\_TOTAL} = \left[e_n^2 + 4kTr_S + \left(i_n R_S\right)^2\right]^{1/2} \quad (15)$$

Where:
e_n = the input voltage noise density of the amplifier.
i_n = the input current noise of the amplifier.
R_S = source resistance connected to the noninverting terminal.
k = Boltzmann's constant (1.38×10^{-23} J/K).
T = ambient temperature in Kelvin (K = 273.15 + °C).

The input voltage noise density (e_n) of the AD8551/AD8552/AD8554 is 42 nV/√Hz, and the input noise, i_n, is 2 fA/√Hz. The $e_{n, TOTAL}$ is dominated by the input voltage noise, provided the source resistance is less than 106 kΩ. With source resistance greater than 106 kΩ, the overall noise of the system is dominated by the Johnson noise of the resistor itself.

Because the input current noise of the AD8551/AD8552/AD8554 is very small, it does not become a dominant term unless R_S is greater than 4 GΩ, which is an impractical value of source resistance.

The total noise ($e_{n, TOTAL}$) is expressed in volts per square root Hertz, and the equivalent rms noise over a certain bandwidth can be found as

$$e_n = e_{n,TOTAL} \times \sqrt{BW} \quad (16)$$

where BW is the bandwidth of interest in Hertz.

OUTPUT OVERDRIVE RECOVERY

The AD8551/AD8552/AD8554 amplifiers have an excellent overdrive recovery of only 200 µs from either supply rail. This characteristic is particularly difficult for autocorrection amplifiers because the nulling amplifier requires a nontrivial amount of time to error correct the main amplifier back to a valid output. Figure 29 and Figure 30 show the positive and negative overdrive recovery times for the AD8551/AD8552/AD8554.

The output overdrive recovery for an autocorrection amplifier is defined as the time it takes for the output to correct to its final voltage from an overload state. It is measured by placing the amplifier in a high gain configuration with an input signal that forces the output voltage to the supply rail. The input voltage is then stepped down to the linear region of the amplifier, usually to halfway between the supplies. The time from the input signal stepdown to the output settling to within 100 µV of its final value is the overdrive recovery time.

INPUT OVERVOLTAGE PROTECTION

Although the AD8551/AD8552/AD8554 are rail-to-rail input amplifiers, exercise care to ensure that the potential difference between the inputs does not exceed 5 V. Under normal operating conditions, the amplifier corrects its output to ensure the two inputs are at the same voltage. However, if the device is configured as a comparator, or is under some unusual operating condition, the input voltages may be forced to different potentials. This can cause excessive current to flow through internal diodes in the AD8551/AD8552/AD8554 used to protect the input stage against overvoltage.

If either input exceeds either supply rail by more than 0.3 V, large amounts of current begin to flow through the ESD protection diodes in the amplifier. These diodes connect between the inputs and each supply rail to protect the input transistors against an electrostatic discharge event and are normally reverse-biased. However, if the input voltage exceeds the supply voltage, these ESD diodes become forward-biased. Without current limiting, excessive amounts of current can flow through these diodes, causing permanent damage to the device. If inputs are subjected to overvoltage, appropriate series resistors should be inserted to limit the diode current to less than 2 mA maximum.

OUTPUT PHASE REVERSAL

Output phase reversal occurs in some amplifiers when the input common-mode voltage range is exceeded. As common-mode voltage moves outside of the common-mode range, the outputs of these amplifiers suddenly jump in the opposite direction to the supply rail. This is the result of the differential input pair shutting down and causing a radical shifting of internal voltages, resulting in the erratic output behavior.

The AD8551/AD8552/AD8554 amplifiers have been carefully designed to prevent any output phase reversal, provided both inputs are maintained within the supply voltages. If there is the potential of one or both inputs exceeding either supply voltage, place a resistor in series with the input to limit the current to less than 2 mA to ensure the output does not reverse its phase.

CAPACITIVE LOAD DRIVE

The AD8551/AD8552/AD8554 have excellent capacitive load driving capabilities and can safely drive up to 10 nF from a single 5 V supply. Although the device is stable, capacitive loading limits the bandwidth of the amplifier. Capacitive loads also increase the amount of overshoot and ringing at the output. An R-C snubber network, shown in Figure 61, can be used to compensate the amplifier against capacitive load ringing and overshoot.

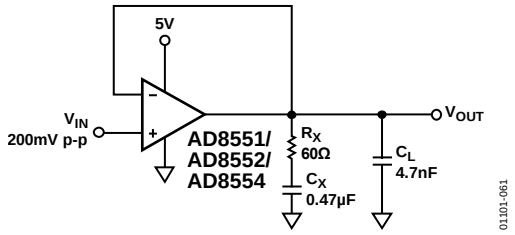


Figure 61. Snubber Network Configuration for Driving Capacitive Loads

Although the snubber does not recover the loss of amplifier bandwidth from the load capacitance, it does allow the amplifier to drive larger values of capacitance while maintaining a minimum of overshoot and ringing. Figure 62 shows the output of an AD8551/AD8552/AD8554 driving a 1 nF capacitor with and without a snubber network.

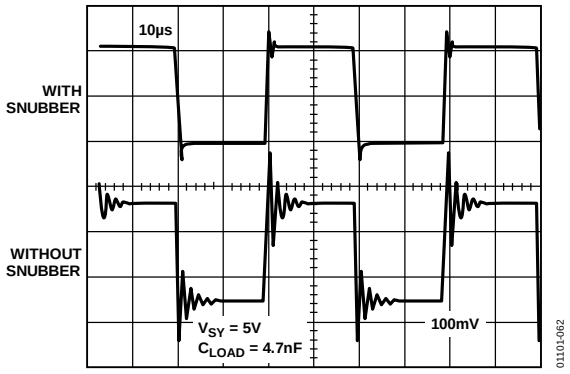


Figure 62. Overshoot and Ringing are Substantially Reduced Using a Snubber Network

The optimum value for the resistor and capacitor is a function of the load capacitance and is best determined empirically because actual C_{LOAD} (C_L) includes stray capacitances and may differ substantially from the nominal capacitive load. Table 5 shows some snubber network values that can be used as starting points.

Table 5. Snubber Network Values for Driving Capacitive Loads

C_{LOAD}	R_X	C_X
1 nF	200 Ω	1 nF
4.7 nF	60 Ω	0.47 µF
10 nF	20 Ω	10 µF

POWER-UP BEHAVIOR

At power-up, the AD8551/AD8552/AD8554 settle to a valid output within 5 µs. Figure 63 shows an oscilloscope photo of the output of the amplifier with the power supply voltage, and Figure 64 shows the test circuit. With the amplifier configured for unity gain, the device takes approximately 5 µs to settle to its final output voltage. This turn-on response time is much faster than most other autocorrection amplifiers, which can take hundreds of microseconds or longer for their output to settle.

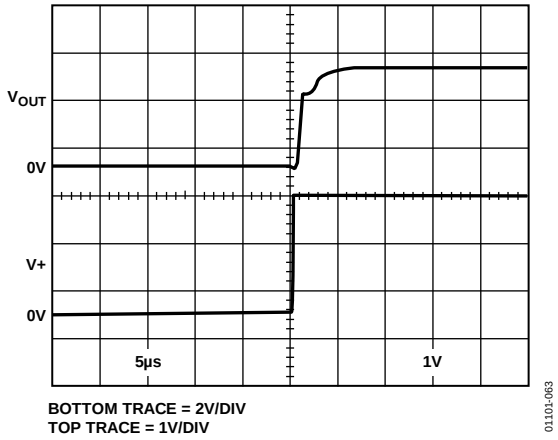


Figure 63. AD8551/AD8552/AD8554 Output Behavior on Power-Up

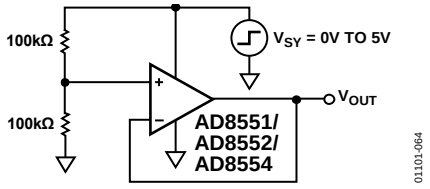


Figure 64. AD8551/AD8552/AD8554 Test Circuit for Turn-On Time

APPLICATIONS INFORMATION

A 5 V PRECISION STRAIN GAGE CIRCUIT

The extremely low offset voltage of the AD8552 makes it an ideal amplifier for any application requiring accuracy with high gains, such as a weigh scale or strain gage. Figure 65 shows a configuration for a single-supply, precision, strain gage measurement system.

A REF192 provides a 2.5 V precision reference voltage for A2. The A2 amplifier boosts this voltage to provide a 4.0 V reference for the top of the strain gage resistor bridge. Q1 provides the current drive for the 350 Ω bridge network. A1 is used to amplify the output of the bridge with the full-scale output voltage equal to

$$\frac{2\times(R_1+R_2)}{R_B} \tag{17}$$

where R_B is the resistance of the load cell.

Using the values given in Figure 65, the output voltage linearly varies from 0 V with no strain to 4.0 V under full strain.

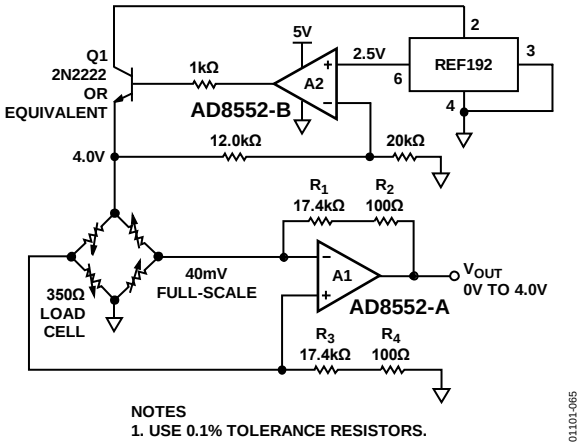


Figure 65. A 5 V Precision Strain Gage Amplifier

3 V INSTRUMENTATION AMPLIFIER

The high common-mode rejection, high open-loop gain, and operation down to 3 V of supply voltage makes the AD8551/AD8552/AD8554 an excellent choice of op amp for discrete single-supply instrumentation amplifiers. The common-mode rejection ratio of the AD8551/AD8552/AD8554 is greater than 120 dB, but the CMRR of the system is also a function of the external resistor tolerances. The gain of the difference amplifier shown in Figure 66 is given as

$$V_{OUT}=V1\left(\frac{R_4}{R_3+R_4}\right)\left(1+\frac{R_1}{R_2}\right)-V2\left(\frac{R_2}{R_1}\right) \tag{18}$$

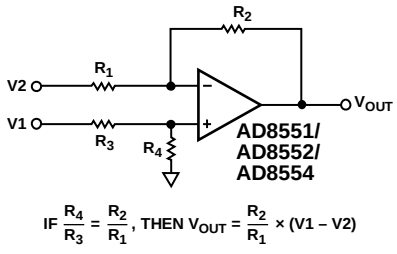


Figure 66. Using the AD8551/AD8552/AD8554 as a Difference Amplifier

In an ideal difference amplifier, the ratio of the resistors are set exactly equal to

$$A_V=\frac{R_2}{R_1}=\frac{R_4}{R_3} \tag{19}$$

Which sets the output voltage of the system to

$$V_{OUT}=A_V(V1-V2) \tag{20}$$

Due to finite component tolerance, the ratio between the four resistors is not exactly equal, and any mismatch results in a reduction of common-mode rejection from the system. Referring to Figure 66, the exact common-mode rejection ratio can be expressed as

$$CMRR=\frac{R_1R_4+2R_2R_4+R_2R_3}{2R_1R_4-2R_2R_3} \tag{21}$$

In the three-op amp, instrumentation amplifier configuration shown in Figure 67, the output difference amplifier is set to unity gain with all four resistors equal in value. If the tolerance of the resistors used in the circuit is given as δ, the worst-case CMRR of the instrumentation amplifier is

$$CMRR_{MIN}=\frac{1}{2\delta} \tag{22}$$

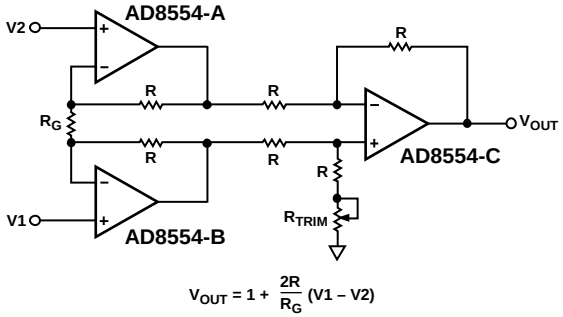


Figure 67. A Discrete Instrumentation Amplifier Configuration

Consequently, using 1% tolerance resistors results in a worst-case system CMRR of 0.02, or 34 dB. Therefore, either high precision resistors or an additional trimming resistor, as shown in Figure 67, must be used to achieve high common-mode rejection. The value of this trimming resistor must be equal to the value of R multiplied by its tolerance. For example, using 10 kΩ resistors with 1% tolerance requires a series trimming resistor equal to 100 Ω.

A HIGH ACCURACY THERMOCOUPLE AMPLIFIER

Figure 68 shows a K-type thermocouple amplifier configuration with cold junction compensation. Even from a 5 V supply, the AD8551 can provide enough accuracy to achieve a resolution of better than 0.02°C from 0°C to 500°C. D1 is used as a temperature measuring device to correct the cold junction error from the thermocouple and should be placed as close as possible to the two terminating junctions. With the thermocouple measuring tip immersed in a 0°C ice bath, R_6 should be adjusted until the output is at 0 V.

Using the values shown in Figure 68, the output voltage tracks temperature at 10 mV/°C. For a wider range of temperature measurement, R_9 can be decreased to 62 kΩ. This creates a 5 mV/°C change at the output, allowing measurements of up to 1000°C.

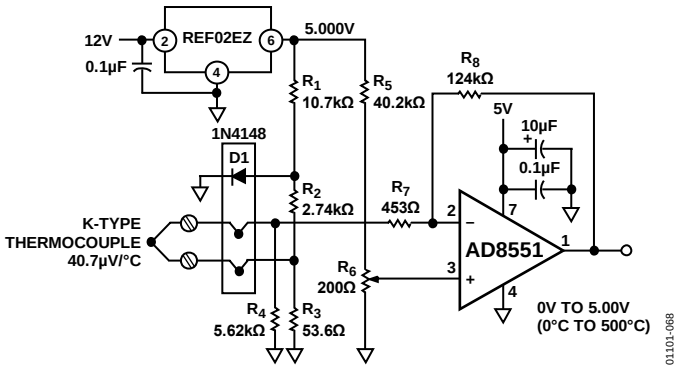


Figure 68. A Precision K-Type Thermocouple Amplifier with Cold Junction Compensation

PRECISION CURRENT METER

Because of its low input bias current and superb offset voltage at single supply voltages, the AD8551/AD8552/AD8554 are excellent amplifiers for precision current monitoring. Its rail-to-rail input allows the amplifier to be used as either a high-side or low-side current monitor. Using both amplifiers in the AD8552 provides a simple method to monitor both current supply and return paths for load or fault detection.

Figure 69 shows a high-side current monitor configuration. In this configuration, the input common-mode voltage of the amplifier is at or near the positive supply voltage. The rail-to-rail input of the amplifier provides a precise measurement even with the input common-mode voltage at the supply voltage. The CMOS input structure does not draw any input bias current, ensuring a minimum of measurement error.

The 0.1 Ω resistor creates a voltage drop to the noninverting input of the AD8551/AD8552/AD8554. The output of the amplifier is corrected until this voltage appears at the inverting input. This creates a current through R_1, which in turn flows through R_2. The monitor output is given by

$$Monitor\ Output = R_2 \times \left(\frac{R_{SENSE}}{R_1}\right) \times I_L \quad (23)$$

Using the components shown in Figure 69, the monitor output transfer function is 2.5 V/A.

Figure 70 shows the low-side monitor equivalent. In this circuit, the input common-mode voltage to the AD8552 is at or near ground. Again, a 0.1 Ω resistor provides a voltage drop proportional to the return current. The output voltage is given as

$$V_{OUT} = (V+) - \left(\frac{R_2}{R_1} \times R_{SENSE} \times I_L\right) \quad (24)$$

For the component values shown in Figure 70, the output transfer function decreases from V+ at −2.5 V/A.

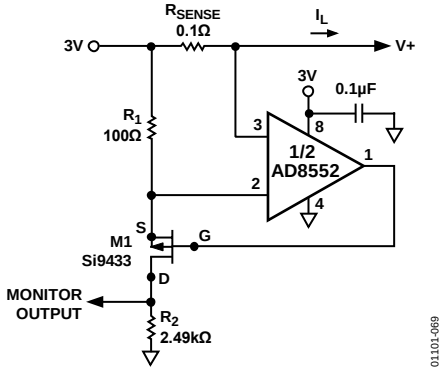


Figure 69. A High-Side Load Current Monitor

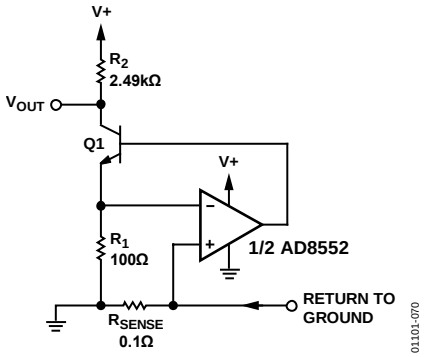
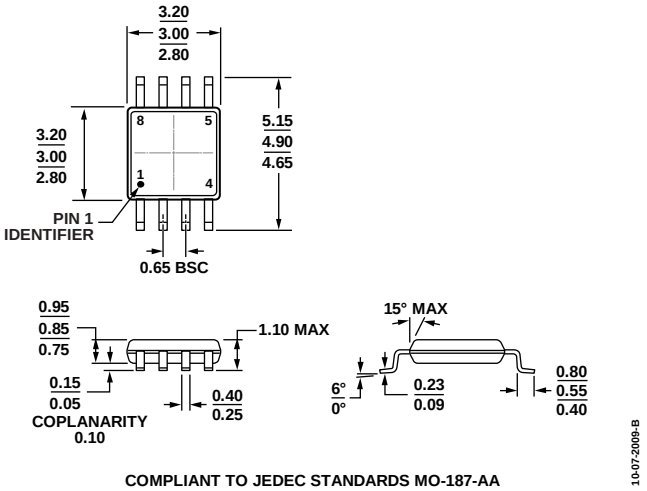


Figure 70. A Low-Side Load Current Monitor

PRECISION VOLTAGE COMPARATOR

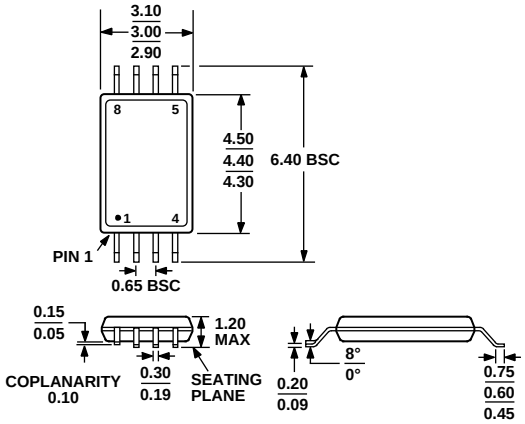
The AD8551/AD8552/AD8554 can be operated open-loop and used as a precision comparator. The AD8551/AD8552/AD8554 have less than 50 µV of offset voltage when run in this configuration. The slight increase of offset voltage stems from the fact that the autocorrection architecture operates with lowest offset in a closed-loop configuration, that is, one with negative feedback. With 50 mV of overdrive, the device has a propagation delay of 15 µs on the rising edge and 8 µs on the falling edge. Ensure the maximum differential voltage of the device is not exceeded. For more information, refer to the Input Overvoltage Protection section.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 71. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AA

Figure 72. 8-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-8)
Dimensions shown in millimeters

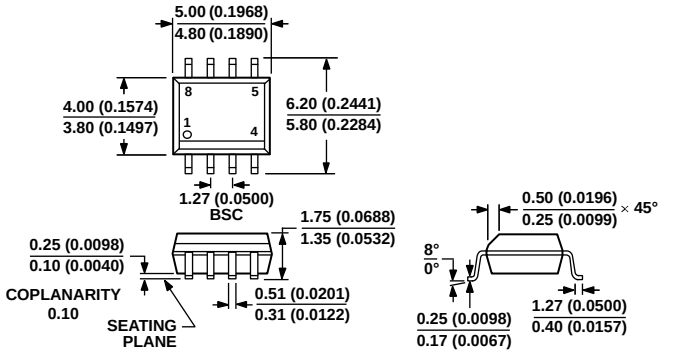
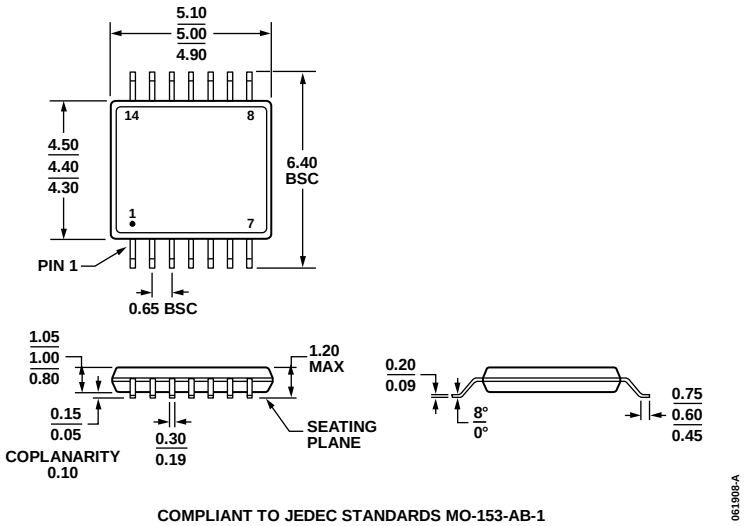
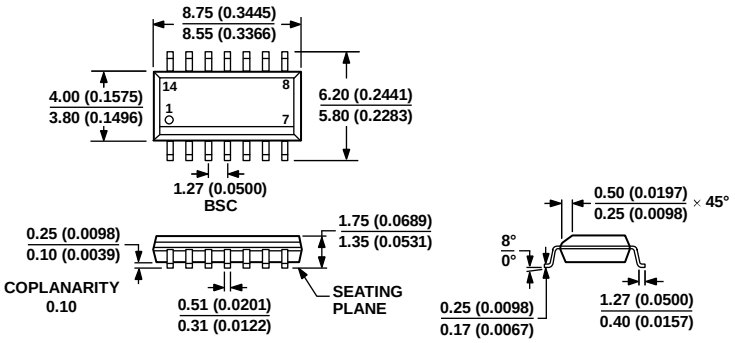


Figure 73. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 74. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 75. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8551ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8551ARZ-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8551ARZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8551ARM-REEL	−40°C to +125°C	8-Lead MSOP	RM-8	AHA
AD8551ARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	AHA#
AD8551ARMZ-REEL	−40°C to +125°C	8-Lead MSOP	RM-8	AHA#
AD8552AR	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8552AR-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8552AR-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8552ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8552ARZ-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8552ARZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8552ARU	−40°C to +125°C	8-Lead TSSOP	RU-8	
AD8552ARU-REEL	−40°C to +125°C	8-Lead TSSOP	RU-8	
AD8552ARUZ	−40°C to +125°C	8-Lead TSSOP	RU-8	
AD8552ARUZ-REEL	−40°C to +125°C	8-Lead TSSOP	RU-8	
AD8554ARZ	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8554ARZ-REEL	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8554ARZ-REEL7	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8554ARUZ	−40°C to +125°C	14-Lead TSSOP	RU-14	
AD8554ARUZ-REEL	−40°C to +125°C	14-Lead TSSOP	RU-14	

[1] Z = RoHS Compliant Part, # denotes RoHS compliant part may be top or bottom marked.

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