Precision Analog Front End and Controller for Battery Test/Formation Systems

Data Sheet **AD8450**

FEATURES

- Integrated constant current and voltage modes with automatic switchover
- Charge and discharge modes
- Precision voltage and current measurement
- Integrated precision control feedback blocks
- Precision interface to PWM or linear power converters
- Programmable gain settings
  - Current sense gains: 26, 66, 133, and 200
  - Voltage sense gains: 0.2, 0.27, 0.4, and 0.8
- Programmable OVP and OCP fault detection
- Current sharing and balancing
- Excellent ac and dc performance
- Maximum offset voltage drift: 0.6 µV/°C
- Maximum gain drift: 3 ppm/°C
- Low current sense amplifier input voltage noise: ≤9 nV/√Hz
- Current sense CMRR: 126 dB minimum (gain = 200)
- TTL compliant logic

APPLICATIONS

- Battery cell formation and testing
- Battery module testing

GENERAL DESCRIPTION

The AD8450 is a precision analog front end and controller for testing and monitoring battery cells. A precision programmable gain instrumentation amplifier (PGIA) measures the battery charge/discharge current, and a programmable gain difference amplifier (PGDA) measures the battery voltage (see Figure 1). Internal laser trimmed resistor networks set the gains for the PGIA and the PGDA, optimizing the performance of the AD8450 over the rated temperature range. PGIA gains are 26, 66, 133, and 200. PGDA gains are 0.2, 0.27, 0.4, and 0.8.

Voltages at the ISET and VSET inputs set the desired constant current (CC) and constant voltage (CV) values. CC to CV switching is automatic and transparent to the system.

A TTL logic level input, MODE, selects the charge or discharge mode (high for charge, low for discharge). An analog output, VCTRL, interfaces directly with the Analog Devices, Inc., ADP1972 PWM controller.

The AD8450 includes resistor programmable overvoltage and overcurrent detection and current sharing circuitry. Current sharing is used to balance the output current of multiple bridged channels.

The AD8450 simplifies designs by providing excellent accuracy, performance over temperature, flexibility with functionality, and overall reliability in a space-saving package. The AD8450 is available in an 80-lead, 14 mm × 14 mm × 1 mm LQFP package and is rated for an operating temperature of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

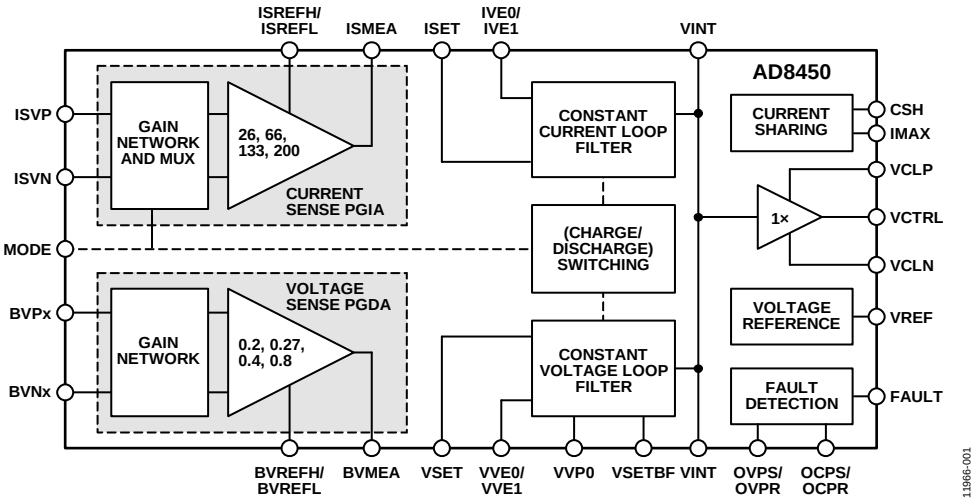

Figure 1.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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SPECIFICATIONS

AVCC = +25 V, AVEE = −5 V; AVCC = +15 V, AVEE = −15 V; DVCC = +5 V; PGIA gain = 26, 66, 133, or 200; PGDA gain = 0.2, 0.27, 0.4, or 0.8; T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT SENSE PGIA					
Internal Fixed Gains			26, 66, 133, 200		V/V
Gain Error	V_{ISMEA} = ±10 V			±0.1	%
Gain Drift	$T_A = T_{MIN}$ to T_{MAX}			3	ppm/°C
Gain Nonlinearity	V_{ISMEA} = ±10 V, R_L = 2 kΩ			3	ppm
Offset Voltage (RTI)	Gain = 200, ISREFH and ISREFL pins grounded	−110		+110	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.6	µV/°C
Input Bias Current			15	30	nA
Temperature Coefficient	$T_A = T_{MIN}$ to T_{MAX}			150	pA/°C
Input Offset Current				2	nA
Temperature Coefficient	$T_A = T_{MIN}$ to T_{MAX}			10	pA/°C
Input Common-Mode Voltage Range	$V_{ISVP} - V_{ISVN}$ = 0 V	AVEE + 2.3		AVCC − 2.4	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 2.6		AVCC − 2.6	V
Overvoltage Input Range		AVCC − 55		AVEE + 55	V
Differential Input Impedance			150		GΩ
Input Common-Mode Impedance			150		GΩ
Output Voltage Swing		AVEE + 1.5		AVCC − 1.2	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.4	V
Capacitive Load Drive				1000	pF
Short-Circuit Current			40		mA
Reference Input Voltage Range	ISREFH and ISREFL pins tied together	AVEE		AVCC	V
Reference Input Bias Current	$V_{ISVP} = V_{ISVN}$ = 0 V		5		µA
Output Voltage Level Shift	ISREFL pin grounded				
Maximum	ISREFH pin connected to VREF pin	17	20	23	mV
Scale Factor	V_{ISMEA}/V_{ISREFH}	6.8	8	9.2	mV/V
CMRR	ΔV_{CM} = 20 V				
Gain = 26		108			dB
Gain = 66		116			dB
Gain = 133		122			dB
Gain = 200		126			dB
Temperature Coefficient	$T_A = T_{MIN}$ to T_{MAX}			0.01	µV/V/°C
PSRR	ΔV_S = 20 V				
Gain = 26		108	122		dB
Gain = 66		116	130		dB
Gain = 133		122	136		dB
Gain = 200		126	140		dB
Voltage Noise	f = 1 kHz				
Gain = 26			9		nV/√Hz
Gain = 66			8		nV/√Hz
Gain = 133			7		nV/√Hz
Gain = 200			7		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz, all fixed gains		0.2		µV p-p
Current Noise	f = 1 kHz		80		fA/√Hz
Current Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		5		pA p-p

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Small Signal −3 dB Bandwidth					
Gain = 26			1.5		MHz
Gain = 66			630		kHz
Gain = 133			330		kHz
Gain = 200			220		kHz
Slew Rate	ΔV_{ISMEA} = 10 V		5		V/µs
VOLTAGE SENSE PGDA					
Internal Fixed Gains			0.2, 0.27, 0.4, 0.8		V/V
Gain Error	V_{IN} = ±10 V			±0.1	%
Gain Drift	$T_A = T_{MIN}$ to T_{MAX}			3	ppm/°C
Gain Nonlinearity	V_{BVMEA} = ±10 V, R_L = 2 kΩ			3	ppm
Offset Voltage (RTO)	BVREFH and BVREFL pins grounded			500	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			4	µV/°C
Differential Input Voltage Range	Gain = 0.8, V_{BVN0} = 0 V, V_{BVREFL} = 0 V				
	AVCC = +15 V, AVEE = −15 V	−16		+16	V
	AVCC = +25 V, AVEE = −5 V	−4		+29	V
Input Common-Mode Voltage Range	Gain = 0.8, V_{BVMEA} = 0 V				
	AVCC = +15 V, AVEE = −15 V	−27		+27	V
	AVCC = +25 V, AVEE = −5 V	−7		+50	V
Differential Input Impedance					
Gain = 0.2			800		kΩ
Gain = 0.27			600		kΩ
Gain = 0.4			400		kΩ
Gain = 0.8			200		kΩ
Input Common-Mode Impedance					
Gain = 0.2			240		kΩ
Gain = 0.27			190		kΩ
Gain = 0.4			140		kΩ
Gain = 0.8			90		kΩ
Output Voltage Swing		AVEE + 1.5		AVCC − 1.5	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.7	V
Capacitive Load Drive				1000	pF
Short-Circuit Current			30		mA
Reference Input Voltage Range	BVREFH and BVREFL pins tied together	AVEE		AVCC	V
Output Voltage Level Shift	BVREFL pin grounded				
Maximum	BVREFH pin connected to VREF pin	4.5	5	5.5	mV
Scale Factor	V_{BVMEA}/V_{BVREFH}	1.8	2	2.2	mV/V
CMRR	ΔV_{CM} = 10 V, all fixed gains, RTO	80			dB
Temperature Coefficient	$T_A = T_{MIN}$ to T_{MAX}			0.05	µV/V/°C
PSRR	ΔV_S = 20 V, all fixed gains, RTO	100			dB
Output Voltage Noise	f = 1 kHz, RTI				
Gain = 0.2			325		nV/√Hz
Gain = 0.27			250		nV/√Hz
Gain = 0.4			180		nV/√Hz
Gain = 0.8			105		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz, RTI				
Gain = 0.2			6		µV p-p
Gain = 0.27			5		µV p-p
Gain = 0.4			3		µV p-p
Gain = 0.8			2		µV p-p

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Small Signal −3 dB Bandwidth					
Gain = 0.2			420		kHz
Gain = 0.27			730		kHz
Gain = 0.4			940		kHz
Gain = 0.8			1000		kHz
Slew Rate			0.8		V/µs
CONSTANT CURRENT AND CONSTANT VOLTAGE LOOP FILTER AMPLIFIERS					
Offset Voltage				150	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.6	µV/°C
Input Bias Current		−5		+5	nA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	−5		+5	nA
Input Common-Mode Voltage Range		AVEE + 1.5		AVCC − 1.8	V
Output Voltage Swing	V_{VCLN} = AVEE + 1 V, V_{VCLP} = AVCC − 1 V	AVEE + 1.5		AVCC − 1	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1	V
Closed-Loop Output Impedance			0.01		Ω
Capacitive Load Drive				1000	pF
Source Short-Circuit Current			1		mA
Sink Short-Circuit Current			40		mA
Open-Loop Gain			140		dB
CMRR	ΔV_{CM} = 10 V			100	dB
PSRR	ΔV_S = 20 V			100	dB
Voltage Noise	f = 1 kHz		10		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		0.3		µV p-p
Current Noise	f = 1 kHz		80		fA/√Hz
Current Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		5		pA p-p
Small Signal Gain Bandwidth Product			3		MHz
Slew Rate	ΔV_{VINT} = 10 V		1		V/µs
CC to CV Transition Time			1.5		µs
UNCOMMITTED OP AMP					
Offset Voltage				150	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.6	µV/°C
Input Bias Current		−5		+5	nA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	−5		+5	nA
Input Common-Mode Voltage Range		AVEE + 1.5		AVCC − 1.8	V
Output Voltage Swing		AVEE + 1.5		AVCC − 1.5	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.5	V
Closed-Loop Output Impedance			0.01		Ω
Capacitive Load Drive				1000	pF
Short-Circuit Current			40		mA
Open-Loop Gain	R_L = 2 kΩ		140		dB
CMRR	ΔV_{CM} = 10 V			100	dB
PSRR	ΔV_S = 20 V			100	dB
Voltage Noise	f = 1 kHz		10		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		0.3		µV p-p
Current Noise	f = 1 kHz		80		fA/√Hz
Current Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		5		pA p-p
Small Signal Gain Bandwidth Product			3		MHz
Slew Rate	ΔV_{OAVO} = 10 V		1		V/µs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT SHARING BUS AMPLIFIER					
Nominal Gain			1		V/V
Offset Voltage				150	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.6	µV/°C
Output Voltage Swing		AVEE + 1.5		AVCC − 1.5	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.7	V
Capacitive Load Drive				1000	pF
Source Short-Circuit Current			40		mA
Sink Short-Circuit Current			0.5		mA
CMRR	ΔV_{CM} = 10 V			100	dB
PSRR	ΔV_S = 20 V			100	dB
Voltage Noise	f = 1 kHz		10		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		0.4		µV p-p
Small Signal −3 dB Bandwidth			3		MHz
Slew Rate	ΔV_{CS} = 10 V		1		V/µs
Transition Time			1.5		µs
CURRENT SHARING, VINT, AND CONSTANT VOLTAGE BUFFERS					
Nominal Gain			1		V/V
Offset Voltage				150	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.6	µV/°C
Input Bias Current	CV buffer only	−5		+5	nA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	−5		+5	nA
Input Voltage Range		AVEE + 1.5		AVCC − 1.8	V
Output Voltage Swing					
Current Sharing and Constant Voltage Buffers		AVEE + 1.5		AVCC − 1.5	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.5	V
VINT Buffer		V_{VCLN} − 0.6		V_{VCLP} + 0.6	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	V_{VCLN} − 0.6		V_{VCLP} + 0.6	V
Output Clamps Voltage Range	VINT buffer only				
VCLP Pin		V_{VCLN}		AVCC − 1	V
VCLN Pin		AVEE + 1		V_{VCLP}	V
Closed-Loop Output Impedance			1		Ω
Capacitive Load Drive				1000	pF
Short-Circuit Current			40		mA
PSRR	ΔV_S = 20 V			100	dB
Voltage Noise	f = 1 kHz		10		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		0.3		µV p-p
Current Noise	f = 1 kHz, CV buffer only		80		fA/√Hz
Current Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		5		pA p-p
Small Signal −3 dB Bandwidth			3		MHz
Slew Rate	ΔV_{OUT} = 10 V		1		V/µs
OVERCURRENT AND OVERVOLTAGE FAULT COMPARATORS					
High Threshold Voltage	With respect to OVPR and OCPR pins		30	45	mV
Temperature Coefficient			100		µV/°C
Low Threshold Voltage	With respect to OVPR and OCPR pins	−45	−30		mV
Temperature Coefficient			−100		µV/°C
Input Bias Current			250		nA
Input Voltage Range	OVPR, OCPR, OVPS, and OCPS pins	AVEE		AVCC − 3	V
Differential Input Voltage Range		−7		+7	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Fault Output Logic Levels	FAULT pin (Pin 46)				
Output Voltage High, V_{OH}	I_{LOAD} = 200 µA	4.5			V
Output Voltage Low, V_{OL}	I_{LOAD} = 200 µA			0.5	V
Propagation Delay	C_{LOAD} = 10 pF		500		ns
Fault Rise Time	C_{LOAD} = 10 pF		150		ns
Fault Fall Time	C_{LOAD} = 10 pF		150		ns
VOLTAGE REFERENCE					
Nominal Output Voltage	With respect to AGND		2.5		V
Output Voltage Error				±1	%
Temperature Drift	$T_A = T_{MIN}$ to T_{MAX}			10	ppm/°C
Line Regulation	ΔV_S = 10 V			40	ppm/V
Load Regulation	ΔI_{VREF} = 1 mA (source only)			400	ppm/mA
Output Current, Sourcing				10	mA
Voltage Noise	f = 1 kHz		100		nV/√Hz
Voltage Noise, Peak-to-Peak	f = 0.1 Hz to 10 Hz		5		µV p-p
DIGITAL INTERFACE, MODE INPUT	MODE pin (Pin 39)				
Input Voltage High, V_{IH}	With respect to DGND	2.0		DVCC	V
Input Voltage Low, V_{IL}	With respect to DGND	DGND		0.8	V
Mode Switching Time			500		ns
POWER SUPPLY					
Operating Voltage Range					
AVCC		5		36	V
AVEE		−31		0	V
Analog Supply Range	AVCC − AVEE	5		36	V
DVCC		3		5	V
Quiescent Current					
AVCC			7	10	mA
AVEE			6.5	10	mA
DVCC			40	70	µA
TEMPERATURE RANGE					
For Specified Performance		−40		+85	°C
Operational		−55		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Analog Supply Voltage (AVCC − AVEE)	36 V
Digital Supply Voltage (DVCC − DGND)	36 V
Maximum Voltage at Input Pins (ISVP, ISVN, BVPx, and BVNx)	AVEE + 55 V
Minimum Voltage at Input Pins (ISVP, ISVN, BVPx, and BVNx)	AVCC − 55 V
Maximum Voltage at All Input Pins, Except ISVP, ISVN, BVPx, and BVNx	AVCC
Minimum Voltage at All Input Pins, Except ISVP, ISVN, BVPx, and BVNx	AVEE
Maximum Digital Supply Voltage with Respect to the Positive Analog Supply (DVCC − AVCC)	+0.5 V
Minimum Digital Supply Voltage with Respect to the Negative Analog Supply (DVCC − AVEE)	−0.5 V
Maximum Digital Ground with Respect to the Positive Analog Supply (DGND − AVCC)	+0.5 V
Minimum Digital Ground with Respect to the Negative Analog Supply (DGND − AVEE)	−0.5 V
Maximum Analog Ground with Respect to the Positive Analog Supply (AGND − AVCC)	+0.5 V
Minimum Analog Ground with Respect to the Negative Analog Supply (AGND − AVEE)	−0.5 V
Maximum Analog Ground with Respect to the Digital Ground (AGND − DGND)	+0.5 V
Minimum Analog Ground with Respect to the Digital Ground (AGND − DGND)	−0.5 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The θ_{JA} value assumes a 4-layer JEDEC standard board with zero airflow.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
80-Lead LQFP	54.7	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

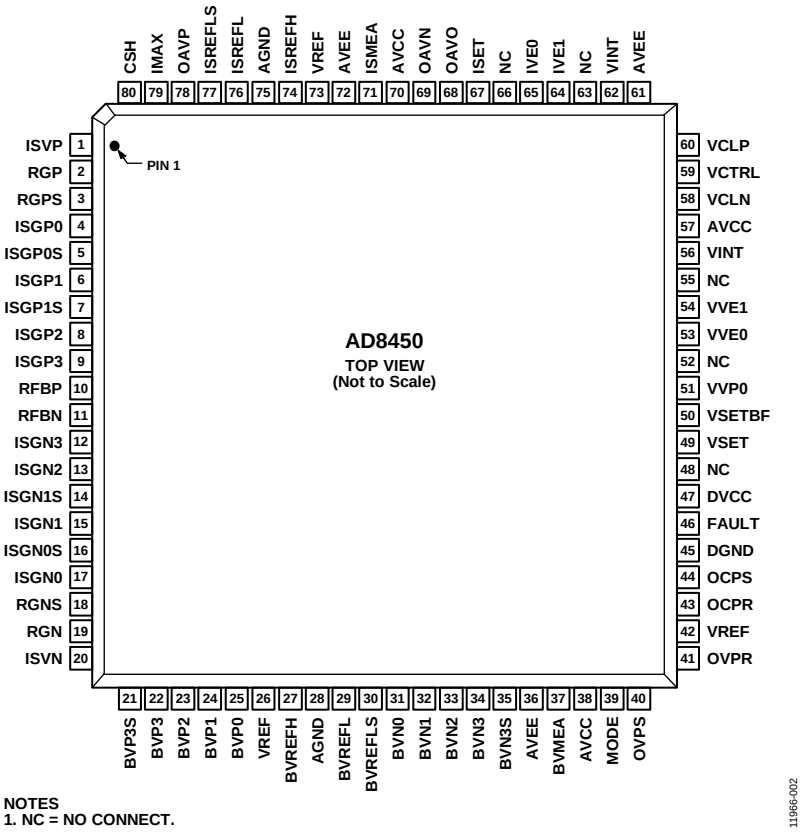

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output[1]	Description
1, 20	ISVP, ISVN	Input	Current Sense Instrumentation Amplifier Positive (Noninverting) and Negative (Inverting) Inputs. Connect these pins across the current sense shunt resistor.
2, 19	RGP, RGN	N/A	Current Sense Instrumentation Amplifier Gain Setting Pins. Connect these pins to the appropriate resistor network gain pins to select the current sense gain (see Table 5).
3, 18	RGPS, RGNS	N/A	Kelvin Sense Pins for the Current Sense Instrumentation Amplifier Gain Setting Pins (RGP and RGN).
4, 6, 8, 9, 12, 13, 15, 17	ISGP0, ISGP1, ISGP2, ISGP3, ISGN3, ISGN2, ISGN1, ISGN0	N/A	Current Sense Instrumentation Amplifier Resistor Network Gain Pins (see Table 5).
5, 7, 14, 16	ISGP0S, ISGP1S, ISGN1S, ISGN0S	N/A	Kelvin Sense Pins for the ISGP0, ISGP1, ISGN1, and ISGN0 Pins.
10, 11	RFBP, RFBN	Output	Current Sense Preamplifier Positive and Negative Outputs.
21, 35	BVP3S, BVN3S	N/A	Kelvin Sense Pins for the Voltage Sense Difference Amplifier Inputs BVP3 and BVN3.
22, 23, 24, 25, 31, 32, 33, 34	BVP3, BVP2, BVP1, BVP0, BVN0, BVN1, BVN2, BVN3	Input	Voltage Sense Difference Amplifier Inputs. Each input pair (BVPx and BVNx) corresponds to a different voltage sense gain (see Table 6).
26, 42, 73	VREF	Output	Voltage Reference Output Pins. VREF = 2.5 V.
27	BVREFH	Input	Reference Input for the Voltage Sense Difference Amplifier. To level shift the voltage sense difference amplifier output by approximately 5 mV, connect this pin to the VREF pin. Otherwise, connect this pin to the BVREFL pin.
28, 75	AGND	N/A	Analog Ground Pins.
29	BVREFL	Input	Reference Input for the Voltage Sense Difference Amplifier. The default connection is to ground.
30	BVREFLS	N/A	Kelvin Sense Pin for the BVREFL Pin.

Pin No.	Mnemonic	Input/ Output[1]	Description
36, 61, 72	AVEE	N/A	Analog Negative Supply Pins. The default voltage is −5 V.
38, 57, 70	AVCC	N/A	Analog Positive Supply Pins. The default voltage is +25 V.
37	BVMEA	Output	Voltage Sense Difference Amplifier Output.
39	MODE	Input	TTL-Compliant Logic Input to Select the Charge or Discharge Mode. Low = discharge, high = charge.
40	OVPS	Input	Noninverting Sense Input of the Overvoltage Protection Comparator.
41	OVPR	Input	Inverting Reference Input of the Overvoltage Protection Comparator. Typically, this pin connects to the 2.5 V reference voltage (VREF).
43	OCPR	Input	Inverting Reference Input of the Overcurrent Protection Sense Comparator. Typically, this pin connects to the 2.5 V reference voltage (VREF).
44	OCPS	Input	Noninverting Sense Input of the Overcurrent Protection Sense Comparator.
45	DGND	N/A	Digital Ground Pin.
46	FAULT	Output	Overvoltage or Overcurrent Fault Detection Logic Output (Active Low).
47	DVCC	N/A	Digital Supply. The default voltage is +5 V.
48, 52, 55, 63, 66	NC	N/A	No Connect. There are no internal connections to these pins.
49	VSET	Input	Target Voltage for the Voltage Sense Control Loop.
50	VSETBF	Output	Buffered Voltage VSET.
51	VVP0	Input	Noninverting Input of the Voltage Sense Integrator for Discharge Mode.
53	VVE0	Input	Inverting Input of the Voltage Sense Integrator for Discharge Mode.
54	VVE1	Input	Inverting Input of the Voltage Sense Integrator for Charge Mode.
56, 62	VINT	Output	Minimum Output of the Voltage Sense and Current Sense Integrator Amplifiers.
58	VCLN	Input	Low Clamp Voltage for VCTRL.
59	VCTRL	Output	Controller Output Voltage. Connect this pin to the input of the PWM controller (for example, the COMP pin of the ADP1972).
60	VCLP	Input	High Clamp Voltage for VCTRL.
64	IVE1	Input	Inverting Input of the Current Sense Integrator for Charge Mode.
65	IVE0	Input	Inverting Input of the Current Sense Integrator for Discharge Mode.
67	ISET	Input	Target Voltage for the Current Sense Control Loop.
68	OAVO	Output	Output of the Uncommitted Operational Amplifier.
69	OAVN	Input	Inverting Input of the Uncommitted Operational Amplifier.
71	ISMEA	Output	Current Sense Instrumentation Amplifier Output.
74	ISREFH	Input	Reference Input for the Current Sense Amplifier. To level shift the current sense instrumentation amplifier output by approximately 20 mV, connect this pin to the VREF pin. Otherwise, connect this pin to the ISREFL pin.
76	ISREFL	Input	Reference Input for the Current Sense Amplifier. The default connection is to ground.
77	ISREFLS	N/A	Kelvin Sense Pin for the ISREFL Pin.
78	OAVP	Input	Noninverting Input of the Uncommitted Operational Amplifier.
79	IMAX	Output	Maximum Voltage of All Voltages Applied to the Current Sharing (CSH) Pin.
80	CSH	N/A	Current Sharing Bus.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, AVCC = +25 V, AVEE = −5 V, R_L = ∞, unless otherwise noted.

PGIA CHARACTERISTICS

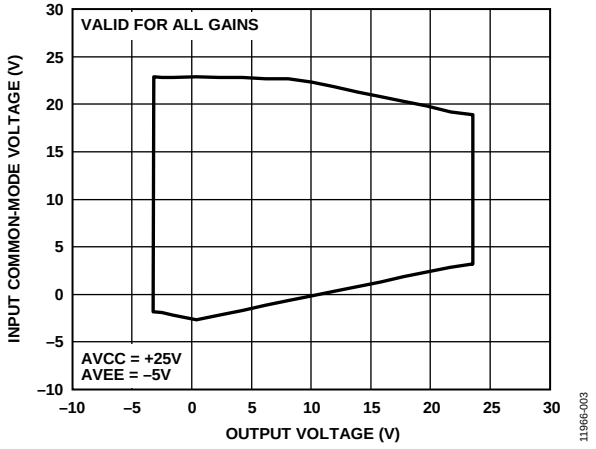

Figure 3. Input Common-Mode Voltage vs. Output Voltage for AVCC = +25 V and AVEE = −5 V

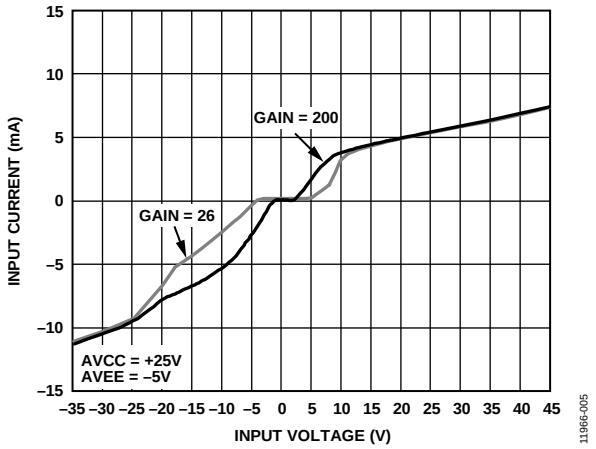

Figure 4. Input Overvoltage Performance for AVCC = +25 V and AVEE = −5 V

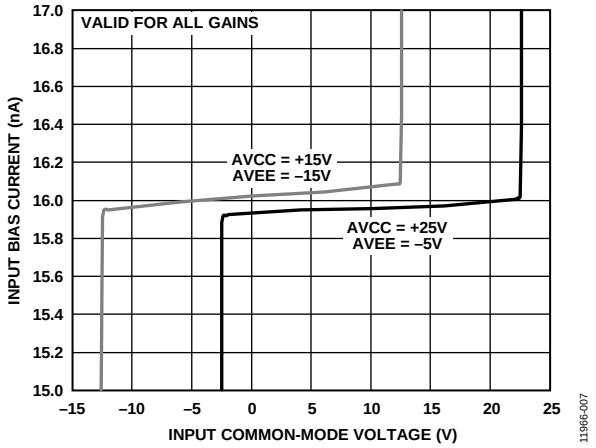

Figure 5. Input Bias Current vs. Input Common-Mode Voltage

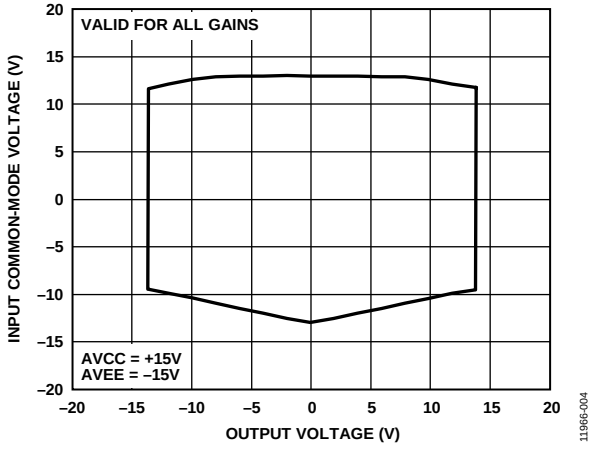

Figure 6. Input Common-Mode Voltage vs. Output Voltage for AVCC = +15 V and AVEE = −15 V

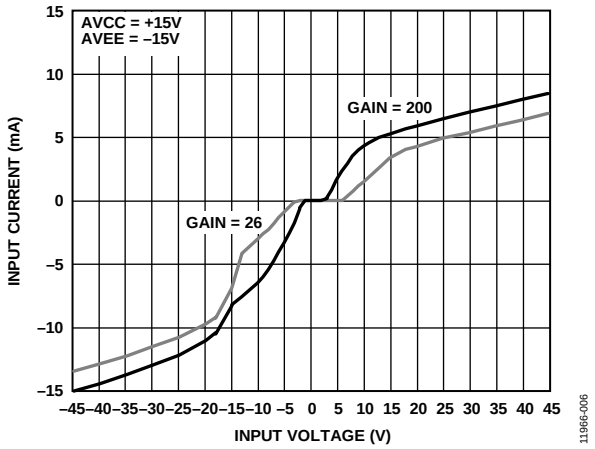

Figure 7. Input Overvoltage Performance for AVCC = +15 V and AVEE = −15 V

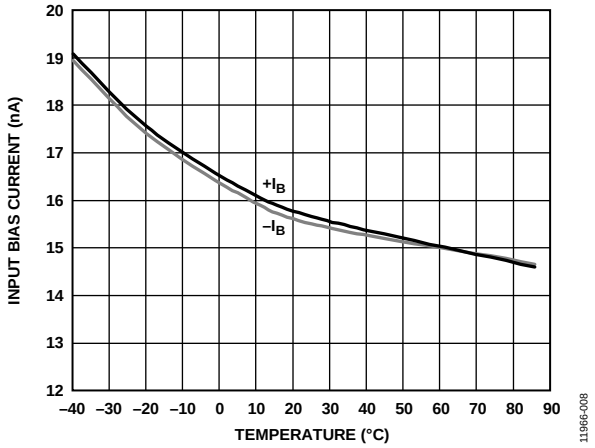

Figure 8. Input Bias Current vs. Temperature

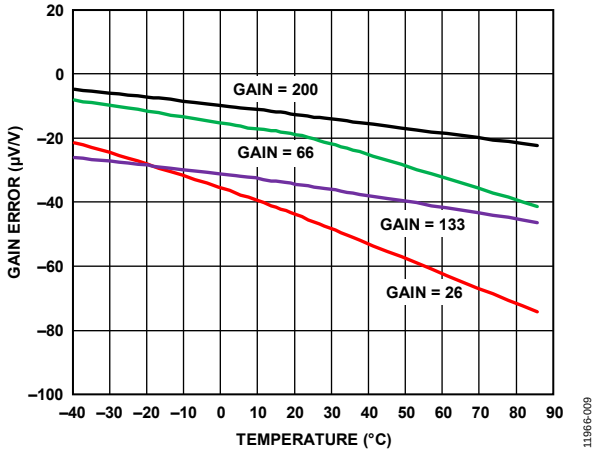

Figure 9. Gain Error vs. Temperature

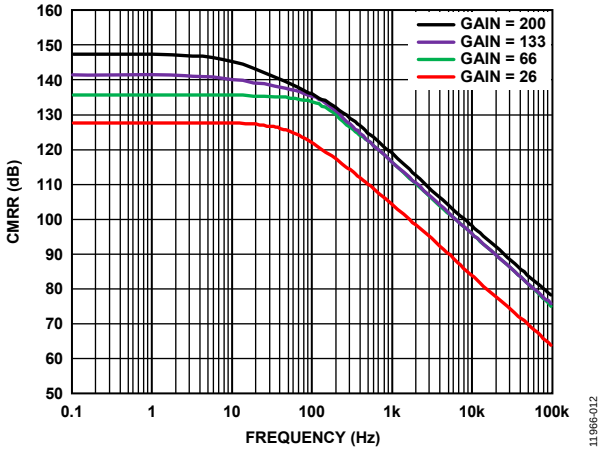

Figure 12. CMRR vs. Frequency

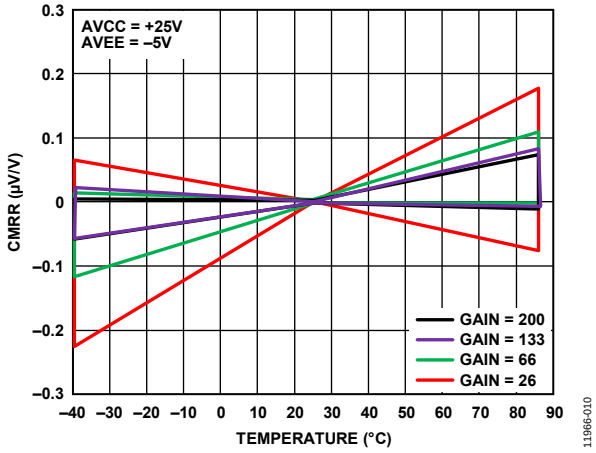

Figure 10. Normalized CMRR vs. Temperature

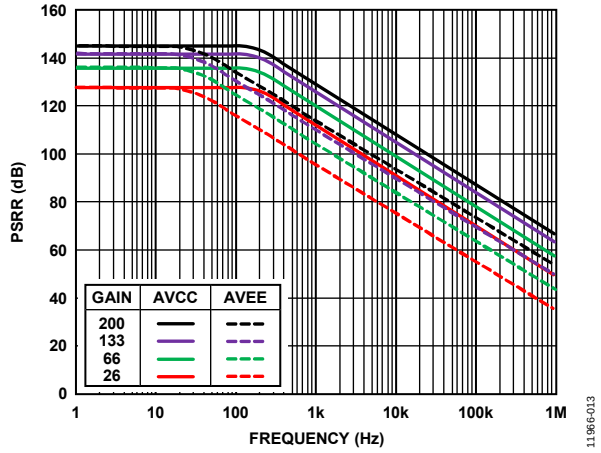

Figure 13. PSRR vs. Frequency

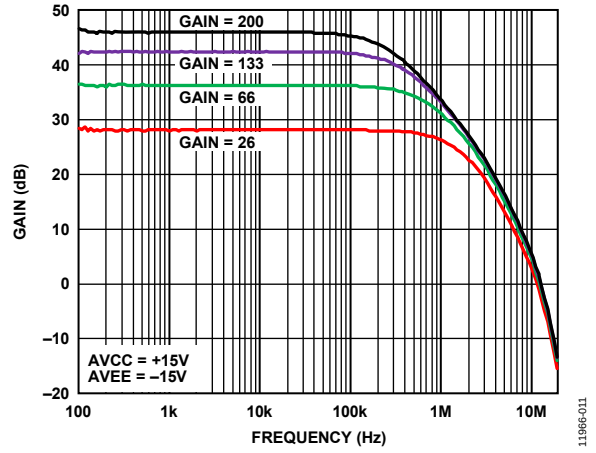

Figure 11. Gain vs. Frequency

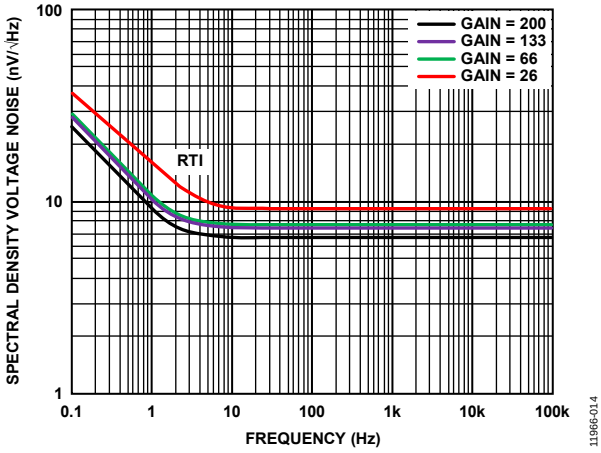

Figure 14. Spectral Density Voltage Noise, RTI vs. Frequency

PGDA CHARACTERISTICS

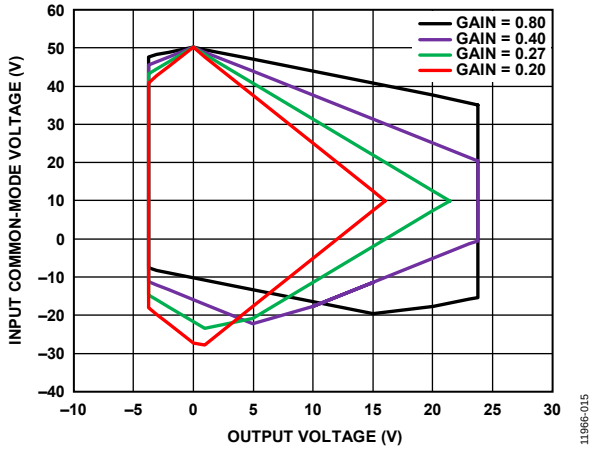

Figure 15. Input Common-Mode Voltage vs. Output Voltage for AVCC = +25 V and AVEE = −5 V

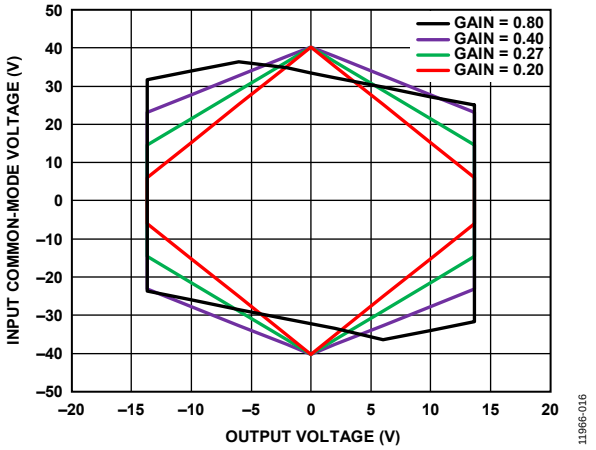

Figure 18. Input Common-Mode Voltage vs. Output Voltage for AVCC = +15 V and AVEE = −15 V

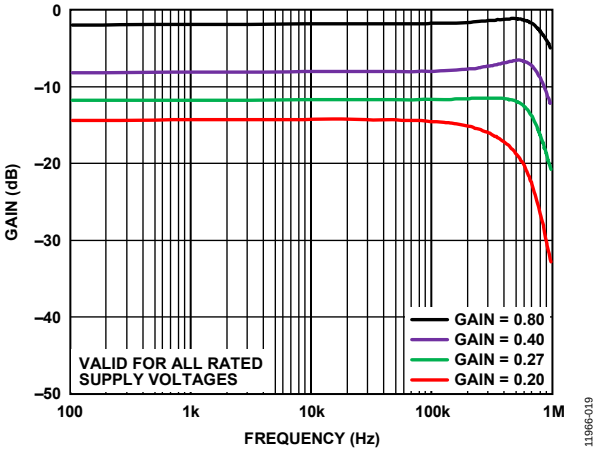

Figure 16. Gain vs. Frequency

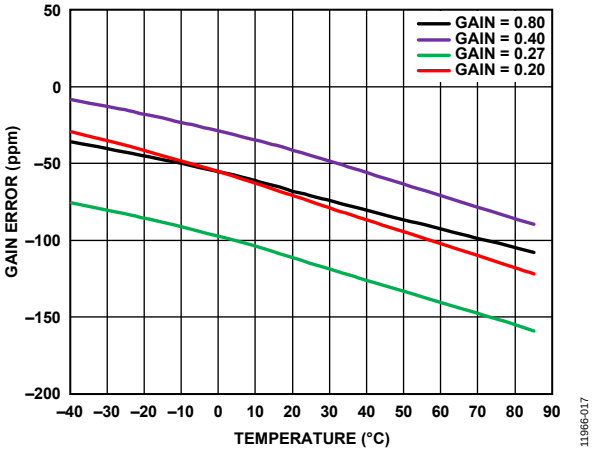

Figure 19. Gain Error vs. Temperature

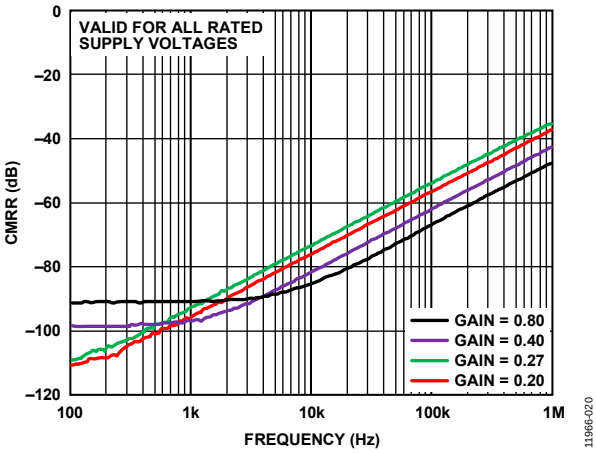

Figure 17. CMRR vs. Frequency

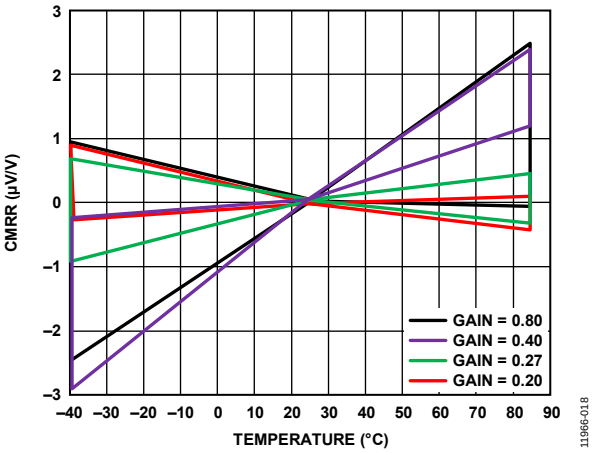

Figure 20. Normalized CMRR vs. Temperature

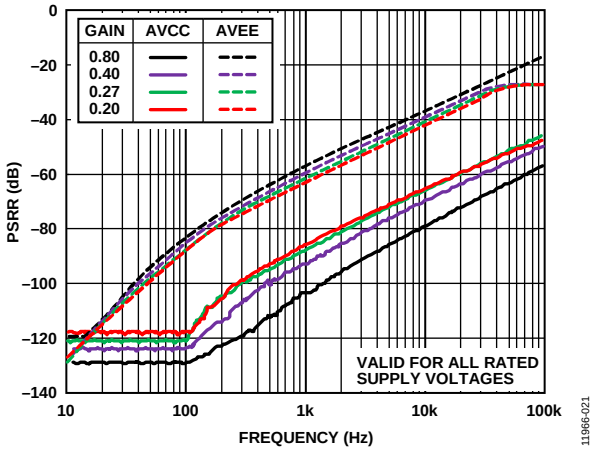

Figure 21. PSRR vs. Frequency

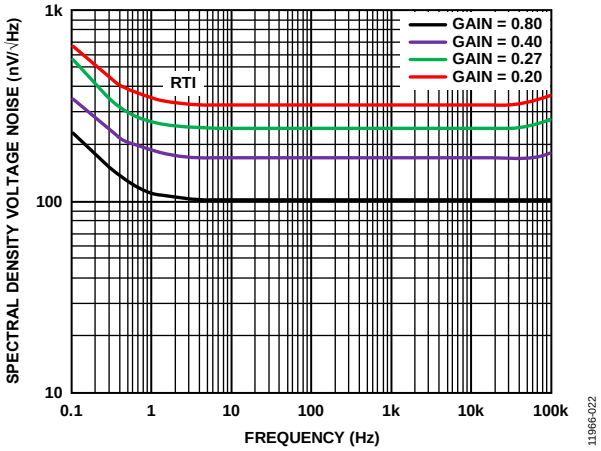

Figure 22. Spectral Density Voltage Noise, RTI vs. Frequency

CC AND CV LOOP FILTER AMPLIFIERS, UNCOMMITTED OP AMP, AND VSET BUFFER

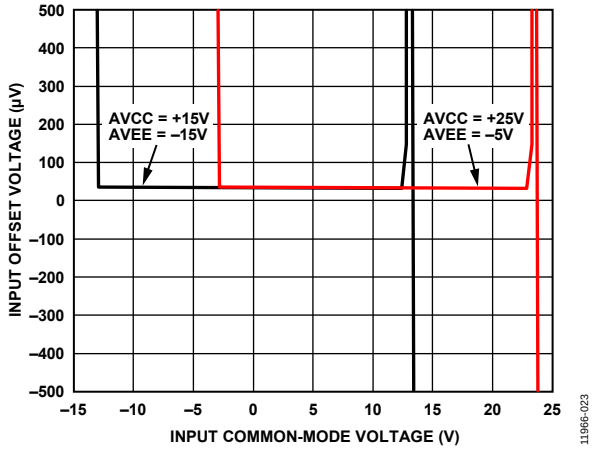

Figure 23. Input Offset Voltage vs. Input Common-Mode Voltage for Two Supply Voltage Combinations

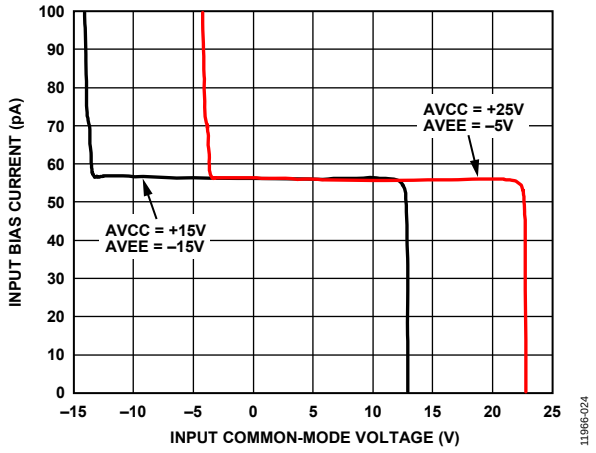

Figure 24. Input Bias Current vs. Input Common-Mode Voltage for Two Supply Voltage Combinations

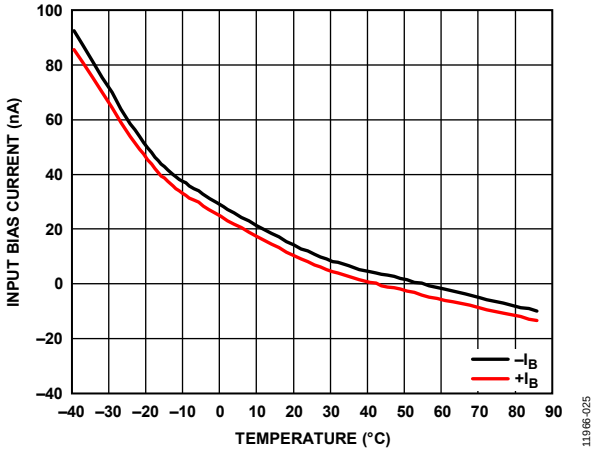

Figure 25. Input Bias Current vs. Temperature

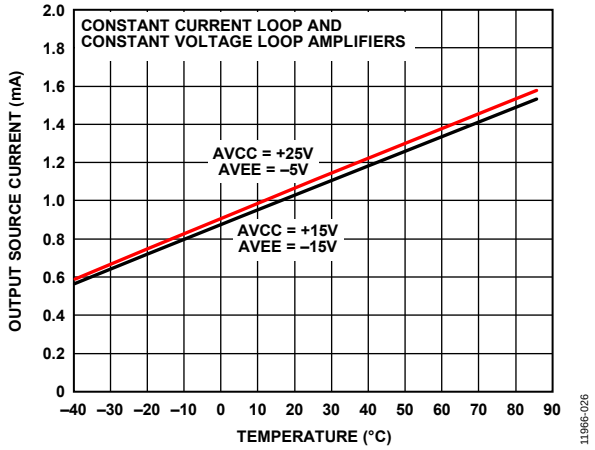

Figure 26. Output Source Current vs. Temperature for Two Supply Voltage Combinations

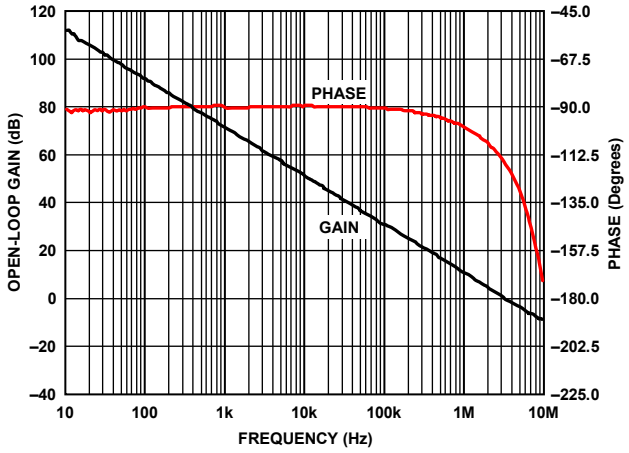

Figure 27. Open-Loop Gain and Phase vs. Frequency

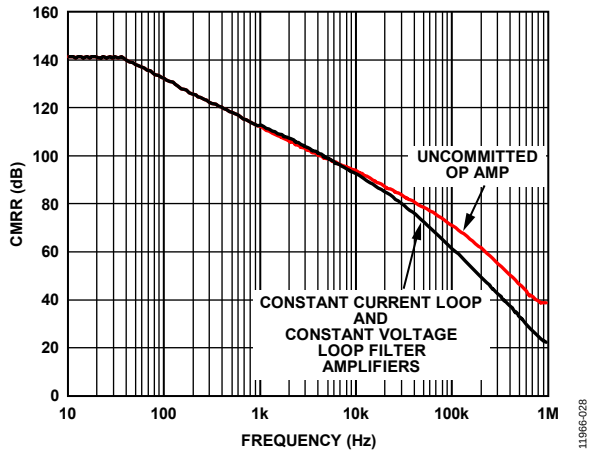

Figure 28. CMRR vs. Frequency

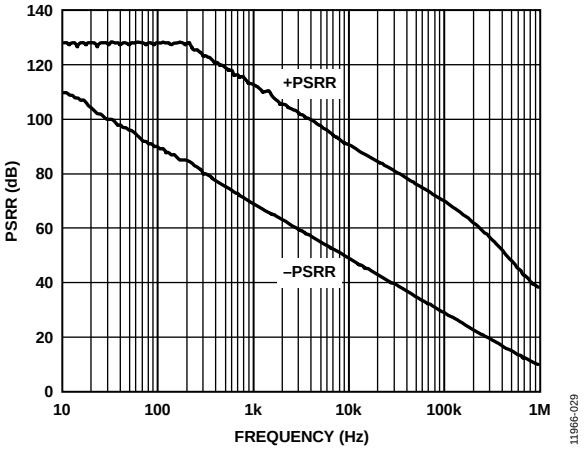

Figure 29. PSRR vs. Frequency

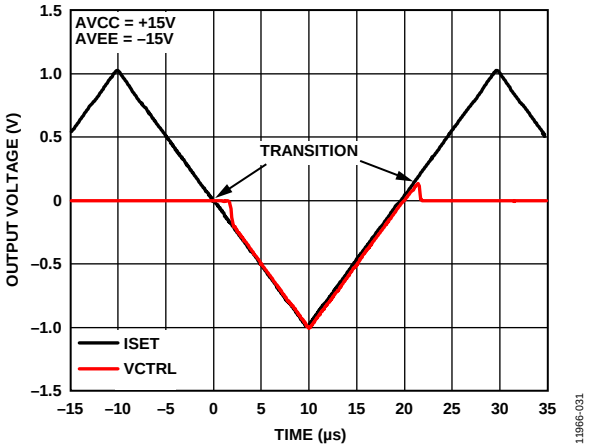

Figure 31. CC to CV Transition

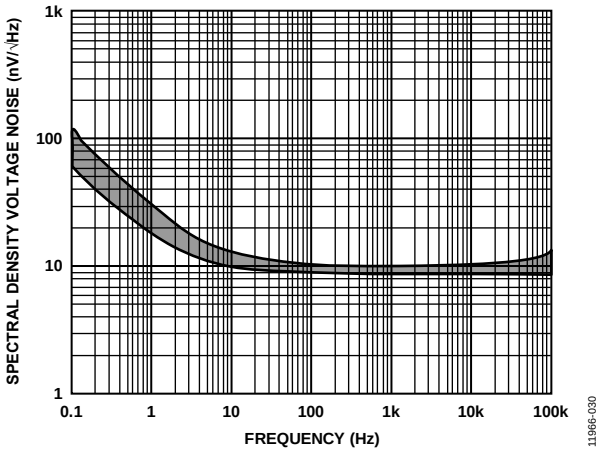

Figure 30. Range of Spectral Density Voltage Noise vs. Frequency for the Op Amps and Buffers

VINT BUFFER

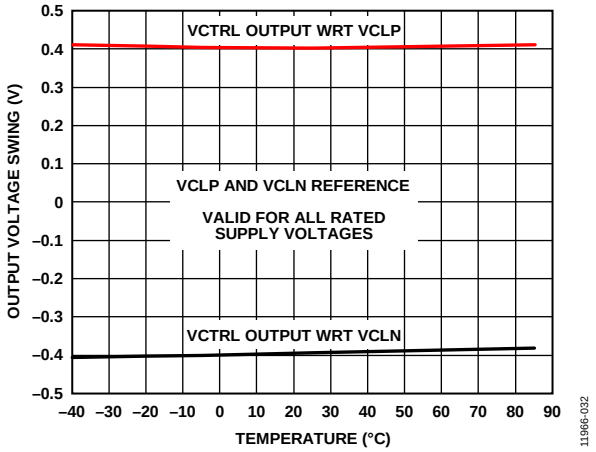

Figure 32. Output Voltage Swing with Respect to VCLP and VCLN vs. Temperature

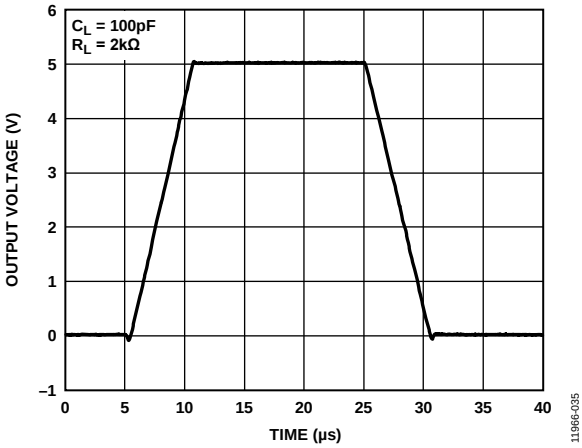

Figure 35. Large Signal Transient Response, R_L = 2 kΩ, C_L = 100 pF

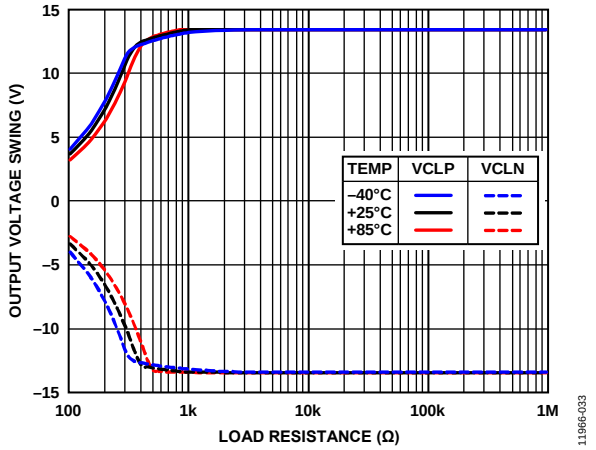

Figure 33. Output Voltage Swing vs. Load Resistance at Three Temperatures

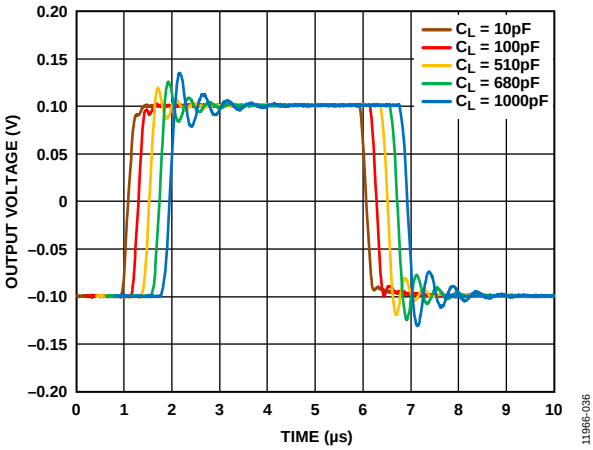

Figure 36. Small Signal Transient Response vs. Capacitive Load

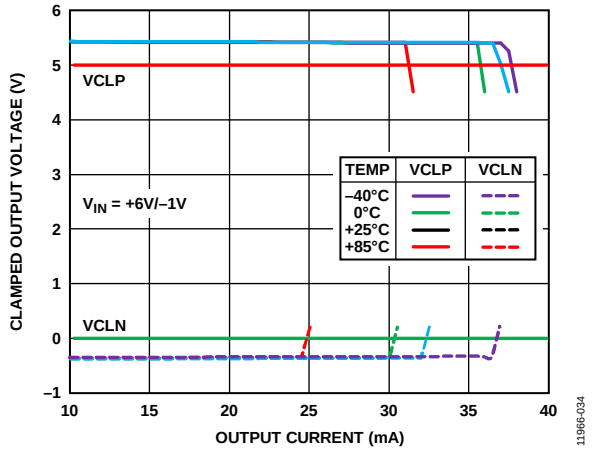

Figure 34. Clamped Output Voltage vs. Output Current at Four Temperatures

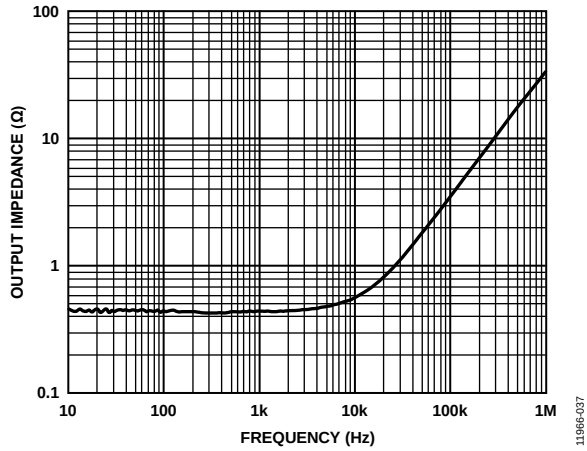

Figure 37. Output Impedance vs. Frequency

CURRENT SHARING AMPLIFIER

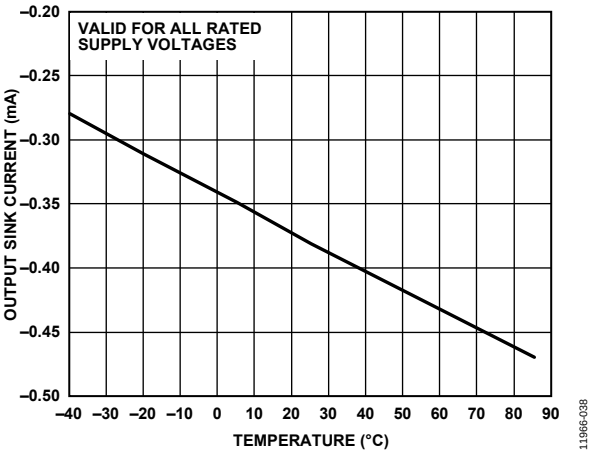

Figure 38. Output Sink Current vs. Temperature

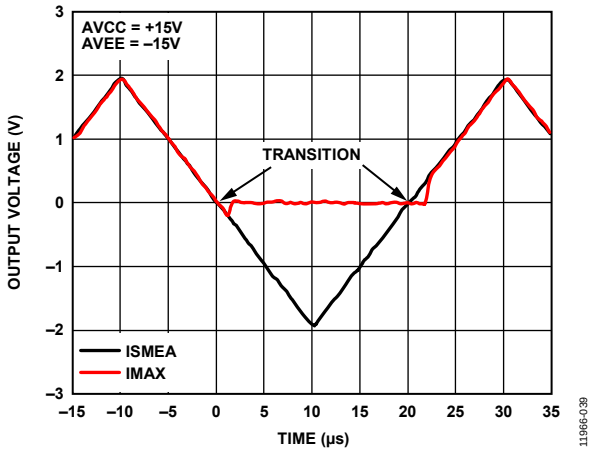

Figure 39. Current Sharing Bus Transition Characteristics

COMPARATORS

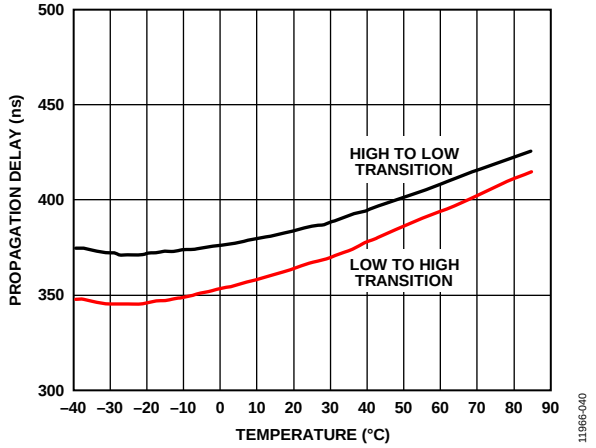

Figure 40. Propagation Delay vs. Temperature

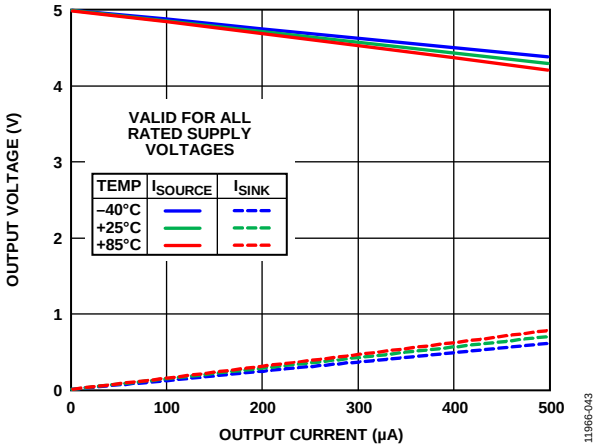

Figure 43. Output Voltage vs. Output Current at Three Temperatures

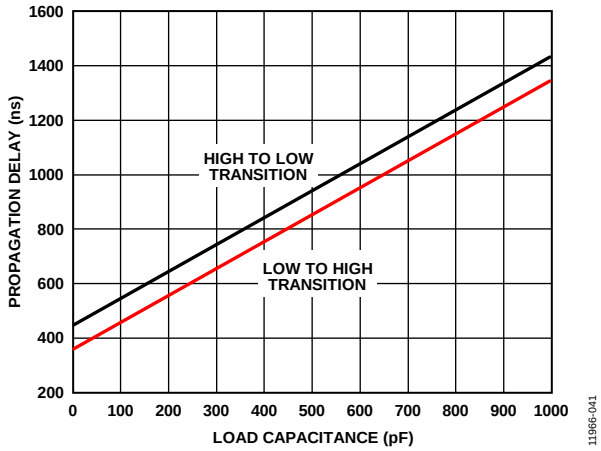

Figure 41. Propagation Delay vs. Load Capacitance

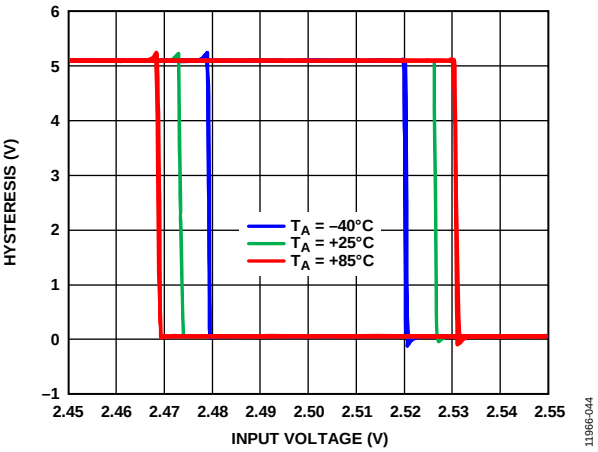

Figure 44. Comparator Transfer Function at Three Temperatures

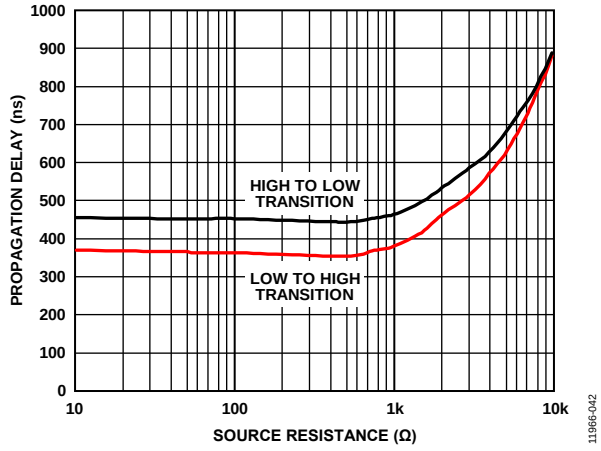

Figure 42. Propagation Delay vs. Source Resistance

REFERENCE CHARACTERISTICS

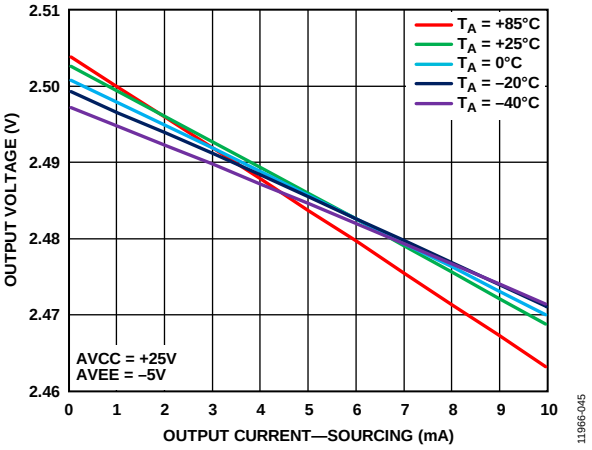

Figure 45. Output Voltage vs. Output Current (Sourcing) over Temperature

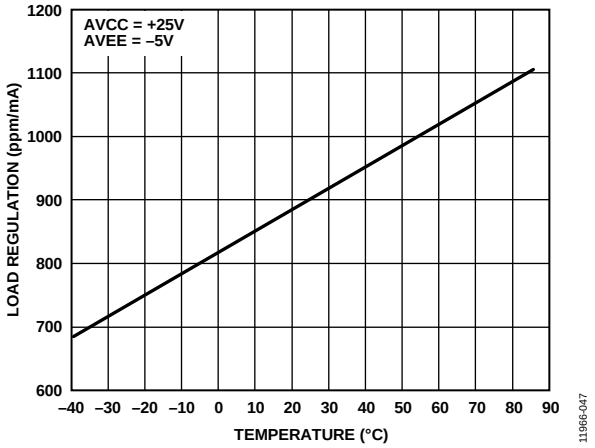

Figure 47. Source and Sink Load Regulation vs. Temperature

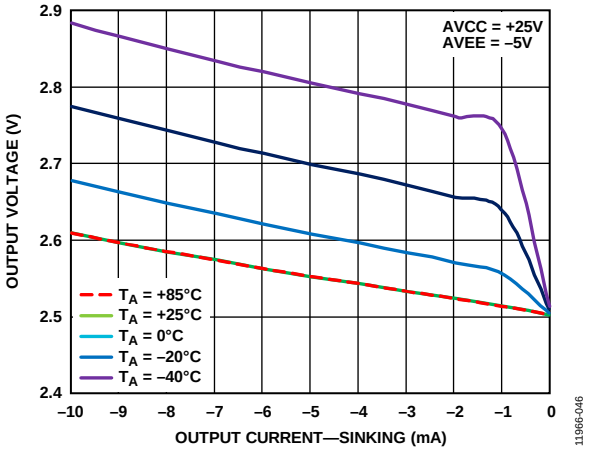

Figure 46. Output Voltage vs. Output Current (Sinking) over Temperature

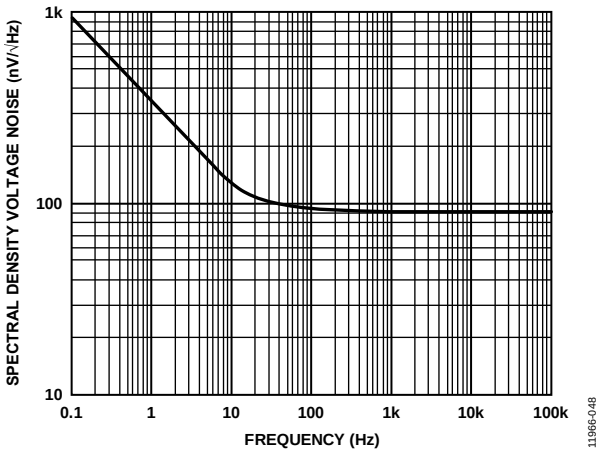

Figure 48. Spectral Density Voltage Noise vs. Frequency

THEORY OF OPERATION

INTRODUCTION

To form and test a battery, the battery must undergo charge and discharge cycles. During these cycles, the battery terminal current and voltage must be precisely controlled to prevent battery failure or a reduction in the capacity of the battery. Therefore, battery formation and test systems require a high precision analog front end to monitor the battery current and terminal voltage.

The analog front end of the AD8450 includes a precision current sense programmable gain instrumentation amplifier (PGIA) to measure the battery current, and a precision voltage sense programmable gain difference amplifier (PGDA) to measure the battery voltage. The gain programmability of the PGIA allows the system to set the battery charge/discharge current to any of four discrete values with the same shunt resistor. The gain programmability of the PGDA allows the system to handle up to four batteries in series (4S).

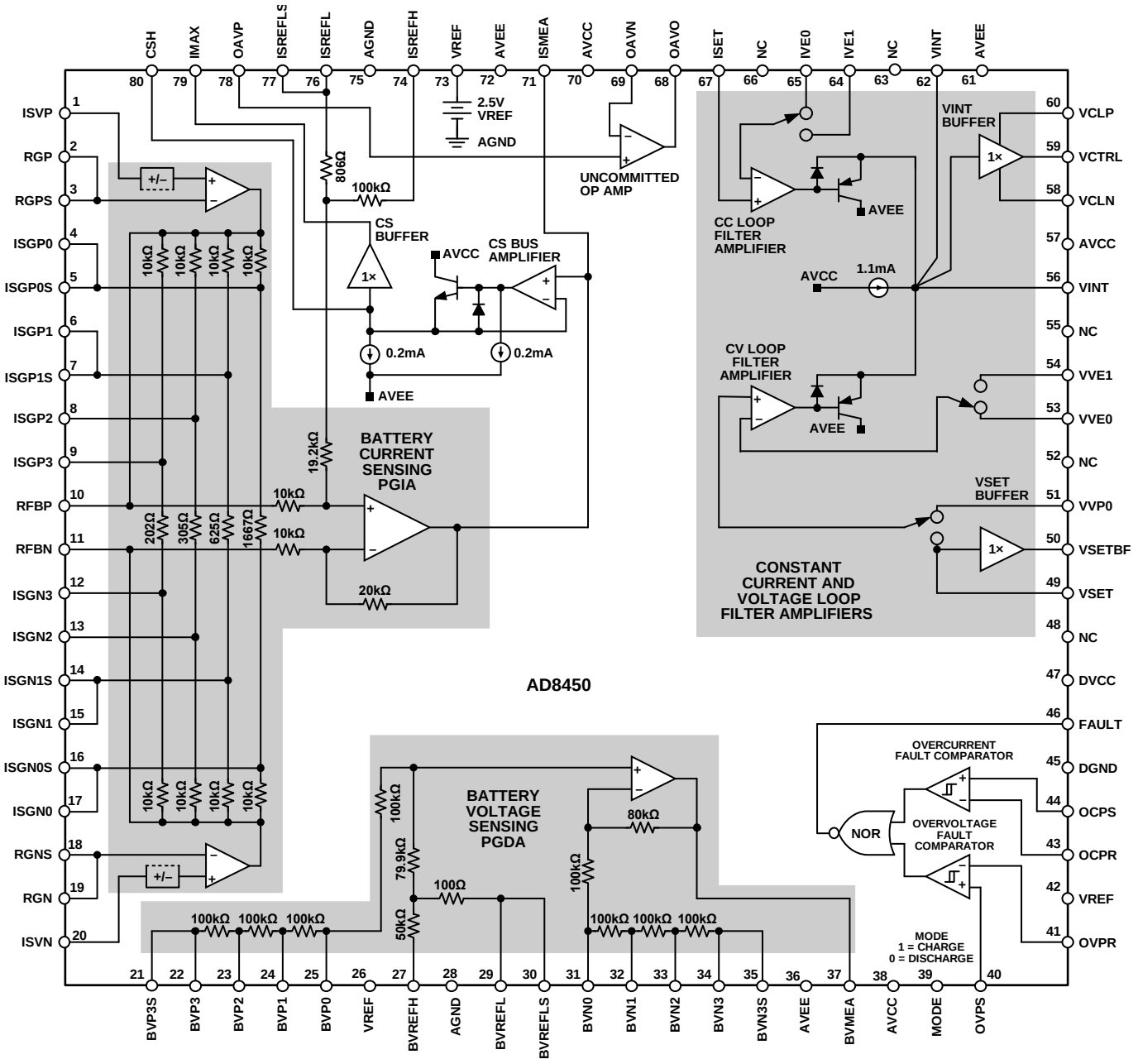

Figure 49. AD8450 Detailed Block Diagram

Battery formation and test systems charge and discharge batteries using a constant current/constant voltage (CC/CV) algorithm. In other words, the system first forces a set constant current in or out of the battery until the battery voltage reaches a target value. At this point, a set constant voltage is forced across the battery terminals.

The AD8450 provides two control loops—a constant current (CC) loop and a constant voltage (CV) loop—that transition automatically after the battery reaches the user defined target voltage. These loops are implemented via two precision specialty amplifiers with external feedback networks that set the transfer function of the CC and CV loops. Moreover, in the AD8450, these loops reconfigure themselves to charge or discharge the battery by toggling the MODE pin.

Battery formation and test systems must also be able to detect overvoltage and overcurrent conditions in the battery to prevent damage to the battery and/or the control system.

The AD8450 includes two comparators to detect overcurrent and overvoltage events. These comparators output a logic low at the FAULT pin when either comparator is tripped.

Battery formation and test systems used to condition high current battery cells often employ multiple independent channels to charge or discharge high currents to or from the battery. To maximize efficiency, these systems benefit from circuitry that enables precise current sharing (or balancing) among the channels—that is, circuitry that actively matches the output current of each channel. The AD8450 includes a specialty precision amplifier that detects the maximum output current among several channels by identifying the channel with the maximum voltage at its PGIA output. This maximum voltage can then be compared to all the PGIA output voltages to actively adjust the output current of each channel.

Figure 49 is a block diagram of the AD8450 that illustrates the distinct sections of the AD8450, including the PGIA and PGDA measurement blocks, the loop filter amplifiers, the fault comparators, and the current sharing circuitry. Figure 50 is a block diagram of a battery formation and test system.

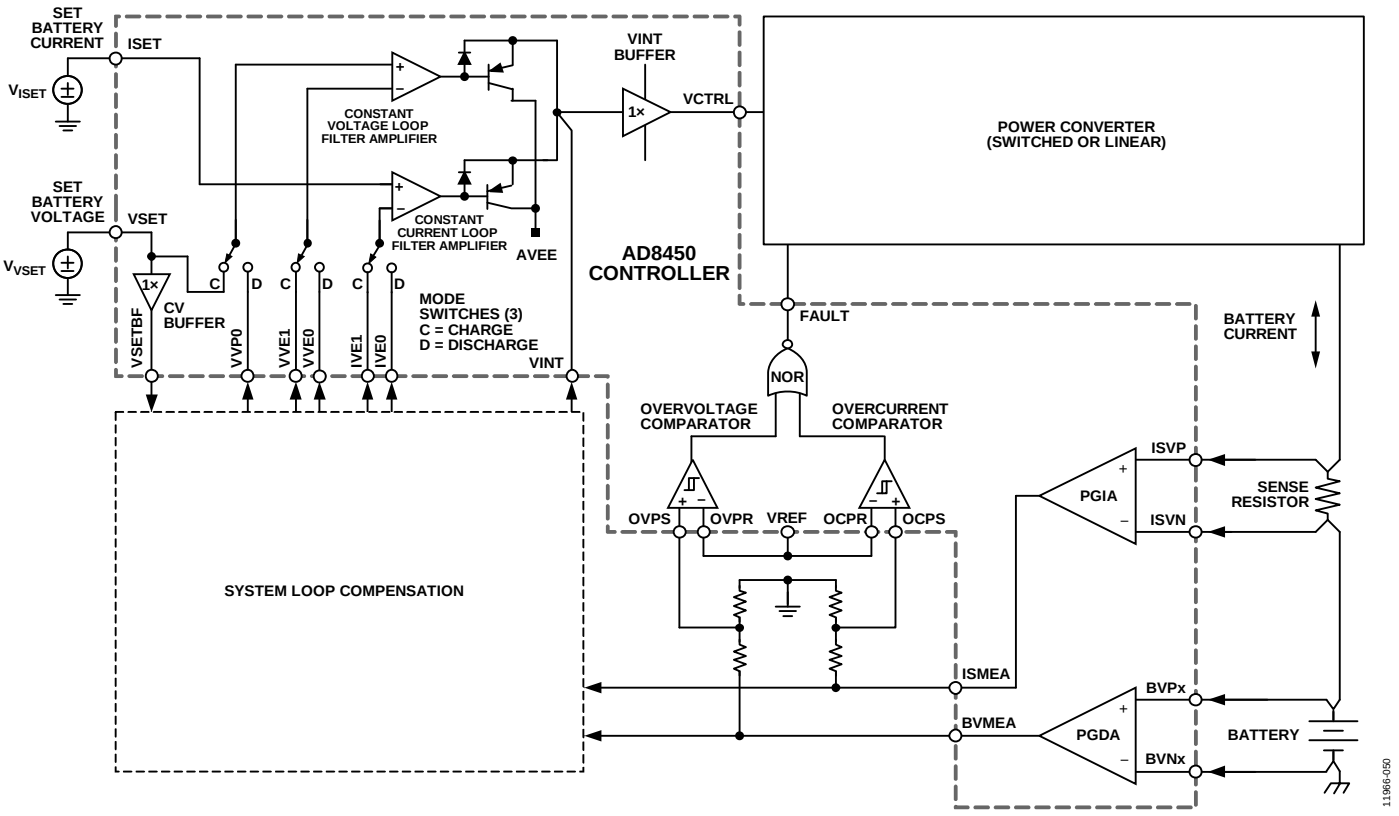

Figure 50. Signal Path of a Li-Ion Battery Formation and Test System Using the AD8450

PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER (PGIA)

Figure 51 is a block diagram of the PGIA, which is used to monitor the battery current. The architecture of the PGIA is the classic 3-op-amp topology, similar to the Analog Devices industry-standard AD8221 and AD620. This architecture provides the highest achievable CMRR at a given gain, enabling high-side battery current sensing without the introduction of significant errors in the measurement. For more information about instrumentation amplifiers, see *A Designer's Guide to Instrumentation Amplifiers*.

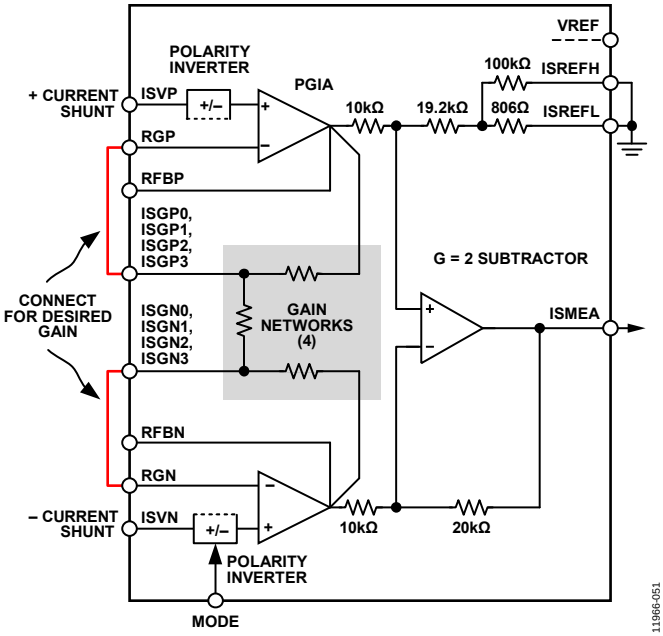

Figure 51. PGIA Simplified Block Diagram

Gain Selection

The PGIA includes four fixed internal gain options. The PGIA can also use an external gain network for arbitrary gain selection. The internal gain options are established via four independent three-resistor networks, which are laser trimmed to a matching level better than ±0.1%. The internal gains are optimized to minimize both PGIA gain error and gain error drift, allowing the controller to set a stable charge/discharge current over temperature. If the built in internal gains are not adequate, the PGIA gain can be set via an external three-resistor network.

The internal gains of the PGIA are selected by tying the inverting inputs of the PGIA preamplifiers (RGP and RGN pins) to the corresponding gain pins of the internal three-resistor network (ISGP[0:3] and ISGN[0:3] pins). For example, to set the PGIA gain to 26, tie the RGP pin to the ISGP0 pin, and tie the RGN pin to the ISGN0 pin. See Table 5 for information about the gain selection connections.

The external PGIA gain is set by tying 10 kΩ feedback resistors between the inverting inputs of the PGIA preamplifiers (RGP and RGN pins) and the outputs of the PGIA preamplifiers (RFBP and RFBN pins) and by tying a gain resistor (R_G) between the RGP and RGN pins. When using external resistors, the PGIA gain is

$$Gain = 2 \times (1 + 20\ k\Omega/R_G)$$

Note that the PGIA subtractor has a closed-loop gain of 2 to increase the common-mode range of the preamplifiers.

Reversing Polarity When Charging and Discharging

Figure 50 shows that during the charge cycle, the power converter feeds current into the battery, generating a positive voltage across the current sense resistor. During the discharge cycle, the power converter draws current from the battery, generating a negative voltage across the sense resistor. In other words, the battery current polarity reverses when the battery discharges.

In the constant current (CC) control loop, this change in polarity can be problematic if the polarity of the target current is not reversed. To solve this problem, the AD8450 PGIA includes a multiplexer preceding its inputs that inverts the polarity of the PGIA gain. This multiplexer is controlled via the MODE pin. When the MODE pin is logic high (charge mode), the PGIA gain is noninverting, and when the MODE pin is logic low (discharge mode), the PGIA gain is inverting.

PGIA Offset Option

As shown in Figure 51, the PGIA reference node is connected to the ISREFL and ISREFH pins via an internal resistor divider. This resistor divider can be used to introduce a temperature insensitive offset to the output of the PGIA such that the PGIA output always reads a voltage higher than zero for a zero differential input. Because the output voltage of the PGIA is always positive, a unipolar ADC can digitize it.

When the ISREFH pin is tied to the VREF pin with the ISREFL pin grounded, the voltage at the ISMEA pin is increased by 20 mV, guaranteeing that the output of the PGIA is always positive for zero differential inputs. Other voltage shifts can be realized by tying the ISREFH pin to an external voltage source. The gain from the ISREFH pin to the ISMEA pin is 8 mV/V. For zero offset, tie the ISREFL and ISREFH pins to ground.

Battery Reversal and Overvoltage Protection

The AD8450 PGIA can be configured for high-side or low-side current sensing. If the PGIA is configured for high-side current sensing (see Figure 50) and the battery is connected backward, the PGIA inputs may be held at a voltage that is below the negative power rail (AVEE), depending on the battery voltage.

To prevent damage to the PGIA under these conditions, the PGIA inputs include overvoltage protection circuitry that allows them to be held at voltages of up 55 V from the opposite power rail. In other words, the safe voltage span for the PGIA inputs extends from AVCC − 55 V to AVEE + 55 V.

PROGRAMMABLE GAIN DIFFERENCE AMPLIFIER (PGDA)

Figure 52 is a block diagram of the PGDA, which is used to monitor the battery voltage. The architecture of the PGDA is a subtractor amplifier with four selectable inputs: the BVP[0:3] and BVN[0:3] pins. Each input pair corresponds to one of the internal gains of the PGDA: 0.2, 0.27, 0.4, and 0.8. These gain values allow the PGDA to funnel the voltage of up to four 5 V batteries in series (4S) to a level that can be read by a 5 V ADC. See Table 6 for information about the gain selection connections.

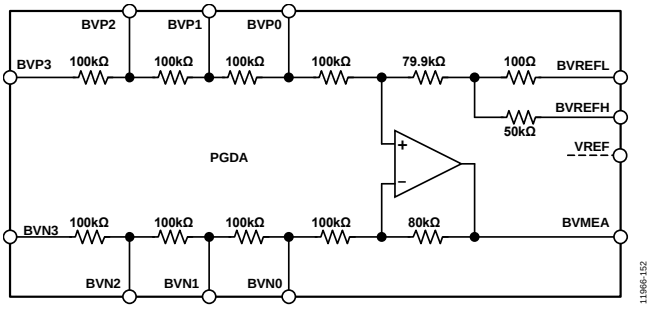

Figure 52. PGDA Simplified Block Diagram

The resistors that form the PGDA gain network are laser trimmed to a matching level better than ±0.1%. This level of matching minimizes the gain error and gain error drift of the PGDA while maximizing the CMRR of the PGDA. This matching also allows the controller to set a stable target voltage for the battery over temperature while rejecting the ground bounce in the battery negative terminal.

Like the PGIA, the PGDA can also level shift its output voltage via an internal resistor divider that is tied to the PGDA reference node. This resistor divider is connected to the BVREFH and BVREFL pins.

When the BVREFH pin is tied to the VREF pin with the BVREFL pin grounded, the voltage at the BVMEA pin is increased by 5 mV, guaranteeing that the output of the PGDA is always positive for zero differential inputs. Other voltage shifts can be realized by tying the BVREFH pin to an external voltage source. The gain from the BVREFH pin to the BVMEA pin is 2 mV/V. For zero offset, tie the BVREFL and BVREFH pins to ground.

CC AND CV LOOP FILTER AMPLIFIERS

The constant current (CC) and constant voltage (CV) loop filter amplifiers are high precision, low noise specialty amplifiers with very low offset voltage and very low input bias current. These amplifiers serve two purposes:

- Using external components, the amplifiers implement active loop filters that set the dynamics (transfer function) of the CC and CV loops.
- The amplifiers perform a seamless transition from CC to CV mode after the battery reaches its target voltage.

Figure 53 is the functional block diagram of the AD8450 CC and CV feedback loops for charge mode (MODE pin is logic high). For illustration purposes, the external networks connected to the loop amplifiers are simple RC networks configured to form single-pole inverting integrators. The outputs of the CC and CV loop filter amplifiers are coupled to the VINT pin via an analog NOR circuit (minimum output selector circuit), such that they can only pull the VINT node down. In other words, the loop amplifier that requires the lowest voltage at the VINT pin is in control of the node. Thus, only one loop amplifier, CC or CV, can be in control of the system charging control loop at any given time.

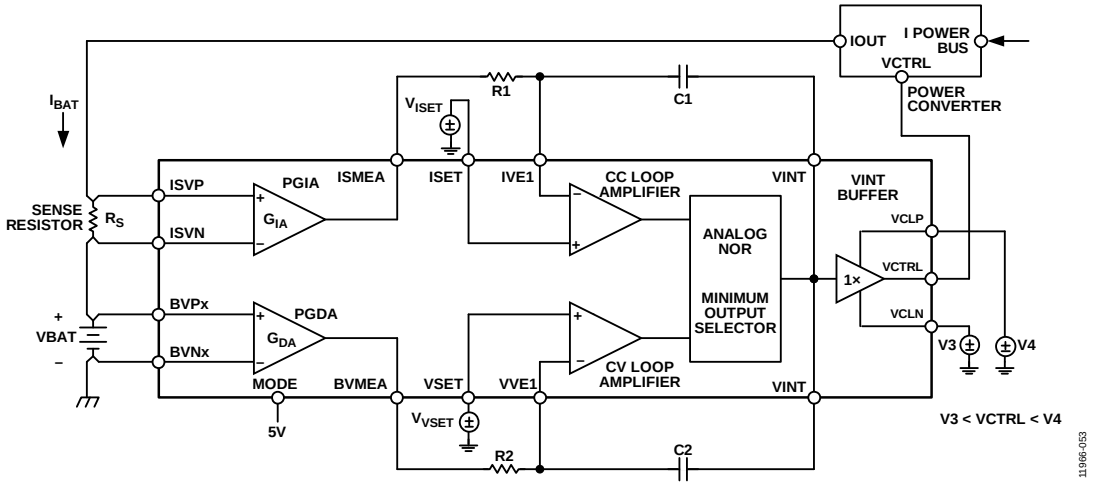

Figure 53. Functional Block Diagram of the CC and CV Loops in Charge Mode (MODE Pin High)

The unity-gain amplifier (VINT buffer) buffers the VINT pin and drives the VCTRL pin. The VCTRL pin is the control output of the AD8450 and the control input of the power converter. The V_{ISET} and V_{VSET} voltage sources set the target constant current and the target constant voltage, respectively. When the CC and CV feedback loops are in steady state, the charging current is set at

$$I_{BAT\_SS} = \frac{V_{ISET}}{G_{IA} \times R_S}$$

where:
G_{IA} is the PGIA gain.
R_S is the value of the shunt resistor.

The target voltage is set at

$$V_{BAT\_SS} = \frac{V_{VSET}}{G_{DA}}$$

where G_{DA} is the PGDA gain.

Because the offset voltage of the loop amplifiers is in series with the target voltage sources, V_{ISET} and V_{VSET}, the high precision of these amplifiers minimizes this source of error.

Figure 54 shows a typical CC/CV charging profile for a Li-Ion battery. In the first stage of the charging process, the battery is charged with a constant current (CC) of 1 A. When the battery voltage reaches a target voltage of 4.2 V, the charging process transitions such that the battery is charged with a constant voltage (CV) of 4.2 V.

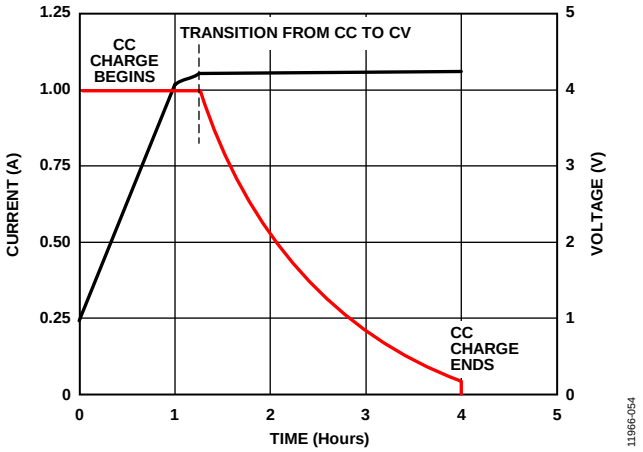

Figure 54. Representative Constant Current to Constant Voltage Transition Near the End of a Battery Charging Cycle

The following steps describe how the AD8450 implements the CC/CV charging profile (see Figure 53). In this scenario, the battery begins in the fully discharged state, and the system has just been turned on such that I_{BAT} = 0 A at Time 0.

1. Because the voltages at the ISMEA and BVMEA pins are below the target voltages (V_{ISET} and V_{VSET}) at Time 0, both integrators begin to ramp, increasing the voltage at the VINT node.
2. As the voltage at the VINT node increases, the voltage at the VCRTL node rises, and the output current of the power converter, I_{BAT}, increases (assuming that an increasing voltage at the VCRTL node increases the output current of the power converter).
3. When the I_{BAT} current reaches the CC steady state value, I_{BAT_SS}, the battery voltage is still below the target steady state value, V_{BAT_SS}. Therefore, the CV loop tries to keep pulling the VINT node up while the CC loop tries to keep it at its current voltage. At this point, the voltage at the ISMEA pin equals V_{ISET}, so the CC loop stops integrating.
4. Because the loop amplifiers can only pull the VINT node down due to the analog NOR circuit, the CC loop takes control of the charging feedback loop and the CV loop is disabled.
5. As the charging process continues, the battery voltage increases until it reaches the steady state value, V_{BAT_SS}, and the voltage at the BVMEA pin reaches the target voltage, V_{VSET}.
6. The CV loop tries to pull the VINT node down to reduce the charging current (I_{BAT}) and prevent the battery voltage from rising any farther. At the same time, the CC loop tries to keep the VINT node at its current voltage to keep the battery current at I_{BAT_SS}.
7. Because the loop amplifiers can only pull the VINT node down due to the analog NOR circuit, the CV loop takes control of the charging feedback loop and the CC loop is disabled.

The analog NOR (minimum output selector) circuit that couples the outputs of the loop amplifiers is optimized to minimize the transition time from CC to CV control. Any delay in the transition causes the CC loop to remain in control of the charge feedback loop after the battery voltage reaches its target value. Therefore, the battery voltage continues to rise beyond V_{BAT_SS} until the control loop transitions; that is, the battery voltage overshoots its target voltage. When the CV loop takes control of the charge feedback loop, it reduces the battery voltage to the target voltage. A large overshoot in the battery voltage due to transition delays can damage the battery; thus, it is crucial to minimize delays by implementing a fast CC to CV transition.

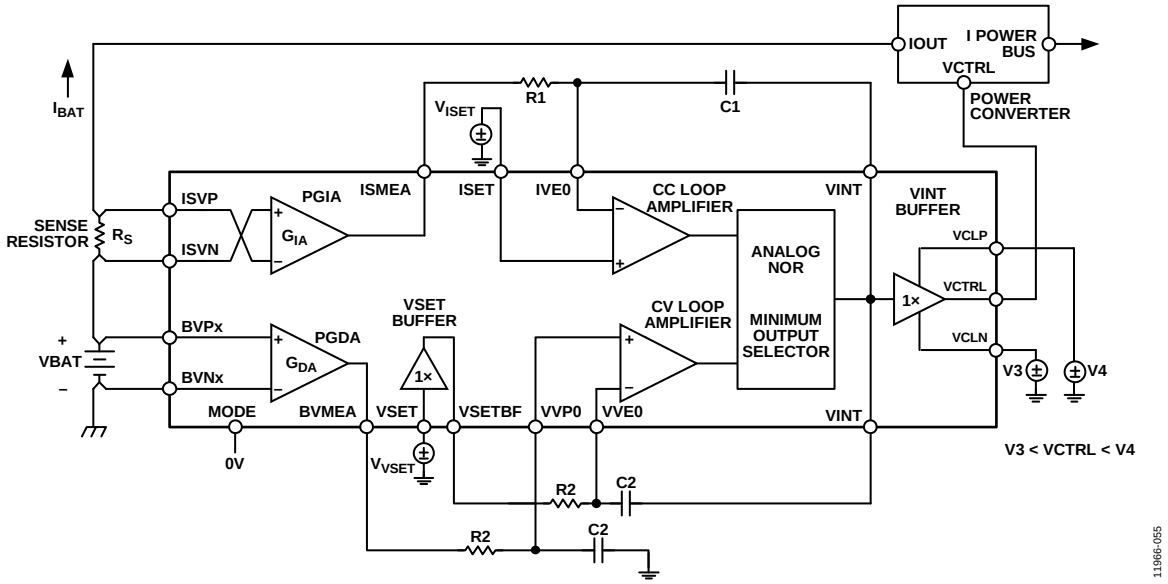

Figure 55. Functional Block Diagram of the CC and CV Loops in Discharge Mode (MODE Pin Low)

Figure 55 is the functional block diagram of the AD8450 CC and CV feedback loops for discharge mode (MODE pin is logic low. In discharge mode, the feedback loops operate in a similar manner as in charge mode. The only difference is in the CV loop amplifier, which operates as a noninverting integrator in discharge mode. For illustration purposes, the external networks connected to the loop amplifiers are simple RC networks configured to form single-pole integrators (see Figure 55).

COMPENSATION

In battery formation and test systems, the CC and CV feedback loops have significantly different open-loop gain and crossover frequencies; therefore, each loop requires its own frequency compensation. The active filter architecture of the AD8450 CC and CV loops allows the frequency response of each loop to be set independently via external components. Moreover, due to the internal switches in the CC and CV amplifiers, the frequency response of the loops in charge mode does not affect the frequency response of the loops in discharge mode.

Unlike simpler controllers that use passive networks to ground for frequency compensation, the AD8450 allows the use of feedback networks for its CC and CV loop filter amplifiers. These networks enable the implementation of both PD (Type II) and PID (Type III) compensators. Note that in charge mode, both the CC and CV loops implement inverting compensators, whereas in discharge mode, the CC loop implements an inverting compensator and the CV loop implements a noninverting compensator. As a result, the CV loop in discharge mode includes an additional amplifier, VSET buffer, to buffer the VSET node from the feedback network (see Figure 55).

VINT BUFFER

The unity-gain amplifier (VINT buffer) is a clamp amplifier that drives the VCTRL pin. The VCTRL pin is the control output of the AD8450 and the control input of the power converter (see Figure 53 and Figure 55). The output voltage range of this amplifier is bounded by the clamp voltages at the VCLP and VCLN pins such that

$$V_{VCLN} - 0.5\ V < V_{VCTRL} < V_{VCLP} + 0.5\ V$$

The reduction in the output voltage range of the amplifier is a safety feature that allows the AD8450 to drive devices such as the ADP1972 pulse-width modulation (PWM) controller, whose input voltage range must not exceed 5.5 V (that is, the voltage at the COMP pin of the ADP1972 must be below 5.5 V).

MODE PIN, CHARGE AND DISCHARGE CONTROL

The MODE pin is a TTL logic input that configures the AD8450 for either charge or discharge mode. A logic low (V_{MODE} < 0.8 V) corresponds to discharge mode, and a logic high (V_{MODE} > 2 V) corresponds to charge mode. Internal to the AD8450, the MODE pin toggles all SPDT switches in the CC and CV loop amplifiers and inverts the gain polarity of the PGIA.

OVERCURRENT AND OVERVOLTAGE COMPARATORS

The AD8450 includes overcurrent protection (OCP) and overvoltage protection (OVP) comparators to detect overvoltage and overcurrent conditions in the battery. Because the outputs of the comparators are combined by a NOR logic gate, these comparators output a logic low at the FAULT pin when either comparator is tripped (see Figure 49).

The OCP and OVP comparators can be configured to detect a fault in one of two ways. In the configuration shown in Figure 56, the voltages at the ISMEA and BVMEA pins are divided down and compared to the internal 2.5 V reference of the AD8450. In this configuration, the FAULT pin registers a logic low (a fault condition) when

$$V_{ISMEA} > \frac{R1 + R2}{R2} \times 2.5\ \text{V}$$

or

$$V_{BVMEA} > \frac{R3 + R4}{R3} \times 2.5\ \text{V}$$

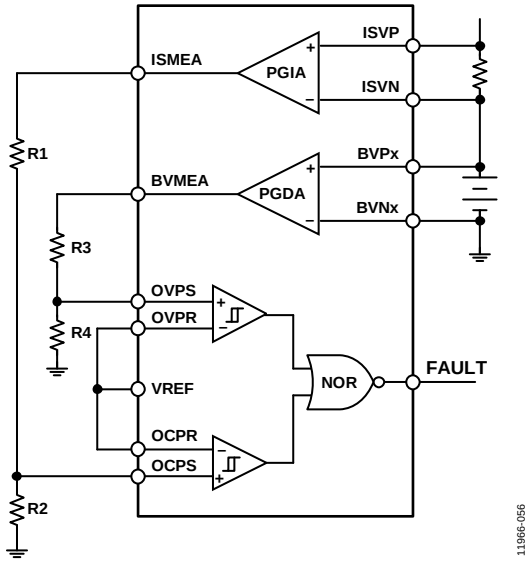

Figure 56. OVP and OCP Comparator Configuration Using the Internal Reference

Alternatively, the outputs of the PGIA and PGDA can be tied directly to the sense inputs of the comparators (OCPS and OVPS pins) such that the voltages at the ISMEA and BVMEA pins are compared to the external reference voltages, V_{OCP_REF} and V_{OVP_REF} (see Figure 57). In this configuration, the FAULT pin registers a logic low (a fault condition) when

$$V_{ISMEA} > V_{OCP\_REF}$$

or

$$V_{BVMEA} > V_{OVP\_REF}$$

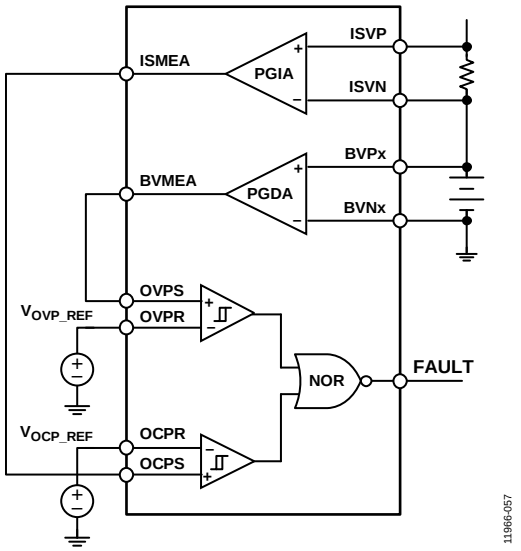

Figure 57. OVP and OCP Comparator Configuration Using an External Reference (For Example, a DAC)

CURRENT SHARING BUS AND IMAX OUTPUT

Battery formation and test systems that use multiple channels bridged together to condition high current battery cells require circuitry to balance the total output current among the channels. Current balance, or current sharing (CS), can be implemented by actively matching the output current of each channel during the battery charge/discharge process.

The current sharing bus amplifier is a precision unity-gain specialty amplifier with an output stage that can only pull up its output node (the CSH pin). The amplifier is configured as a unity-gain buffer with its input connected to the ISMEA pin (the output of the PGIA). If the CSH pin is left unconnected, the voltage at the pin is a replica of the voltage at the ISMEA pin.

Figure 58 is a functional block diagram of the current sharing circuit. In this example, Channel 0 through Channel n are bridged together to charge a high current battery.

The CS output of each channel is tied to a common bus (CS bus), which is buffered by the CS buffer amplifier to the IMAX pin.

By means of external resistors, the uncommitted operational amplifier is configured as a difference amplifier to measure the voltage difference between the IMAX and ISMEA nodes.

During the charge process, the charging current and, therefore, the voltage at the ISMEA pin, is slightly different in each channel due to mismatches in the components that make up each channel. Because the CS bus amplifiers are driven by their respective PGIAs and have output stages that can only pull up their output nodes, the amplifier that requires the highest voltage takes control of the CS bus. Therefore, the voltage at the CS bus is pulled up to match the V_{ISMEA} voltage of the channel with the largest output current.

The output voltage of the uncommitted op amp in each channel is proportional to the difference between the channel's output current and the largest output current. This output voltage can then be used to form a feedback loop that actively corrects the channel's output current by adjusting the channel's target current and target voltage, that is, adjusting V_{ISET} and V_{VSET} voltages.

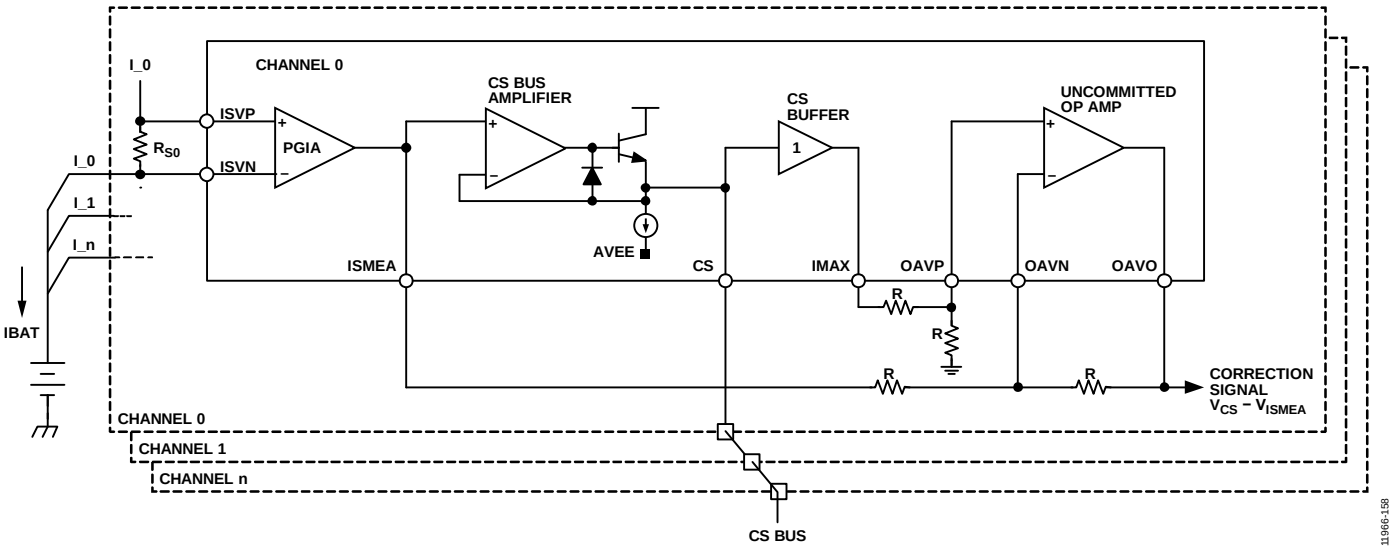

Figure 58. Functional Block Diagram of the Current Sharing Circuit

APPLICATIONS INFORMATION

This section describes how to use the AD8450 in the context of a battery formation and test system. This section includes a design example of a small scale model of an actual system. An evaluation board for the AD8450 is available and is described in the Evaluation Board section.

FUNCTIONAL DESCRIPTION

The AD8450 is a precision analog front end and controller for battery formation and test systems. These systems use precision controllers and power stages to put batteries through charge and discharge cycles. Figure 59 shows the signal path of a simplified switching battery formation and test system using the AD8450 controller and the ADP1972 PWM controller. For more information about the ADP1972, see the ADP1972 data sheet.

The AD8450 is suitable for systems that form and test NiCad, NiMH, and Li-Ion batteries and is designed to operate in conjunction with both linear and switching power stages.

The AD8450 includes the following blocks (see Figure 49 and the Theory of Operation section for more information).

- Pin programmable gain instrumentation amplifier (PGIA) that senses low-side or high-side battery current.
- Pin programmable gain difference amplifier (PGDA) that measures the terminal voltage of the battery.
- Two loop filter error amplifiers that receive the battery target current and voltage and establish the dynamics of the constant current (CC) and constant voltage (CV) feedback loops.
- Minimum output selector circuit that combines the outputs of the loop filter error amplifiers to perform automatic CC to CV switching.
- Output clamp amplifier that drives the VCTRL pin. The voltage range of this amplifier is bounded by the voltage at the VCLP and VCLN pins such that it cannot overrange the subsequent stage. The output clamp amplifier can drive switching and linear power converters. Note that an increasing voltage at the VCTRL pin must translate to a larger output current in the power converter.
- Overcurrent and overvoltage comparators whose outputs are combined using a NOR gate to drive the FAULT pin. The FAULT pin presents a logic low when either comparator is tripped.
- 2.5 V reference that can be used as the reference voltage for the overcurrent and overvoltage comparators. The output node of the 2.5 V reference is the VREF pin.
- Current sharing amplifier that detects the maximum battery current among several charging channels and whose output can be used to implement current balancing.
- Logic input pin (MODE) that changes the configuration of the controller from charge to discharge mode. A logic high at the MODE pin configures charge mode; a logic low configures discharge mode.

POWER SUPPLY CONNECTIONS

The AD8450 requires two analog power supplies (AVCC and AVEE), one digital power supply (DVCC), one analog ground (AGND), and one digital ground (DGND). AVCC and AVEE power all the analog blocks, including the PGIA, PGDA, op amps, and comparators. DVCC powers the MODE input logic circuit and the FAULT output logic circuit. AGND provides a reference and return path for the 2.5 V reference, and DGND provides a reference and return path for the digital circuitry.

The rated absolute maximum value for AVCC − AVEE is 36 V, and the minimum operating AVCC and AVEE voltages are +5 V and −5 V, respectively. Due to the high PSRR of the AD8450 analog blocks, AVCC can be connected directly to the high current power bus (the input voltage of the power converter) without risking the injection of supply noise to the controller outputs.

A commonly used power supply combination is +25 V and −5 V for AVCC and AVEE, and +5 V for DVCC. The +25 V rail for AVCC provides enough headroom to the PGIA such that it can be connected in a high-side current sensing configuration with up to four batteries in series (4S). The −5 V rail for AVEE allows the PGDA to sense accidental reverse battery conditions (see the Reverse Battery Conditions section).

Connect decoupling capacitors to all the supply pins. A 1 µF capacitor in parallel with a 0.1 µF capacitor is recommended.

POWER SUPPLY SEQUENCING

As detailed in the absolute maximum ratings table (see Table 2), the voltage at any input pin other than ISVP, ISVN, BVPx, and BVNx cannot exceed the positive analog supply (AVCC) by more than 0.5 V and cannot be exceeded by the analog negative supply (AVEE) by 0.5V.

Additionally, supply and ground pins (DVCC, DGND, and AGND) cannot exceed the positive analog supply (AVCC) by more than 0.5 V and cannot be exceeded by the analog negative supply (AVEE) by 0.5V.

Therefore, power-on and power-off sequencing may be required to comply with the absolute maximum ratings.

Failure to comply with the absolute maximum ratings can result in functional failure or damage to the internal ESD diodes. Damaged ESD diodes can cause parametric failures and cannot provide full ESD protection, reducing reliability.

POWER-ON SEQUENCE

To power on the device, take the following steps:

1. Turn on AVCC
2. Turn on AVEE
3. Turn on DVCC
4. Turn on the input signals

The positive analog supply (AVCC) and the negative analog supply (AVEE) may be turned on simultaneously.

POWER-OFF SEQUENCE

To power off the device, take the following steps:

1. Turn off the input signals.
2. Turn off DVCC.
3. Turn off AVEE.
4. Turn off AVCC.

The positive analog supply (AVCC) and the negative analog supply (AVEE) may be turned off simultaneously.

PGIA CONNECTIONS

For a description of the PGIA, see the Theory of Operation section, Figure 49, and Figure 51. The internal gains of the PGIA (26, 66, 133, and 200) are selected by hardwiring the appropriate pin combinations (see Table 5).

Table 5. PGIA Gain Connections

PGIA Gain	Connect RGP (Pin 2) to	Connect RGN (Pin 19) to
26	ISGP0 (Pin 4)	ISGN0 (Pin 17)
66	ISGP1 (Pin 6)	ISGN1 (Pin 15)
133	ISGP2 (Pin 8)	ISGN2 (Pin 13)
200	ISGP3 (Pin 9)	ISGN3 (Pin 12)

If a different gain value is desired, connect 10 kΩ feedback resistors between the inverting inputs of the PGIA preamplifiers (RGP and RGN pins) and the outputs of the PGIA preamplifiers (RFBP and RFBN pins). Also, connect a gain resistor (R_G) between the RGP and RGN pins. When using external resistors, the gain of the PGIA is

$$Gain = 2 \times (1 + 20\ k\Omega/R_G)$$

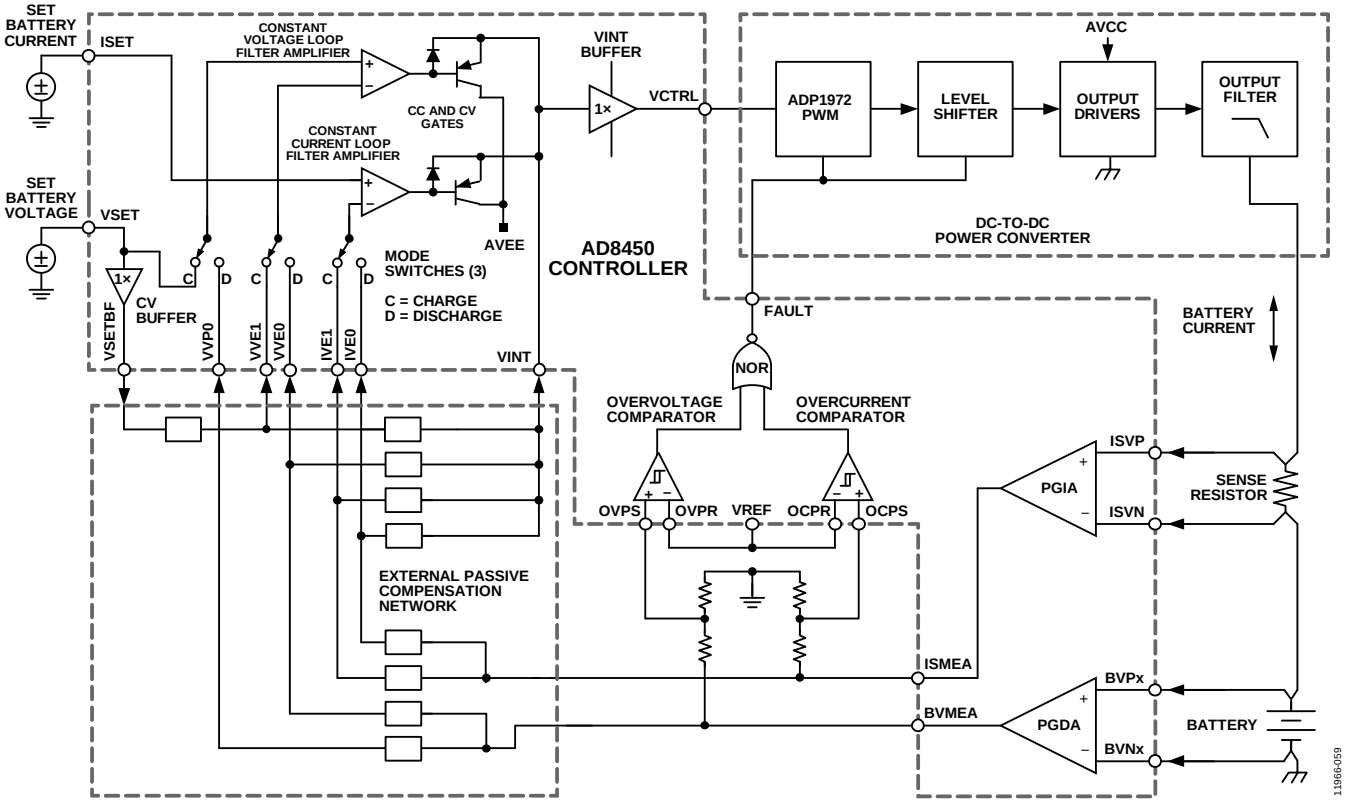

Figure 59. Complete Signal Path of a Battery Test or Formation System Suitable for Li-Ion Batteries

Current Sensors

Two common options for current sensors are isolated current sensing transducers and shunt resistors. Isolated current sensing transducers are galvanically isolated from the power converter and are affected less by the high frequency noise generated by switch mode power supplies. Shunt resistors are less expensive and easier to deploy.

If a shunt resistor sensor is used, a 4-terminal, low resistance shunt resistor is recommended. Two of the four terminals conduct the battery current, whereas the other two terminals conduct virtually no current. The terminals that conduct no current are sense terminals that are used to measure the voltage drop across the resistor (and, therefore, the current flowing through it) using an amplifier such as the PGIA of the AD8450. To interface the PGIA with the current sensor, connect the sense terminals of the sensor to the ISVP and ISVN pins of the AD8450 (see Figure 60).

Optional Low-Pass Filter

The AD8450 is designed to control both linear regulators and switching power converters. Linear regulators are generally noise free, whereas switch mode power converters generate switching noise. Connecting an external differential low-pass filter between the current sensor and the PGIA inputs reduces the injection of switching noise into the PGIA (see Figure 60).

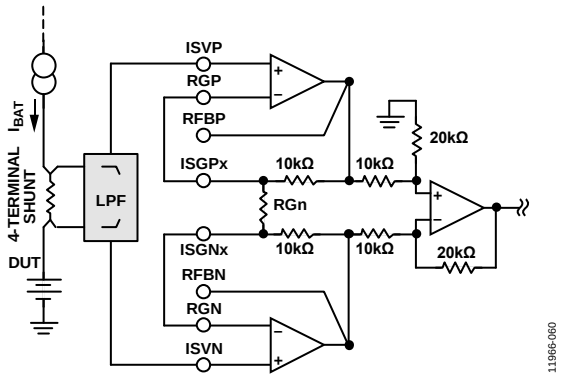

Figure 60. 4-Terminal Shunt Resistor Connected to the Current Sense PGIA

PGDA CONNECTIONS

For a description of the PGDA, see the Theory of Operation section, Figure 49, and Figure 52. The internal gains of the PGDA (0.2, 0.27, 0.4, and 0.8) are selected by connecting the appropriate input pair to the battery terminals (see Table 6).

Table 6. PGDA Gain Connections

PGDA Gain	Connect Battery Positive Terminal to	Connect Battery Negative Terminal to
0.8	BVP0 (Pin 25)	BVN0 (Pin 31)
0.4	BVP1 (Pin 24)	BVN1 (Pin 32)
0.27	BVP2 (Pin 23)	BVN2 (Pin 33)
0.2	BVP3 (Pin 22)	BVN3 (Pin 34)

Set the PGDA gain value to attenuate the voltage of up to four 5 V battery cells in series to a full-scale voltage of 4 V. For example, a 5 V battery voltage is attenuated to 4 V using the gain of 0.8, and a 20 V battery voltage (four 5 V batteries in series) is attenuated to 4 V using the gain of 0.2. This voltage scaling enables the use of a 5 V ADC to read the battery voltage at the BVMEA output pin.

Reverse Battery Conditions

The output voltage of the AD8450 PGDA can be used to detect a reverse battery connection. A −5 V rail for AVEE allows the output of the PGDA to go below ground when the battery is connected backward. Therefore, the condition can be detected by monitoring the BVMEA pin for a negative voltage.

BATTERY CURRENT AND VOLTAGE CONTROL INPUTS (ISET AND VSET)

The voltages at the ISET and VSET input pins set the target battery current and voltage for the constant current (CC) and constant voltage (CV) loops. These inputs must be driven by a precision voltage source (or a DAC connected to a precision reference) whose output voltage is referenced to the same voltage as the PGIA and PGDA reference pins (ISREFH/ISREFL and BVREFH/BVREFL, respectively). For example, if the PGIA reference pins are connected to AGND, the voltage source connected to ISET must also be referenced to AGND. In the same way, if the PGDA reference pins are connected to AGND, the voltage source connected to VSET must also be referenced to AGND.

In constant current mode, when the CC feedback loop is in steady state, the ISET input sets the battery current as follows:

$$I_{BAT\_SS} = \frac{V_{ISET}}{G_{IA} \times R_S}$$

where:
G_{IA} is the PGIA gain.
R_S is the value of the shunt resistor.

In constant voltage mode, when the CV feedback loop is in steady state, the VSET input sets the battery voltage as follows:

$$V_{BAT\_SS} = \frac{V_{VSET}}{G_{DA}}$$

where G_{DA} is the PGDA gain.

Therefore, the accuracy and temperature stability of the formation and test system are dependent not only on the precision of the AD8450, but also on the accuracy of the ISET and VSET inputs.

LOOP FILTER AMPLIFIERS

The AD8450 has two loop filter amplifiers, also known as error amplifiers (see Figure 59). One amplifier is for constant current control (CC loop filter amplifier), and the other amplifier is for constant voltage control (CV loop filter amplifier). The outputs of these amplifiers are combined using a minimum output selector circuit to perform automatic CC to CV switching.

Table 7 lists the inputs of the loop filter amplifiers for charge mode and discharge mode.

Table 7. Integrator Input Connections

Feedback Loop Function	Reference Input	Feedback Terminal
Control the Current While Discharging a Battery	ISET	IVE0
Control the Current While Charging a Battery	ISET	IVE1
Control the Voltage While Discharging a Battery	VSET	VVE0
Control the Voltage While Charging a Battery	VSET	VVE1

The CC and CV amplifiers in charge mode and the CC amplifier in discharge mode are inverting integrators, whereas the CV amplifier in discharge mode is a noninverting integrator. Therefore, the CV amplifier in discharge mode uses an extra amplifier, the VSET buffer, to buffer the VSET input pin (see Figure 49). Also, the CV amplifier in discharge mode uses the VVP0 pin to couple the signal from the BVMEA pin to the integrator.

CONNECTING TO A PWM CONTROLLER (VCTRL PIN)

The VCTRL output pin of the AD8450 is designed to interface with linear power converters and with pulse-width modulation (PWM) controllers such as the ADP1972. The voltage range of the VCTRL output pin is bounded by the voltages at the VCLP and VCLN pins, as follows:

$$V_{VCLN} - 0.5\text{ V} < V_{VCTRL} < V_{VCLP} + 0.5\text{ V}$$

Because the maximum rated input voltage at the COMP pin of the ADP1972 is 5.5 V, connect the clamp voltages of the output amplifier to +5 V (VCLP) and ground (VCLN) to prevent overranging of the COMP input. As an additional precaution, install an external 5.1 V Zener diode from the COMP pin to ground with a series 1 kΩ resistor connected between the VCTRL and COMP pins. Consult the ADP1972 data sheet for additional applications information.

Given the architecture of the AD8450, the controller requires that an increasing voltage at the VCTRL pin translate to a larger output current in the power converter. If this is not the case, a unity-gain inverting amplifier can be added in series with the AD8450 output to add an extra inversion.

OVERVOLTAGE AND OVERCURRENT COMPARATORS

The reference inputs of the overvoltage and overcurrent comparators can be driven with external voltage references or with the internal 2.5 V reference (adjacent VREF pin). If external voltage references are used, the sense inputs can be driven directly by the PGIA and PGDA output nodes, ISMEA and BVMEA, respectively. If the internal 2.5 V reference is used, the sense inputs can be driven by resistor dividers, which attenuate the voltage at the ISMEA and BVMEA nodes. For more information, see the Overcurrent and Overvoltage Comparators section.

STEP BY STEP DESIGN EXAMPLE

This section describes the systematic design of a 1 A battery charger/discharger using the AD8450 controller and the ADP1972 pulse-width modulation (PWM) controller. The power converter used in this design is a nonisolated buck boost dc-to-dc converter. The target battery is a 4.2 V fully charged, 2.7 V fully discharged Li-Ion battery.

Step 1: Design the Switching Power Converter

Select the switches and passive components of the buck boost power converter to support the 1 A maximum battery current. The design of the power converter is beyond the scope of this data sheet; however, there are many application notes and other helpful documents available from manufacturers of integrated driver circuits and power MOSFET output devices that can be used for reference.

Step 2: Identify the Control Voltage Range of the ADP1972

The control voltage range of the ADP1972 (voltage range of the COMP input pin) is 0.5 V to 4.5 V. An input voltage of 4.5 V results in the highest duty cycle and output current, whereas an input voltage of 0.5 V results in the lowest duty cycle and output current. Because the COMP pin connects directly to the VCTRL output pin of the AD8450, the battery current is proportional to the voltage at the VCTRL pin.

For information about how to interface the ADP1972 to the power converter switches, see the ADP1972 data sheet.

Step 3: Determine the Control Voltage for the CV Loop and the PGDA Gain

The relationship between the control voltage for the CV loop (the voltage at the VSET pin), the target battery voltage, and the PGDA gain is as follows:

$$CV\ Battery\ Target\ Voltage = \frac{V_{VSET}}{PGDA\ Gain}$$

In charge mode, for a CV battery target voltage of 4.2 V, the PGDA gain of 0.8 maximizes the dynamic range of the PGDA. Therefore, select a CV control voltage of 3.36 V. In discharge mode, for a CV battery target voltage of 2.7 V, the CV control voltage is 2.16 V.

Step 4: Determine the Control Voltage for the CC Loop, the Shunt Resistor, and the PGIA Gain

The relationship between the control voltage for the CC loop (the voltage at the ISET pin), the target battery current, and the PGIA gain is as follows:

$$CC\ Battery\ Target\ Current = \frac{V_{ISET}}{R_S \times PGIA\ Gain}$$

The voltage across the shunt resistor is as follows:

$$Shunt\ Resistor\ Voltage = \frac{V_{ISET}}{PGIA\ Gain}$$

Selecting the highest PGIA gain of 200 reduces the voltage across the shunt resistor, minimizing dissipated power and inaccuracies due to self heating. For a PGIA gain of 200 and a target current of 1 A, choosing a 20 mΩ shunt resistor results in a control voltage of 4 V.

When selecting a shunt resistor, pay close attention to the resistor style and construction. For low power applications, many surface-mount (SMD), temperature stable styles are available that solder to a mating pad on a printed circuit board (PCB). For optimum accuracy, specify a 4-terminal shunt resistor that provides separate high current and sense terminals. This type of resistor directs the majority of the battery current through a high current path. An additional pair of terminals provides a separate connection for the input leads to the PGIA, avoiding the power loss inherent to forcing the full battery current through the distance to the PGIA pins. Because the bias current is so low, the sense error is significantly less than if the battery current were to transverse the additional lead length.

Step 5: Choose the Control Voltage Sources

The input control voltages (the voltages at the ISET and VSET pins) can be generated by an analog voltage source such as a voltage reference or by a digital-to-analog converter (DAC). In both cases, select a device that provides a stable, low noise output voltage. If a DAC is preferred, Analog Devices offers a wide range of precision converters. For example, the AD5668 16-bit DAC provides up to eight 0 V to 4 V sources when connected to an external 2 V reference.

To maximize accuracy, the control voltage sources must be referenced to the same potential as the outputs of the PGIA and PGDA. For example, if the PGIA and PGDA reference pins are connected to AGND, connect the reference pins of the control voltage sources to AGND.

Step 6: Select the Compensation Devices

Feedback controlled switching power converters require frequency compensation to guarantee loop stability. There are many references available about how to design the compensation for such power converters. The AD8450 provides active loop-filter error-amplifiers for the CC and CV control loops that can implement PI, PD, and PID compensators using external passive components.

ADDITIONAL INFORMATION

Additional information relative to using the AD8450 is available in the AN-1319, *Compensator Design for a Battery Charge/Discharge Unit Using the AD8450 or the AD8451*.

EVALUATION BOARD

INTRODUCTION

Figure 61 is a photograph of the AD8450-EVALZ. The evaluation board is a convenient standalone platform for evaluating the major elements of the AD8450 (such as the PGIA and PGDA). The circuit architecture is particularly suitable for evaluating PID loop compensation when connected within an operating charge/discharge system. Four separate loop dynamic networks are available for constant current charge and discharge, and constant voltage charge and discharge. The network subcircuits are shown on the right hand side of the board schematic (Figure 62).

SMA connectors provide shielded access to the highly sensitive programmable gain instrumentation amplifier (PGIA) and the programmable gain difference amplifier (PGDA). SMA connectors ISET and VSET are the constant current and constant voltage control inputs. The ISMEA and VCTRL outputs, current and voltage alarm references, and trigger voltages are accessible for testing. The MODE switch selects either the charge or discharge option. Figure 62 is a schematic of the AD8450-EVALZ. Table 8 lists and describes the various switches and their functions and lists the SMA connector I/O.

FEATURES AND TESTS

The AD8450-EVALZ contains many user friendly features to facilitate evaluation of the AD8450 performance. Numerous connectors, test loops, and points facilitate the attachment of scope probes and cables, and I/O switches conveniently exercise various device options.

TESTING THE AD8450-EVALZ

The schematic item abbreviation TP signifies a test loop. Prior to testing, install Jumpers TST1 through TST5 and move the Shunts RUN1 through RUN5 to a single pin to open the connection. Connect +25 V at AVCC, −5 V at AVEE, and +5 V at DVCC.

PGIA and Offset

PGIA Gain Test

Apply 10 mV dc across TPISVP and TPISVN. For bench testing, connect ISVN to ground using an external jumper. Use the ISGN switch to select the desired PGIA gain option, and measure the output voltage at TPISMEA or TPIMAX (referenced to ground). For gains of 26, 66, 133, and 200, the output voltages are 260 mV, 660 mV, 1.33 V, and 2 V, respectively. Subtract any residual offset voltages from the output reading before calculating the gain.

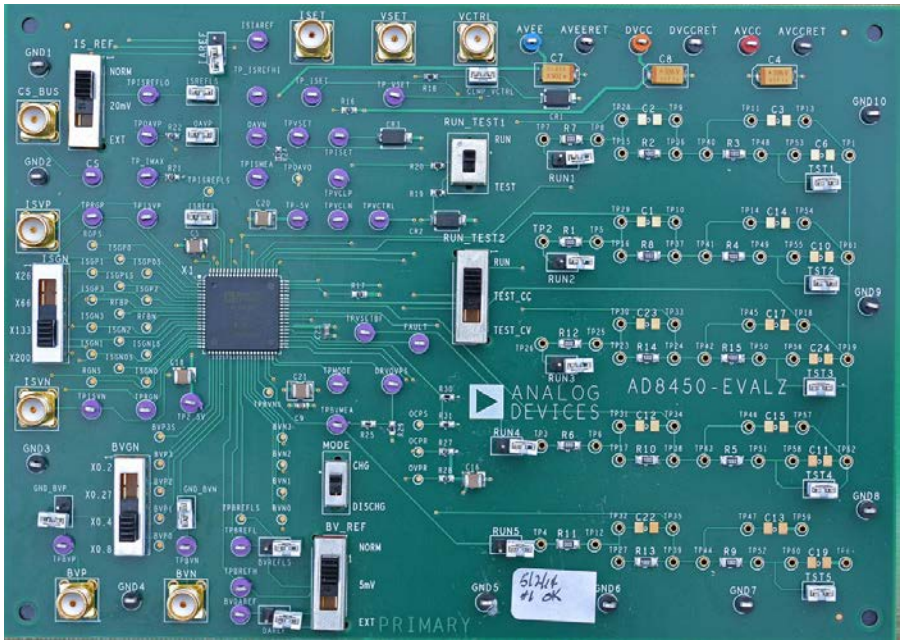

Figure 61. Photograph of the AD8450-EVALZ

Table 8. AD8450-EVALZ Test Switches and Their Functions

Switch	Function	Operation	Default Position[1]
ISGN	PGIA gain switch	The ISGN switch selects one of four fixed gain values: 26, 66, 133, or 200.	User select
BVGN	PGDA gain switch	The BVGN switch selects one of four fixed gain values: 0.2, 0.27, 0.4, or 0.8.	N/A
IS_REF	Selects between offset options for the PGIA	NORM: 0 V reference. 20mV: offsets the PGIA reference by 20 mV. EXT: An externally supplied reference voltage is applied to the PGIA.	NORM
BV_REF	Selects input source option for the BVREFH pin	NORM: Overvoltage (OV) reference applied. 5mV: The BVDA is offset by 5 mV. EXT: An externally supplied reference voltage is applied to the BVDA.	NORM
MODE	Selects charge or discharge mode	The MODE switch selects CHG (logic high) or DISCH (logic low).	CHG
RUN_TEST1	Configures the ISET and VSET inputs to test the integrators.	RUN: The ISET and VSET inputs are connected to SMA connectors ISET and VSET. TEST: connectors the ISET and VSET inputs to the 2.5 V reference.	RUN
RUN_TEST2	Configures the ISET and VSET outputs to test the integrators.	RUN: configures the ISET and VSET outputs as integrators. TEST: configures the ISET and VSET outputs as followers.	RUN

[1] N/A means not applicable.

Table 9. AD8450-EVALZ SMA Connector Functions

Connector	Function
ISVP	Input from the battery current sensor to the PGIA positive input.
ISVN	Input from the battery current sensor to the PGIA negative input.
BVP	Input from the battery positive voltage terminal to the PGDA positive input.
BVN	Input from the battery negative voltage terminal to the PGDA negative input.
ISET	Input to the AD8450 ISET pin.
VSET	Input to the AD8450 VSET pin.
VCTRL	AD8450 control voltage output to the PWM or analog power supply COMP input.
CS_BUS	AD8450 current sharing input/output bus.

PGIA in an Application

The differential inputs of the PGIA assume the use of a high-side current shunt in series with the battery. To connect the evaluation board in an application, simply connect the ISVP and ISVN to the positive and negative shunt connections. Be sure that both inputs are floating (ungrounded). The ISVP and ISVN inputs tolerate the full AVCC common-mode voltage applied to the board.

Simple Offset Test

Short the PGIA inputs from TPISVP to TPISVN to one of the black ground loops. The ISMEA output is 0 V ± the residual offset voltage multiplied by the gain. Move the IS_REF switch to the 20 mV position to increase ISMEA by 20 mV.

Offset in an Application

In certain instances, the system operates with various ground voltage levels. Although the PGIA is differential and floating, it may be advantageous to refer the PGIA to a ground at or near the battery load.

PGDA and Offset

Simple Test

The PGDA has four gain options (0.8, 0.4, 0.27, and 0.2) selected with the four-position BVGN slide switch. Set the BV_REF switch to the NORM position. Test the PGDA amplifier in the same manner as PGIA. Apply 1 V dc between TPBVP and TPBVN. Measure the output voltages at TPBVMEA. The output voltages are 0.8 V, 0.4 V, 0.27 V, and 0.2 V, respectively, at the four BVGN switch positions.

PGDA in an Application

For connection to an application, simply connect the input terminal across the battery. It is good practice to take advantage of the differential input to achieve the most accurate measurements.

PGDA Offset

The BV_REF offset works just the same as the IS_REF except that the fixed offset is 5 mV. Simply use the BV_REF switch to select the option. For an external offset reference, move the BV_REF switch to EXT and connect a wire from the TPBREFL and TPBREFH test loops to the desired reference points.

Overload Comparators

The AD8450 features identical fault sensing comparators for overcurrent (OCPS pin) and overvoltage (OVPS pin) to help protect against battery damage. The reference pins, OVPR and OCPR, are hardwired via 0 Ω resistors, R27 and R28, to the 2.5 V reference. The outputs of the comparators are connected together internally, and are active low in the event of an overdrive of either parameter.

For reference, the sense pins are set at 20% greater than the reference. For other sense voltage ratios, simply calculate a new value for the resistor divider. The 2.49 kΩ resistor was selected as an easy equivalent to the 2.5 V reference, the 499 Ω resistors to the ISMEA and BVMEA as 20% greater. These values were selected for an experimental 1 A charge/discharge system built in the lab. Other ratios and values are user selected.

As a basic test or experiment, simply apply enough voltage at the PGIA or PGDA inputs to exceed 3 V at ISMEA or BVMEA. The FAULT output pin switches from 5 V to 0 V if either input exceeds the sense trigger level.

VSET Buffer

The VSET buffer is a unity gain, voltage follower pin accessible for testing. Apply a voltage up to 5 V at the VSET input, and measure the output at TPVSETBF.

CV and CC Loop Filter Amplifiers

The constant voltage (CV) and constant current (CC) integrators are identical circuits and are the two active integrator elements of the master loop compensation and switching block (see Figure 49). Except for their external connections, the two circuits are identical and are tested in the same way, sequentially. The integrator outputs are analog OR'ed together, creating the V_{CTRL} output to the input of an external pulse-width modulation controller.

As shown in Figure 49, the integrator op amp inputs are called IVE0, IVE1, VVE0, VVE1, and VVP0. The first two letters (IV or VV) signify the constant current or constant voltage integrator. The third letter identifies the noninverting input (P) or the inverting input (E for error input). The final digit (0 or 1) indicates the state of the mode circuit (0 for discharge and 1 for charge). Because the integrators are connected in parallel, a static test of either integrator requires disabling the other by forcing the output to the supply rail, reverse biasing the transistor/diode gate.

CC and CV Integrator Tests

The RUN_TEST1 and RUN_TEST2 switches provide all the circuit switching required to test the integrator. Set RUN_TEST1 to the TEST position and apply 2.5 V to the ISET and VSET inputs; then read 2.5 V at the VCTRL output. Set RUN_TEST2 to TEST_CC, then TEST_CV, and the VCTRL output voltage still measures 2.5 V.

Uncommitted Op Amp

The uncommitted op amp is configured as a follower (R24 is installed between the OAVN pin and the OAVO pin). The input pin, OAVP, is jumper connected to ground via OAVP. To test the uncommitted op amp, simply connect a jumper from TP2.5V and Pin 1 of Jumper OAVP. The output TPOAVO reads 2.5 V.

USING THE AD8450

Except for the power converter and accessories, such as filters and current sensing, the AD8450-EVALZ includes all of the signal path elements necessary to implement a battery charging/forming system (see Figure 59).

The AD8450 is usable with either linear or switch mode power converters. Switching converters typically generate higher noise levels than linear; however, switching converters are the most popular by far because of significantly higher efficiency and lower cost. Regardless of the power converter architecture used, the PID loop must be configured to reflect the phase shift and gain of the power stage. Circuit simulation is helpful with this task.

On the right hand side of Figure 62 are four universal loop compensation circuits. All or part of the circuits are usable for installing fixed components when the AD8450-EVALZ is connected to a battery system for design verification. There are two feedback amplifiers, but four potentially distinctive separate configurations. The types and values of passive components vary according to the power converter and its characteristics.

To use the board for setting up a charging system, replace the 10 kΩ resistors in the feedback (there are no capacitors installed) and connect the measured feedback voltages by installing jumpers RUN1 through RUN5. Remove jumpers TST1 through TST5 and install capacitors associated with the integrator.

SCHEMATIC AND ARTWORK

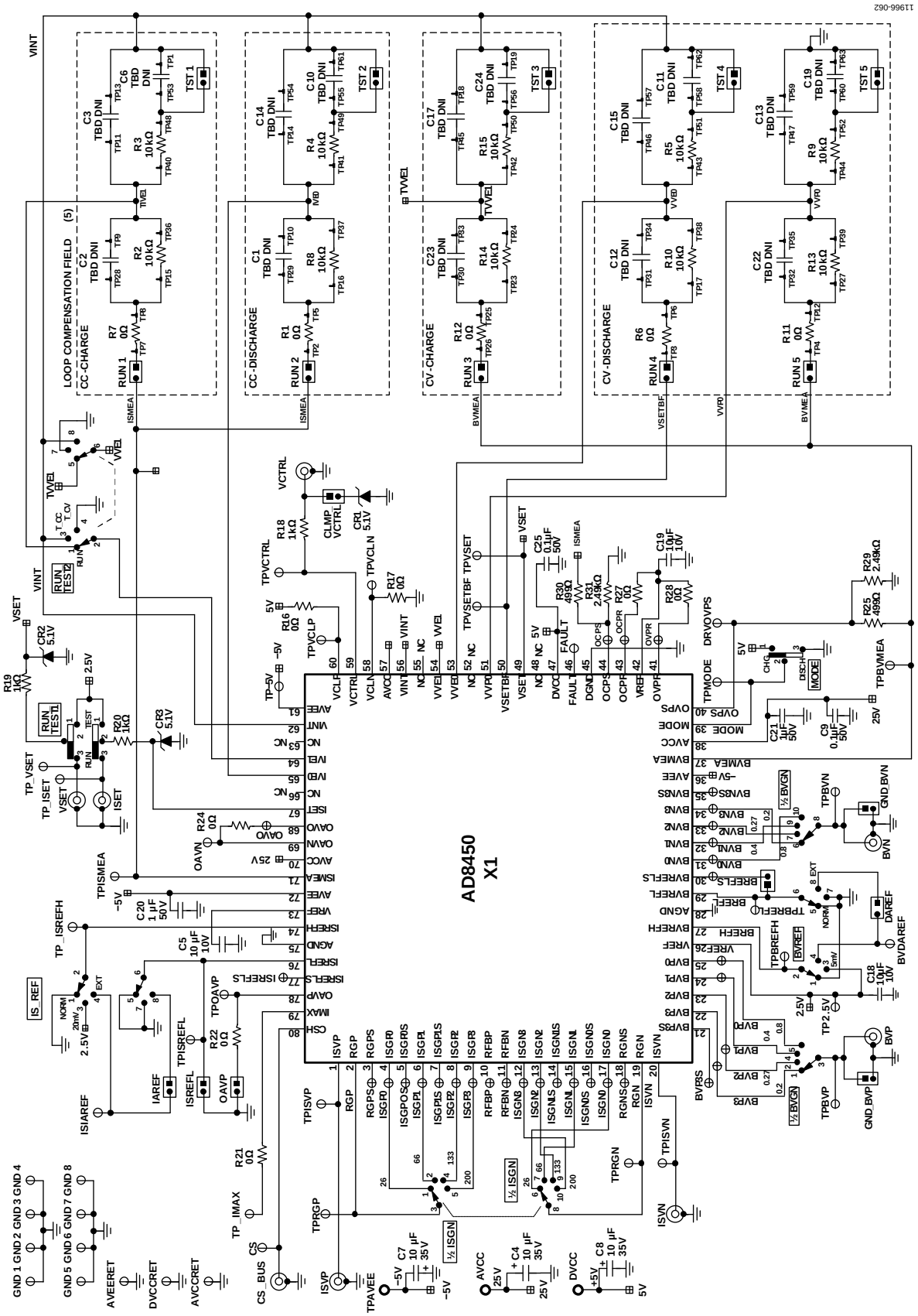

Figure 62. Schematic of the AD8450 Evaluation Board

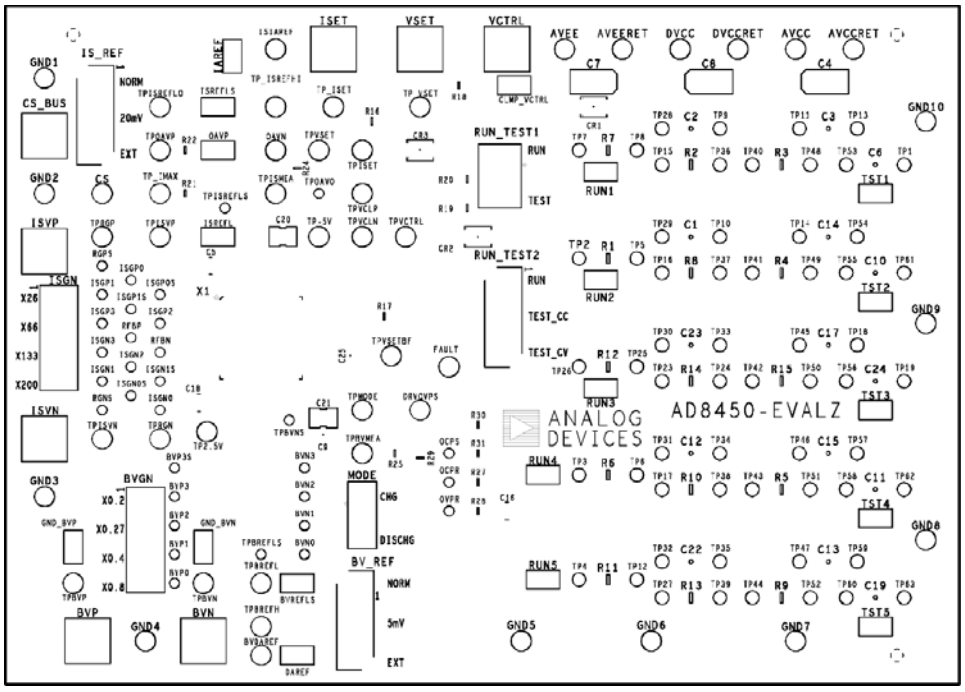

Figure 63. Top Silkscreen of the AD8450-EVALZ

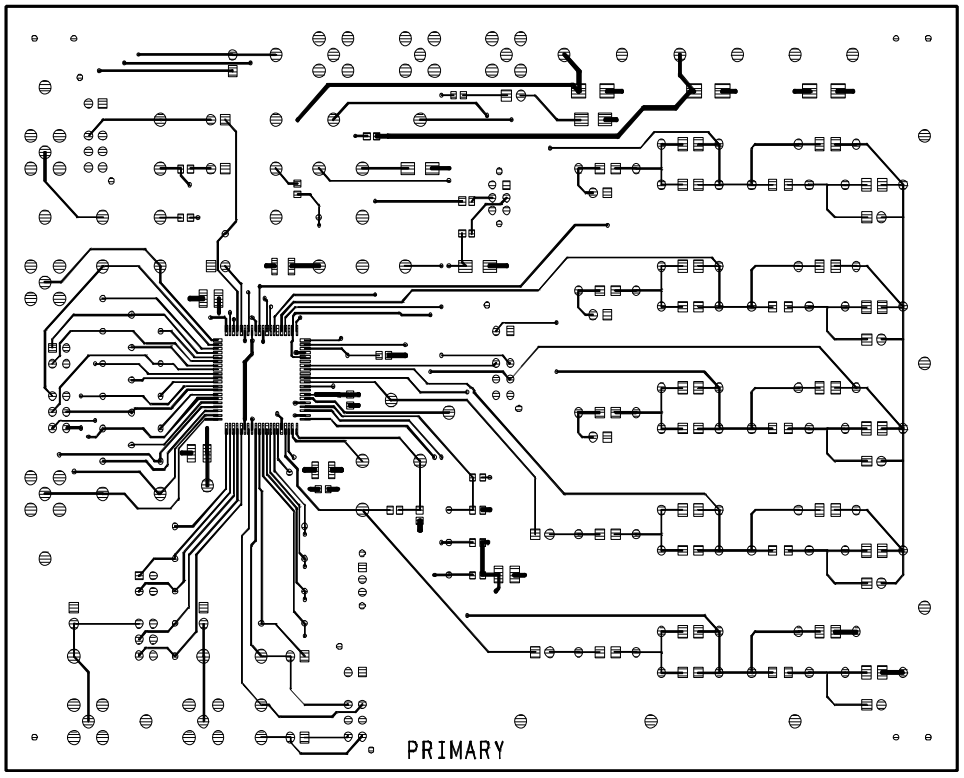

Figure 64. AD8450-EVALZ Primary Side Copper

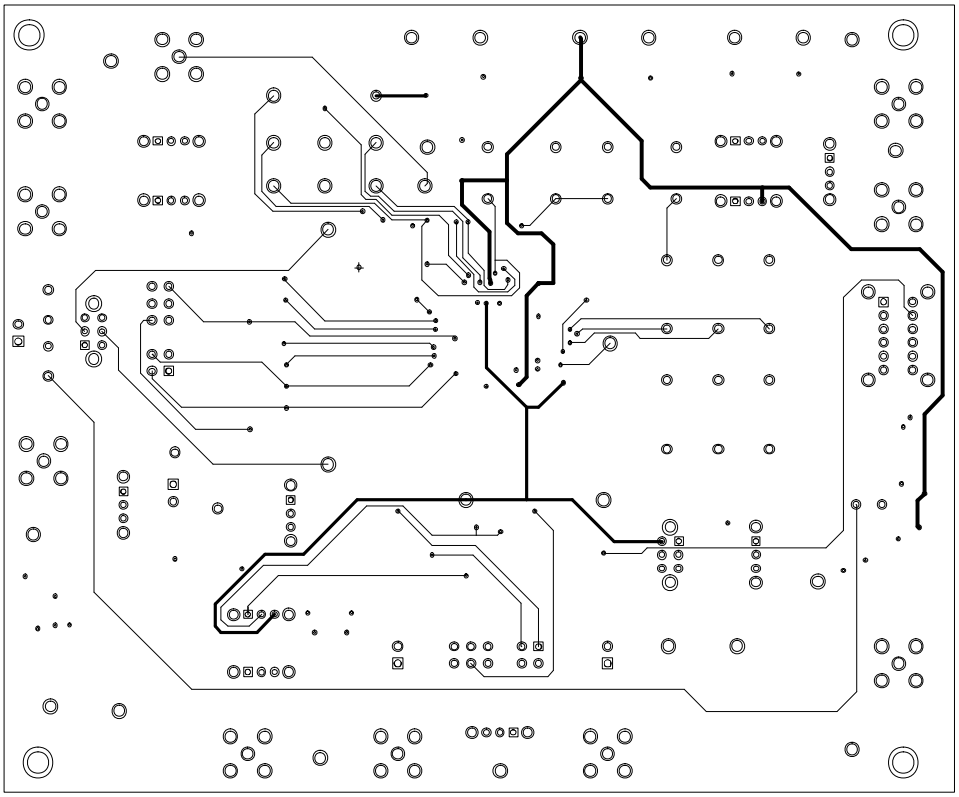

Figure 65. AD8450-EVALZ Secondary Side Copper

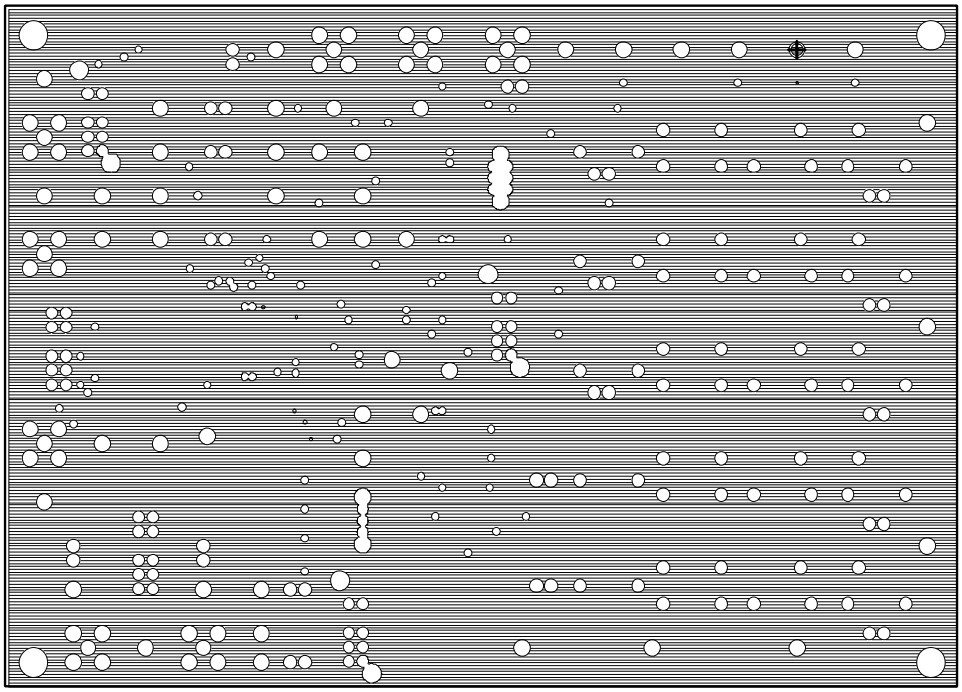

Figure 66. AD8450-EVALZ Power Plane

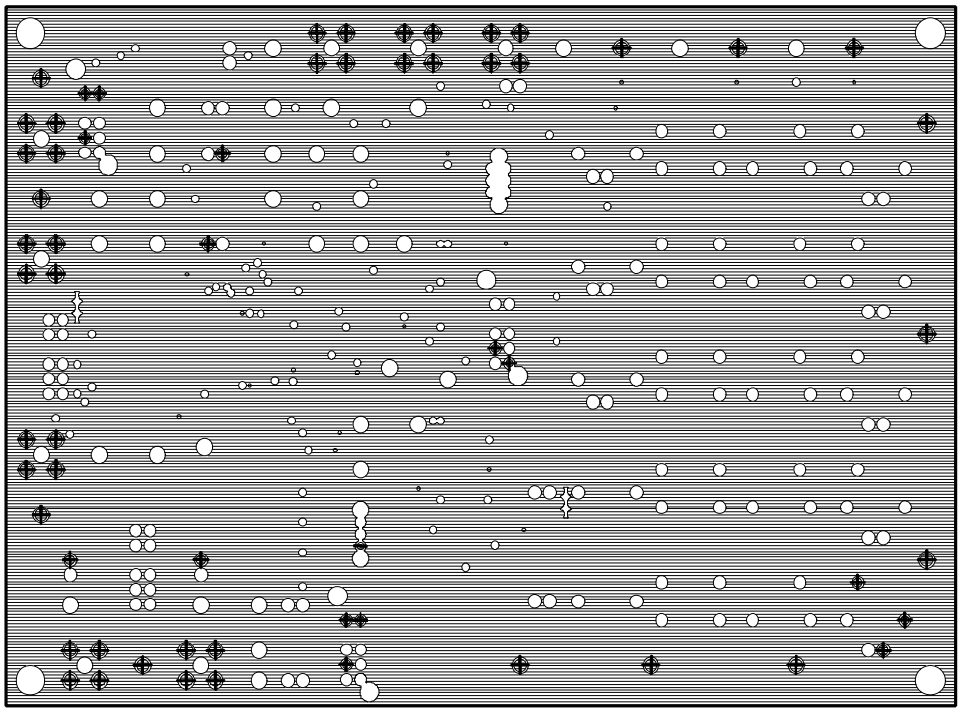

Figure 67. AD8450-EVALZ Ground Plane

OUTLINE DIMENSIONS

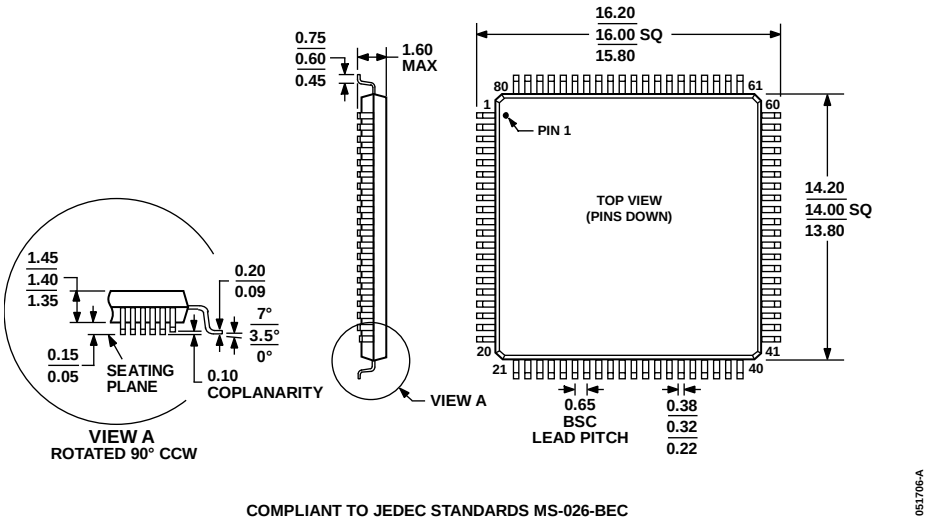

Figure 68. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8450ASTZ	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2
AD8450ASTZ-RL	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2
AD8450-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.