# 3 mW, 100 kSPS, 14-Bit ADC in 6-Lead SOT-23

# AD7940

## FEATURES

- Fast throughput rate: 100 kSPS
- Specified for $V_{DD}$ of 2.5 V to 5.5 V
- Low power
  - 4 mW typ at 100 kSPS with 3 V supplies
  - 17 mW typ at 100 kSPS with 5 V supplies
- Wide input bandwidth:
  - 81 dB SINAD at 10 kHz input frequency
- Flexible power/serial clock speed management
- No pipeline delays
- High speed serial interface
  - SPI®/QSPI™/MICROWIRE™/DSP compatible
- Standby mode: 0.5 µA max
- 6-Lead SOT-23 and 8-Lead MSOP packages

## APPLICATIONS

- Battery-powered systems
  - Personal digital assistants
  - Medical instruments
  - Mobile communications
- Instrumentation and control systems
- Remote data acquisition systems

## FUNCTIONAL BLOCK DIAGRAM

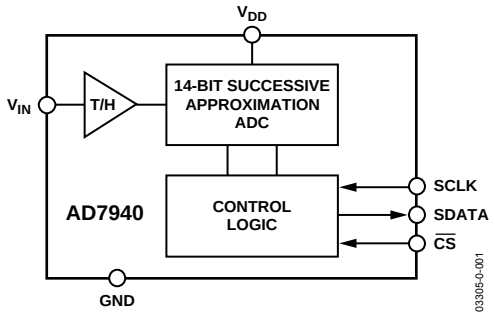


*Figure 1.*

**Table 1. 16-Bit and 14-Bit ADC (MSOP and SOT-23)**

| Type | 100 kSPS | 250 kSPS | 500 kSPS |
|---|---|---|---|
| 16-Bit True Differential | AD7684 | AD7687 | AD7688 |
| 16-Bit Pseudo Differential | AD7683 | AD7685 | AD7686 |
| 16-Bit Unipolar | AD7680 | | |
| 14-Bit True Differential | | AD7944 | AD7947 |
| 14-Bit Pseudo Differential | | AD7942 | AD7946 |
| 14-Bit Unipolar | AD7940 | | |

## GENERAL DESCRIPTION

The AD7940[1] is a 14-bit, fast, low power, successive approximation ADC. The part operates from a single 2.50 V to 5.5 V power supply and features throughput rates up to 100 kSPS. The part contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 7 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point. There are no pipelined delays associated with the part.

The AD7940 uses advanced design techniques to achieve very low power dissipation at fast throughput rates. The reference for the part is taken internally from $V_{DD}$, which allows the widest dynamic input range to the ADC. Thus, the analog input range for this part is 0 V to $V_{DD}$. The conversion rate is determined by the SCLK frequency.

This part features a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

## PRODUCT HIGHLIGHTS

1. First 14-bit ADC in a SOT-23 package.
2. High throughput with low power consumption.
3. Flexible power/serial clock speed management. The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. This allows the average power consumption to be reduced when a power-down mode is used while not converting. The part also features a shutdown mode to maximize power efficiency at lower throughput rates. Power consumption is 0.5 µA max when in shutdown.
4. Reference derived from the power supply.
5. No pipeline delay.

[1]Protected by US. Patent No. 6,681,332.

**Rev. A**


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**8/11—Rev. 0 to Rev. A**

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**7/04—Revision 0: Initial Version**

# SPECIFICATIONS[1]

$V_{DD}$ = 2.50 V to 5.5 V, $f_{SCLK}$ = 2.5 MHz, $f_{SAMPLE}$ = 100 kSPS, unless otherwise noted; $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| Parameter | B Version[1] | Unit | Test Conditions/Comments |
|---|---|---|---|
| DYNAMIC PERFORMANCE | | | $f_{IN}$ = 10 kHz sine wave |
| Signal-to-Noise + Distortion (SINAD)[2] | 81 | dB min | |
| Total Harmonic Distortion (THD)[2] | −98 | dB typ | |
| Peak Harmonic or Spurious Noise (SFDR)[2] | −95 | dB typ | |
| Intermodulation Distortion (IMD)[2] | | | |
| Second-Order Terms | −94 | dB typ | |
| Third-Order Terms | −100 | dB typ | |
| Aperture Delay | 20 | ns max | |
| Aperture Jitter | 30 | ps typ | |
| Full Power Bandwidth | 7 | MHz typ | @ −3 dB |
| | 2 | MHz typ | @ −0.1 dB |
| DC ACCURACY | | | |
| Resolution | 14 | Bits min | $V_{DD}$ = 2.5 V to 4.096 V |
| | 13 | Bits min | $V_{DD}$ > 4.096 V |
| Integral Nonlinearity[2] | ±1 | LSB max | $V_{DD}$ = 2.5 V to 4.096 V |
| | ±2 | LSB max | $V_{DD}$ > 4.096 V |
| Offset Error[2] | ±6 | LSB max | |
| Gain Error[2] | ±8 | LSB max | |
| ANALOG INPUT | | | |
| Input Voltage Ranges | 0 to $V_{DD}$ | V | |
| DC Leakage Current | ±0.3 | µA max | |
| Input Capacitance | 30 | pF typ | |
| LOGIC INPUTS | | | |
| Input High Voltage, $V_{INH}$ | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | 0.4 | V max | $V_{DD}$ = 3 V |
| | 0.8 | V max | $V_{DD}$ = 5 V |
| Input Current, $I_{IN}$ | ±0.3 | µA max | Typically 10 nA, $V_{IN}$ = 0 V or $V_{DD}$ |
| Input Capacitance, $C_{IN}$[2, 3] | 10 | pF max | |
| LOGIC OUTPUTS | | | |
| Output High Voltage, $V_{OH}$ | $V_{DD}$ − 0.2 | V min | $I_{SOURCE}$ = 200 µA; $V_{DD}$ = 2.50 V to 5.25 V |
| Output Low Voltage, $V_{OL}$ | 0.4 | V max | $I_{SINK}$ = 200 µA |
| Floating-State Leakage Current | ±0.3 | µA max | |
| Floating-State Output Capacitance[2, 3] | 10 | pF max | |
| Output Coding | Straight (Natural) Binary | | |
| CONVERSION RATE | | | |
| Conversion Time | 8 | µs max | 16 SCLK cycles |
| Track-and-Hold Acquisition Time | 500 | ns max | Full-scale step input |
| | 400 | ns max | Sine wave input ≤ 10 kHz |
| Throughput Rate | 100 | kSPS max | See the Serial Interface section |
| POWER REQUIREMENTS | | | |
| $V_{DD}$ | 2.50/5.5 | V min/V max | |
| $I_{DD}$ | | | Digital $I/P_S$ = 0 V or $V_{DD}$ |
| Normal Mode (Static) | 5.2 | mA max | $V_{DD}$ = 5.5 V; SCLK on or off |
| | 2 | mA max | $V_{DD}$ = 3.6 V; SCLK on or off |
| Normal Mode (Operational) | 4.8 | mA max | $V_{DD}$ = 5.5 V; $f_{SAMPLE}$ = 100 kSPS; 3.3 mA typ |
| | 1.9 | mA max | $V_{DD}$ = 3.6 V; $f_{SAMPLE}$ = 100 kSPS; 1.29 mA typ |
| Full Power-Down Mode | 0.5 | µA max | SCLK on or off. $V_{DD}$ = 5.5 V |
| | 0.3 | µA max | SCLK on or off. $V_{DD}$ = 3.6 V |

| Parameter | B Version[1] | Unit | Test Conditions/Comments |
|---|---|---|---|
| Power Dissipation[4] | | | $V_{DD}$ = 5.5 V |
| Normal Mode (Operational) | 26.4 | mW max | $V_{DD}$ = 5.5 V; $f_{SAMPLE}$ = 100 kSPS |
| | 6.84 | mW max | $V_{DD}$ = 3.6 V; $f_{SAMPLE}$ = 100 kSPS |
| Full Power-Down | 2.5 | μW max | $V_{DD}$ = 5.5 V |
| | 1.08 | μW max | $V_{DD}$ = 3.6 V |

[1] Temperature range for B Version is –40°C to +85°C.
[2] See the Terminology section.
[3] Sample tested at initial release to ensure compliance.
[4] See the Power vs. Throughput Rate section.

# TIMING SPECIFICATIONS

Sample tested at initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of $V_{DD}$) and timed from a voltage level of 1.6 V.

$V_{DD}$ = 2.50 V to 5.5 V; $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 3.**

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | | Unit | Description |
|---|---|---|---|---|
| | 3 V | 5 V | | |
| $f_{SCLK}$[1] | 250 | 250 | kHz min | |
| | 2.5 | 2.5 | MHz max | |
| $t_{CONVERT}$ | 16 × $t_{SCLK}$ | 16 × $t_{SCLK}$ | min | |
| $t_{QUIET}$ | 50 | 50 | ns min | Minimum quiet time required between bus relinquish and start of next conversion |
| $t_1$ | 10 | 10 | ns min | Minimum $\overline{CS}$ pulse width |
| $t_2$ | 10 | 10 | ns min | $\overline{CS}$ to SCLK setup time |
| $t_3$[2] | 48 | 35 | ns max | Delay from $\overline{CS}$ until SDATA three-state disabled |
| $t_4$[2] | 120 | 80 | ns max | Data access time after SCLK falling edge |
| $t_5$ | 0.4 $t_{SCLK}$ | 0.4 $t_{SCLK}$ | ns min | SCLK low pulse width |
| $t_6$ | 0.4 $t_{SCLK}$ | 0.4 $t_{SCLK}$ | ns min | SCLK high pulse width |
| $t_7$ | 10 | 10 | ns min | SCLK to data valid hold time |
| $t_8$[3] | 45 | 35 | ns max | SCLK falling edge to SDATA high impedance |
| $t_{POWER-UP}$[4] | 1 | 1 | µs typ | Power up time from full power-down |

[1] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[2] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.8 V or 2.0 V.
[3] $t_8$ is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, $t_8$, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.
[4] See the Power vs. Throughput Rate section.

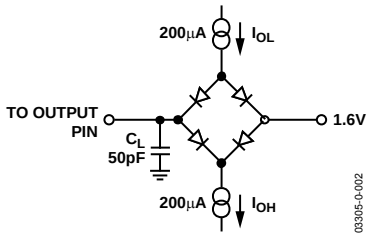


*Figure 2. Load Circuit for Digital Output Timing Specification*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| Analog Input Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to +7 V |
| Digital Output Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Input Current to Any Pin Except Supplies[1] | ±10 mA |
| Operating Temperature Range | |
| Commercial (B Version) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| SOT-23 Package, Power Dissipation | 450 mW |
| $\theta_{JA}$ Thermal Impedance | 229.6°C/W |
| $\theta_{JC}$ Thermal Impedance | 91.99°C/W |
| MSOP Package, Power Dissipation | 450 mW |
| $\theta_{JA}$ Thermal Impedance | 205.9°C/W |
| $\theta_{JC}$ Thermal Impedance | 43.74°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 secs) | 215°C |
| Infared (15 secs) | 220°C |
| ESD | 4 kV |

[1] Transient currents of up to 100 mA will not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

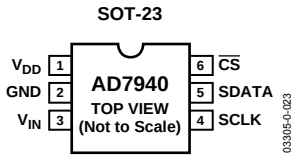


*Figure 3. SOT-23 Pin Configuration*

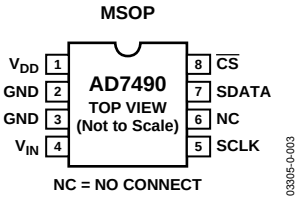


*Figure 4. MSOP Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. SOT-23 | Pin No. MSOP | Mnemonic | Function |
|---|---|---|---|
| 1 | 1 | $V_{DD}$ | Power Supply Input. The $V_{DD}$ range for the AD7940 is from 2.5 V to 5.5 V. |
| 2 | 2, 3 | GND | Analog Ground. Ground reference point for all circuitry on the AD7940. All analog input signals should be referred to this GND voltage. |
| 3 | 4 | $V_{IN}$ | Analog Input. Single-ended analog input channel. The input range is 0 V to $V_{DD}$. |
| 4 | 5 | SCLK | Serial Clock. Logic input. SCLK provides the serial clock for accessing data from this part. This clock input is also used as the clock source for the AD7940's conversion process. |
| 5 | 7 | SDATA | Data Out. Logic output. The conversion result from the AD7940 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7940 consists of two leading zeros followed by 14 bits of conversion data that are provided MSB first. This will be followed by four trailing zeroes if $\overline{CS}$ is held low for a total of 24 SCLK cycles. See the Serial Interface section. |
| 6 | 8 | $\overline{CS}$ | Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7940 and framing the serial data transfer. |
| N/A | 6 | NC | No Connect. This pin should be left unconnected. |

# TERMINOLOGY

**Integral Nonlinearity**
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

**Differential Nonlinearity**
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Offset Error**
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 1 LSB.

**Gain Error**
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., $V_{REF}$ − 1 LSB) after the offset error has been adjusted out.

**Track-and-Hold Acquisition Time**
The track-and-hold amplifier returns to track mode at the end of conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of the conversion. See the Serial Interface section for more details.

**Signal-to-(Noise + Distortion) Ratio**
This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S$/2, excluding dc). The ratio depends on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

*Signal-to-*(*Noise* + *Distortion*) = (6.02 N + 1.76) dB

Thus, for a 14-bit converter, this is 86.04 dB.

**Total Harmonic Distortion (THD)**
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7940, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where $V_1$ is the rms amplitude of the fundamental and $V_2$, $V_3$, $V_4$, $V_5$, and $V_6$ are the rms amplitudes of the second through the sixth harmonics.

**Peak Harmonic or Spurious Noise**
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S$/2, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

**Intermodulation Distortion**
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where *m*, *n* = 0, 1, 2, 3. Intermodulation distortion terms are those for which neither *m* nor *n* are equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa −2fb).

The AD7940 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

# TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5 shows a typical FFT plot for the AD7940 at 100 kSPS sample rate and 10 kHz input frequency. Figure 6 shows the signal-to-(noise + distortion) ratio performance versus the input frequency for various supply voltages while sampling at 100 kSPS with an SCLK of 2.5 MHz.

Figure 7 shows a graph of the total harmonic distortion versus the analog input frequency for various supply voltages, while Figure 8 shows a graph of the total harmonic distortion versus the analog input frequency for various source impedances (see the Analog Input section). Figure 9 and Figure 10 show the typical INL and DNL plots for the AD7940.

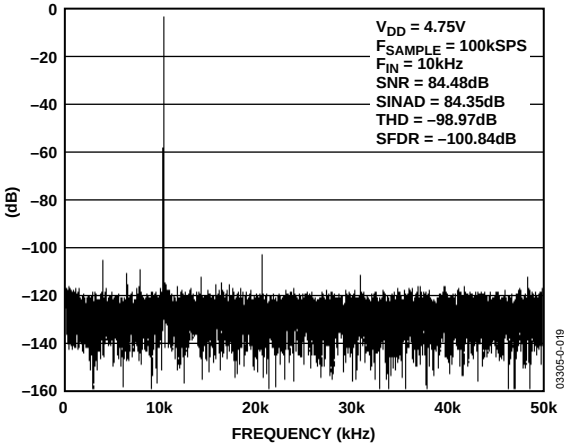


*Figure 5. AD7940 Dynamic Performance at 100 kSPS*

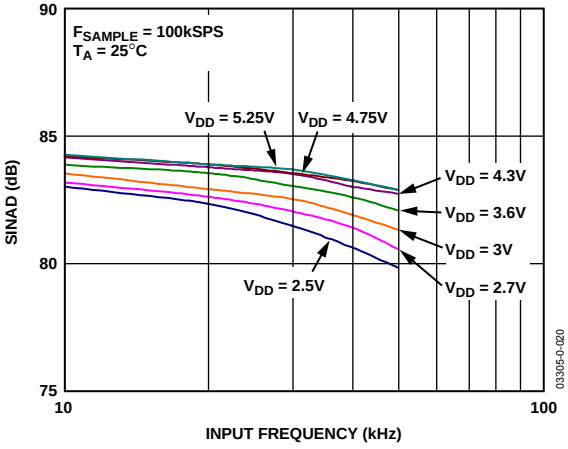


*Figure 6. AD7940 SINAD vs. Analog Input Frequency for Various Supply Voltages at 100 kSPS*

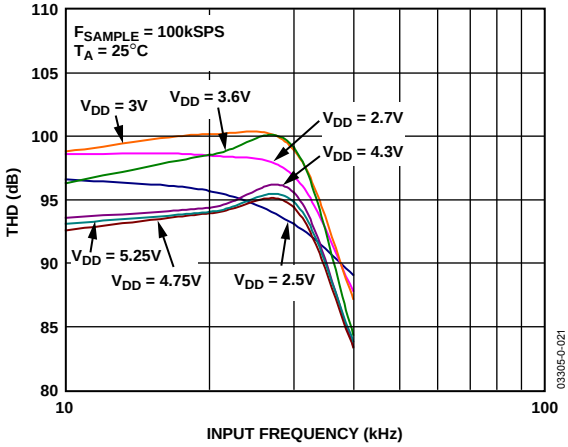


*Figure 7. AD7940 THD vs. Analog Input Frequency for Various Supply Voltages at 100 kSPS*

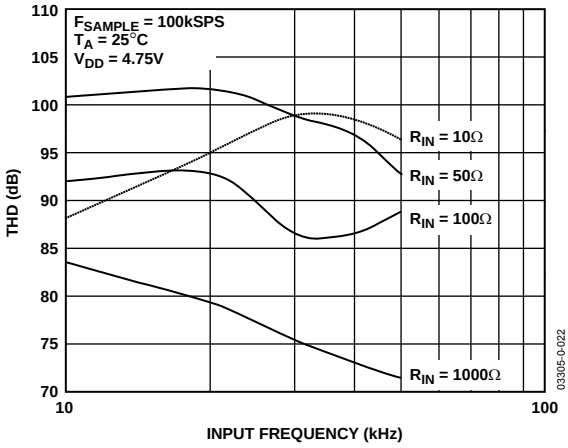


*Figure 8. AD7940 THD vs. Analog Input Frequency for Various Source Impedances*

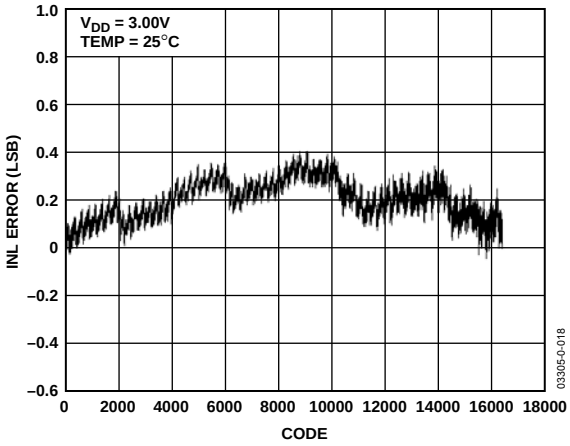


*Figure 9. AD7940 Typical INL*

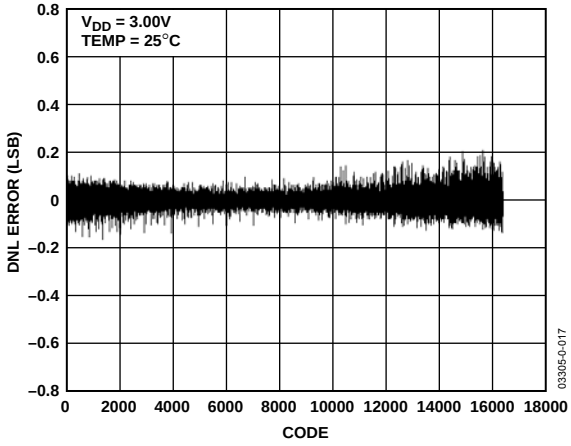


*Figure 10. AD7940 Typical DNL*

# CIRCUIT INFORMATION

The AD7940 is a fast, low power, 14-bit, single-supply ADC. The part can be operated from a 2.50 V to 5.5 V supply. When operated at either 5 V or 3 V supply, the AD7940 is capable of throughput rates of 100 kSPS when provided with a 2.5 MHz clock.

The AD7940 provides the user with an on-chip track-and-hold ADC and a serial interface housed in a tiny 6-lead SOT-23 package or in an 8-lead MSOP package, which offer the user considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the part and also provides the clock source for the successive approximation ADC. The analog input range for the AD7940 is 0 V to $V_{DD}$. An external reference is not required for the ADC nor is there a reference on-chip. The reference for the AD7940 is derived from the power supply and thus gives the widest dynamic input range.

The AD7940 also features a power-down option to save power between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section.

## CONVERTER OPERATION

The AD7940 is a 14-bit, successive approximation ADC based around a capacitive DAC. The AD7940 can convert analog input signals in the 0 V to $V_{DD}$ range. Figure 11 and Figure 12 show simplified schematics of the ADC. The ADC comprises of control logic, SAR, and a capacitive DAC. Figure 11 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on the selected $V_{IN}$ channel.

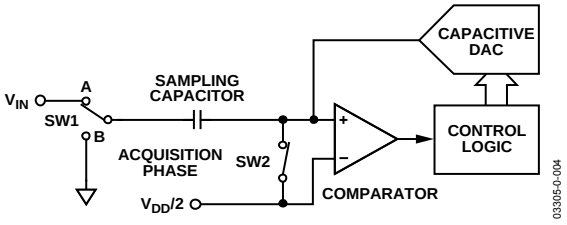


*Figure 11. ADC Acquisition Phase*

When the ADC starts a conversion, SW2 will open and SW1 will move to Position B, causing the comparator to become unbalanced (Figure 12). The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code (see the ADC Transfer Function section).

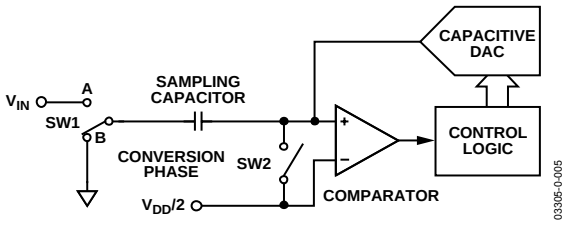


*Figure 12. ADC Conversion Phase*

## ANALOG INPUT

Figure 13 shows an equivalent circuit of the analog input structure of the AD7940. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300 mV. This will cause these diodes to become forward-biased and to start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the part is 10 mA. Capacitor C1 in Figure 13 is typically about 5 pF and primarily can be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a switch (track-and-hold switch). This resistor is typically about 25 Ω. Capacitor C2 is the ADC sampling capacitor and has a capacitance of 25 pF typically. For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application. When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases, and performance will degrade (see Figure 8).

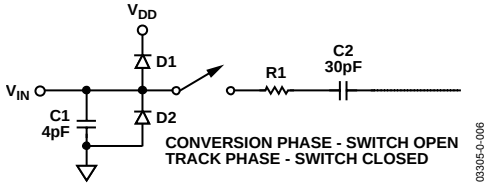


*Figure 13. Equivalent Analog Input Circuit*

# ADC TRANSFER FUNCTION

The output coding of the AD7940 is straight binary. The designed code transitions occur at successive integer LSB values, i.e., 1 LSB, 2 LSBs. The LSB size is $V_{DD}$/16384. The ideal transfer characteristic for the AD7940 is shown in Figure 14.

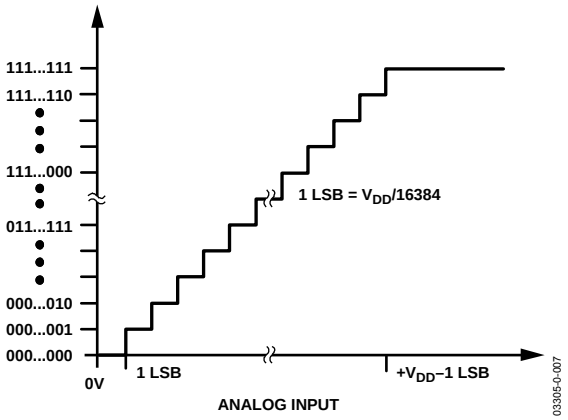


*Figure 14. AD7940 Transfer Characteristic*

## TYPICAL CONNECTION DIAGRAM

Figure 15 shows a typical connection diagram for the AD7940. $V_{REF}$ is taken internally from $V_{DD}$ and as such should be well decoupled. This provides an analog input range of 0 V to $V_{DD}$. The conversion result is output in a 16-bit word. This 16-bit data stream consists of two leading zeros, followed by the 14 bits of conversion data, MSB first. For applications where power consumption is a concern, the power-down mode should be used between conversions or bursts of several conversions to improve power performance (see the Modes of Operation section).

In fact, because the supply current required by the AD7940 is so low, a precision reference can be used as the supply source to the AD7940. For example, a REF19x voltage reference (REF195 for 5 V or REF193 for 3 V) or an AD780 can be used to supply the required voltage to the ADC (see Figure 15). This configuration is especially useful if the power supply available is quite noisy, or if the system supply voltages are at some value other than the required operating voltage of the AD7940, e.g., 15 V. The REF19x or AD780 will output a steady voltage to the AD7940. Recommended decoupling capacitors are a 100 nF low ESR ceramic (Farnell 335-1816) and a 10 µF low ESR tantalum (Farnell 197-130).

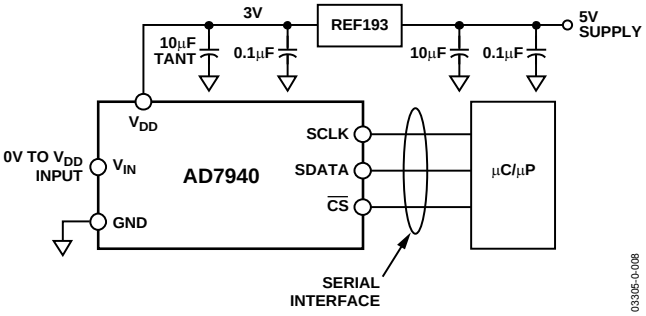


*Figure 15. Typical Connection Diagram*

### *Digital Inputs*

The digital inputs applied to the AD7940 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied can go to 7 V and are not restricted by the $V_{DD}$ + 0.3 V limit as on the analog inputs. For example, if the AD7940 were operated with a $V_{DD}$ of 3 V, 5 V logic levels could be used on the digital inputs. However, it is important to note that the data output on SDATA will still have 3 V logic levels when $V_{DD}$ = 3 V.

Another advantage of SCLK and $\overline{CS}$ not being restricted by the $V_{DD}$ + 0.3 V limit is the fact that power supply sequencing issues are avoided. If one of these digital inputs is applied before $V_{DD}$, there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V were applied prior to $V_{DD}$.

# MODES OF OPERATION

The mode of operation of the AD7940 is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion. There are two possible modes of operation, normal and power-down. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine whether or not the AD7940 will enter power-down mode. Similarly, if already in power-down, $\overline{CS}$ can control whether the device will return to normal operation or remain in power-down. These modes of operation are designed to provide flexible power management options. These options can optimize the power dissipation/throughput rate ratio for differing application requirements.

## NORMAL MODE

This mode provides the fastest throughput rate performance because the user does not have to worry about the power-up times with the AD7940 remaining fully powered all the time. Figure 16 shows the general diagram of the operation of the AD7940 in this mode.

The conversion is initiated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure that the part remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge, but before the 16th SCLK falling edge, the part will remain powered up, but the conversion will be terminated and SDATA will go back into three-state. At least 16 serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{CS}$ may idle high until the next conversion or may idle low until $\overline{CS}$ returns high sometime prior to the next conversion, effectively idling $\overline{CS}$ low.

Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time, $t_{QUIET}$, has elapsed by bringing $\overline{CS}$ low again.

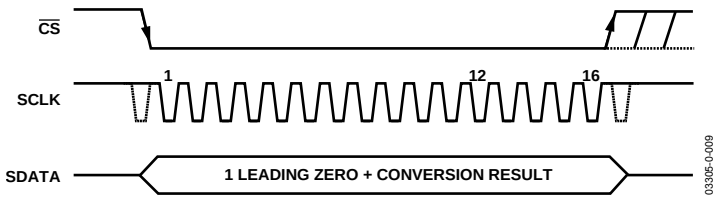


*Figure 16. Normal Mode Operation*

## POWER-DOWN MODE

This mode is intended for use in applications where slower throughput rates are required. Either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate, and then the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7940 is in power-down, all analog circuitry is powered down.

To enter power-down, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK as shown in Figure 17. Once $\overline{CS}$ has been brought high in this window of SCLKs, the part will enter power-down, the conversion that was initiated by the falling edge of $\overline{CS}$ will be terminated, and SDATA will go back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, the part will remain in normal mode and will not power down. This will avoid accidental power-down due to glitches on the $\overline{CS}$ line.

In order to exit this mode of operation and power up the AD7940 again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device will begin to power up and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device will be fully powered up once at least 16 SCLKs (or approximately 6 μs) have elapsed and valid data will result from the next conversion as shown in Figure 18. If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, regardless of the SCLK frequency, the AD7940 will go back into power-down again. This avoids accidental power-up due to glitches on the $\overline{CS}$ line or an inadvertent burst of 8 SCLK cycles while $\overline{CS}$ is low. So although the device may begin to power-up on the falling edge of $\overline{CS}$, it will power down again on the rising edge of $\overline{CS}$ as long as it occurs before the 10th SCLK falling edge.

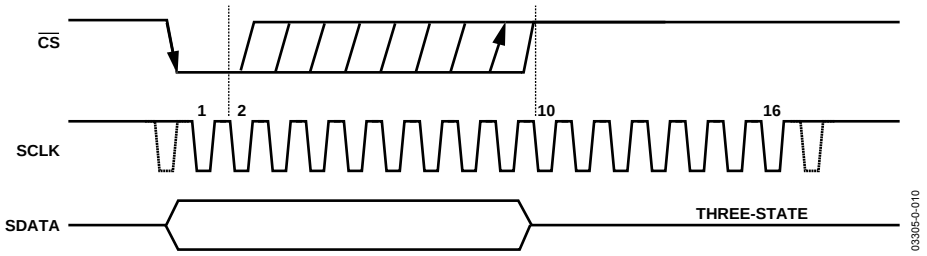


*Figure 17. Entering Power-Down Mode*

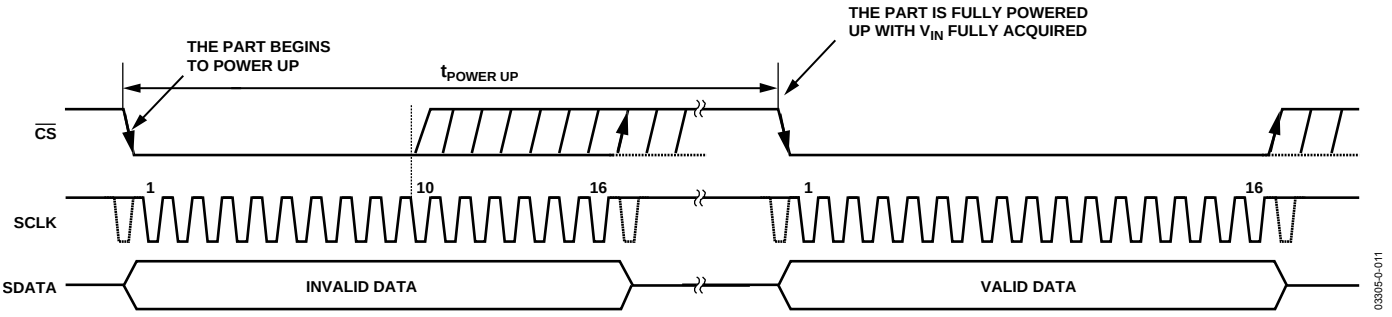


*Figure 18. Exiting Power-Down Mode*

# POWER VS. THROUGHPUT RATE

By using the power-down mode on the AD7940 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 19 shows how as the throughput rate is reduced, the part remains in its shutdown state longer, and the average power consumption over time drops accordingly.

For example, if the AD7940 is operated in a continuous sampling mode, with a throughput rate of 10 kSPS and an SCLK of 2.5 MHz ($V_{DD}$ = 3.6 V), and the device is placed in power-down mode between conversions, the power consumption is calculated as follows. The maximum power dissipation during normal operation is 6.84 mW ($V_{DD}$ = 3.6 V). If the power-up time from power-down is 1 µs, and the remaining conversion time is 6.4 µs, (using a 16 SCLK transfer), then the AD7940 can be said to dissipate 6.84 mW for 7.4 µs during each conversion cycle. With a throughput rate of 10 kSPS, the cycle time is 100 µs. For the remainder of the conversion cycle, 92.6 µs, the part remains in power-down mode. The AD7940 can be said to dissipate 1.08 µW for the remaining 92.6 µs of the conversion cycle. Therefore, with a throughput rate of 10 kSPS, the average power dissipated during each cycle is

$$(7.4/100) \times (6.84 \text{ mW}) + (92.6/100) \times (1.08 \text{ µW}) = 0.51 \text{ mW}$$

Figure 19 shows the power dissipation versus the throughput rate when using the power-down mode with 3.6 V supplies and a 2.5 MHz SCLK.

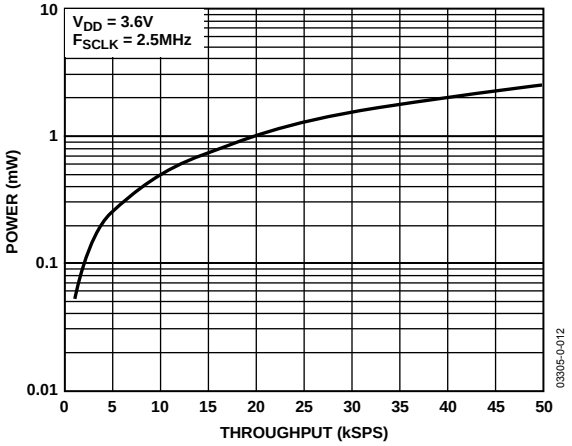


*Figure 19. Power vs. Throughput Using Power-Down Mode at 3.6 V*

# SERIAL INTERFACE

Figure 20 shows the detailed timing diagram for serial interfacing to the AD7940. The serial clock provides the conversion clock and also controls the transfer of information from the AD7940 during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, takes the bus out of three-state, and samples the analog input. The conversion is also initiated at this point and will require at least 16 SCLK cycles to complete. Once 15 SCLK falling edges have elapsed, the track-and-hold will go back into track mode on the next SCLK rising edge as shown in Figure 20 at Point B. On the 16th SCLK falling edge, the SDATA line will go back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion will be terminated and the SDATA line will go back into three-state; otherwise SDATA returns to three-state on the 16th SCLK falling edge as shown in Figure 20.

Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7940. $\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the second leading zero, thus the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. The data transfer will consist of two leading zeros followed by the 14 bits of data. The final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge.

It is also possible to take valid data on each SCLK rising edge rather than falling edge, since the SCLK cycle time is long enough to ensure the data is ready on the rising edge of SCLK. However, the first leading zero will still be driven by the $\overline{CS}$ falling edge, and so it can be taken only on the first SCLK falling edge. It may be ignored, and the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the second leading zero provided and the 15th rising SCLK edge would have DB0 provided. This method may not work with most microcontrollers/DSPs, but could possibly be used with FPGAs and ASICs.

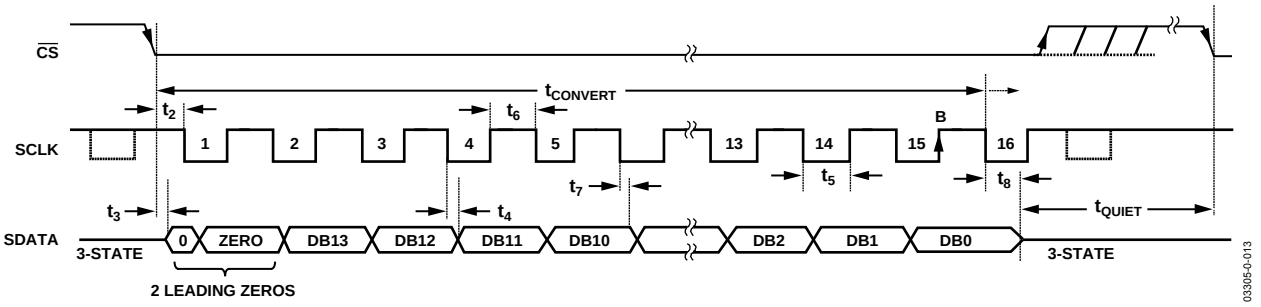


*Figure 20. AD7940 Serial Interface Timing Diagram*

# MICROPROCESSOR INTERFACING

The serial interface on the AD7940 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7940 with some of the more common microcontroller and DSP serial interface protocols.

## AD7940 TO TMS320C541

The serial interface on the TMS320C541 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices such as the AD7940. The $\overline{CS}$ input allows easy interfacing between the TMS320C541 and the AD7940 with no glue logic required. The serial port of the TMS320C541 is set up to operate in burst mode with internal CLKX (TX serial clock) and FSX (TX frame sync). The serial port control register (SPC) must have the following setup:

FO = 0

FSM = 1

MCM = 1

TXM = 1

The format bit, FO, must be set to 1 to set the word length to 8 bits, in order to implement the power-down mode on the AD7940. The connection diagram is shown in Figure 21. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the TMS320C541 provide equidistant sampling.

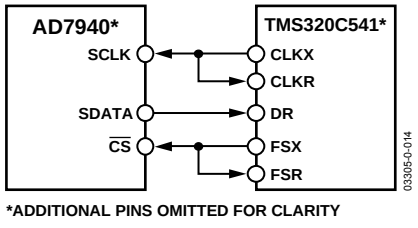


*Figure 21. Interfacing to the TMS320C541*

## AD7940 TO ADSP-218x

The ADSP-218x family of DSPs can be interfaced directly to the AD7940 with no glue logic required. The SPORT control register should be set up as follows:

TFSW = RFSW = 1, Alternate Framing

INVRFS = INVTFS = 1, Active Low Frame Signal

DTYPE = 00, Right Justify Data

SLEN = 1111, 16-Bit Data-Words

ISCLK = 1, Internal Serial Clock

TFSR = RFSR = 0, Frame First Word

IRFS = 0

ITFS = 1

To implement power-down mode, SLEN should be set to 0111 to issue an 8-bit SCLK burst.

The connection diagram is shown in Figure 22. The ADSP-218x has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in alternate framing mode, and the SPORT control register is set up as described. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$, and, as with all signal processing applications, equidistant sampling is necessary. In this example, the timer interrupt is used to control the sampling rate of the ADC.

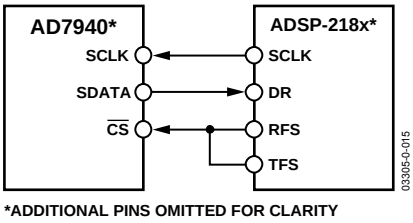


*Figure 22. Interfacing to the ADSP-218x*

The timer register is loaded with a value that provides an interrupt at the required sample interval. When an interrupt is received, the values in the transmit autobuffer start to be transmitted and TFS is generated. The TFS is used to control the
RFS and, therefore, the reading of data. The data is stored in the receive autobuffer for processing or to be shifted later. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given, i.e., TX0 = AX0, the state of the SCLK is checked. The DSP waits until the SCLK has gone high, low, and high before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data may be transmitted, or it may wait until the next clock edge.

For example, if the ADSP-2189 had a 20 MHz crystal, such that it had a master clock frequency of 40 MHz, the master cycle time would be 25 ns. If the SCLKDIV register is loaded with the value 7, then a SCLK of 2.5 MHz is obtained, and 16 master clock periods will elapse for every 1 SCLK period. Depending on the throughput rate selected, if the timer register was loaded with the value 803 (803 + 1 = 804), then 50.25 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in nonequidistant sampling since the transmit instruction is occurring on a SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N, then equidistant sampling will be implemented by the DSP.

## AD7940 TO DSP563xx

The connection diagram in Figure 23 shows how the AD7940 can be connected to the ESSI (synchronous serial interface) of the DSP-563xx family of DSPs from Motorola. Each ESSI (two on board) is operated in synchronous mode (SYN bit in CRB = 1) with internally generated 1-bit clock period frame sync for both Tx and Rx (Bits FSL1 = 0 and FSL0 = 0 in CRB). Normal operation of the ESSI is selected by making MOD = 0 in the CRB. Set the word length to 16 by setting bits WL1 = 1 and WL0 = 0 in CRA. The FSP bit in the CRB should be set to 1 so that the frame sync is negative. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the DSP-563xx provide equidistant sampling.

In the example shown in Figure 23, the serial clock is taken from the ESSI so the SCK0 pin must be set as an output, SCKD = 1.

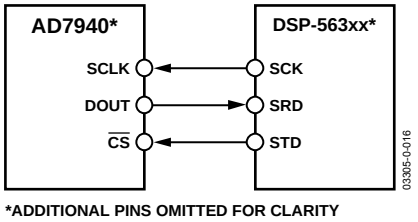


*Figure 23. Interfacing to the DSP-563xx*

# APPLICATION HINTS

## GROUNDING AND LAYOUT

The printed circuit board that houses the AD7940 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes, since it gives the best shielding. Digital and analog ground planes should be joined at only one place. If the AD7940 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7940.

Avoid running digital lines under the device since these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7940 to avoid noise coupling. The power supply lines to the AD7940 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other, which will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while the signals are placed on the solder side.

Good decoupling is also very important. All analog supplies should be decoupled with 10 μF tantalum in parallel with 0.1 μF capacitors to AGND, as discussed in the Typical Connection Diagram section. To achieve the best performance from these decoupling components, the user should attempt to keep the distance between the decoupling capacitors and the $V_{DD}$ and GND pins to a minimum, with short track lengths connecting the respective pins.

## EVALUATING THE AD7940 PERFORMANCE

The recommended layout for the AD7940 is outlined in the evaluation board for the AD7940. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the evaluation board controller. The evaluation board controller can be used in conjunction with the AD7940 evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7940.

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7940. The software and documentation are on a CD shipped with the evaluation board.

# OUTLINE DIMENSIONS

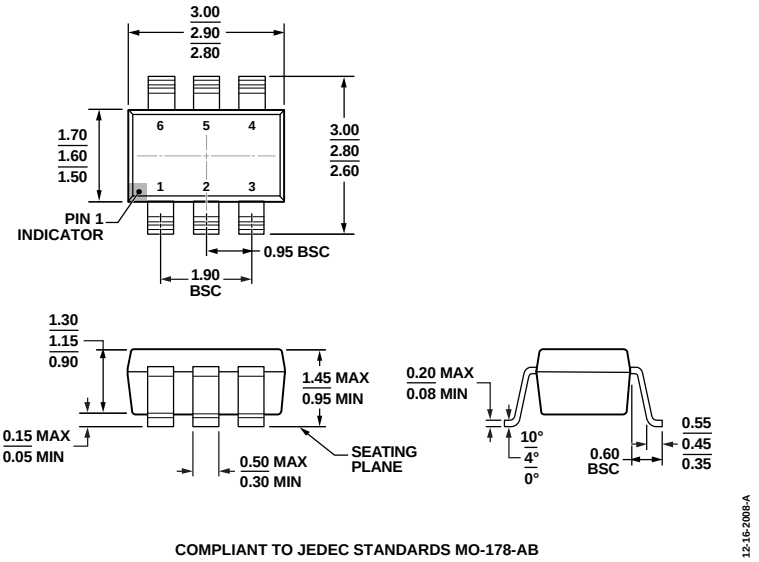


*Figure 24. 6-Lead Small Outline Transistor Package [SOT-23] (RJ-6). Dimensions shown in millimeters*

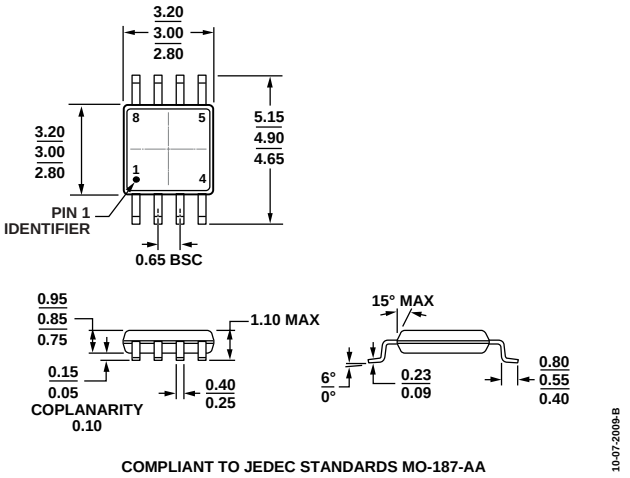


*Figure 25. 8-Lead Mini Small Outline Package [MSOP] (RM-8). Dimensions shown in millimeters*

## ORDERING GUIDE

| Models[1] | Notes | Temperature Range | Linearity Error (LSB)[2] | Package Description | Package Option | Branding |
|---|---|---|---|---|---|---|
| AD7940BRM | | −40°C to +85°C | 14 bits min | Mini Small Outline Package (MSOP) | RM-8 | CRB |
| AD7940BRM-REEL7 | | −40°C to +85°C | 14 bits min | Mini Small Outline Package (MSOP) | RM-8 | CRB |
| AD7940BRMZ | | −40°C to +85°C | 14 bits min | Mini Small Outline Package (MSOP) | RM-8 | C06 |
| AD7940BRMZ-REEL7 | | −40°C to +85°C | 14 bits min | Mini Small Outline Package (MSOP) | RM-8 | C06 |
| AD7940BRJZ-REEL7 | | −40°C to +85°C | 14 bits min | Small Outline Transistor Package (SOT-23) | RJ-6 | C06 |
| EVAL-AD7940CBZ | [3] | | | Evaluation Board | | |
| EVAL-CONTROL BRD2 | [4] | | | Controller Board | | |

[1] Z = RoHS Compliant Part.
[2] Linearity error here refers to no missing codes.
[3] This can be used as a standalone evaluation board or in conjunction with the Evaluation Controller Board for evaluation/demonstration purposes.
[4] This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete evaluation kit, the particular ADC evaluation board needs to be ordered, e.g., EVAL-AD7940CB, the EVAL-CONTROL BRD2, and a 12 V ac transformer. See the Evaluation Board application note for more information.


D03305-0-8/11(A)