Data Sheet

AD5770R

6-Channel, 14-Bit, Current Output DAC with On-Chip Reference, SPI Interface

FEATURES

- 6-channel, current output DAC
- 14-bit resolution
- Programmable output current ranges
  - Channel 0: 0 mA to 300 mA, −60 mA to +300 mA, −60 mA to 0 mA
  - Channel 1: 0 mA to 140 mA, 0 mA to 250 mA
  - Channel 2: 0 mA to 55 mA, 0 mA to 150 mA
  - Channel 3, Channel 4, Channel 5: 0 mA to 45 mA, 0 mA to 100 mA
  - All current sourcing output ranges scale back by up to 0.5×
- 1.25 V, on-chip voltage reference
- Integrated precision reference resistor
- SPI interface
- Reset function
- Output current monitor
- Compliance voltage monitor
- Die temperature monitor
- Integrated thermal shutdown
- 49-ball, 4 mm × 4 mm WLCSP package
- Operating temperature: −40°C to +105°C

APPLICATIONS

- Photonics control
- LED driver programmable current source
- Current mode biasing

GENERAL DESCRIPTION

The AD5770R is a 6-channel, 14-bit resolution, low noise, programmable current output, digital-to-analog converter (DAC) for photonics control applications. The device incorporates a 1.25 V, on-chip voltage reference, a 2.5 kΩ precision resistor for reference current generation, die temperature, output monitoring functions, fault alarm, and reset functions.

The AD5770R contains five 14-bit resolution current sourcing DAC channels and one 14-bit resolution current sourcing and sinking DAC channel.

Channel 0 can be configured to sink up to 60 mA and source up to 300 mA. Channel 1 to Channel 5 have multiple programmable output current sourcing ranges set by register access.

Each DAC operates with a wide power supply rail from 0.8 V to AVDD − 0.4 V for optimizing power efficiency and thermal power dissipation.

The AD5770R operates from a 2.9 V to 5.5 V AVDD supply and is specified over the −40°C to +105°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

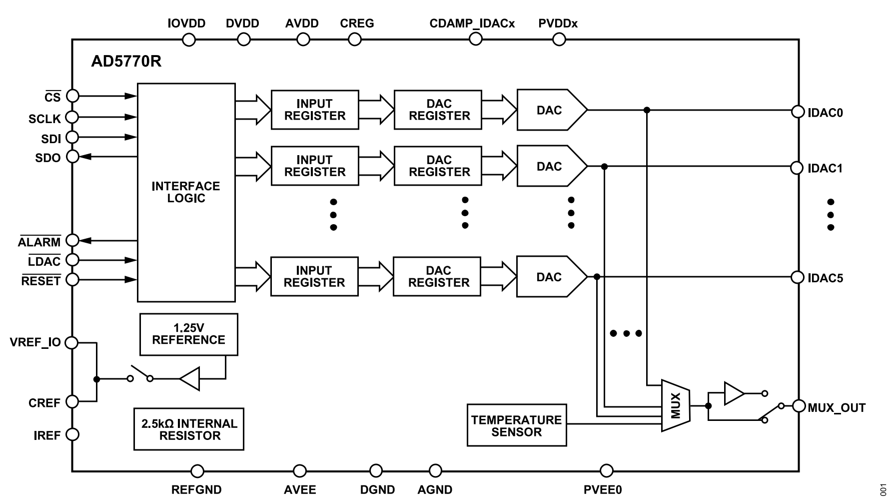

Figure 1.

Rev. B

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1/2023—Rev. A to Rev. B

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SPECIFICATIONS

AVDD = DVDD = 2.9 V to 5.5 V, PVDD = 0.8 V to AVDD − 0.4 V, AVEE = −3.0 V to 0 V, 2.5 V ≤ PVDD − AVEE ≤ 5.5 V, IOVDD = 1.65 V to 5.5 V, AVEE ≤ PVEE0 ≤ 0 V, AVDD − PVEE0 ≤ 5.5 V, VREF = 1.25 V external voltage reference, ambient temperature (T_A) = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE, EXTERNAL R_{SET}[2]					VREF = 1.25 V external voltage reference, assumes ideal 2.5 kΩ external R_{SET} resistor, all channels and all output current ranges
Resolution	14			Bits	
Relative Accuracy (INL)	−6.5		+6.5	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	T_A = −20°C to +105°C, guaranteed monotonic
	−1		+1.2	LSB	Guaranteed monotonic
Total Unadjusted Error	−1.3		+1.3	% full-scale range (FSR)	
Zero-Scale Error			+600	μA	All 0s loaded into the DAC register
Zero-Scale Error Drift		500		nA/°C	Channel 0, Channel 1
		300		nA/°C	Channel 2
		170		nA/°C	Channel 3, Channel 4, Channel 5
Offset Error	−600		+600	μA	
Offset Error Drift		1		μA/°C	Channel 0, Channel 1
		0.5		μA/°C	Channel 2, Channel 3, Channel 4, Channel 5
Full-Scale Error	−1.3		+1.3	% FSR	All 1s loaded into the DAC register
Full-Scale Error Drift		20		ppm/°C	Channel 0, Channel 1
		50		ppm/°C	Channel 2, Channel 3, Channel 4, Channel 5
Gain Error	−1.3		+1.3	% FSR	
Gain Temperature Coefficient		30		ppm/°C	Channel 0, Channel 1
		80		ppm/°C	Channel 2, Channel 3, Channel 4, Channel 5
DC Crosstalk		2		LSB	T_A = 25°C, due to full-scale change in output current on a single adjacent channel
DC Power Supply Rejection Ratio (PSRR)		17		μA/V	T_A = 25°C, DAC register loaded to full scale
STATIC PERFORMANCE, INTERNAL R_{SET}					VREF = 1.25 V internal voltage reference, all channels and all output current ranges
Resolution	14			Bits	
Relative Accuracy (INL)	−6.5		+6.5	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	T_A = −20°C to +105°C, guaranteed monotonic
	−1		+1.2	LSB	Guaranteed monotonic
Total Unadjusted Error (TUE)	−1.3		+1.3	% FSR	
Zero-Scale Error			+600	μA	All 0s loaded into the DAC register
Zero-Scale Error Drift		500		nA/°C	Channel 0, Channel 1
		300		nA/°C	Channel 2
		170		nA/°C	Channel 3, Channel 4, Channel 5
Offset Error	−600		+600	μA	
Offset Error Drift		1		μA/°C	Channel 0, Channel 1
		0.5		μA/°C	Channel 2, Channel 3, Channel 4, Channel 5
Full-Scale Error	−1.3		+1.3	% FSR	All 1s loaded into the DAC register
Full-Scale Error Drift		20		ppm/°C	Channel 0, Channel 1
		50		ppm/°C	Channel 2, Channel 3, Channel 4, Channel 5
Gain Error	−1.3		+1.3	% FSR	
Gain Temperature Coefficient		30		ppm/°C	Channel 0, Channel 1
		80		ppm/°C	Channel 2, Channel 3, Channel 4, Channel 5

SPECIFICATIONS

Table 1. (Continued)

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DC Crosstalk		2		LSB	T_A = 25°C, due to 200 mW change in output power on a single channel
DC PSRR		17		µA/V	T_A = 25°C, DAC register loaded to midscale
OUTPUT CHARACTERISTICS					
Output Current Ranges					
Channel 0	−60		0	mA	
	−60		+300	mA	
	0		300	mA	
Channel 1	0		140	mA	
	0		250	mA	
Channel 2	0		55	mA	
	0		150	mA	
Channel 3, Channel 4, Channel 5	0		45	mA	
	0		100	mA	
Output Compliance Voltage[3]					
Channel 0	0		PVDD0 − 0.45	V	When sourcing in the 0 mA to 300 mA range, DAC register is loaded to full scale
	PVEE0 + 0.5				When sinking current on the −60 mA to 0 mA and the −60 mA to +300 mA ranges, DAC register is loaded to zero scale
Channel 1	0		PVDD1 − 0.275	V	When configured to the 140 mA range with low headroom, DAC register is loaded to full scale
	0		PVDD1 − 0.45	V	When configured to the 250 mA range or to the 140 mA range with low noise, DAC register is loaded to full scale
Channel 2, Channel 3, Channel 4, Channel 5	0		PVDDx − 0.275	V	All output ranges, DAC register loaded to full scale
DC Output Impedance		600		kΩ	T_A = 25°C
VOLTAGE REFERENCE INPUT					
Reference Input Impedance		60		GΩ	T_A = 25°C, external 1.25 V reference option
		115		kΩ	T_A = 25°C, external 2.5 V reference option
Reference Input Range		1.25		V	For specified performance, external 1.25 V reference option
		2.5		V	External 2.5 V reference option
VOLTAGE REFERENCE OUTPUT					
Output Voltage	1.245	1.25	1.255	V	T_A = 25°C, reference output on
Reference Temperature Coefficient		15		ppm/°C	Internal R_{SET} resistor
Output Impedance		0.01		Ω	
Output Current Load Capability		±5		mA	
Maximum Capacitive Load		10		µF	
Load Regulation Sourcing		250		µV/mA	
Load Regulation Sinking		250		µV/mA	
Output Voltage Noise		920		nV rms	T_A = 25°C, 0.1 Hz to 10 Hz
Output Voltage Noise Spectral Density		70		nV/√Hz	T_A = 25°C , 1 kHz
		70		nV/√Hz	T_A = 25°C, 10 kHz
Line Regulation		35		µV/V	T_A = 25°C, due to change in AVDD
INTEGRATED MULTIPLEXER					
Buffer Output Current		±8		mA	
Buffer Output Impedance		0.5		Ω	
Buffer Offset		0.3		mV	

SPECIFICATIONS

Table 1. (Continued)

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Buffer Maximum Capacitive Load		100		pF	
LOGIC INPUTS					$\overline{CS}$, SCLK, SDI, $\overline{LDAC}$, $\overline{RESET}$
Input Current	−3.5		+3.5	μA	Per pin
Input Voltage					
Input Low Voltage (V_{INL})			0.3 × IOVDD	V	
Input High Voltage (V_{INH})	0.7 × IOVDD			V	
Pin Capacitance		4.5		pF	Per pin
LOGIC OUTPUTS					
SDO Pin					
Output Low Voltage (V_{OL})			0.4	V	
Output High Voltage (V_{OH})	IOVDD − 0.4			V	
Floating State Output Capacitance		4		pF	
ALARM Pin					
Output Low Voltage (V_{OL})			0.4	V	Open-drain enabled[4], 10 kΩ pull-up resistor to IOVDD
Output High Voltage (V_{OH})	IOVDD – 0.4			V	Open-drain enabled[4], 10 kΩ pull-up resistor to IOVDD
TEMPERATURE MEASUREMENT DIODE					
Diode Output Voltage		700		mV	T_A = 25°C, internal bias current
		880		mV	T_A = 25°C, 100 μA external bias current
		1.04		V	T_A = 25°C, 200 μA external bias current
Temperature Coefficient		−1.8		mV/°C	Internal bias current
		−1.3		mV/°C	100 μA external bias current
		−0.9		mV/°C	200 μA external bias current
External Bias Current[5]	100		200	μA	Temperature diode bias current is supplied externally
THERMAL ALARMS					
Overheat Warning Temperature		125		°C	Junction temperature, warning flag activated
Overheat Shutdown Temperature		150		°C	Junction temperature, thermal shutdown
Overheat Warning Hysteresis		4		°C	
Overheat Shutdown Hysteresis		20		°C	
POWER REQUIREMENTS					
Analog Power Supply Voltage					
AVDD	2.9		5.5	V	AVDD must be equal to DVDD
AVEE	−3.0		0	V	
PVDD0 to PVDD5	0.8		AVDD − 0.4	V	2.5 V ≤ PVDD − AVEE ≤ 5.5 V
PVEE0	AVEE		0	V	AVDD − PVEE0 ≤ 5.5 V
Analog Power Supply Current					
AVDD Supply Current		32		mA	Internal voltage reference option selected
AVEE Supply Current		−16		mA	
PVDD0 to PVDD5 Supply Current		125		μA	
Digital Power Supply Voltage					
DVDD	2.9		5.5	V	AVDD must be equal to DVDD
IOVDD	1.65		5.5	V	
Digital Power Supply Current					
DVDD Supply Current		1.1		mA	
IOVDD Supply Current		200		nA	
Power Consumption		110		mW	All outputs at 0 A, nominal supplies

[1] See the Terminology section.

SPECIFICATIONS

[2] See the Precision RSET Resistor section for more information about the internal and external R_{SET} resistors.

[3] When sourcing current, the output compliance voltage is the maximum voltage at the IDACx pin, for which the output current is within 0.1% of the measured full-scale range. When sinking current on Channel 0, the output compliance voltage is the minimum voltage at the IDAC0 pin, for which the output current is within 0.1% of the measured zero-scale current.

[4] The active low $\overline{\text{ALARM}}$ pin can be configured as an open drain. Refer to the ALARM section.

[5] The internal temperature sensing diode can be biased with an internal or external current. Refer to the Internal Die Temperature Monitoring section.

AC PERFORMANCE CHARACTERISTICS

AVDD = DVDD = 2.9 V to 5.5 V, PVDD = 0.8 V to AVDD − 0.4 V, AVEE = −3.0 V to 0 V, 2.5 V ≤ PVDD − AVEE ≤ 5.5 V, IOVDD = 1.65 V to 5.5 V, AVEE ≤ PVEE0 ≤ 0 V, AVDD − PVEE0 ≤ 5.5 V, VREF = 1.25 V external voltage reference, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments[2]
DYNAMIC PERFORMANCE					
Output Current Settling Time		13		µs	Zero-scale to full-scale step settling to ±4 LSB, 0 mA to 300 mA range
		10		µs	Zero-scale to full-scale step settling to ±4 LSB, 0 mA to 45 mA range, Channel 3, Channel 4, and Channel 5
Slew Rate		50		mA/µs	Channel 0 , 0 mA to 300 mA range
		10		mA/µs	Channel 3, Channel 4, Channel 5, 0 mA to 45 mA range
Digital-to-Analog Glitch Impulse		0.057		nA-sec	1 LSB change around major carry
Multiplexer Switching Glitch		14		pA-sec	Switching monitored channel
Digital Feedthrough		0.03		nA-sec	
Digital Crosstalk		0.03		nA-sec	
DAC-to-DAC Crosstalk		0.8		nA-sec	Victim Channel 4, due to a 300 mA step change on Channel 0
Output Noise Spectral Density (NSD)		35		nA/√Hz	Channel 0, 0 mA to 300 mA range, at 1 kHz, DAC register loaded to midscale
		18		nA/√Hz	Channel 1, 0 mA to 140 mA low noise range, at 1 kHz, DAC register loaded to midscale
		19		nA/√Hz	Channel 2, 0 mA to 150 mA range, at 1 kHz, DAC register loaded to midscale
		13		nA/√Hz	Channel 3, Channel 4, Channel 5, 0 mA to 100 mA range, at 1 kHz, DAC register loaded to midscale
		16		nA/√Hz	Channel 0, 0 mA to 300 mA range, at 10 kHz, DAC register loaded to midscale
		9		nA/√Hz	Channel 1, 0 mA to 140 mA low noise range, at 10 kHz, DAC register loaded to midscale
		9		nA/√Hz	Channel 2, 0 mA to 150 mA range, at 10 kHz, DAC register loaded to midscale
		6		nA/√Hz	Channel 3, Channel 4, Channel 5, 0 mA to 100 mA range, at 10 kHz, DAC register loaded to midscale
Output Noise		900		nA rms	0.1 Hz to 10 Hz, Channel 0, 0 mA to 300 mA range, DAC register loaded to full scale
		180		nA rms	0.1 Hz to 10 Hz, Channel 1, 0 mA to 140 mA low noise range, DAC register loaded to full scale
		400		nA rms	0.1 Hz to 10 Hz, Channel 2, 0 mA to 150 mA range, DAC register loaded to full scale
		300		nA rms	0.1 Hz to 10 Hz, Channel 3, Channel 4, Channel 5, 0 mA to 100 mA range, DAC register loaded to full scale
PVDDx AC PSRR		−98		dB	100 Hz
		−87		dB	1 kHz
		−67		dB	10 kHz

SPECIFICATIONS

Table 2. (Continued)

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments[2]
		−23		dB	1000 kHz
		−8		dB	3000 kHz

[1] See the Terminology section.

[2] Temperature range is −40°C to +105°C, typically at 25°C.

TIMING SPECIFICATIONS

Table 3.

Parameter	1.65 V ≤ IOVDD ≤ 5.5 V	Unit	Test Conditions/Comments
f_{SCLK}	20	MHz max	SCLK frequency, write operation.
	10	MHz max	SCLK frequency, read operation.
t_1	50	ns min	SCLK cycle time, write operation.
	100	ns min	SCLK cycle time, read operation.
t_2	20	ns min	SCLK high time.
t_3	20	ns min	SCLK low time.
t_4	25	ns min	$\overline{CS}$ to SCLK rising edge setup time.
t_5	10	ns min	Data setup time.
t_6	10	ns min	Data hold time.
t_7	0	ns min	SCLK rising edge to $\overline{CS}$ rising edge. LDAC idle high mode.
t_7[1]	250	ns min	SCLK rising edge to $\overline{CS}$ rising edge. LDAC idle low mode.
t_8	30	ns min	$\overline{CS}$ high time.
t_9	40	ns min	$\overline{CS}$ rising edge to SCLK rising edge.
t_{10}	5	ns min	SCLK rising edge to $\overline{CS}$ falling edge.
t_{11}	90	ns max	SDO data valid from SCLK falling edge.
t_{12}	40	ns min	$\overline{CS}$ rising edge to SDO disabled.
t_{13}	100	ns min	$\overline{LDAC}$ pulse width low.
t_{14}	10	ns min	$\overline{LDAC}$ falling edge to $\overline{CS}$ rising edge.
t_{15}	100	ns min	SCLK rising edge to $\overline{LDAC}$ falling edge.
t_{16}	10	ns min	$\overline{RESET}$ minimum pulse width low.
t_{17}	100	ns max	$\overline{RESET}$ pulse activation time.

[1] $t_7 \geq 250$ ns only applies to the first SCLK rising edge to $\overline{CS}$ rising edge after $\overline{LDAC}_{(IDLE\ LOW)}$ falling edge. $t_7 \geq 0$ ns applies for all other SCLK rising edge to $\overline{CS}$ rising edge. Refer to Figure 3.

Table 4. LDAC Idle Low Timing

Parameter	1.65 V ≤ IOVDD ≤ 5.5 V	Unit	Test Conditions/Comments
t_1	250	ns min	SCLK rising edge to $\overline{CS}$ rising edge. The first SCLK rising edge to $\overline{CS}$ rising edge after $\overline{LDAC}$ idle low falling edge.
t_2	0	ns min	SCLK rising edge to $\overline{CS}$ rising edge.
t_3	10	ns min	$\overline{LDAC}$ falling edge to $\overline{CS}$ rising edge.

SPECIFICATIONS

TIMING DIAGRAMS

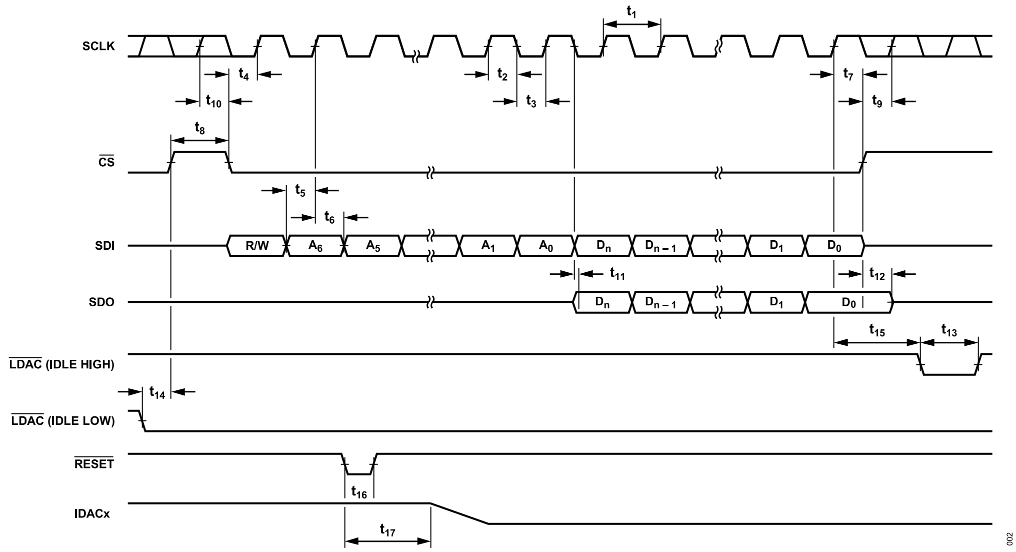


Figure 2. Timing Diagram (Not to Scale)

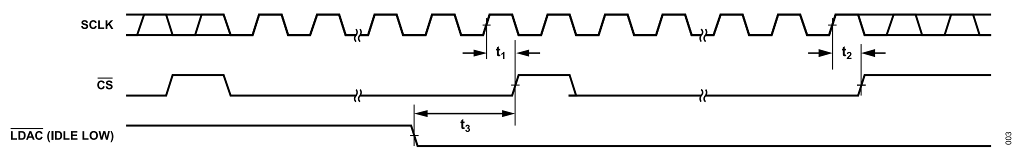


Figure 3. $\overline{LDAC}$ Idle Low Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
AVDD to DVDD	−0.3 V to +0.3 V
AVDD to AGND	−0.3 V to +6.5 V
AVDD to PVDDx	−0.3 V to +6.5 V
AVDD to AVEE	−0.3 V to +10 V
AVEE to AGND	+0.3 V to −3.5 V
PVEE0 to AGND	+0.3 V to −3.5 V
AVEE to PVEE0	−3 .0 V to +0.3 V
PVDDx to AGND	−0.3 V to +6.5 V
PVDDx to AVEE	−0.3 V to +8.5 V
AVDD to PVEE0	−0.3 V to +6.5 V
VREF_IO to AGND	−0.3 V to AVDD + 0.3 V
IDAC0 to PVEE0	−0.3 V to +6.5 V
IDAC1 through IDAC5 to AGND	−0.3 V to PVDDx + 0.3 V
DVDD to DGND	−0.3 V to +6.5 V
IOVDD to DGND	−0.3 V to +6.5 V
REFGND to AGND	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
Digital Inputs to DGND[1]	−0.3 V to IOVDD + 0.3 V
Digital Outputs to DGND[2]	−0.3 V to IOVDD + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature, T_{JMAX}	150°C
Power Dissipation	$(T_{JMAX} – T_A)/\theta_{JA}$
Lead Temperature, Soldering Reflow	260°C, as per JEDEC J-STD-020

[1] Digital inputs include SCLK, SDI, $\overline{\text{RESET}}$, and $\overline{\text{LDAC}}$.

[2] Digital outputs include SDO and $\overline{\text{ALARM}}$.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

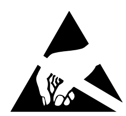
θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
CB-49-5	30[1]	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with 16 thermal vias. See JEDEC JESD51.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

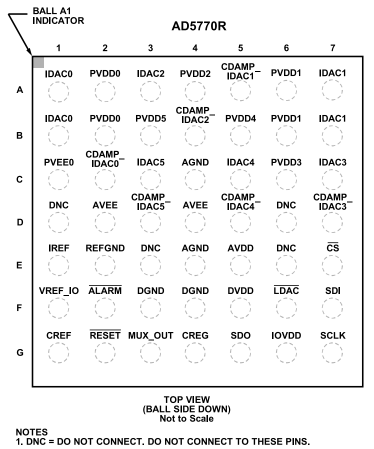


Figure 4. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1, B1	IDAC0	AO	Current Output of Channel 0 is Available on this Pin. Channel 0 sinks up to 60 mA and sources up to 300 mA.
A2, B2	PVDD0	S	Power Supply for IDAC0.
A3	IDAC2	AO	Current Output of Channel 2 is Available on this Pin. Channel 2 sources up to 150 mA.
A4	PVDD2	S	Power Supply for IDAC2.
A5	CDAMP_IDAC1	AI	Damping Capacitor for IDAC1. Connect a 10 nF capacitor between this pin and the PVDD1 supply.
A6, B6	PVDD1	S	Power Supply for IDAC1.
A7, B7	IDAC1	AO	Current Output of Channel 1 is Available on this Pin. Channel 1 sources up to 250 mA.
B3	PVDD5	S	Power Supply for IDAC5.
B4	CDAMP_IDAC2	AI	Damping Capacitor for IDAC2. Connect a 10 nF capacitor between this pin and the PVDD2 supply.
B5	PVDD4	S	Power Supply for IDAC4.
C1	PVEE0	S	Power Supply Return for IDAC0 Sink. When sinking this current on Channel 0, up to 60 mA flows out of PVEE0.
C2	CDAMP_IDAC0	AI	Damping Capacitor for IDAC0. Connect a 10 nF capacitor between this pin and the PVDD0 supply.
C3	IDAC5	AO	Current Output of Channel 5 is Available on this Pin. Channel 5 sources up to 100 mA.
C4, E4	AGND	S	Analog Supply Ground Pin.
C5	IDAC4	AO	Current Output of Channel 4 is Available on this Pin. Channel 4 sources up to 100 mA.
C6	PVDD3	S	Power Supply for IDAC3.
C7	IDAC3	AO	Current Output of Channel 3 is Available on this Pin. Channel 3 sources up to 100 mA.
D1, D6, E3, E6	DNC	DNC	Do Not Connect. Do not connect to this pin.
D2, D4	AVEE	S	Negative Power Supply. AVEE must be between −3 V and 0 V. This pin supplies the low side voltage for biasing some analog circuit blocks.
D3	CDAMP_IDAC5	AI	Damping Capacitor for IDAC5. Connect a 10 nF capacitor between this pin and the PVDD5 supply.
D5	CDAMP_IDAC4	AI	Damping Capacitor for IDAC4. Connect a 10 nF capacitor between this pin and the PVDD4 supply.
D7	CDAMP_IDAC3	AI	Damping Capacitor for IDAC3. Connect a 10 nF capacitor between this pin and the PVDD3 supply.
E1	IREF	AI/O	External Resistor Pin for Reference Current Generation (Optional). When using an external R_{SET} resistor, connect this pin directly to REFGND via a low drift, 2.5 kΩ external resistor.
E2	REFGND	S	Reference Supply Ground Pin. Connect this pin with a low impedance path to AGND. If using an external resistor, the low side of the R_{SET} resistor must be connected to REFGND before the connection to AGND.
E5	AVDD	S	Analog Power Supply. AVDD must be between 2.9 V and 5.5 V. This pin supplies power to the analog circuit blocks on the device. This pin must be at the same potential as DVDD.
E7	$\overline{CS}$	DI	Active Low Control Input. $\overline{CS}$ is used to frame data during a SPI transaction. When $\overline{CS}$ is low, data is transferred on the rising edges of SCLK.
F1	VREF_IO	AI/O	Voltage Reference Input/Output. When the internal reference is enabled, the buffered 1.25 V reference voltage can be made available on this pin. When the internal reference is disabled, an external reference must be applied to this pin. The external reference voltage must be 1.25 V or 2.5 V.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 7. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
F2	$\overline{\text{ALARM}}$	DO	Active Low Output. When $\overline{\text{ALARM}}$ goes low, this alerts the user of a change in the status register. User must read the status register to deassert this pin.
F3, F4	DGND	S	Digital Power Supply Ground.
F5	DVDD	S	Digital Power Supply. DVDD must be between 2.9 V and 5.5 V. This pin supplies power to the digital core and internal oscillator blocks on the device. This pin must be at the same potential as AVDD.
F6	$\overline{\text{LDAC}}$	DI	Logic Input. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data, allowing any or all DAC outputs to update synchronously. Alternatively, this pin can be tied low.
F7	SDI	DI	Serial Data Input. Data to be written to the device is provided on this input and is clocked into the register on the rising edge of SCLK.
G1	CREF	AI/O	Filter Capacitor for Voltage Reference. A 0.1 µF capacitor connected from the CREF pin to AGND is recommended to achieve the specified performance from the AD5770R.
G2	$\overline{\text{RESET}}$	DI	Active Low Reset Input. Tie this pin high for normal operation. Asserting this pin low resets the AD5770R to the default configuration.
G3	MUX_OUT	AI/O	Analog Output. An external analog-to-digital converter (ADC) reads voltages on this pin for diagnostic purposes. Use external excitation current for the temperature sensing diode and force the current on this pin.
G4	CREG	AI/O	Filter Capacitor for Internal Regulator. A 1 µF capacitor connected from the CREG pin to AGND is recommended to achieve the specified performance from the AD5770R.
G5	SDO	DO	Serial Data Output. A read back operation provides data on this output pin as a serial data stream. Data is clocked out on the falling edge of SCLK and is valid on the rising edge of SCLK.
G6	IOVDD	S	Logic Power Supply. IOVDD must be between 1.65 V and 5.5 V. This pin supplies power to the serial interface circuit blocks on the device.
G7	SCLK	DI	Serial Clock Input. Data is clocked into the input shift register on the rising edge of the serial clock input. Data can be transferred at rates up to 20 MHz when writing to the AD5770R. This pin has a maximum speed of 10 MHz when performing a read operation from the AD5770R.

[1] AO is analog output, S is power, AI is analog input, DNC is do not connect, AI/O is analog input and output, DI is digital input, and DO is digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

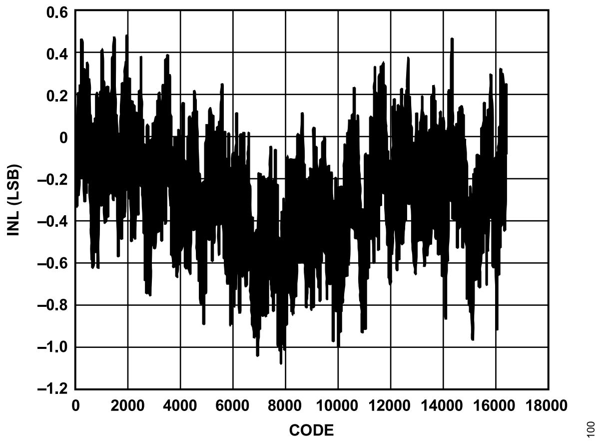


Figure 5. INL Error vs. DAC Code (Channel 0, 0 mA to 300 mA Range)

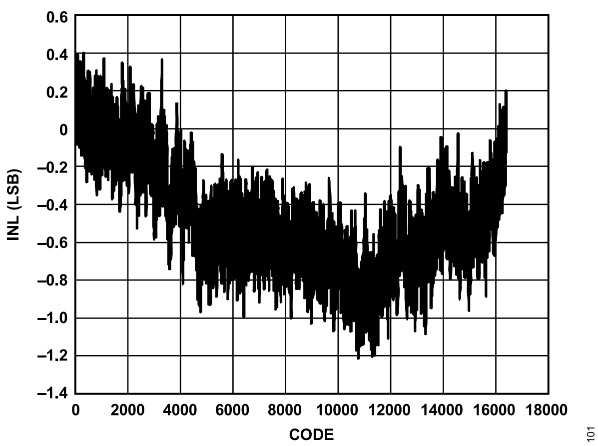


Figure 6. INL Error vs. DAC Code (Channel 1, 0 mA to 250 mA Range)

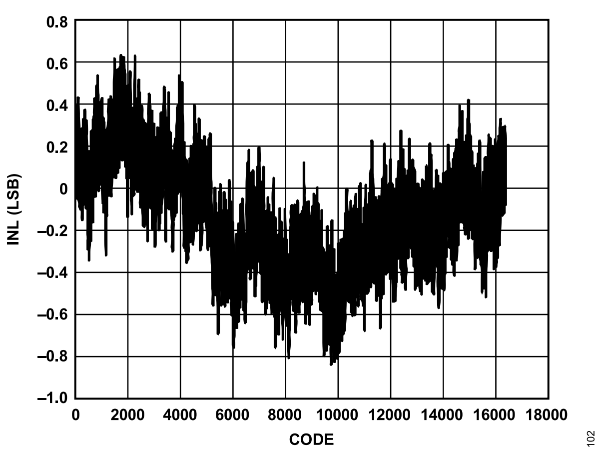


Figure 7. INL Error vs. DAC Code (Channel 2, 0 mA to 150 mA Range)

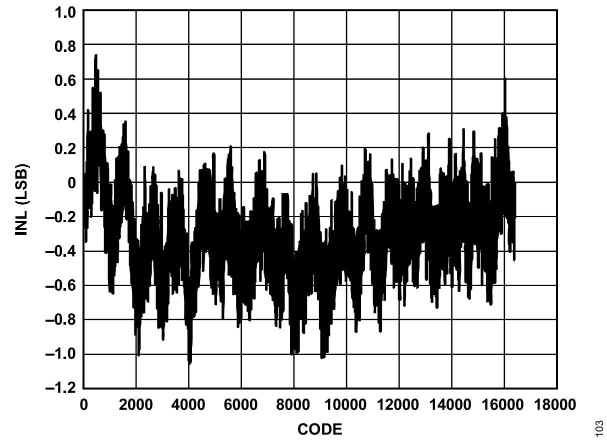


Figure 8. INL Error vs. DAC Code (Channel 3, 0 mA to 100 mA Range)

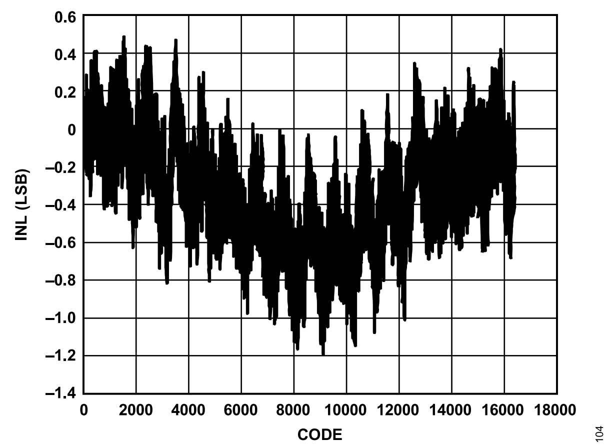


Figure 9. INL Error vs. DAC Code (Channel 4, 0 mA to 100 mA Range)

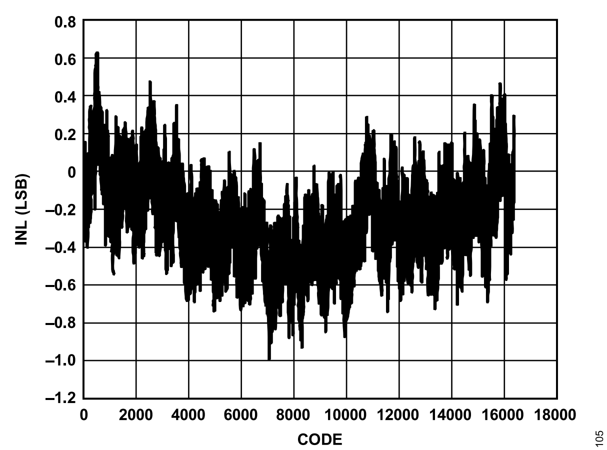


Figure 10. INL Error vs. DAC Code (Channel 5, 0 mA to 100 mA Range)

TYPICAL PERFORMANCE CHARACTERISTICS

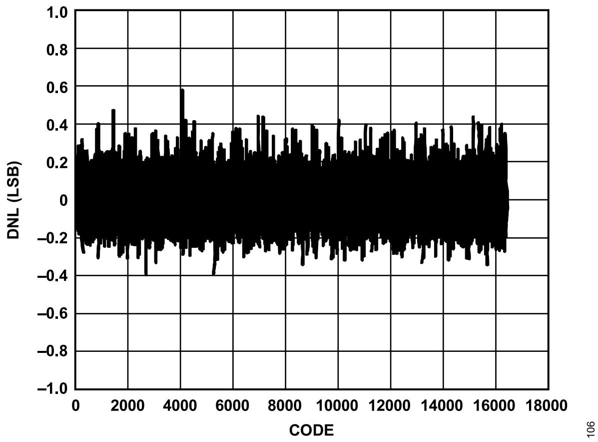


Figure 11. DNL Error vs. DAC Code (Channel 0, 0 mA to 300 mA Range)

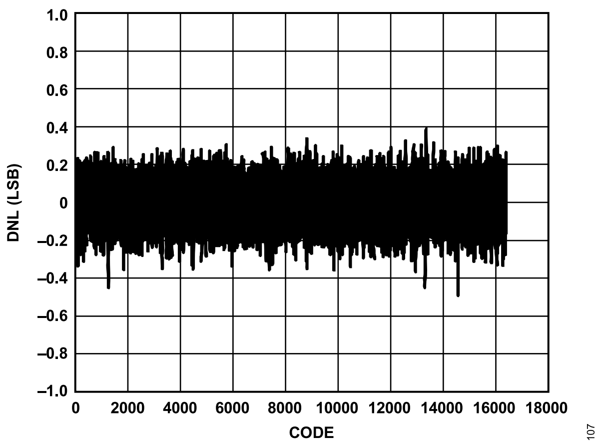


Figure 12. DNL Error vs. DAC Code (Channel 1, 0 mA to 250 mA Range)

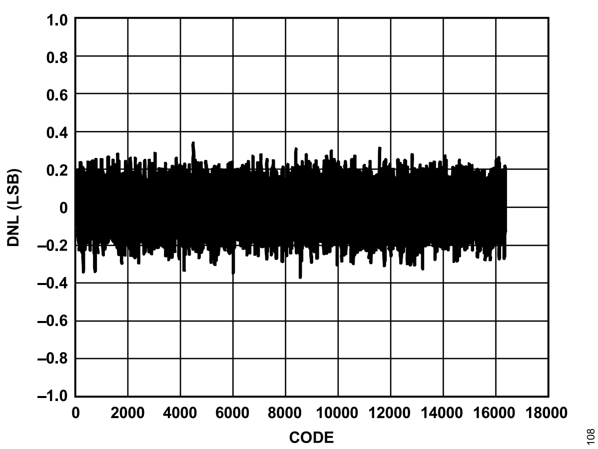


Figure 13. DNL Error vs. DAC Code (Channel 2, 0 mA to 150 mA Range)

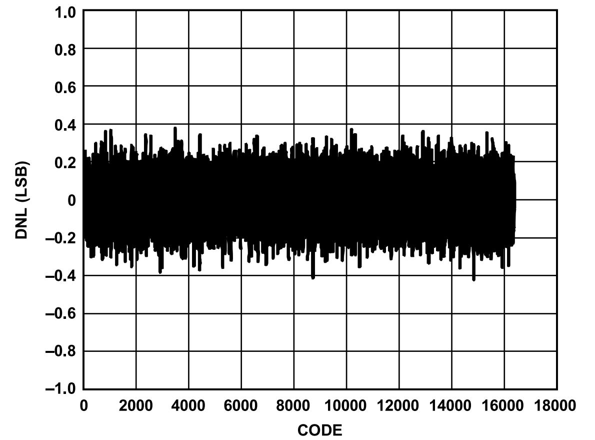


Figure 14. DNL Error vs. DAC Code (Channel 3, 0 mA to 100 mA Range)

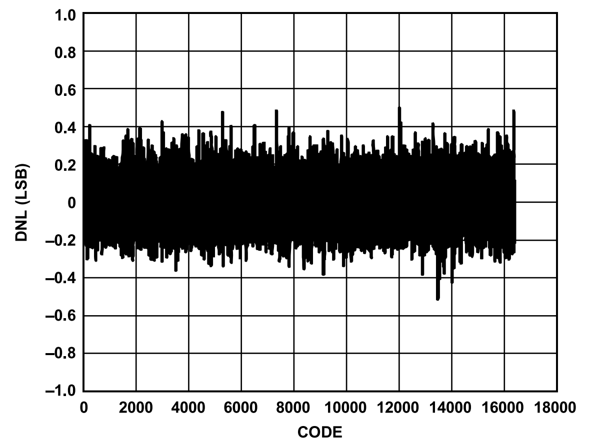


Figure 15. DNL Error vs. DAC Code (Channel 4, 0 mA to 100 mA Range)

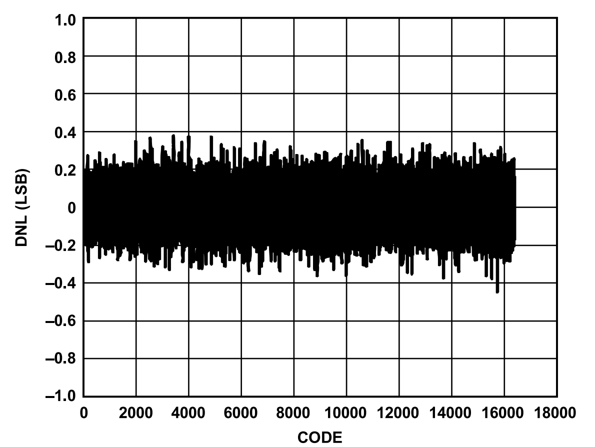


Figure 16. DNL Error vs. DAC Code (Channel 5, 0 mA to 100 mA Range)

TYPICAL PERFORMANCE CHARACTERISTICS

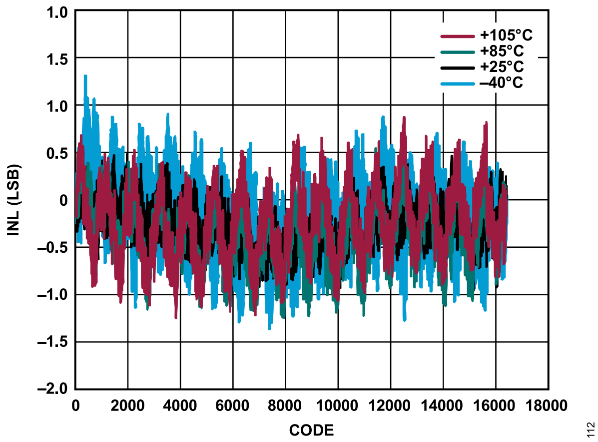


Figure 17. INL Error vs. DAC Code for Various Temperatures (Channel 0, 0 mA to 300 mA Range)

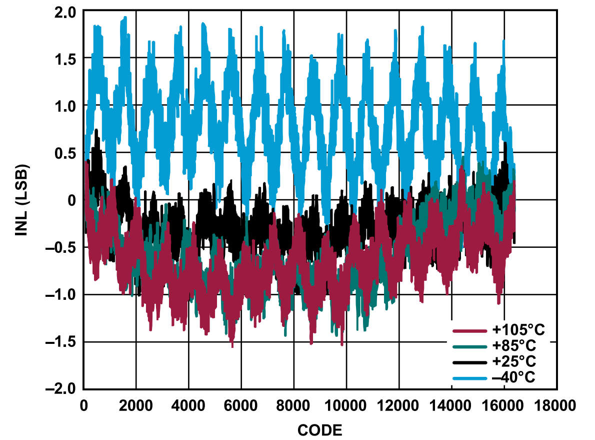


Figure 20. INL Error vs. DAC Code for Various Temperatures (Channel 3, 0 mA to 100 mA Range)

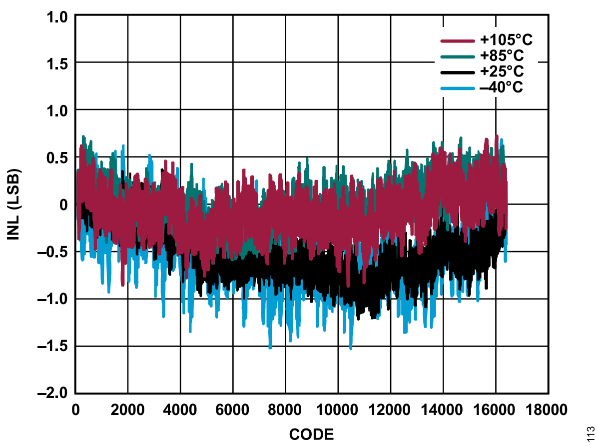


Figure 18. INL Error vs. DAC Code for Various Temperatures (Channel 1, 0 mA to 250 mA Range)

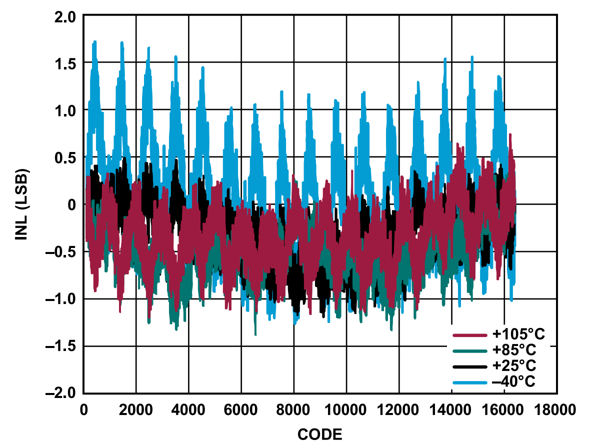


Figure 21. INL Error vs. DAC Code for Various Temperatures (Channel 4, 0 mA to 100 mA Range)

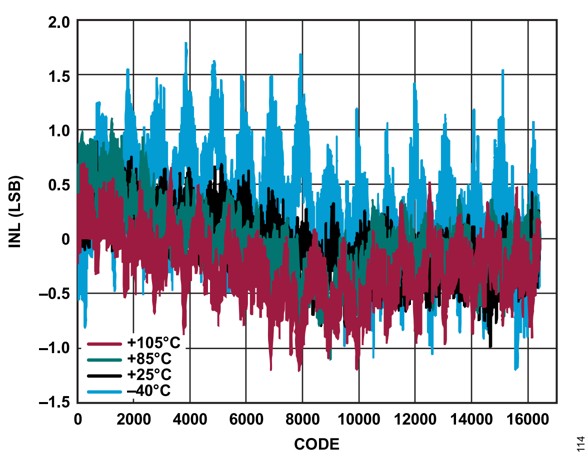


Figure 19. INL Error vs. DAC Code for Various Temperatures (Channel 2, 0 mA to 150 mA Range)

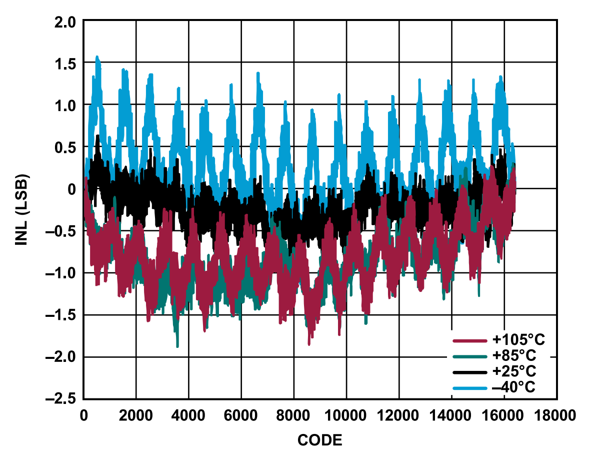


Figure 22. INL Error vs. DAC Code for Various Temperatures (Channel 5, 0 mA to 100 mA Range)

TYPICAL PERFORMANCE CHARACTERISTICS

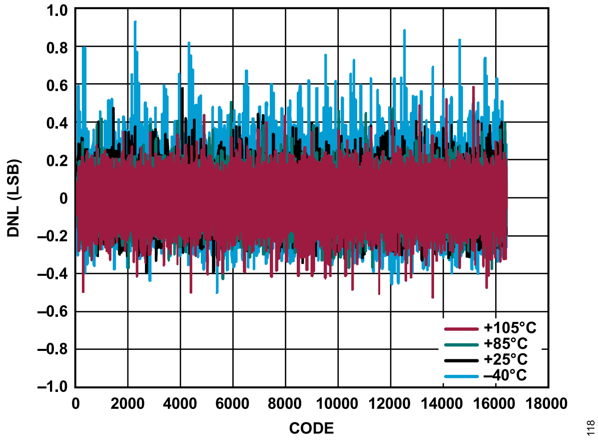


Figure 23. DNL Error vs. DAC Code for Various Temperatures (Channel 0, 0 mA to 300 mA Range)

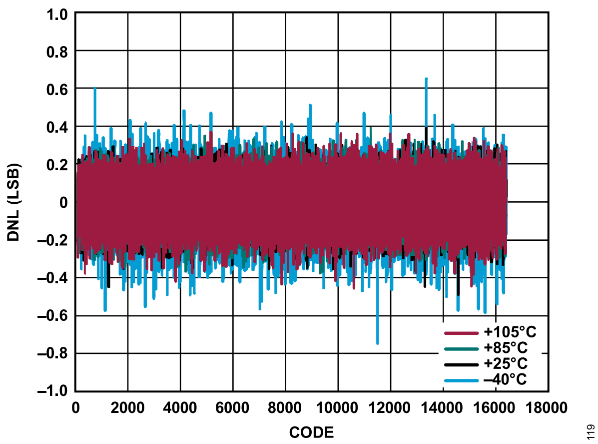


Figure 24. DNL Error vs. DAC Code for Various Temperatures (Channel 1, 0 mA to 250 mA Range)

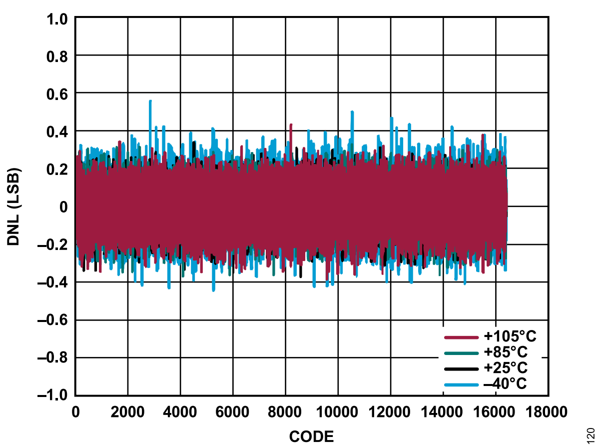


Figure 25. DNL Error vs. DAC Code for Various Temperatures (Channel 2, 0 mA to 150 mA Range)

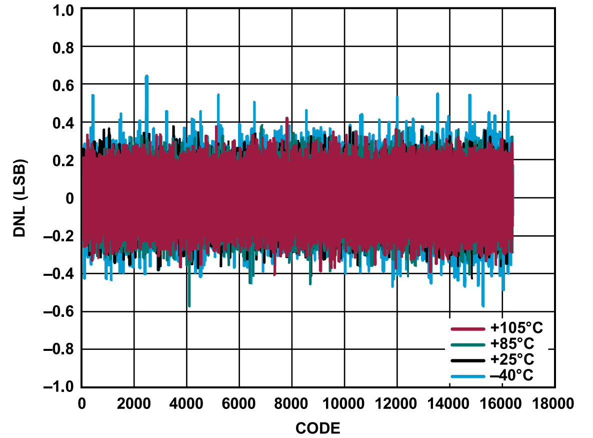


Figure 26. DNL Error vs. DAC Code for Various Temperatures (Channel 3, 0 mA to 100 mA Range)

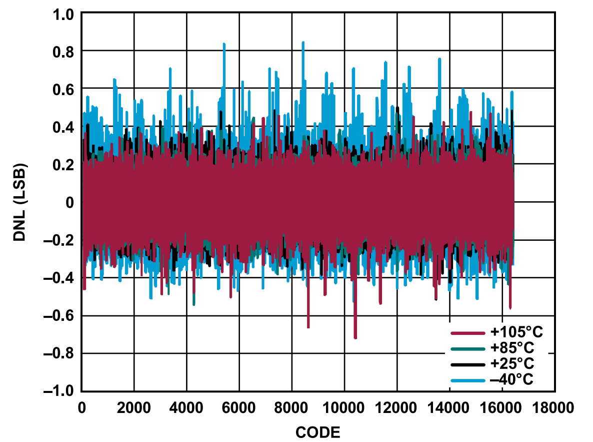


Figure 27. DNL Error vs. DAC Code for Various Temperatures (Channel 4, 0 mA to 100 mA Range)

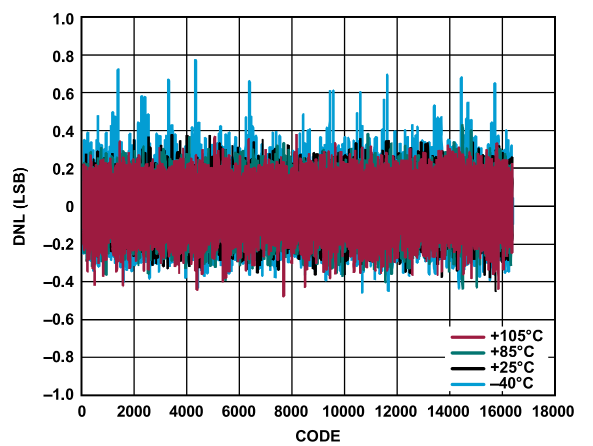


Figure 28. DNL Error vs. DAC Code for Various Temperatures (Channel 5, 0 mA to 100 mA Range)

TYPICAL PERFORMANCE CHARACTERISTICS

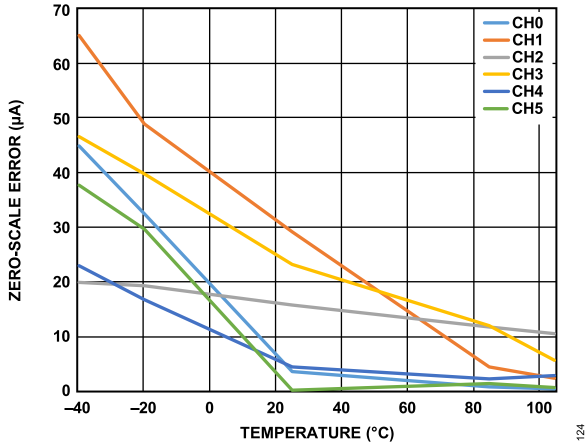


Figure 29. Zero-Scale Error vs. Temperature

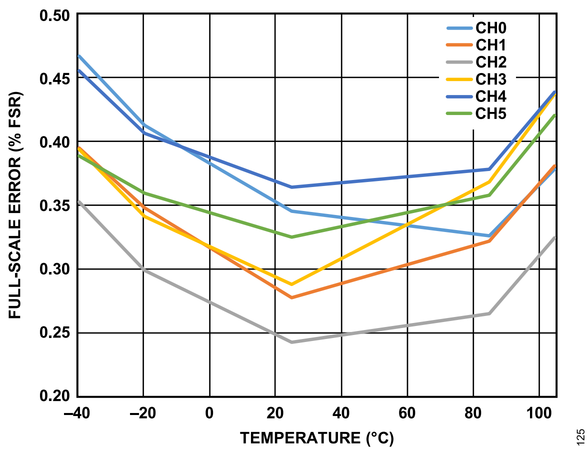


Figure 30. Full-Scale Error vs. Temperature

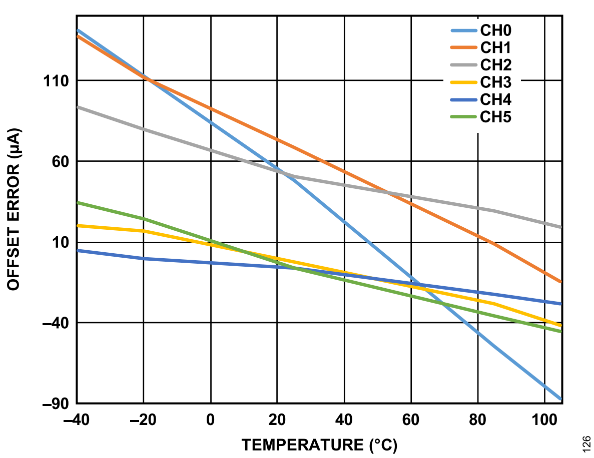


Figure 31. Offset Error vs. Temperature

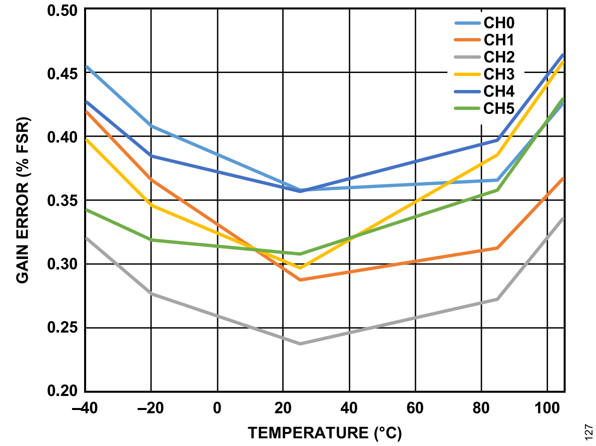


Figure 32. Gain Error vs. Temperature

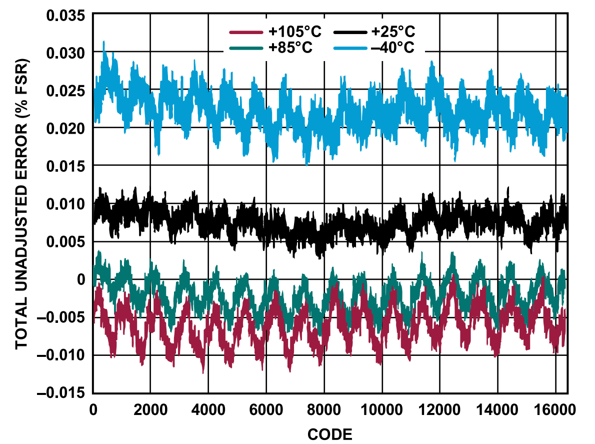


Figure 33. Total Unadjusted Error vs. DAC Code for Various Temperatures (Channel 0, 0 mA to 300 mA Range)

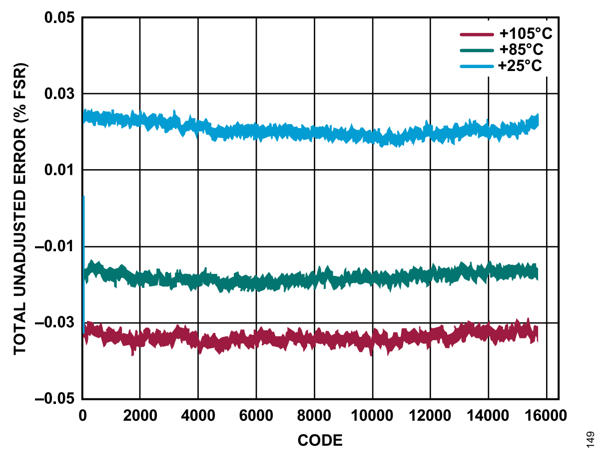


Figure 34. Total Unadjusted Error vs. DAC Code for Various Temperatures (Channel 1, 0 mA to 250 mA Range)

TYPICAL PERFORMANCE CHARACTERISTICS

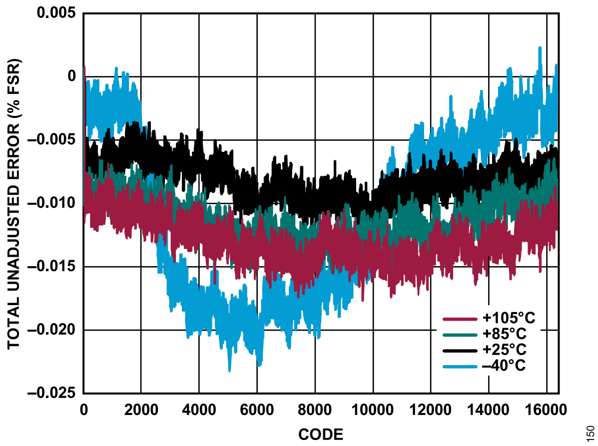


Figure 35. Total Unadjusted Error vs. DAC Code for Various Temperatures (Channel 2, 0 mA to 150 mA Range)

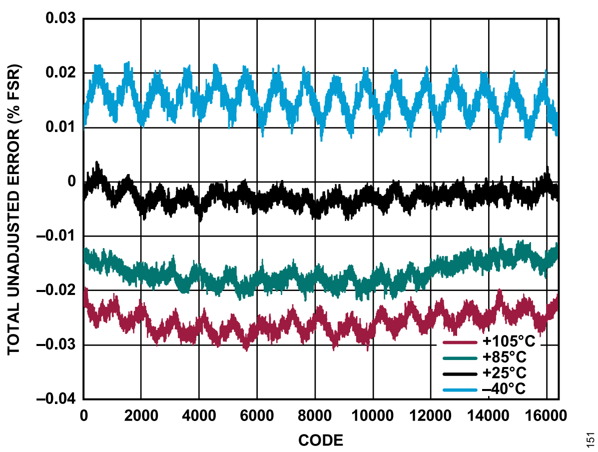


Figure 36. Total Unadjusted Error vs. DAC Code for Various Temperatures (Channel 3, 0 mA to 100 mA Range)

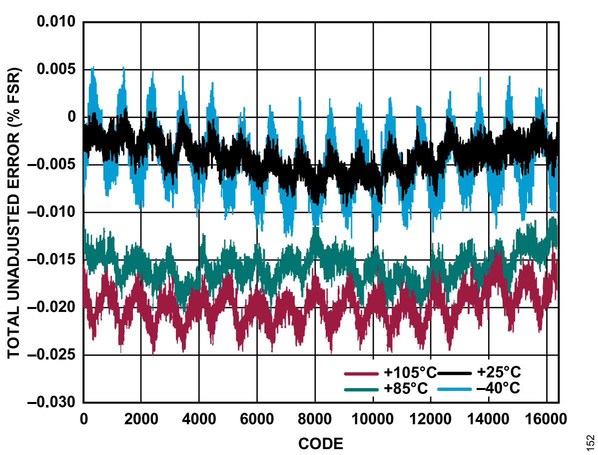


Figure 37. Total Unadjusted Error vs. DAC Code for Various Temperatures (Channel 4, 0 mA to 100 mA Range)

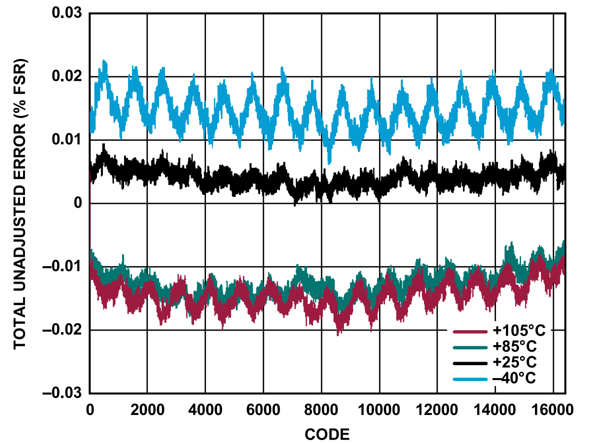


Figure 38. Total Unadjusted Error vs. DAC Code for Various Temperatures (Channel 5, 0 mA to 100 mA Range)

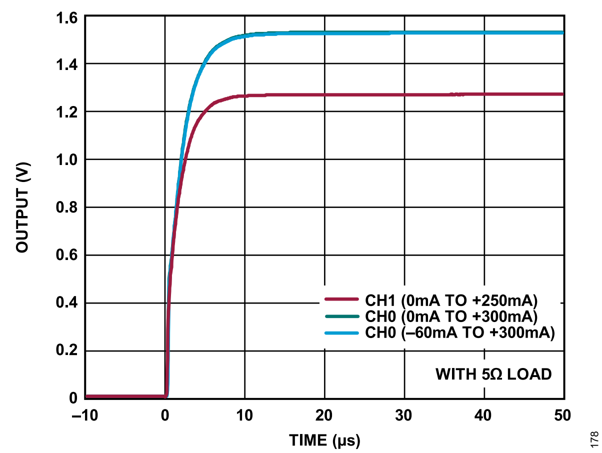


Figure 39. Full-Scale Settling Time (Rising Step)

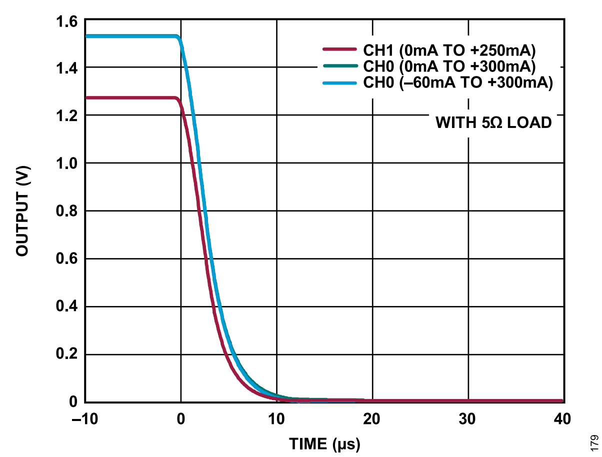


Figure 40. Full-Scale Settling Time (Falling Step)

TYPICAL PERFORMANCE CHARACTERISTICS

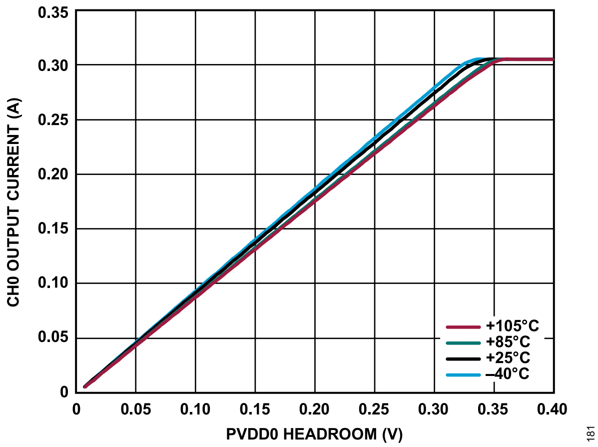


Figure 41. CH0 Output Current vs. PVDD0 Headroom for Various Temperatures

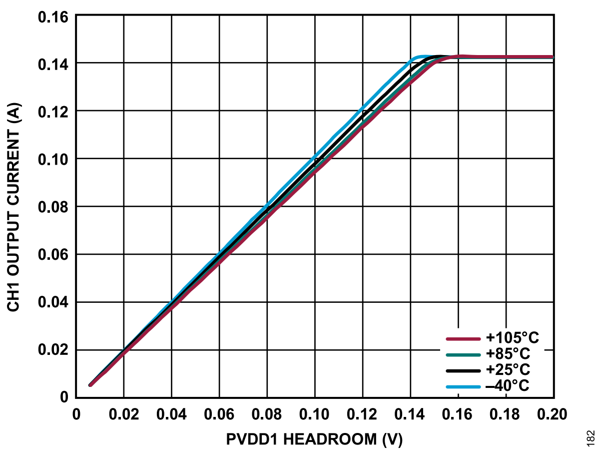


Figure 42. CH1 Output Current vs. PVDD1 Headroom for Various Temperatures

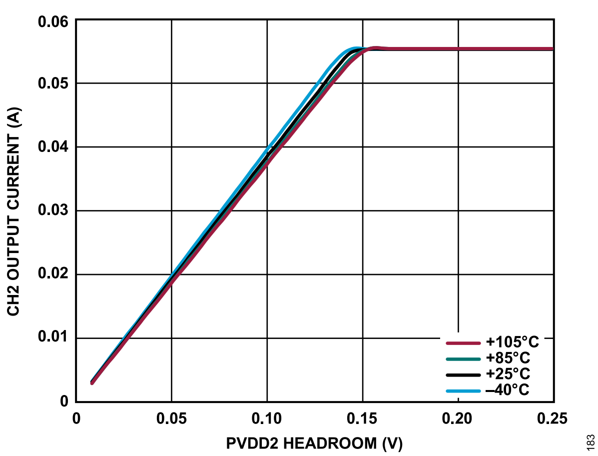


Figure 43. CH2 Output Current vs. PVDD2 Headroom for Various Temperatures

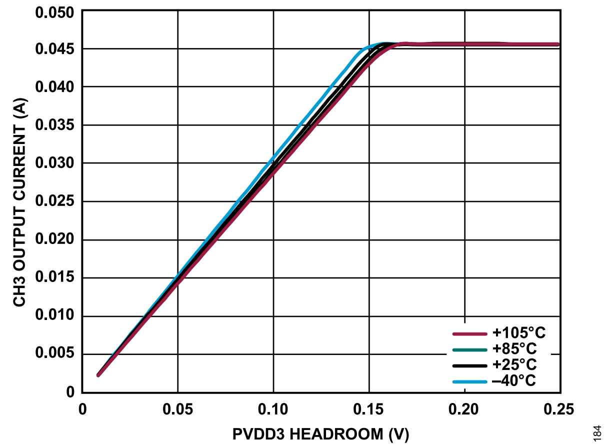


Figure 44. CH3 Output Current vs. PVDD3 Headroom for Various Temperatures

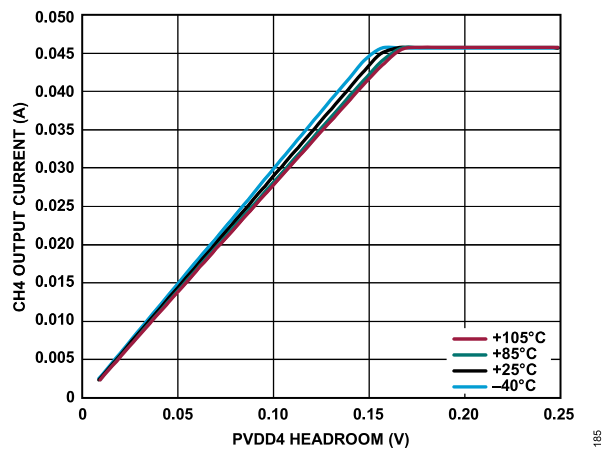


Figure 45. CH4 Output Current vs. PVDD4 Headroom for Various Temperatures

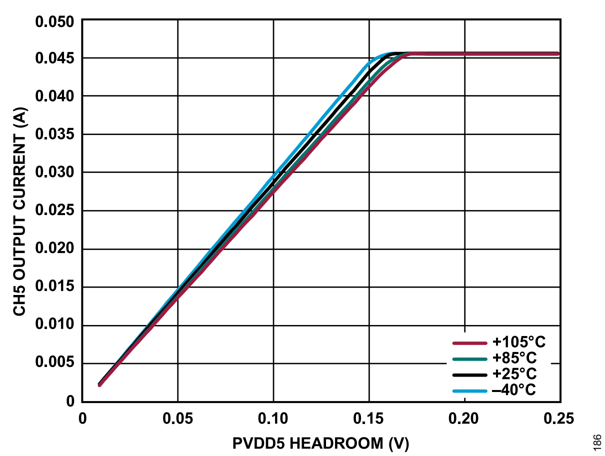


Figure 46. CH5 Output Current vs. PVDD5 Footroom for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

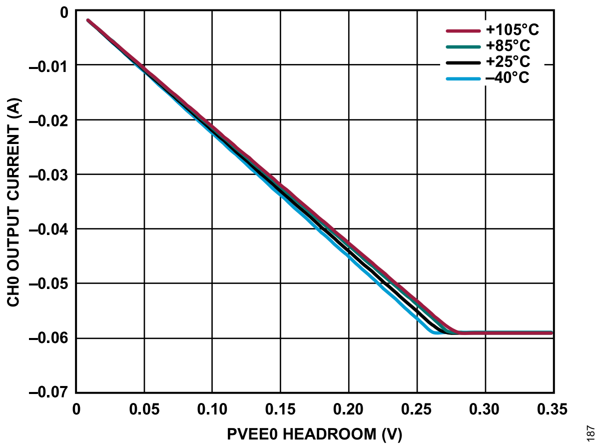


Figure 47. CH0 Output Current vs. PVEE0 Footroom for Various Temperatures

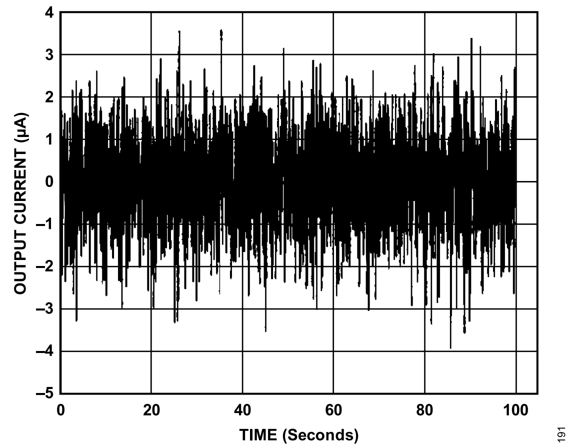


Figure 50. Peak-to-Peak Noise, 0.1 Hz to 10 Hz Bandwidth, (CH0 0 mA to 300 mA Range)

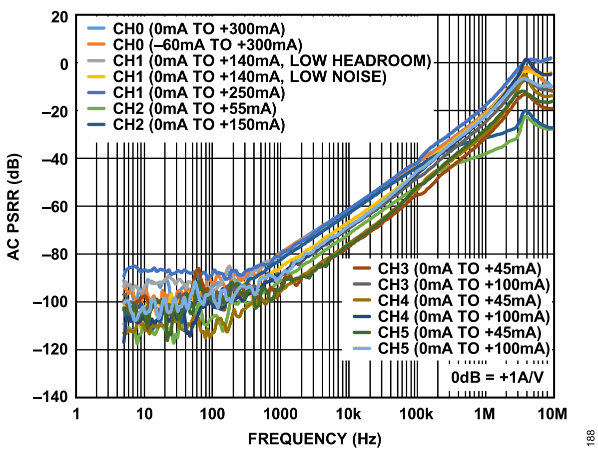


Figure 48. AC PSRR vs. Frequency (All Ranges)

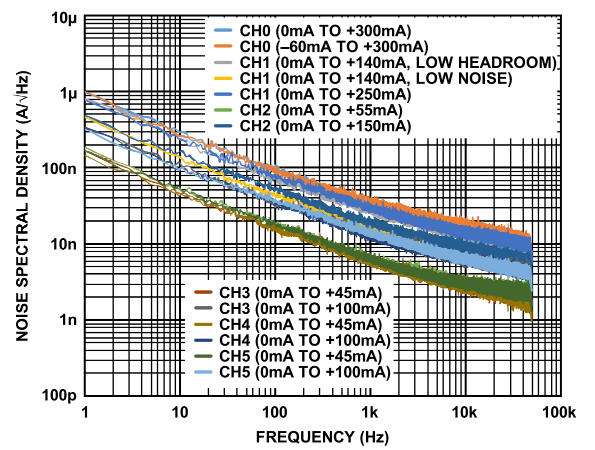


Figure 51. Output NSD vs. Frequency (All Ranges)

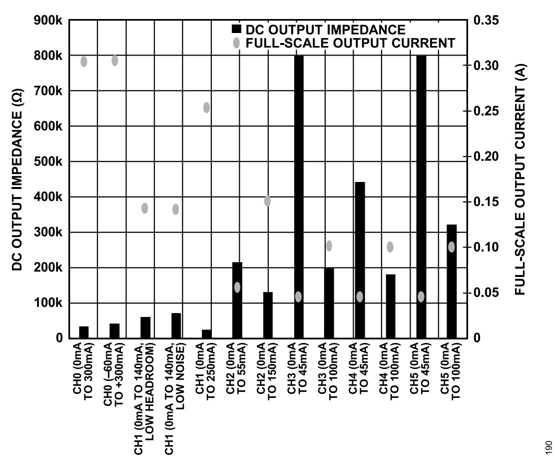


Figure 49. DC Output Impedance vs. Full-Scale Output Current (All Ranges)

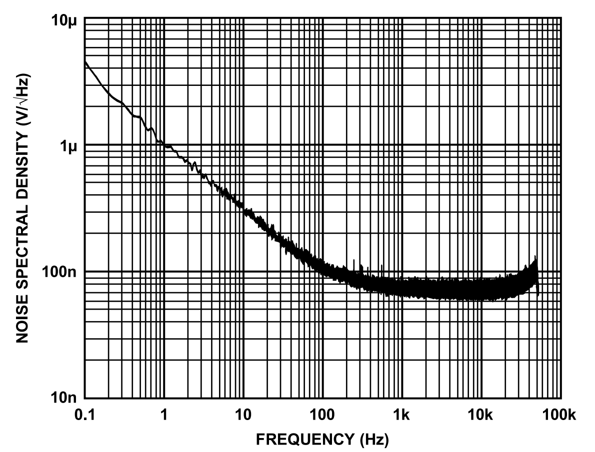


Figure 52. VREF_IO Output NSD vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

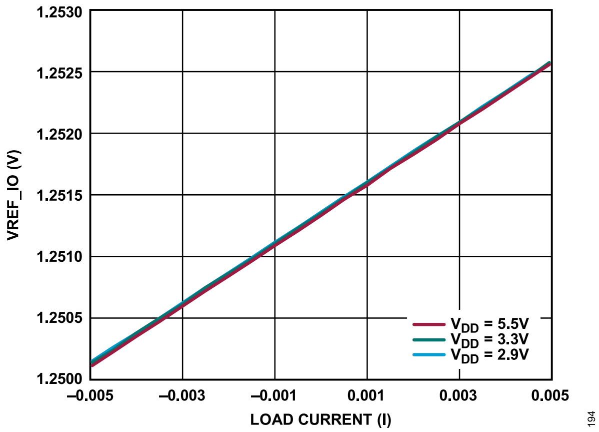


Figure 53. VREF_IO Voltage vs. Load Current

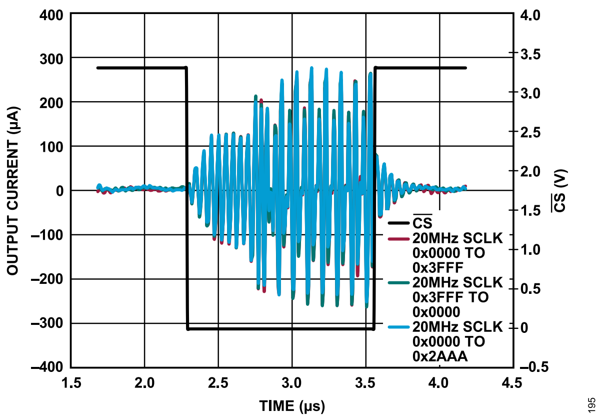


Figure 54. Digital Feedthrough

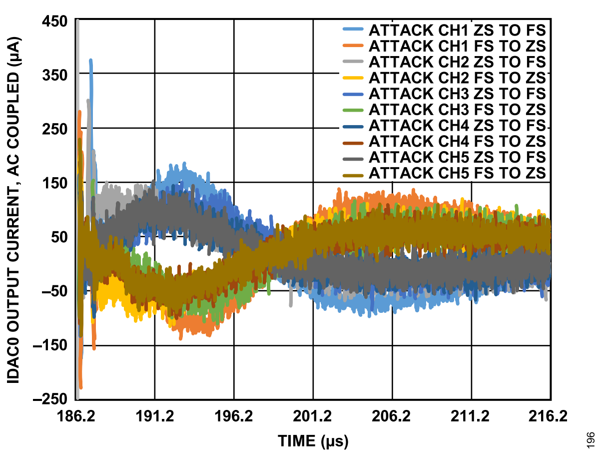


Figure 55. DAC to DAC Crosstalk (Victim Channel Zero)

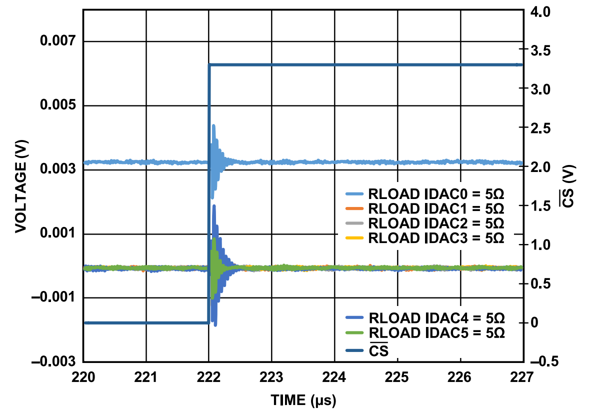


Figure 56. Analog Crosstalk

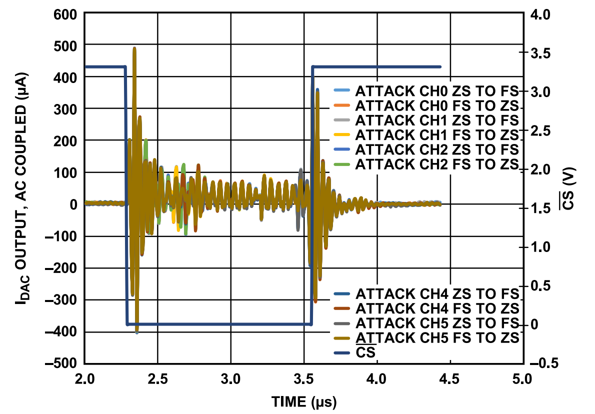


Figure 57. Digital Crosstalk

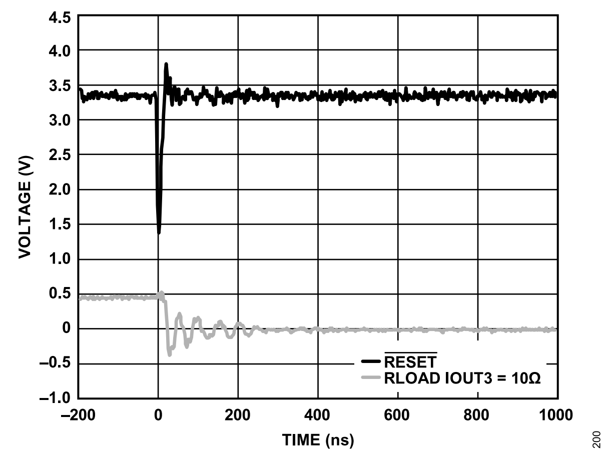


Figure 58. Reset Glitch

TYPICAL PERFORMANCE CHARACTERISTICS

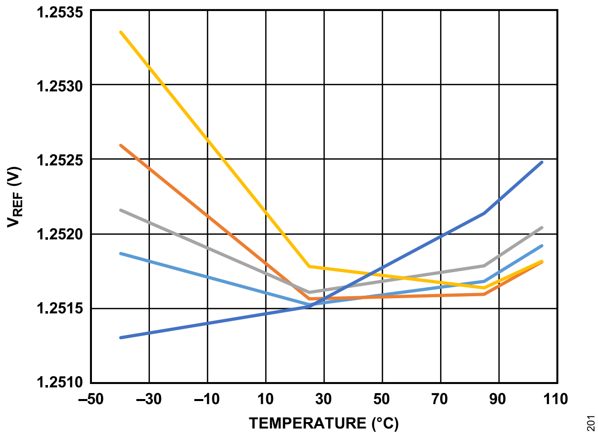


Figure 59. V_{REF} vs. Temperature for Devices for Five AD5770R Devices

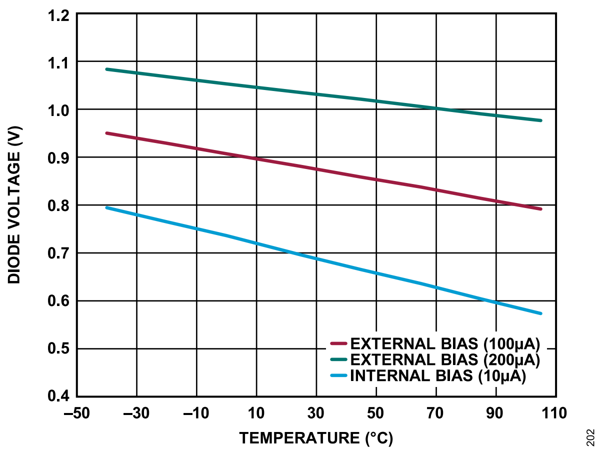


Figure 60. Diode Voltage vs. Temperature

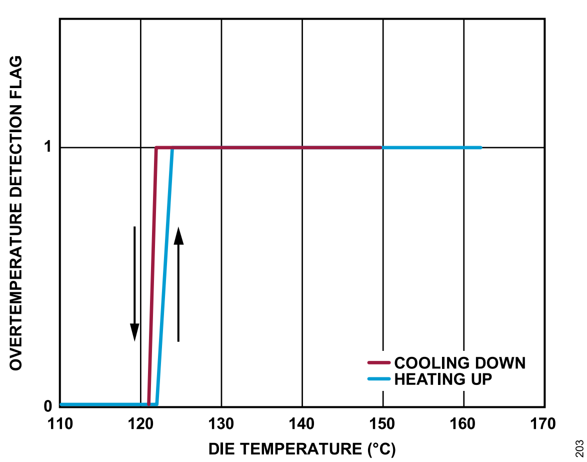


Figure 61. Overheat Warning

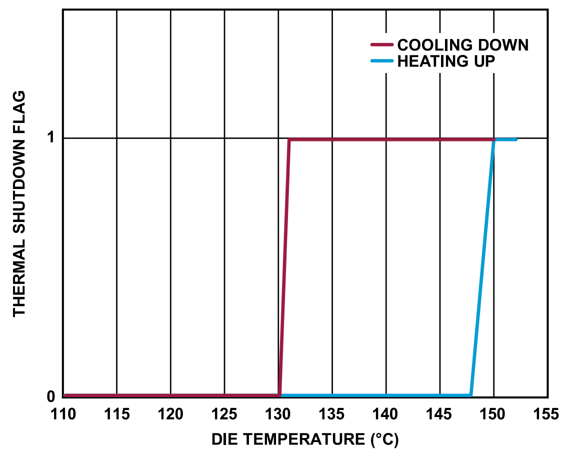


Figure 62. Overheat Shutdown

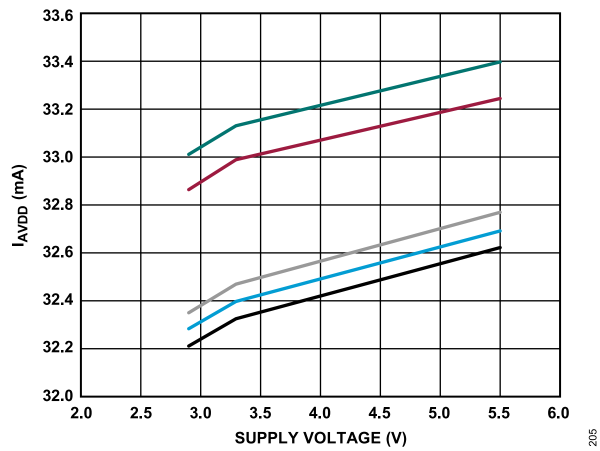


Figure 63. AVDD Supply Current (I_{AVDD}) vs. Supply Voltage for Five AD5770R Devices

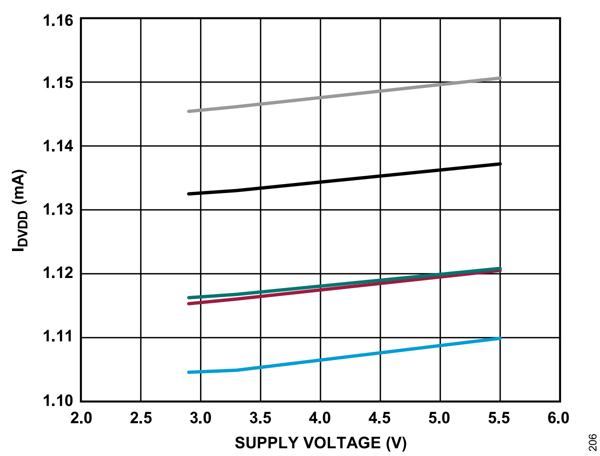


Figure 64. DVDD Supply Current (I_{DVDD}) vs. Supply Voltage for Five AD5770R Devices

TYPICAL PERFORMANCE CHARACTERISTICS

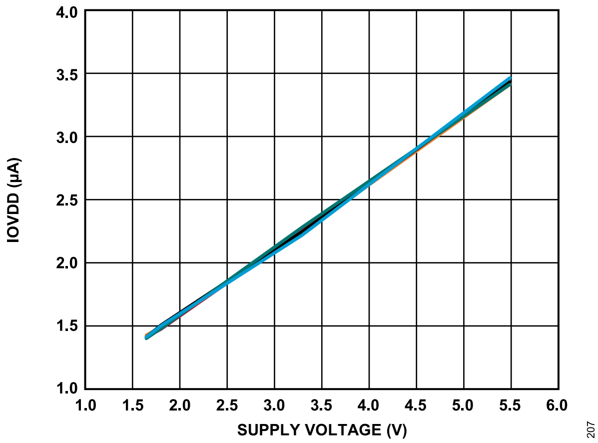


Figure 65. IOVDD Supply Current vs. IOVDD Supply Voltage for Five AD5770R Devices

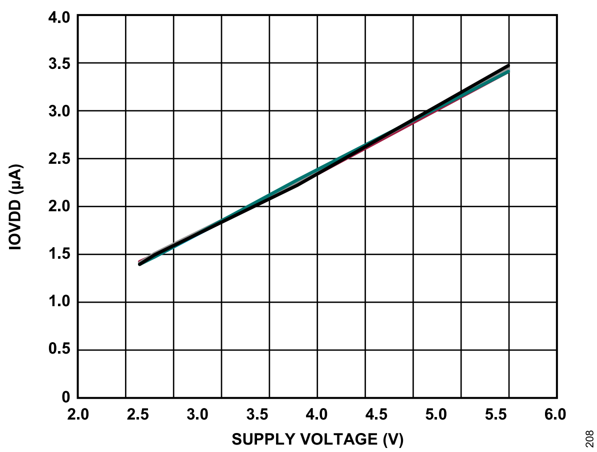


Figure 66. IOVDD Supply Current vs. IOVDD Supply Voltage for Five AD5770R Devices

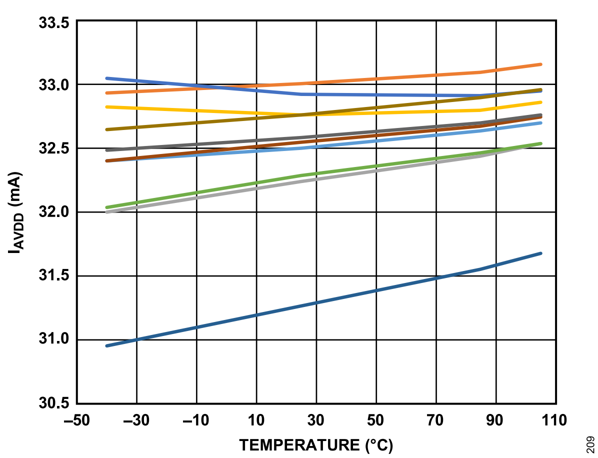


Figure 67. I_{AVDD} vs. Temperature for Ten AD5770R Devices

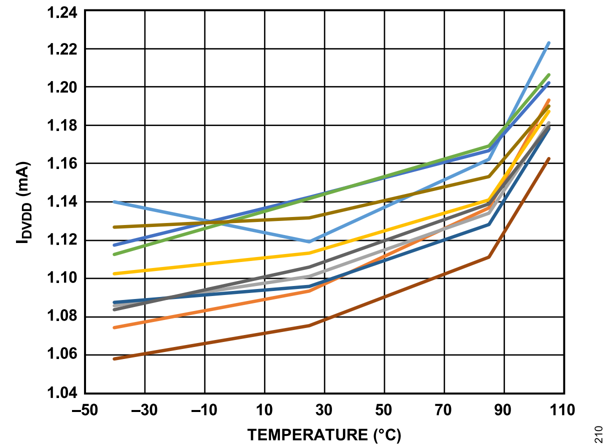


Figure 68. I_{DVDD} vs. Temperature for Ten AD5770R Devices

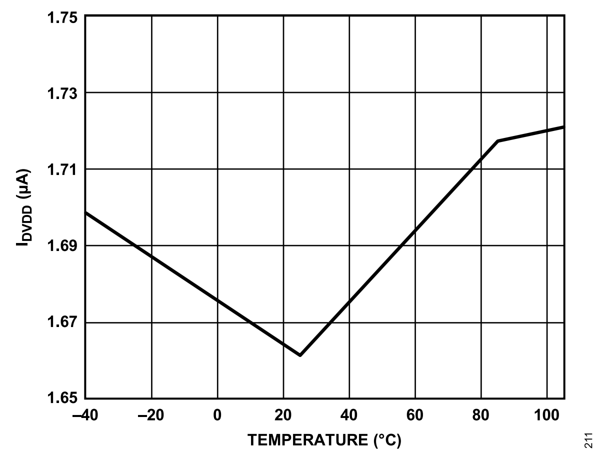


Figure 69. I_{DVDD} vs. Temperature

TERMINOLOGY

TUE

Total unadjusted error is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Relative Accuracy or Integral Nonlinearity (INL)

Relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Typical INL error vs. DAC code plots are shown in Figure 5 to Figure 10.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL error vs. DAC code plots are shown in Figure 11 to Figure 16.

Zero-Scale Error

Zero-scale error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Zero code error is expressed in µA.

Zero-Scale Error Temperature Coefficient

Zero code error drift is a measure of the change in zero code error with a change in temperature. It is expressed in nA/°C.

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % FSR.

Gain Error Temperature Coefficient

Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error

Offset error is a measurement of the difference between I_{OUT}x (actual) and I_{OUT}x (ideal), expressed in µA, in the linear region of the transfer function. Offset error can be negative or positive.

Offset Error Drift

Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in µA/°C.

DC Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in I_{OUT}x to a change in AVDD for a full-scale output of the DAC. It is measured in µA/V.

Output Settling Time

Output settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a zero-scale to full-scale input change and is measured from the falling edge of $\overline{\text{LDAC}}$.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nA-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x1FFF to 0x2000 for the AD5770R).

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nA-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC when monitoring another DAC maintained at midscale. It is expressed in nA-sec.

Digital Crosstalk

Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nA-sec.

DAC to DAC Crosstalk

DAC to DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands when monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nA-sec.

Output Noise Spectral Density

Output noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nA/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nA/√Hz.

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Multiplexer Switching Glitch

The multiplexer switching glitch is a measure of the impulse injected into the analog output of the DAC when the monitor mux is changed to monitor a different channel.

AC Power Supply Rejection Ratio (AC PSRR)

AC power supply rejection ratio is a measure of the rejection of the output current to ac changes in the power supplies applied to the DAC. AC PSRR is measured for a given amplitude and frequency change in power supply voltage and is expressed in decibels.

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DIGITAL TO ANALOG CONVERTER

The AD5770R is a 6-channel, 14-bit, serial input, current output DAC capable of multiple low noise output current ranges with high power efficiency. Each of the six DACs has a segmented current steering architecture, chosen to achieve low glitch performance when changing codes.

PRECISION REFERENCE CURRENT GENERATION

The AD5770R requires a 500 μA precision reference current for all four DAC cores, which is generated using a 1.25 V voltage reference and a 2.5 kΩ precision R_{SET} resistor. The AD5770R integrates an internal 1.25 V voltage reference and 2.5 kΩ internal precision R_{SET} resistor for this function. The AD5770R can also use an external voltage reference and external precision R_{SET} resistor for the reference current generation. Ensure that the voltage reference and the precision R_{SET} resistor have low noise, high accuracy, and low temperature drift to help minimize the overall IDACx gain error and gain error drift. Table 1 outlines the performance specifications of the AD5770R with both the internal reference and internal R_{SET} resistor, and an external 1.25 V reference and external precision R_{SET} resistor.

Voltage Reference

The AD5770R can use an external voltage reference for the precision reference current generation. The external reference voltage can be either 1.25 V or 2.5 V, configured by writing to the REFERENCE_VOLTAGE_SEL bits in the reference register. When the user selects the 2.5 V external voltage reference option, an internal voltage divider attenuates to achieve the 1.25 V required.

The device powers up with the external 2.5 V reference voltage option selected.

The AD5770R integrates a low noise, on-chip, 15 ppm/°C, 1.25 V voltage reference that can be used as the voltage reference. The on-chip reference is powered down by default and is enabled when the REFERENCE_VOLTAGE_SEL bits in the reference register select the internal reference.

The buffered 1.25 V internal reference voltage can be made available at the VREF_IO pin for use as a system reference.

Regardless of the voltage reference scheme used, it is recommended that a 100 nF capacitor is placed between the CREF pin and AGND to achieve specified performance. A simplified diagram of the voltage reference configuration is shown in Figure 70.

When the internal 1.25 V reference is selected and made available on the VREF_IO pin, switch SWA1 and switch SWA2 are closed, and switch SWA3 is connected to switch SWA2.

When the internal 1.25 V reference is selected but not made available on the VREF_IO pin, switch SWA1 is open, switch SWA2 is closed, and switch SWA3 is connected to switch SWA2.

When the external 1.25 V reference option is selected, switch SWA1 is closed, switch SWA2 is open, and switch SWA3 is connected to switch SWA2.

When the external 2.5 V option is selected, switch SWA1 and switch SWA2 are open and switch SWA3 is connected to the resistor divider shown in Figure 70.

Precision R_{SET} Resistor

The AD5770R integrates an on-chip 2.5 kΩ (10 ppm/°C, 0.1%) precision R_{SET} resistor that can be used for the reference current generation. If required, an external precision R_{SET} resistor can be used for reference current generation. The user selects an internal or an external reference resistor by writing to the REFERENCE_RESISTOR_SEL bit in the reference register. The AD5770R powers up with the internal precision R_{SET} resistor selected.

The AD5770R integrates fault protection circuitry when using an external resistor. The AD5770R automatically switches from an external to an internal resistor if the external resistor option is selected, and if the external resistance is below the minimum specification. A simplified diagram of the how the reference resistor is configured by changing switch SWB1 is shown in Figure 70.

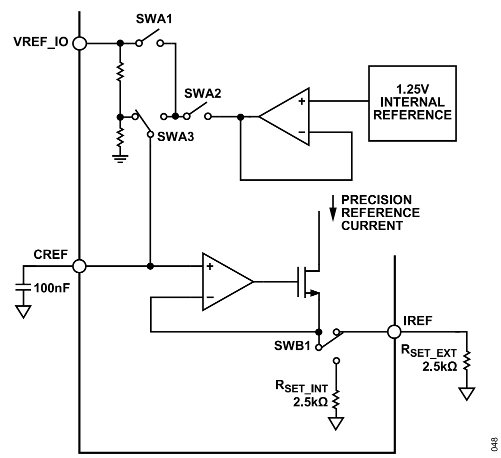

Figure 70. AD5770R Reference Options

DIAGNOSTIC MONITORING

The AD5770R diagnostic feature allows the user to monitor output compliance voltages, output currents, and the internal die temperature of the device. The output compliance voltages, which are voltages representative of output current and internal die temperature, are multiplexed on-chip and are available on the MUX_OUT pin and can be measured using an external ADC.

Diagnostics monitoring is disabled on power up and can be enabled by writing to the MON_FUNCTION bits in the MONITOR_SETUP register.

The AD5770R integrates a voltage buffer on the multiplexer output to ease system design. The multiplexer buffer is disabled and

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bypassed on power up. The multiplexer buffer is enabled by setting the MUX_BUFFER bit in the MONITOR_SETUP register.

Compliance Voltage Monitoring

When the MON_FUNCTION bits in the MONITOR_SETUP register are set to select output voltage monitoring, the output compliance voltage of the selected DAC channel is multiplexed onto the MUX_OUT pin. The IDACx channel to be monitored is selected using the MON_CH bits in the MONITOR_SETUP register.

Output Current Monitoring

When the MON_FUNCTION bits in the MONITOR_SETUP register select output current monitoring, a voltage representation of the output current of the selected DAC channel is multiplexed onto the MUX_OUT pin. The output current can only be monitored in current sourcing mode. The IDACx channel to be monitored is selected using the MON_CH bits in the MONITOR_SETUP register.

The output current is calculated by

$$I_{SOURCE} = \frac{I_{FULLSCALE} \times (V_{MUX} - V_{OS})}{400\ \text{mV}} \quad (1)$$

where:
I_{SOURCE} is the output current being sourced.
$I_{FULLSCALE}$ is the full-scale output current.
V_{MUX} is the measured voltage at the MUX_OUT pin.
V_{OS} is the monitor offset voltage, nominally 28 mV.

Uncalibrated, the current monitoring feature is accurate to within 10% of the full-scale output range. To improve the accuracy of the current monitor feature, calibrate V_{OS} by measuring the voltage at the MUX_OUT pin at zero scale. To calibrate the 400 mV term, measure the voltage at the MUX_OUT pin at full scale.

For 0 mA to 140 mA low headroom mode on Channel 1, use a value of 250 mA for $I_{FULLSCALE}$.

Internal Die Temperature Monitoring

When temperature monitoring is selected in the MONITOR_SETUP register, a voltage representation of the internal die temperature is multiplexed onto the MUX_OUT pin. To monitor the internal die temperature, a precision current is forced through a diode on the chip, and the voltage across the diode is multiplexed onto the MUX_OUT pin. Choose to use an external bias current for the temperature monitoring function by setting the IB_EXT_EN bit high in the MONITOR_SETUP register. The external bias current must be forced into the MUX_OUT pin. The multiplexer buffer must be bypassed when using an external bias current for temperature monitoring.

Using the internal bias current with the IB_EXT_EN bit set low, calculate the internal die temperature as follows:

$$T = \frac{700\ mV - V_D}{1.8\ mV} + 25 \quad (2)$$

where:
T is the die temperature (°C).
V_D is the diode voltage.

Using an external bias current of 100 µA, with the IB_EXT_EN bit set high, the internal die temperature can be calculated as follows:

$$T = \frac{880\ mV - V_D}{1.3\ mV} + 25 \quad (3)$$

When using an external bias current of 200 µA, with the IB_EXT_EN bit set high, the die temperature can be calculated as follows:

$$T = \frac{1.04\ V - V_D}{0.9\ mV} + 25 \quad (4)$$

SERIAL INTERFACE

The AD5770R has a 4-wire ($\overline{CS}$, SCLK, SDI, and SDO) interface that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most digital signal processors (DSPs).

For both read and write SPI transactions, data must be valid on the rising edge of SCLK (SCLK clock polarity = 0, SCLK clock phase = 0). For all SPI transactions, data is shifted MSB first. Communication with the device is separated into two distinct phases of operation. The first phase is the instruction phase and is used to initiate some action of the device. The second phase is the data phase where data is either passed to the device to operate on or received from the device in response to the instruction phase. Figure 71 illustrates the SPI transaction phases.

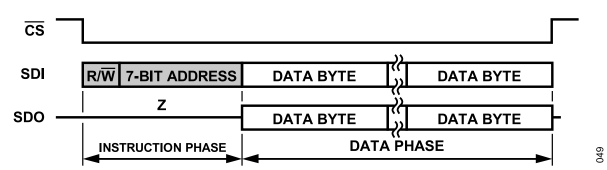

Figure 71. SPI Transaction Phases

Instruction Phase

The instruction phase immediately follows the falling edge of $\overline{CS}$ that initiates the SPI transaction. The instruction phase consists of a read/write bit (R/$\overline{W}$) followed by a register address word. Setting R/$\overline{W}$ high selects a read instruction. Setting R/$\overline{W}$ low selects a write instruction. The address word is 7 bits long. The register address sent in the instruction phase is used as the starting address to start writing or reading from. Refer to Table 12 and Table 13 for a full list of registers and the associated addresses.

Data Phase

The data phase immediately follows the instruction phase. When a write instruction is sent to the device, data is written to the register location selected. When a read instruction is sent to the device, data stored in the register location selected is shifted out on the SDO pin.

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SPI Frame Synchronization

The $\overline{CS}$ pin is used to frame data during an SPI transaction. A falling edge on $\overline{CS}$ initiates a SPI transaction. Deasserting $\overline{CS}$ during a SPI transaction terminates part or all of the data transfer. If $\overline{CS}$ is deasserted (returned high) before the instruction phase is complete, the transaction aborts and the AD5770R returns to the ready state. If $\overline{CS}$ is deasserted before the first data word is written, the transaction aborts and the AD5770R returns to the ready state. If $\overline{CS}$ is deasserted after one or more data words have been written, those completed data words are written or read, but any partial written data words are aborted.

Streaming Mode

The $\overline{CS}$ pin can be held low, and multiple data bytes can be shifted during the data phase, which reduces the amount of overhead associated with data transfer. This mode of operation is known as streaming mode. When in streaming mode, the register address sent in the instruction phase is automatically incremented or decremented after each byte of data is processed. The ADDR_ASCENSION_MSB bit and ADDR_ASCENSION_ LSB bit in the INTERFACE_CONFIG_A register selects the address increment or decrement. The default operation is to decrement addresses when streaming data. Figure 72 illustrates a streaming mode SPI write transaction in which the six input registers are accessed using only a single instruction byte. The register address is automatically decremented after each data byte is processed. Figure 73 illustrates a streaming mode SPI read transaction in which the six DAC registers are accessed using a decrementing address.

Single Instruction Mode

When the single instruction bit is set in the INTERFACE_ CONFIG_B register, streaming mode is disabled, and the AD5770R is placed in single instruction mode. In single instruction mode, the internal SPI state machine resets after the data phase as if $\overline{CS}$ was deasserted, and awaits the next instruction. Single instruction mode forces each data phase to be preceded with a new instruction phase even though the $\overline{CS}$ line has not been deasserted by the SPI master. Single instruction mode allows the user to access one or more registers in a single synchronization frame without having to deassert the $\overline{CS}$ line after each data bye. The default for this bit is cleared, resulting in streaming mode being enabled.

Figure 74 illustrates an SPI transaction in single instruction mode in which the following sequence of events occur:

1. Sets the output range of Channel 1.
2. Enables the output of Channel 1.
3. Writes to the Channel 1 DAC register.
4. Reads the status register.

Multibyte Registers

If writing to a multibyte register, $\overline{CS}$ must be held low for the whole transaction for the write to be valid. The address used must be the address of the most significant byte. The ADDR_ ASCENSION_MSB bit and the ADDR_ASCENSION_LSB bit in the INTERFACE_CONFIG_A register must be cleared. This applies when reading or writing to any multibyte register in both single instruction mode and streaming mode. Figure 75 illustrates a multibyte register access. The AD5770R contains 14 multibyte registers, as follows:

- Six input registers.
- Six DAC registers.
- One input page mask register.
- One DAC page mask register.

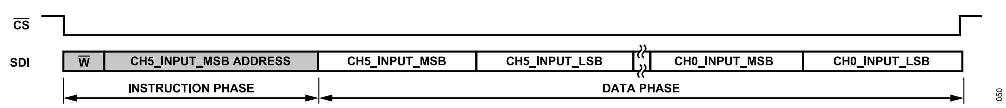

Figure 72. Streaming Mode SPI Write Transaction with Decrementing Address

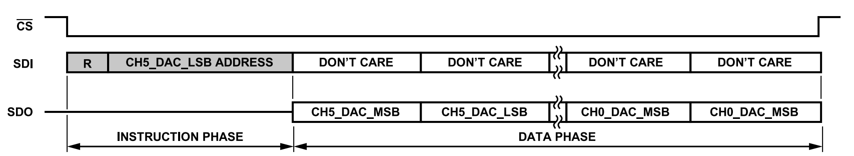

Figure 73. Streaming Mode SPI Read Transaction with Decrementing Address

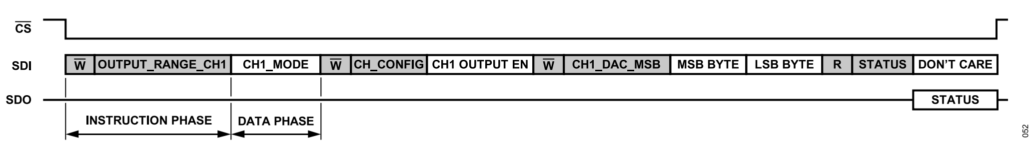

Figure 74. SPI Transaction in Single Instruction Mode

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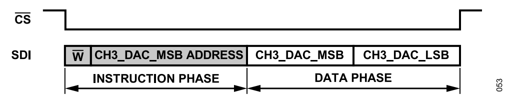

Figure 75. Multibyte Register Write

RESET FUNCTION

The AD5770R has an asynchronous RESET pin. For normal operation, RESET is tied high. Asserting the RESET pin to logic low for at least 10 ns resets all registers to their default values. The reset function takes 100 ns, maximum. Data must not be written to the device during this time.

The AD5770R has a software reset function that performs the same function as the RESET pin, with the exception of not resetting the INTERFACE_CONFIG_A register. The reset function is activated by setting the SW_RESET_MSB and SW_RESET_LSB bits in the INTERFACE_CONFIG_A register. The SW_RESET_MSB and SW_RESET_LSB bits clear automatically during a software reset.

A reset function must not be performed when the TEMP_ WARNING bit in the status register is high. Ensure that the device reads the correct trim values from the internal memory.

LOAD DAC

The AD5770R DAC consists of double buffered registers for the DAC code. Data for one or many channels can be written to the input register without changing the DAC outputs. A load DAC command issued to the device transfers input register content into the DAC register, updating the DAC output.

Hardware LDAC Pin

The AD5770R has an active low LDAC pin that can synchronize updates to the outputs of the DACs. When LDAC is held high, DAC codes can be written to the input registers of the DAC without affecting the output. When LDAC is taken low, the contents of the input register are transferred to the DAC register of the corresponding channel, and the output updates. The LDAC idle high behavior is shown in Figure 2.

When the LDAC pin is held low before the last rising edge of CS prior to the beginning of a new SPI transaction and the input registers contents are modified, the update to the DAC output happens when the LSB of the DAC input register is written. The LDAC idle low behavior is shown in Figure 2 and Figure 3.

The LDAC pin functionality can be masked for any or all channels by configuring the corresponding HW_LDAC_ MASK_CHx bits high in the HW_LDAC register, which is useful in cases where only a selection of channels are required to update synchronously.

Software LDAC

It is possible to transfer data from any or all input registers to the corresponding DAC registers with a write to the SW_LDAC register, which is useful in cases where only a selection of channels are required to update synchronously.

Setting the SW_LDAC register for any channel updates the selected channels DAC register with the input register contents. The contents of the SW_LDAC register clear to 0x00 after a software LDAC operation.

INPUT PAGE MASK REGISTER

Following a write to the input page mask register, the code loaded into this register is copied into the input register of any channels selected in the CH_SELECT register.

DAC PAGE MASK REGISTER

Following a write to the DAC page mask register, the DAC code loaded into this register is copied into the DAC register of any channels selected in the CH_SELECT register.

OUTPUT STAGES

Each of the six AD5770R channels has a programmable current output stage that sets the required output current.

Channel 0 Sink Current Generator

To sink current on Channel 0, the sink current generator must be enabled by setting the CH0_SINK_EN bit in the CHANNEL_ CONFIG register to one. On power-up, the sink current generator is enabled.

Output Shutdown

On power-up, the outputs of each channel are in shutdown mode. When a DAC output is in shutdown mode, the output current is set to 0 mA. However, the bias circuitry for each IDACx channel remains powered up, and only the output is shut down. The shutdown bits for each register are located in the CHANNEL_CONFIG register. When changing between output modes on a DAC channel, the output stage of the channel must be shut down to prevent glitches on the output.

Channel 0

Channel 0 of the AD5770R sinks up to 60 mA and sources up to 300 mA of current. This channel has three different modes of operation. The CH0_MODE bits in the OUTPUT_RANGE_CH0 register configure the different modes. The configuration options for Channel 0 are listed in Table 8.

On power-up, Channel 0 defaults to the 0 mA to 300 mA range.

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Channel 0 has a sinking only mode of −60 mA to 0 mA. In this mode, the DAC has a zero-scale output of −60 mA and a full-scale output of 0 mA. To enter this mode safely without output glitches, the output must be shut down first by setting CH0_SHUTDOWN_B high in the CHANNEL_CONFIG register.

Channel 0 has a sourcing and sinking mode where the DAC has a zero-scale output of −60 mA and a full-scale output of +300 mA. To reduce glitches on the output of Channel 0, CH0_MODE must be configured before taking the output out of shutdown.

Channel 1

Channel 1 can be set up to source 0 mA to 140 mA or 0 mA to 250 mA. The full-scale output range for Channel 1 must be set by writing to the CH1_MODE bits of the OUTPUT_RANGE_CH1 register. In addition to the 0 mA to 250 mA range, Channel 1 has two 0 mA to 140 mA ranges; the channel can be set up to optimize for better noise and PSRR or for reduced headroom. The configuration options for Channel 1 are listed in Table 8.

Channel 2

Channel 2 can be set up to source 0 mA to 55 mA or 0 mA to 150 mA. The full-scale output range for Channel 2 must be set by writing to the CH2_MODE bits of the OUTPUT_RANGE_ CH2 register. Table 8 lists configuration options for Channel 2.

Channel 3 to Channel 5

Channel 3, Channel 4, and Channel 5 of the AD5770R can be set up to source 0 mA to 45 mA or 0 mA to 100 mA. The full-scale output rages for Channel 3, Channel 4, and Channel 5 must be set by writing to the CH3_MODE, CH4_MODE, and CH5_MODE bits of the OUTPUT_RANGE_CH3, OUTPUT_ RANGE_CH4, and OUTPUT_RANGE_CH5 registers. The configuration options for Channel 3, Channel 4, and Channel 5 are listed in Table 8.

Table 8. Output Range Mode Register Setup

Channel	Mode Bit Name	Mode	Zero-Scale Output (mA)	Full-Scale Output (mA)[1]	Minimum Headroom (mV)	Comments
Channel 0	CH0_MODE	0x0	0	300	450	
		0x1	−60	0	0[2]	
		0x2	−60	300	450[2]	
Channel 1	CH1_MODE	0x1	0	140	275	Low headroom
		0x2	0	140	450	Low noise and PSRR
		0x3	0	250	450	
Channel 2	CH2_MODE	0x0	0	55	275	
		0x1	0	150	275	
Channel 3	CH3_MODE	0x0	0	45	275	
		0x1	0	100	275	
Channel 4	CH4_MODE	0x0	0	45	275	
		0x1	0	100	275	
Channel 5	CH5_MODE	0x0	0	45	275	
		0x1	0	100	275	

[1] Output current scaling feature disabled. See the Output Current Scaling section for more information.

[2] 500 mV footroom from PVEE0 supply required when sinking current.

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OUTPUT FILTER

Each channel of the AD5770R has a user programmable variable resistor in the output stage used for filtering. The output filter resistor creates a low-pass RC filter with the 10 nF external capacitor connected to the CDAMP_IDACx pin. The value loaded into the OUTPUT_FILTER_CH0x register configures the value of the variable resistor. Table 9 shows the cutoff frequency of each resistor setting.

Table 9. IDACx Filter Bandwidth Control Settings

OUTPUT_FIILTER_CHx Setting	Resistor Value	Cutoff Frequency
0x0	60 Ω	262 kHz
0x5	5.6 kΩ	2.8 kHz
0x6	11.2 kΩ	1.4 kHz
0x7	22.2 kΩ	715 Hz
0x8	44.4 kΩ	357 Hz
0x9	104 kΩ	153 Hz

OUTPUT CURRENT SCALING

When in current sourcing mode only, the full-scale output current of each channel of the AD5770R can be scaled by up to ½ of the nominal full-scale current and maintain 14-bit monotonicity.

The full-scale output current of any channel can be scaled by writing to the CHx_OUTPUT_SCALING bits of the OUTPUT_RANGE_CHx register. The value loaded into the CHx_OUTPUT_SCALING bits determines the multiplier, which scales the full-scale current. The adjusted full-scale current of an IDACx channel is calculated by

$$I_{ADJ} = I_{NOM} \times \left(1 - \frac{x}{128}\right) \quad (5)$$

where:
I_{ADJ} is the adjusted full-scale output current.
I_{NOM} is the nominal full-scale output current.
x is the code loaded into output scaling register, $0 \leq x \leq 63$.

For the range scaling feature to take effect on the output current for a particular channel, write to the DAC register for that channel after writing to the OUTPUT_RANGE_CHx register.

Refer to Table 10 for a list of output current ranges achievable using the scaling feature.

$\overline{\text{ALARM}}$

The AD5770R provides a number of fault alerts that are signaled via the $\overline{\text{ALARM}}$ pin and the status register. The active low $\overline{\text{ALARM}}$ pin can be configured as an open-drain output by setting the OPEN_DRAIN_EN bit in the ALARM_CONFIG register, allowing several devices to be connected together to one pull-up resistor for global fault detection. Open drain mode on the $\overline{\text{ALARM}}$ pin is disabled on power up.

Background CRC Failure

The AD5770R periodically performs a background cyclic redundancy check (CRC) on the status of the on-chip registers to ensure that the memory bits are not corrupted. In the unlikely event that the background CRC fails, the $\overline{\text{ALARM}}$ pin activates and the BACKGROUND_CRC_STATUS bit in the status register is set high. Reading the status register deasserts the $\overline{\text{ALARM}}$ pin. A hardware or software reset is required to clear the BACKGROUND _CRC_STATUS bit. The $\overline{\text{ALARM}}$ pin can be set to ignore background CRC failures by setting the BACKGROUND_CRC_ALARM_MASK bit of the ALARM_CONFIG register.

Overtemperature Warning and Shutdown

To protect the device from damage from overtemperature occurrences during operation, the AD5770R has an overtemperature warning alert and an overtemperature shutdown alert.

When the internal die temperature reaches approximately 125°C, the $\overline{\text{ALARM}}$ pin activates, and the TEMP_WARNING bit in the status register is set high. The user must read the status register to deassert the $\overline{\text{ALARM}}$ pin.

When the internal die temperature reaches approximately 145°C, the $\overline{\text{ALARM}}$ pin activates (if not already activated) and the OVER_TEMP bit in the status register is set. The user must read the status register to deassert the $\overline{\text{ALARM}}$ pin.

If the THERMAL_SHUTDOWN_EN bit in the ALARM_CONFIG register is set to high, the device shuts down the output stages to protect from over temperature, and the outputs remain shut down until the user initiates a software or hardware reset to the device.

The TEMP_WARNING and OVER_TEMP flags in the status register clear when the device temperature returns below approximately 120°C. To guarantee proper data downloads from the internal memory, a reset function must not be performed when the TEMP_WARNING bit in the status register is high.

The $\overline{\text{ALARM}}$ pin can be set to ignore over temperature faults and over temperature warnings by setting the OVER_TEMP_ALARM_MASK and TEMP_WARNING_ALARM_MASK bits of the ALARM_CONFIG register.

Negative Compliance Voltage

The compliance voltage on IDAC0 pin of the AD5770R can be a negative value when sinking current. The AD5770R has a negative compliance voltage alert feature to protect an external unipolar ADC connected to the MUX_OUT pin.

The following sequence of events occurs if the user enables voltage monitoring of Channel 0 when the voltage on IDAC0 is negative:

1. The $\overline{\text{ALARM}}$ pin activates.
2. The MUX_OUT pin is disabled.
3. The NEGATIVE_CHANNEL0 bit in the status register is set.

THEORY OF OPERATION

The status register must be read to dessert the $\overline{\text{ALARM}}$ pin.

The following sequence of events occurs if the voltage on IDAC0 goes negative after the user enables voltage monitoring of Channel 0:

1. The $\overline{\text{ALARM}}$ pin activates.
2. The MUX_OUT pin is set to the same voltage as PVDD0.
3. The NEGATIVE_CHANNEL0 bit in the status register is set.

The status register must be read to dessert the $\overline{\text{ALARM}}$ pin.

The $\overline{\text{ALARM}}$ pin can be set to ignore the negative compliance voltage warning by setting the NEGATIVE_CHANNEL0_ALARM_MASK bit of the ALARM_CONFIG register.

IREF Fault

When the external R_{SET} resistor option is selected, it is important that the value of this external R_{SET} resistor cannot create a reference current that is too high and can damage the device. The AD5770R incorporates an internal protection circuit that protects the device if the reference current is too high.

When the protection circuit detects a reference current that is too high, the following events occur:

1. This circuit switches to the internal R_{SET} resistor.
2. The $\overline{\text{ALARM}}$ pin activates.
3. The IREF_FAULT bit in the status register is set.

The user must then read the status register to deassert the $\overline{\text{ALARM}}$ pin. The $\overline{\text{ALARM}}$ pin can be set to ignore IREF faults by setting the IREF_FAULT_ALARM_MASK bit of the ALARM_CONFIG register.

Table 10. Full-Scale Output Current Per Channels, for All Scaling Code Values

Scaling Code	Channel 0, 0 mA to 300 mA Range (mA)	Channel 1, 0 mA to 140 mA Range (mA)	Channel 1, 0 mA to 250 mA Range (mA)	Channel 2, 0 mA to 55 mA Range (mA)	Channel 2, 0 mA to 150 mA Range (mA)	Channel 3 to Channel 5, 0 mA to 45 mA Range (mA)	Channel 3 to Channel 5, 0 mA to 100 mA Range (mA)
0 (Default)	300	140	250	55	150	45	100
1	298	139	248	55	149	45	99
2	295	138	246	54	148	44	98
3	293	137	244	54	146	44	98
4	291	136	242	53	145	44	97
5	288	135	240	53	144	43	96
6	286	133	238	52	143	43	95
7	284	132	236	52	142	43	95
8	281	131	234	52	141	42	94
9	279	130	232	51	139	42	93
10	277	129	230	51	138	41	92
11	274	128	229	50	137	41	91
12	272	127	227	50	136	41	91
13	270	126	225	49	135	40	90
14	267	125	223	49	134	40	89
15	265	124	221	49	132	40	88
16	263	123	219	48	131	39	88
17	260	121	217	48	130	39	87
18	258	120	215	47	129	39	86
19	255	119	213	47	128	38	85
20	253	118	211	46	127	38	84
21	251	117	209	46	125	38	84
22	248	116	207	46	124	37	83
23	246	115	205	45	123	37	82
24	244	114	203	45	122	37	81
25	241	113	201	44	121	36	80
26	239	112	199	44	120	36	80
27	237	110	197	43	118	36	79
28	234	109	195	43	117	35	78
29	232	108	193	43	116	35	77

THEORY OF OPERATION

Table 10. Full-Scale Output Current Per Channels, for All Scaling Code Values (Continued)

Scaling Code	Channel 0, 0 mA to 300 mA Range (mA)	Channel 1, 0 mA to 140 mA Range (mA)	Channel 1, 0 mA to 250 mA Range (mA)	Channel 2, 0 mA to 55 mA Range (mA)	Channel 2, 0 mA to 150 mA Range (mA)	Channel 3 to Channel 5, 0 mA to 45 mA Range (mA)	Channel 3 to Channel 5, 0 mA to 100 mA Range (mA)
30	230	107	191	42	115	34	77
31	227	106	189	42	114	34	76
32	225	105	188	41	113	34	75
33	223	104	186	41	111	33	74
34	220	103	184	40	110	33	73
35	218	102	182	40	109	33	73
36	216	101	180	40	108	32	72
37	213	100	178	39	107	32	71
38	211	98	176	39	105	32	70
39	209	97	174	38	104	31	70
40	206	96	172	38	103	31	69
41	204	95	170	37	102	31	68
42	202	94	168	37	101	30	67
43	199	93	166	37	100	30	66
44	197	92	164	36	98	30	66
45	195	91	162	36	97	29	65
46	192	90	160	35	96	29	64
47	190	89	158	35	95	28	63
48	188	88	156	34	94	28	63
49	185	86	154	34	93	28	62
50	183	85	152	34	91	27	61
51	180	84	150	33	90	27	60
52	178	83	148	33	89	27	59
53	176	82	146	32	88	26	59
54	173	81	145	32	87	26	58
55	171	80	143	31	86	26	57
56	169	79	141	31	84	25	56
57	166	78	139	31	83	25	55
58	164	77	137	30	82	25	55
59	162	75	135	30	81	24	54
60	159	74	133	29	80	24	53
61	157	73	131	29	79	24	52
62	155	72	129	28	77	23	52
63	152	71	127	28	76	23	51

APPLICATIONS INFORMATION

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5770R is via a serial bus that uses a standard protocol compatible with DSPs and microcontrollers. The communications channel requires a 4-wire serial interface consisting of a clock signal, a data input signal, a data output signal, and a synchronization signal.

AD5770R TO SPI INTERFACE

The SPI interface of the AD5770R is designed to be easily connected to industry-standard DSPs and microcontrollers. Figure 76 shows the AD5770R connected to the ADuCM320. The ADuCM320 has an integrated SPI port that can be connected directly to the SPI pins of the AD5770R.

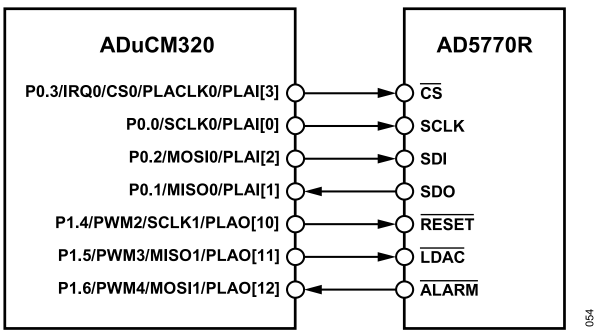


Figure 76. ADuCM320 SPI Interface

THERMAL CONSIDERATIONS

The AD5770R has a maximum junction temperature of 150°C (see Table 5). To ensure reliable and specified operation over the lifetime of the device, it is important that the AD5770R is not operated under conditions that cause the junction temperature to exceed 150°C. The junction temperature is directly affected by the power dissipated across the AD5770R and the ambient temperature.

Table 1 specifies the output current ranges for each AD5770R channel and the maximum power supply voltages. Therefore, it is important to understand the effects of power dissipation on the package and the effects the package has on the junction temperature. The AD5770R is packaged in a 49-ball, 4 mm × 4 mm, wafer level chip scale packaging (WLCSP) package. The thermal impedance, θ_{JA}, is specified in Table 6.

Table 11 provides examples of the maximum allowed power dissipation and the maximum allowed ambient temperature under certain conditions.

COMBINING CHANNELS TO INCREASE CURRENT RANGE

The maximum current that can be sourced from IDAC0 is 300 mA. It is possible to increase the current source capability by connecting two channels directly together. Figure 77 shows IDAC1 combined with IDAC2 to create a full-scale output current of 400 mA. When channels are combined, care must be taken to ensure the following:

- The output compliance voltage stays within the range specified in Table 1.
- The output voltage stays within the absolute maximum ratings specified in Table 5.

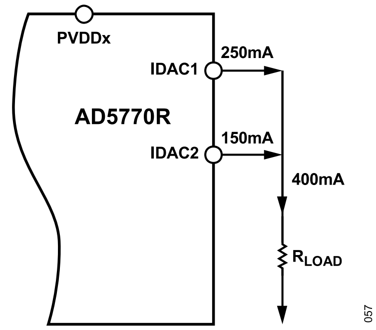


Figure 77. Increasing the Current Range by Summing Channels

LAYOUT GUIDELINES

Take careful consideration of the power supply and ground return layout in order to ensure the rated performance. Design the PCB on which the AD5770R is mounted so that the AD5770R lies on the analog plane.

The AD5770R must have an ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible (ideally directly against the device). The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI). Common ceramic capacitors provide a low impedance path to ground at high frequencies to handle transient currents, due to internal logic switching.

Ensure that the power supply line has as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Shield clocks and other fast switching digital signals from other parts of the board by using a digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only, and the signal traces are placed on the solder side. However, this technique is not always possible with a 2-layer board.

Because the AD5770R can dissipate a large amount of power, it is recommended to provide some heat sinking capability to allow power to dissipate easily.

For the WLCSP package, heat is transferred through the solder balls to the PCB board. θ_{JA} thermal impedance is dependent on board construction. More copper layers enable heat to be removed more effectively.

If using an external R_{SET} resistor, the low side of the R_{SET} resistor must be connected to REFGND before the connection to AGND. Ensure that the width of the trace connecting R_{SET} to the IREF pin

APPLICATIONS INFORMATION

is as wide as possible to reduce the resistance and the temperature coefficient of the trace.

Table 11. Thermal Considerations for 49-Ball WLCSP Package

Parameter	Description
Maximum Power Dissipation[1]	Maximum allowed AD5770R power dissipation (P_{DISS}) when operating at an ambient temperature of 105°C, $\frac{T_{JMAX} - T_A}{\theta_{JA}} = \frac{150°C - 105°C}{30°C/W} = 1.5\ W$
Recommended Power Dissipation[1]	Maximum recommended AD5770R P_{DISS} when operating at an ambient temperature of 85°C and a junction temperature of 115°C, $\frac{T_J - T_A}{\theta_{JA}} = \frac{115°C - 85°C}{30°C/W} = 1\ W$
Ambient Temperature[1]	Maximum recommended ambient temperature when dissipating 980.4 mW across the AD5770R while maintaining a junction temperature of 115°C. $T_J - P_{DISS} \times \theta_{JA}$ = 115°C – (980.4 mW × 30°C/W) = 85.58°C Power dissipation calculation example: AVDD = DVDD = IOVDD = 3.3 V, PVDDx = 2.5 V AVEE = PVEE0 = 0 V, R_{LOAD} = 6 Ω per channel, AD5770R quiescent power dissipation = 110 mW IDAC0 = 300 mA, power dissipation = 210 mW IDAC1 = 150 mA, power dissipation = 240 mW IDAC2 = 55 mA, power dissipation = 119.35 mW IDAC3, IDAC4, IDAC5 = 45 mA, power dissipation = 301.05 mW Total power dissipation = 110 mW + 870.4 mW = 980.4 W

[1] T_{JMAX} in Table 5 is the junction temperature that the AD5770R can tolerate, but not operate at. It is recommended that the junction temperature does not exceed 115°C.

REGISTER SUMMARY

SPI CONFIGURATION REGISTERS

Table 12. AD5770R SPI Configuration Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x00	INTERFACE_CONFIG_A	[7:0]	SW_RESET_MSB	Reserved	ADDR_ASCENSION_MSB	SDO_ACTIVE_MSB	SDO_ACTIVE_LSB	ADDR_ASCENSION_LSB	Reserved	SW_RESET_LSB	0x18	R/W
0x01	INTERFACE_CONFIG_B	[7:0]	SINGLE_INST	Reserved			SHORT_INSTRUCTION	Reserved			0x08	R/W
0x03	CHIP_TYPE	[7:0]	Reserved				CHIP_TYPE				0x08	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x04	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x40	R
0x06	CHIP_GRADE	[7:0]	GRADE				DEVICE_REVISION				0x00	R
0x0A	SCRATCH_PAD	[7:0]	VALUE								0x00	R/W
0x0B	SPI_REVISION	[7:0]	VERSION								0x82	R
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x0E	STREAM_MODE	[7:0]	LENGTH								0x00	R/W
0x10	INTERFACE_CONFIG_C	[7:0]	Reserved		STRICT_REGISTER_ACCESS	Reserved					0x20	R
0x11	INTERFACE_STATUS_A	[7:0]	INTERFACE_NOT_READY	Reserved							0x00	R

AD5770R CONFIGURATION REGISTERS

Table 13. AD5770R Configuration Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x14	CHANNEL_CONFIG	[7:0]	CH0_SINK_EN	Reserved	CH5_SHUTDOWN_B	CH4_SHUTDOWN_B	CH3_SHUTDOWN_B	CH2_SHUTDOWN_B	CH1_SHUTDOWN_B	CH0_SHUTDOWN_B	0x80	R/W
0x15	OUTPUT_RANGE_CH0	[7:0]	CH0_OUTPUT_SCALING						CH0_MODE		0x00	R/W
0x16	OUTPUT_RANGE_CH1	[7:0]	CH1_OUTPUT_SCALING						CH1_MODE		0x02	R/W
0x17	OUTPUT_RANGE_CH2	[7:0]	CH2_OUTPUT_SCALING						Reserved	CH2_MODE	0x00	R/W
0x18	OUTPUT_RANGE_CH3	[7:0]	CH3_OUTPUT_SCALING						Reserved	CH3_MODE	0x00	R/W
0x19	OUTPUT_RANGE_CH4	[7:0]	CH4_OUTPUT_SCALING						Reserved	CH4_MODE	0x00	R/W
0x1A	OUTPUT_RANGE_CH5	[7:0]	CH5_OUTPUT_SCALING						Reserved	CH5_MODE	0x00	R/W
0x1B	REFERENCE	[7:0]	Reserved					REFERENCE_RESISTOR_SEL	REFERENCE_VOLTAGE_SEL		0x00	R/W

REGISTER SUMMARY

Table 13. AD5770R Configuration Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x1C	ALARM_CONFIG	[7:0]	BACKGROUND_CRC_ALARM_MASK	IREF_FAULT_ALARM_MASK	NEGATIVE_CHANNEL0_ALARM_MASK	OVER_TEMP_ALARM_MASK	TEMP_WARNING_ALARM_MASK	BACKGROUND_CRC_EN	THERMAL_SHUTDOWN_EN	OPEN_DRAIN_EN	0x06	R/W
0x1D	OUTPUT_FILTER_CH0	[7:0]	Reserved				OUTPUT_FILTER_RESISTOR0				0x00	R/W
0x1E	OUTPUT_FILTER_CH1	[7:0]	Reserved				OUTPUT_FILTER_RESISTOR1				0x00	R/W
0x1F	OUTPUT_FILTER_CH2	[7:0]	Reserved				OUTPUT_FILTER_RESISTOR2				0x00	R/W
0x20	OUTPUT_FILTER_CH3	[7:0]	Reserved				OUTPUT_FILTER_RESISTOR3				0x00	R/W
0x21	OUTPUT_FILTER_CH4	[7:0]	Reserved				OUTPUT_FILTER_RESISTOR4				0x00	R/W
0x22	OUTPUT_FILTER_CH5	[7:0]	Reserved				OUTPUT_FILTER_RESISTOR5				0x00	R/W
0x23	MONITOR_SETUP	[7:0]	MON_FUNCTION		MUX_BUFFER	IB_EXT_EN	MON_CH				0x00	R/W
0x24	STATUS	[7:0]	BACKGROUND_CRC_STATUS	Reserved			IREF_FAULT	NEGATIVE_CHANNEL0	OVER_TEMP	TEMP_WARNING	0x00	R
0x25	HW_LDAC	[7:0]	Reserved		HW_LDAC_MASK_CH5	HW_LDAC_MASK_CH4	HW_LDAC_MASK_CH3	HW_LDAC_MASK_CH2	HW_LDAC_MASK_CH1	HW_LDAC_MASK_CH0	0x00	R/W
0x26	CH0_DAC_LSB	[7:0]	DAC_DATA0[5:0]						Reserved		0x00	R/W
0x27	CH0_DAC_MSB	[7:0]	DAC_DATA0[13:6]								0x00	R/W
0x28	CH1_DAC_LSB	[7:0]	DAC_DATA1[5:0]						Reserved		0x00	R/W
0x29	CH1_DAC_MSB	[7:0]	DAC_DATA1[13:6]								0x00	R/W
0x2A	CH2_DAC_LSB	[7:0]	DAC_DATA2[5:0]						Reserved		0x00	R/W
0x2B	CH2_DAC_MSB	[7:0]	DAC_DATA2[13:6]								0x00	R/W
0x2C	CH3_DAC_LSB	[7:0]	DAC_DATA3[5:0]						Reserved		0x00	R/W
0x2D	CH3_DAC_MSB	[7:0]	DAC_DATA3[13:6]								0x00	R/W
0x2E	CH4_DAC_LSB	[7:0]	DAC_DATA4[5:0]						Reserved		0x00	R/W
0x2F	CH4_DAC_MSB	[7:0]	DAC_DATA4[13:6]								0x00	R/W
0x30	CH5_DAC_LSB	[7:0]	DAC_DATA5[5:0]						Reserved		0x00	R/W

REGISTER SUMMARY

Table 13. AD5770R Configuration Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x31	CH5_DAC_MSB	[7:0]	DAC_DATA5[13:6]								0x00	R/W
0x32	DAC_PAGE_MASK_LSB	[7:0]	DAC_PAGE_MASK[5:0]						Reserved		0x00	R/W
0x33	DAC_PAGE_MASK_MSB	[7:0]	DAC_PAGE_MASK[13:6]								0x00	R/W
0x34	CH_SELECT	[7:0]	Reserved		SEL_CH5	SEL_CH4	SEL_CH3	SEL_CH2	SEL_CH1	SEL_CH0	0x00	R/W
0x35	INPUT_PAGE_MASK_LSB	[7:0]	INPUT_PAGE_MASK[5:0]						Reserved		0x00	R/W
0x36	INPUT_PAGE_MASK_MSB	[7:0]	INPUT_PAGE_MASK[13:6]								0x00	R/W
0x37	SW_LDAC	[7:0]	Reserved		SW_LDAC_CH5	SW_LDAC_CH4	SW_LDAC_CH3	SW_LDAC_CH2	SW_LDAC_CH1	SW_LDAC_CH0	0x00	W
0x38	CH0_INPUT_LSB	[7:0]	INPUT_DATA0[5:0]						Reserved		0x00	R/W
0x39	CH0_INPUT_MSB	[7:0]	INPUT_DATA0[13:6]								0x00	R/W
0x3A	CH1_INPUT_LSB	[7:0]	INPUT_DATA1[5:0]						Reserved		0x00	R/W
0x3B	CH1_INPUT_MSB	[7:0]	INPUT_DATA1[13:6]								0x00	R/W
0x3C	CH2_INPUT_LSB	[7:0]	INPUT_DATA2[5:0]						Reserved		0x00	R/W
0x3D	CH2_INPUT_MSB	[7:0]	INPUT_DATA2[13:6]								0x00	R/W
0x3E	CH3_INPUT_LSB	[7:0]	INPUT_DATA3[5:0]						Reserved		0x00	R/W
0x3F	CH3_INPUT_MSB	[7:0]	INPUT_DATA3[13:6]								0x00	R/W
0x40	CH4_INPUT_LSB	[7:0]	INPUT_DATA4[5:0]						Reserved		0x00	R/W
0x41	CH4_INPUT_MSB	[7:0]	INPUT_DATA4[13:6]								0x00	R/W
0x42	CH5_INPUT_LSB	[7:0]	INPUT_DATA5[5:0]						Reserved		0x00	R/W
0x43	CH5_	[7:0]	INPUT_DATA5[13:6]								0x00	R/W

REGISTER SUMMARY

Table 13. AD5770R Configuration Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
	INPUT_MSB											
0x44	RESERVED	[7:0]	RESERVED0		RESERVED1						0x3F	R

REGISTER DETAILS

Address: 0x00, Reset: 0x18, Name: INTERFACE_CONFIG_A

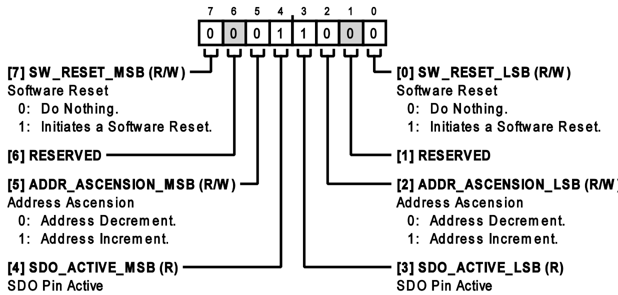


Table 14. Bit Descriptions for INTERFACE_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	SW_RESET_MSB	Software Reset. Setting both software reset bits in a single SPI write will perform a software reset on the part, returning all registers except INTERFACE_CONFIG_A to the default power up state. 0: Do Nothing. 1: Initiates a Software Reset.	0x0	R/W
6	RESERVED	Reserved.	0x0	R
5	ADDR_ASCENSION_MSB	Address Ascension. When set, this bit causes incrementing streaming addresses; otherwise, decrementing addresses are generated. 0: Address Decrement. 1: Address Increment.	0x0	R/W
4	SDO_ACTIVE_MSB	SDO Pin Active. SDO Pin Enabled. This bit is always set.	0x1	R
3	SDO_ACTIVE_LSB	SDO Pin Active. SDO Pin Enabled. This bit is always set.	0x1	R
2	ADDR_ASCENSION_LSB	Address Ascension. When set, this bit causes incrementing streaming addresses; otherwise, decrementing addresses are generated. 0: Address Decrement. 1: Address Increment.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	SW_RESET_LSB	Software Reset. Setting both software reset bits in a single SPI write will perform a software reset on the part, returning all registers except INTERFACE_CONFIG_A to the default power up state. 0: Do Nothing. 1: Initiates a Software Reset.	0x0	R/W

Address: 0x01, Reset: 0x08, Name: INTERFACE_CONFIG_B

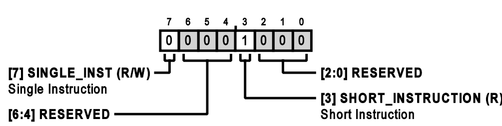


Table 15. Bit Descriptions for INTERFACE_CONFIG_B

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INST	Single Instruction. When this bit is set, streaming mode is disable and each SPI transaction must specify the register address to access.	0x0	R/W

REGISTER DETAILS

Table 15. Bit Descriptions for INTERFACE_CONFIG_B (Continued)

Bits	Bit Name	Description	Reset	Access
		0: Streaming Mode Enabled. 1: Streaming Mode Disabled.		
[6:4]	RESERVED	Reserved.	0x0	R
3	SHORT_INSTRUCTION	Short Instruction. When this bit is clear, the address word must be 7 bits in length.	0x01	R
[2:0]	RESERVED	Reserved.	0x0	R

Address: 0x03, Reset: 0x08, Name: CHIP_TYPE

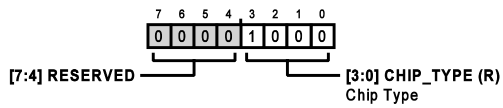


Table 16. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Chip Type. Precision DAC Chip Type = 0x08.	0x8	R

Address: 0x04, Reset: 0x04, Name: PRODUCT_ID_L

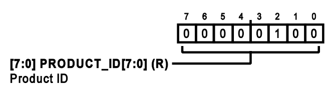


Table 17. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID. AD5770R Product ID = 0x4004.	0x4	R

Address: 0x05, Reset: 0x40, Name: PRODUCT_ID_H

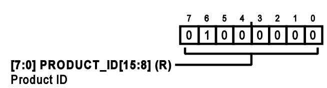


Table 18. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID. AD5770R Product ID = 0x4004.	0x40	R

Address: 0x06, Reset: 0x00, Name: CHIP_GRADE

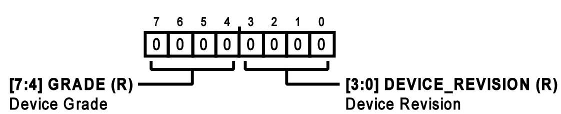


Table 19. Bit Descriptions for CHIP_GRADE

Bits	Bit Name	Description	Reset	Access
[7:4]	GRADE	Device Grade.	0x0	R

REGISTER DETAILS

Table 19. Bit Descriptions for CHIP_GRADE (Continued)

Bits	Bit Name	Description	Reset	Access
[3:0]	DEVICE_REVISION	Device Revision.	0x0	R

Address: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

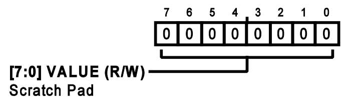


Table 20. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	VALUE	Scratch Pad. This is register can be used to test communication with the device.	0x0	R/W

Address: 0x0B, Reset: 0x82, Name: SPI_REVISION

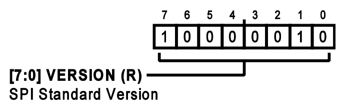


Table 21. Bit Descriptions for SPI_REVISION

Bits	Bit Name	Description	Reset	Access
[7:0]	VERSION	SPI Standard Version. Analog Devices SPI Standard Used.	0x82	R

Address: 0x0C, Reset: 0x56, Name: VENDOR_L

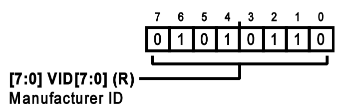
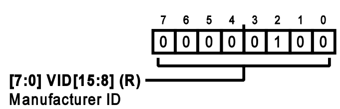


Table 22. Bit Descriptions for VENDOR_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Manufacturer ID. Analog Devices ID = 0x0456.	0x56	R

Address: 0x0D, Reset: 0x04, Name: VENDOR_H



REGISTER DETAILS

Table 23. Bit Descriptions for VENDOR_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Manufacturer ID. Analog Devices ID = 0x0456.	0x4	R

Address: 0x0E, Reset: 0x00, Name: STREAM_MODE

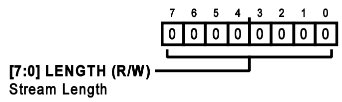


Table 24. Bit Descriptions for STREAM_MODE

Bits	Bit Name	Description	Reset	Access
[7:0]	LENGTH	Stream Length. These bits set the length of registers addresses to increment/decrement when streaming multiple bytes of data before looping back to the first register address. When the contents of this register are cleared, register addresses will increment/decrement when in streaming mode until the end of the address space before looping to the last/first address and continuing to increment/decrement.	0x0	R/W

Address: 0x10, Reset: 0x20, Name: INTERFACE_CONFIG_C

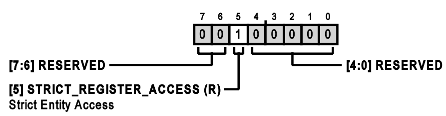


Table 25. Bit Descriptions for INTERFACE_CONFIG_C

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	STRICT_REGISTER_ACCESS	Strict Entity Access. When this bit is set, all multibyte registers must be written to in a single SPI transaction. The address used should be the address of the most significant byte when address ascension is off or the address of the least significant byte when address accession is on.	0x1	R
[4:0]	RESERVED	Reserved.	0x0	R

Address: 0x11, Reset: 0x00, Name: INTERFACE_STATUS_A

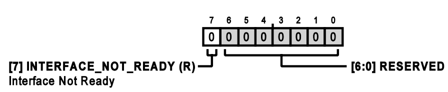


Table 26. Bit Descriptions for INTERFACE_STATUS_A

Bits	Bit Name	Description	Reset	Access
7	INTERFACE_NOT_READY	Interface Not Ready. When this bit is set, the device is not yet ready to receive data on the SPI bus.	0x0	R
[6:0]	RESERVED	Reserved.	0x0	R

Address: 0x14, Reset: 0x80, Name: CHANNEL_CONFIG

REGISTER DETAILS

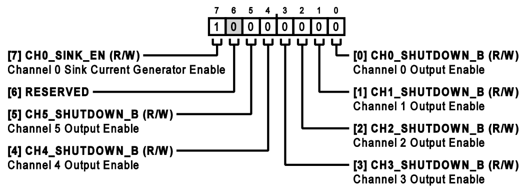


Table 27. Bit Descriptions for CHANNEL_CONFIG

Bits	Bit Name	Description	Reset	Access
7	CH0_SINK_EN	Channel 0 Sink Current Generator Enable. When this bit is set, Channel 0 sink current is enabled. 0: Disable. 1: Enable.	0x1	R/W
6	RESERVED	Reserved.	0x0	R
5	CH5_SHUTDOWN_B	Channel 5 Output Enable. This active low enable bit shuts down the output of IDAC5 when asserted. 0: Output Shutdown. 1: Normal Operation.	0x0	R/W
4	CH4_SHUTDOWN_B	Channel 4 Output Enable. This active low enable bit shuts down the output of IDAC4 when asserted. 0: Output Shutdown. 1: Normal Operation.	0x0	R/W
3	CH3_SHUTDOWN_B	Channel 3 Output Enable. This active low enable bit shuts down the output of IDAC3 when asserted. 0: Output Shutdown. 1: Normal Operation.	0x0	R/W
2	CH2_SHUTDOWN_B	Channel 2 Output Enable. This active low enable bit shuts down the output of IDAC2 when asserted. 0: Output Shutdown. 1: Normal Operation.	0x0	R/W
1	CH1_SHUTDOWN_B	Channel 1 Output Enable. This active low enable bit shuts down the output of IDAC1 when asserted. 0: Output Shutdown. 1: Normal Operation.	0x0	R/W
0	CH0_SHUTDOWN_B	Channel 0 Output Enable. This active low enable bit shuts down the output of IDAC0 when asserted. 0: Output Shutdown. 1: Normal Operation.	0x0	R/W

Address: 0x15, Reset: 0x00, Name: OUTPUT_RANGE_CH0

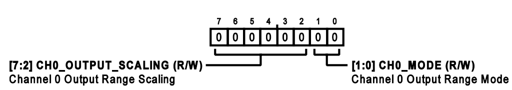


Table 28. Bit Descriptions for OUTPUT_RANGE_CH0

Bits	Bit Name	Description	Reset	Access
[7:2]	CH0_OUTPUT_SCALING	Channel 0 Output Range Scaling. These bits set the output range scaling factor for Channel 0. Output scaling must only be used when in a sourcing current mode.	0x0	R/W
[1:0]	CH0_MODE	Channel 0 Output Range Mode. These bits select the output range mode for Channel 0. 00: 0mA to 300mA. 01: -60mA to 0mA. 10: -60mA to 300mA.	0x0	R/W

REGISTER DETAILS

Address: 0x16, Reset: 0x02, Name: OUTPUT_RANGE_CH1

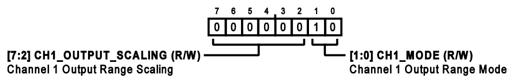


Table 29. Bit Descriptions for OUTPUT_RANGE_CH1

Bits	Bit Name	Description	Reset	Access
[7:2]	CH1_OUTPUT_SCALING	Channel 1 Output Range Scaling. These bits set the output range scaling factor for channel 1.	0x0	R/W
[1:0]	CH1_MODE	Channel 1 Output Range Mode. These bits select the output range mode for channel 1. 01: 0mA to 140mA - Low Headroom. 10: 0mA to 140mA - Low Noise. 11: 0mA to 250mA.	0x2	R/W

Address: 0x17, Reset: 0x00, Name: OUTPUT_RANGE_CH2

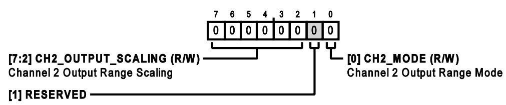


Table 30. Bit Descriptions for OUTPUT_RANGE_CH2

Bits	Bit Name	Description	Reset	Access
[7:2]	CH2_OUTPUT_SCALING	Channel 2 Output Range Scaling. These bits set the output range scaling factor for Channel 2.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	CH2_MODE	Channel 2 Output Range Mode. This bit selects the output range mode for Channel 2. 0: 0mA to 55mA. 1: 0mA to 150mA.	0x0	R/W

Address: 0x18, Reset: 0x00, Name: OUTPUT_RANGE_CH3

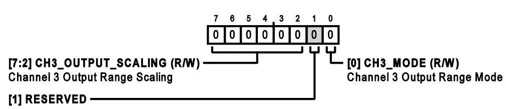


Table 31. Bit Descriptions for OUTPUT_RANGE_CH3

Bits	Bit Name	Description	Reset	Access
[7:2]	CH3_OUTPUT_SCALING	Channel 3 Output Range Scaling. These bits set the output range scaling factor for Channel 3.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	CH3_MODE	Channel 3 Output Range Mode. This bit selects the output range mode for Channel 3. 0: 0mA to 45mA. 1: 0mA to 100mA.	0x0	R/W

Address: 0x19, Reset: 0x00, Name: OUTPUT_RANGE_CH4

REGISTER DETAILS

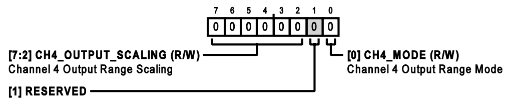


Table 32. Bit Descriptions for OUTPUT_RANGE_CH4

Bits	Bit Name	Description	Reset	Access
[7:2]	CH4_OUTPUT_SCALING	Channel 4 Output Range Scaling. These bits set the output range scaling factor for Channel 4.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	CH4_MODE	Channel 4 Output Range Mode. This bit selects the output range mode for Channel 4. 0: 0mA to 45mA. 1: 0mA to 100mA.	0x0	R/W

Address: 0x1A, Reset: 0x00, Name: OUTPUT_RANGE_CH5

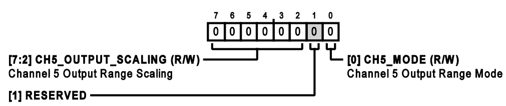


Table 33. Bit Descriptions for OUTPUT_RANGE_CH5

Bits	Bit Name	Description	Reset	Access
[7:2]	CH5_OUTPUT_SCALING	Channel 5 Output Range Scaling. These bits set the output range scaling factor for Channel 5.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	CH5_MODE	Channel 5 Output Range Mode. This bit selects the output range mode for Channel 5. 0: 0mA to 45mA. 1: 0mA to 100mA.	0x0	R/W

Address: 0x1B, Reset: 0x00, Name: REFERENCE

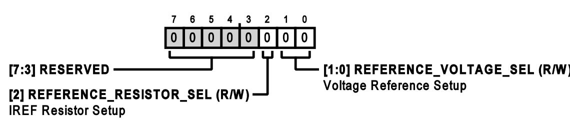


Table 34. Bit Descriptions for REFERENCE

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	REFERENCE_RESISTOR_SEL	IREF Resistor Setup. This bit select whether an internal or external resistor is used for reference current generation. 0: Internal Resistor. 1: External Resistor.	0x0	R/W
[1:0]	REFERENCE_VOLTAGE_SEL	Voltage Reference Setup. These bits select configure the voltage reference scheme used for reference current generation. 00: External 2.5V. 01: Internal 1.25V (Reference Output On). 10: External 1.25V. 11: Internal 1.25V (Reference Output Off).	0x0	R/W

Address: 0x1C, Reset: 0x06, Name: ALARM_CONFIG

REGISTER DETAILS

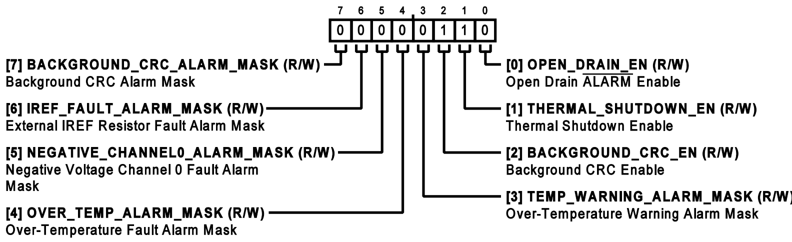


Table 35. Bit Descriptions for ALARM_CONFIG

Bits	Bit Name	Description	Reset	Access
7	BACKGROUND_CRC_ALARM_MASK	Background CRC Alarm Mask. When this bit is set, the $\overline{\text{ALARM}}$ pin does not activate for Background CRC errors. 0: Normal Operation. 1: Mask Background CRC $\overline{\text{ALARM}}$ Activation.	0x0	R/W
6	IREF_FAULT_ALARM_MASK	External IREF Resistor Fault Alarm Mask. When this bit is set, the $\overline{\text{ALARM}}$ pin does not activate for external reference current generation resistor faults. 0: Normal Operation. 1: Mask IREF Fault $\overline{\text{ALARM}}$ Activation.	0x0	R/W
5	NEGATIVE_CHANNEL0_ALARM_MASK	Negative Voltage Channel 0 Fault Alarm Mask. When this bit is set, the $\overline{\text{ALARM}}$ pin does not activate when a negative voltage is multiplexed to the MUX_OUT pin due to monitoring channel 0. 0: Normal Operation. 1: Mask Negative Channel 0 $\overline{\text{ALARM}}$ Activation.	0x0	R/W
4	OVER_TEMP_ALARM_MASK	Over-Temperature Fault Alarm Mask. When this bit is set, the $\overline{\text{ALARM}}$ pin does not activate for an over-temperature fault occurrence. 0: Normal Operation. 1: Mask Over Temperature $\overline{\text{ALARM}}$ Activation.	0x0	R/W
3	TEMP_WARNING_ALARM_MASK	Over-Temperature Warning Alarm Mask. When this bit is set, the $\overline{\text{ALARM}}$ pin does not activate for an over-temperature warning occurrence. 0: Normal Operation. 1: Mask Temperature Warning $\overline{\text{ALARM}}$ Activation.	0x0	R/W
2	BACKGROUND_CRC_EN	Background CRC Enable. When this bit is set, a CRC of the memory map contents is periodically computed by the part. 0: Disable Background CRC. 1: Enable Background CRC.	0x1	R/W
1	THERMAL_SHUTDOWN_EN	Thermal Shutdown Enable. When this bit is set, the AD5770R goes into thermal shutdown in the event of an overtemperature fault. 0: Disable Thermal Shutdown - Not Recommended. 1: Enable Thermal Shutdown.	0x1	R/W
0	OPEN_DRAIN_EN	Open Drain $\overline{\text{ALARM}}$ Enable. When this bit is set, the $\overline{\text{ALARM}}$ pin is configured as an open drain output. 0: $\overline{\text{ALARM}}$ Open Drain Disable. 1: $\overline{\text{ALARM}}$ Open Drain Enable.	0x0	R/W

Address: 0x1D, Reset: 0x00, Name: OUTPUT_FILTER_CH0

REGISTER DETAILS

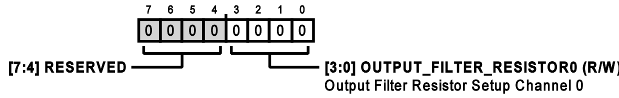


Table 36. Bit Descriptions for OUTPUT_FILTER_CH0

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	OUTPUT_FILTER_RESISTOR0	Output Filter Resistor Setup Channel 0. These bits select the internal variable resistor to be used for the output filter on channel 0. The output filter resistor creates an RC filter with the CDAMP_IDAC0 capacitor. 0000: 60 Ohm. 0101: 5.6 kOhm. 0110: 11.2 kOhm. 0111: 22.2 kOhm. 1000: 44.4 kOhm. 1001: 104 kOhm.	0x0	R/W

Address: 0x1E, Reset: 0x00, Name: OUTPUT_FILTER_CH1

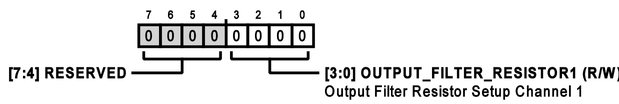


Table 37. Bit Descriptions for OUTPUT_FILTER_CH1

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	OUTPUT_FILTER_RESISTOR1	Output Filter Resistor Setup Channel 1. These bits select the internal variable resistor to be used for the output filter on channel 1. The output filter resistor creates an RC filter with the CDAMP_IDAC1 capacitor. 0000: 60 Ohm. 0101: 5.6 kOhm. 0110: 11.2 kOhm. 0111: 22.2 kOhm. 1000: 44.4 kOhm. 1001: 104 kOhm.	0x0	R/W

Address: 0x1F, Reset: 0x00, Name: OUTPUT_FILTER_CH2

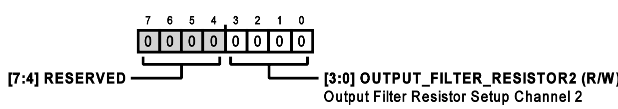


Table 38. Bit Descriptions for OUTPUT_FILTER_CH2

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	OUTPUT_FILTER_RESISTOR2	Output Filter Resistor Setup Channel 2. These bits select the internal variable resistor to be used for the output filter on Channel 2. The output filter resistor creates an RC filter with the CDAMP_IDAC2 capacitor. 0000: 60 Ohm. 0101: 5.6 kOhm. 0110: 11.2 kOhm. 0111: 22.2 kOhm.	0x0	R/W

REGISTER DETAILS

Table 38. Bit Descriptions for OUTPUT_FILTER_CH2 (Continued)

Bits	Bit Name	Description	Reset	Access
		1000: 44.4 kOhm. 1001: 104 kOhm.		

Address: 0x20, Reset: 0x00, Name: OUTPUT_FILTER_CH3

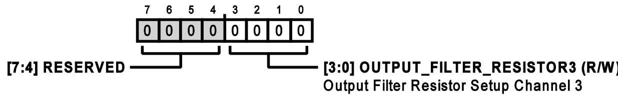


Table 39. Bit Descriptions for OUTPUT_FILTER_CH3

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	OUTPUT_FILTER_RESISTOR3	Output Filter Resistor Setup Channel 3. These bits select the internal variable resistor to be used for the output filter on Channel 3. The output filter resistor creates an RC filter with the CDAMP_IDAC3 capacitor. 0000: 60 Ohm. 0101: 5.6 kOhm. 0110: 11.2 kOhm. 0111: 22.2 kOhm. 1000: 44.4 kOhm. 1001: 104 kOhm.	0x0	R/W

Address: 0x21, Reset: 0x00, Name: OUTPUT_FILTER_CH4

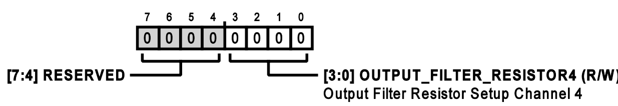


Table 40. Bit Descriptions for OUTPUT_FILTER_CH4

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	OUTPUT_FILTER_RESISTOR4	Output Filter Resistor Setup Channel 4. These bits select the internal variable resistor to be used for the output filter on channel 4. The output filter resistor creates an RC filter with the CDAMP_IDAC4 capacitor. 0000: 60 Ohm. 0101: 5.6 kOhm. 0110: 11.2 kOhm. 0111: 22.2 kOhm. 1000: 44.4 kOhm. 1001: 104 kOhm.	0x0	R/W

Address: 0x22, Reset: 0x00, Name: OUTPUT_FILTER_CH5

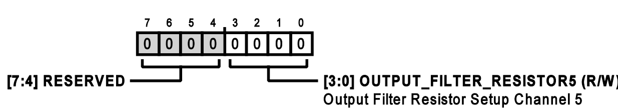


Table 41. Bit Descriptions for OUTPUT_FILTER_CH5

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 41. Bit Descriptions for OUTPUT_FILTER_CH5 (Continued)

Bits	Bit Name	Description	Reset	Access
[3:0]	OUTPUT_FILTER_RESISTOR5	Output Filter Resistor Setup Channel 5. These bits select the internal variable resistor to be used for the output filter on channel 5. The output filter resistor creates an RC filter with the CDAMP_IDAC5 capacitor. 0000: 60 Ohm. 0101: 5.6 kOhm. 0110: 11.2 kOhm. 0111: 22.2 kOhm. 1000: 44.4 kOhm. 1001: 104 kOhm.	0x0	R/W

Address: 0x23, Reset: 0x00, Name: MONITOR_SETUP

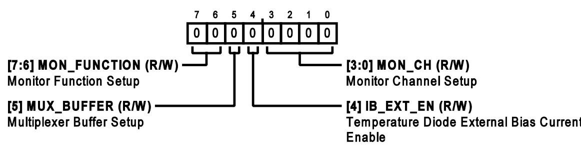


Table 42. Bit Descriptions for MONITOR_SETUP

Bits	Bit Name	Description	Reset	Access
[7:6]	MON_FUNCTION	Monitor Function Setup. These bits configure which on-chip diagnostic function is selected. 00: Disable. 01: Voltage Monitoring. 10: Current Monitoring. 11: Temperature Monitoring.	0x0	R/W
5	MUX_BUFFER	Multiplexer Buffer Setup. When this bit is set, the multiplexer buffer is enabled and used to buffer the multiplexer output. Clearing this bit disables the buffer and bypasses it. 0: Bypass. 1: Enable.	0x0	R/W
4	IB_EXT_EN	Temperature Diode External Bias Current Enable. When this bit is set, an internal bias current for the temperature monitoring diode is shut off. This bias current must then be supplied externally. 0: Internal Bias Current. 1: External Bias Current.	0x0	R/W
[3:0]	MON_CH	Monitor Channel Setup. These bits select the channel to be monitored when output voltage or output current diagnostics are enabled. 000: Channel 0. 001: Channel 1. 010: Channel 2. 011: Channel 3. 100: Channel 4. 101: Channel 5.	0x0	R/W

Address: 0x24, Reset: 0x00, Name: STATUS

REGISTER DETAILS

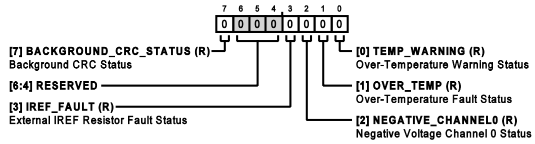
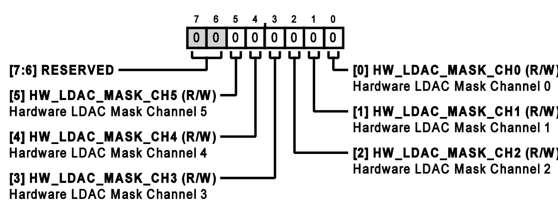


Table 43. Bit Descriptions for STATUS

Bits	Bit Name	Description	Reset	Access
7	BACKGROUND_CRC_STATUS	Background CRC Status. Read only status bit. When this bit is high, this signified that a background CRC of the memory map has failed and a memory bit may have inadvertently flipped. 0: Normal. 1: Background CRC Error Activated.	0x0	R
[6:4]	RESERVED	Reserved.	0x0	R
3	IREF_FAULT	External IREF Resistor Fault Status. Read only status bit. When this bit is set, a fault has been detected with the external reference current generation resistor and the internal resistor has been switched in to avoid damage to the part. 0: Normal. 1: IREF Fault Activated.	0x0	R
2	NEGATIVE_CHANNEL0	Negative Voltage Channel 0 Status. Read only status bit. When this bit is set, a fault has been detected due to a negative voltage being multiplexed to the MUX_OUT pin when monitoring channel 0. 0: Normal. 1: Negative Channel 0 Activated.	0x0	R
1	OVER_TEMP	Over-Temperature Fault Status. Read only status bit. When this bit is set, an over-temperature fault occurrence has been detected. Over-temperature fault occurs when the internal die temperature reaches approx. 145°C. A reset command must be issued to the part to clear this bit. 0: Normal. 1: Over Temperature Activated.	0x0	R
0	TEMP_WARNING	Over-Temperature Warning Status. Read only status bit. When this bit is set, an over-temperature warning occurrence has been detected. Over-temperature warning occurs when the internal die temperature reaches approx. 125°C. This bit is automatically cleared when the internal die temperature returns to below 120°C. 0: Normal. 1: Temperature Warning Activated.	0x0	R

Address: 0x25, Reset: 0x00, Name: HW_LDAC



REGISTER DETAILS

Table 44. Bit Descriptions for HW_LDAC

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	HW_LDAC_MASK_CH5	Hardware LDAC Mask Channel 5. When this bit is set, activity on the $\overline{\text{LDAC}}$ pin is ignored for channel 5. 0: No Operation. 1: Mask $\overline{\text{LDAC}}$ on Channel 5.	0x0	R/W
4	HW_LDAC_MASK_CH4	Hardware LDAC Mask Channel 4. When this bit is set, activity on the $\overline{\text{LDAC}}$ pin is ignored for channel 4. 0: No Operation. 1: Mask $\overline{\text{LDAC}}$ on Channel 4.	0x0	R/W
3	HW_LDAC_MASK_CH3	Hardware LDAC Mask Channel 3. When this bit is set, activity on the $\overline{\text{LDAC}}$ pin is ignored for channel 3. 0: No Operation. 1: Mask $\overline{\text{LDAC}}$ on Channel 3.	0x0	R/W
2	HW_LDAC_MASK_CH2	Hardware LDAC Mask Channel 2. When this bit is set, activity on the $\overline{\text{LDAC}}$ pin is ignored for channel 2. 0: No Operation. 1: Mask $\overline{\text{LDAC}}$ on Channel 2.	0x0	R/W
1	HW_LDAC_MASK_CH1	Hardware LDAC Mask Channel 1. When this bit is set, activity on the $\overline{\text{LDAC}}$ pin is ignored for channel 1. 0: No Operation. 1: Mask $\overline{\text{LDAC}}$ on Channel 1.	0x0	R/W
0	HW_LDAC_MASK_CH0	Hardware LDAC Mask Channel 0. When this bit is set, activity on the $\overline{\text{LDAC}}$ pin is ignored for channel 0. 0: No Operation. 1: Mask $\overline{\text{LDAC}}$ on Channel 0.	0x0	R/W

Address: 0x26, Reset: 0x00, Name: CH0_DAC_LSB

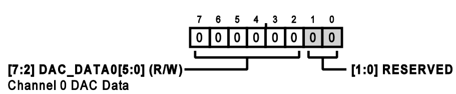


Table 45. Bit Descriptions for CH0_DAC_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	DAC_DATA0[5:0]	Channel 0 DAC Data. This is the DAC code loaded into the DAC register for IDAC0.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x27, Reset: 0x00, Name: CH0_DAC_MSB

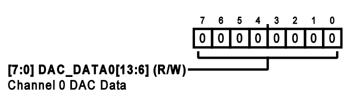


Table 46. Bit Descriptions for CH0_DAC_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	DAC_DATA0[13:6]	Channel 0 DAC Data. This is the DAC code loaded into the DAC register for IDAC0.	0x0	R/W

REGISTER DETAILS

Address: 0x28, Reset: 0x00, Name: CH1_DAC_LSB

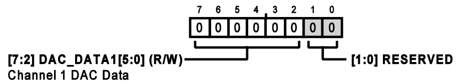


Table 47. Bit Descriptions for CH1_DAC_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	DAC_DATA1[5:0]	Channel 1 DAC Data. This is the DAC code loaded into the DAC register for IDAC1.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x29, Reset: 0x00, Name: CH1_DAC_MSB

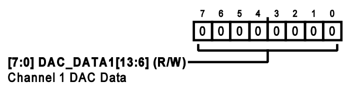


Table 48. Bit Descriptions for CH1_DAC_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	DAC_DATA1[13:6]	Channel 1 DAC Data. This is the DAC code loaded into the DAC register for IDAC1.	0x0	R/W

Address: 0x2A, Reset: 0x00, Name: CH2_DAC_LSB

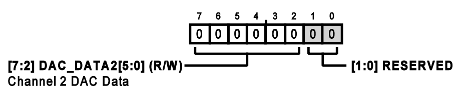


Table 49. Bit Descriptions for CH2_DAC_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	DAC_DATA2[5:0]	Channel 2 DAC Data. This is the DAC code loaded into the DAC register for IDAC2.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x2B, Reset: 0x00, Name: CH2_DAC_MSB

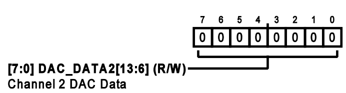


Table 50. Bit Descriptions for CH2_DAC_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	DAC_DATA2[13:6]	Channel 2 DAC Data. This is the DAC code loaded into the DAC register for IDAC2.	0x0	R/W

Address: 0x2C, Reset: 0x00, Name: CH3_DAC_LSB

REGISTER DETAILS

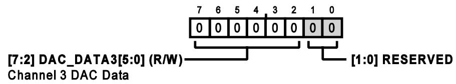


Table 51. Bit Descriptions for CH3_DAC_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	DAC_DATA3[5:0]	Channel 3 DAC Data. This is the DAC code loaded into the DAC register for IDAC3.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x2D, Reset: 0x00, Name: CH3_DAC_MSB

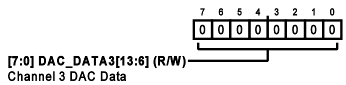


Table 52. Bit Descriptions for CH3_DAC_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	DAC_DATA3[13:6]	Channel 3 DAC Data. This is the DAC code loaded into the DAC register for IDAC3.	0x0	R/W

Address: 0x2E, Reset: 0x00, Name: CH4_DAC_LSB

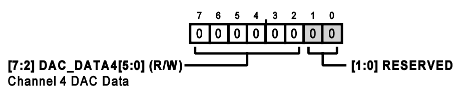


Table 53. Bit Descriptions for CH4_DAC_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	DAC_DATA4[5:0]	Channel 4 DAC Data. This is the DAC code loaded into the DAC register for IDAC4.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x2F, Reset: 0x00, Name: CH4_DAC_MSB

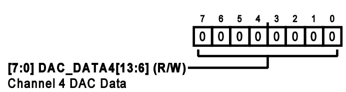
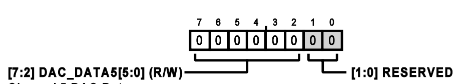


Table 54. Bit Descriptions for CH4_DAC_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	DAC_DATA4[13:6]	Channel 4 DAC Data. This is the DAC code loaded into the DAC register for IDAC4.	0x0	R/W

Address: 0x30, Reset: 0x00, Name: CH5_DAC_LSB



REGISTER DETAILS

Table 55. Bit Descriptions for CH5_DAC_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	DAC_DATA5[5:0]	Channel 5 DAC Data. This is the DAC code loaded into the DAC register for IDAC5.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x31, Reset: 0x00, Name: CH5_DAC_MSB

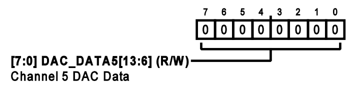


Table 56. Bit Descriptions for CH5_DAC_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	DAC_DATA5[13:6]	Channel 5 DAC Data. This is the DAC code loaded into the DAC register for IDAC5.	0x0	R/W

Address: 0x32, Reset: 0x00, Name: DAC_PAGE_MASK_LSB

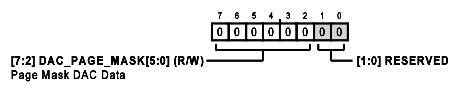


Table 57. Bit Descriptions for DAC_PAGE_MASK_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	DAC_PAGE_MASK[5:0]	Page Mask DAC Data. Following a write to this register, the DAC code loaded into this register is copied into the DAC register of any channels selected in the CH_SELECT register.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x33, Reset: 0x00, Name: DAC_PAGE_MASK_MSB

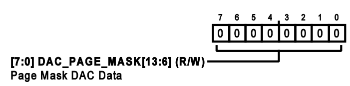


Table 58. Bit Descriptions for DAC_PAGE_MASK_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	DAC_PAGE_MASK[13:6]	Page Mask DAC Data. Following a write to this register, the DAC code loaded into this register is copied into the DAC register of any channels selected in the CH_SELECT register.	0x0	R/W

Address: 0x34, Reset: 0x00, Name: CH_SELECT

REGISTER DETAILS

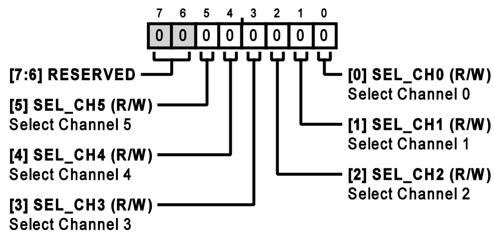
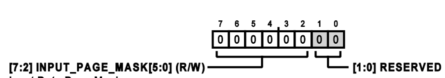


Table 59. Bit Descriptions for CH_SELECT

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	SEL_CH5	Select Channel 5. When this bit is set, data written to the INPUT_PAGE_MASK register will be copied to the INPUT_DATA5 register and data written to the DAC_PAGE_MASK register will be copied to the DAC_DATA5 register. 0: No Operation. 1: Copy to Channel 5.	0x0	R/W
4	SEL_CH4	Select Channel 4. When this bit is set, data written to the INPUT_PAGE_MASK register will be copied to the INPUT_DATA4 register and data written to the DAC_PAGE_MASK register will be copied to the DAC_DATA4 register. 0: No Operation. 1: Copy to Channel 4.	0x0	R/W
3	SEL_CH3	Select Channel 3. When this bit is set, data written to the INPUT_PAGE_MASK register will be copied to the INPUT_DATA3 register and data written to the DAC_PAGE_MASK register will be copied to the DAC_DATA3 register. 0: No Operation. 1: Copy to Channel 3.	0x0	R/W
2	SEL_CH2	Select Channel 2. When this bit is set, data written to the INPUT_PAGE_MASK register will be copied to the INPUT_DATA2 register and data written to the DAC_PAGE_MASK register will be copied to the DAC_DATA2 register. 0: No Operation. 1: Copy to Channel 2.	0x0	R/W
1	SEL_CH1	Select Channel 1. When this bit is set, data written to the INPUT_PAGE_MASK register will be copied to the INPUT_DATA1 register and data written to the DAC_PAGE_MASK register will be copied to the DAC_DATA1 register. 0: No Operation. 1: Copy to Channel 1.	0x0	R/W
0	SEL_CH0	Select Channel 0. When this bit is set, data written to the INPUT_PAGE_MASK register will be copied to the INPUT_DATA0 register and data written to the DAC_PAGE_MASK register will be copied to the DAC_DATA0 register. 0: No Operation. 1: Copy to Channel 0.	0x0	R/W

Address: 0x35, Reset: 0x00, Name: INPUT_PAGE_MASK_LSB



REGISTER DETAILS

Table 60. Bit Descriptions for INPUT_PAGE_MASK_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	INPUT_PAGE_MASK[5:0]	Input Data Page Mask. Following a write to this register, the DAC code loaded into this register is copied into the input register of any channels selected in the CH_SELECT register.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x36, Reset: 0x00, Name: INPUT_PAGE_MASK_MSB

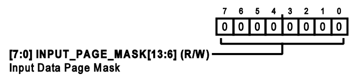


Table 61. Bit Descriptions for INPUT_PAGE_MASK_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	INPUT_PAGE_MASK[13:6]	Input Data Page Mask. Following a write to this register, the DAC code loaded into this register is copied into the input register of any channels selected in the CH_SELECT register.	0x0	R/W

Address: 0x37, Reset: 0x00, Name: SW_LDAC

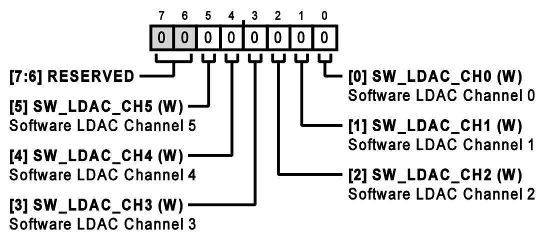


Table 62. Bit Descriptions for SW_LDAC

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	SW_LDAC_CH5	Software LDAC Channel 5. Setting this bit will transfer contents from the INPUT_DATA5 register to the DAC_DATA5 register. This bit automatically resets after a write to the SW_LDAC register. 0: No Operation. 1: Load DAC 5.	0x0	W
4	SW_LDAC_CH4	Software LDAC Channel 4. Setting this bit will transfer contents from the INPUT_DATA4 register to the DAC_DATA4 register. This bit automatically resets after a write to the SW_LDAC register. 0: No Operation. 1: Load DAC 4.	0x0	W
3	SW_LDAC_CH3	Software LDAC Channel 3. Setting this bit will transfer contents from the INPUT_DATA3 register to the DAC_DATA3 register. This bit automatically resets after a write to the SW_LDAC register. 0: No Operation. 1: Load DAC 3.	0x0	W
2	SW_LDAC_CH2	Software LDAC Channel 2. Setting this bit will transfer contents from the INPUT_DATA2 register to the DAC_DATA2 register. This bit automatically resets after a write to the SW_LDAC register. 0: No Operation. 1: Load DAC 2.	0x0	W

REGISTER DETAILS

Table 62. Bit Descriptions for SW_LDAC (Continued)

Bits	Bit Name	Description	Reset	Access
1	SW_LDAC_CH1	Software LDAC Channel 1. Setting this bit will transfer contents from the INPUT_DATA1 register to the DAC_DATA1 register. This bit automatically resets after a write to the SW_LDAC register. 0: No Operation. 1: Load DAC 1.	0x0	W
0	SW_LDAC_CH0	Software LDAC Channel 0. Setting this bit will transfer contents from the INPUT_DATA0 register to the DAC_DATA0 register. This bit automatically resets after a write to the SW_LDAC register. 0: No Operation. 1: Load DAC 0.	0x0	W

Address: 0x38, Reset: 0x00, Name: CH0_INPUT_LSB

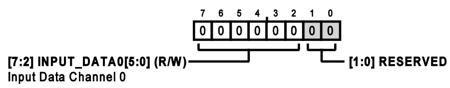


Table 63. Bit Descriptions for CH0_INPUT_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	INPUT_DATA0[5:0]	Input Data Channel 0. This is the DAC code loaded into the input register for IDAC0.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x39, Reset: 0x00, Name: CH0_INPUT_MSB

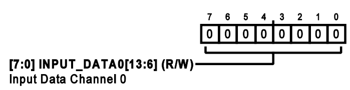


Table 64. Bit Descriptions for CH0_INPUT_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	INPUT_DATA0[13:6]	Input Data Channel 0. This is the DAC code loaded into the input register for IDAC0.	0x0	R/W

Address: 0x3A, Reset: 0x00, Name: CH1_INPUT_LSB

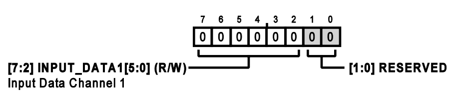


Table 65. Bit Descriptions for CH1_INPUT_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	INPUT_DATA1[5:0]	Input Data Channel 1. This is the DAC code loaded into the input register for IDAC1.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x3B, Reset: 0x00, Name: CH1_INPUT_MSB

REGISTER DETAILS

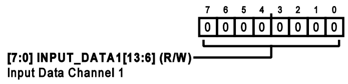


Table 66. Bit Descriptions for CH1_INPUT_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	INPUT_DATA1[13:6]	Input Data Channel 1. This is the DAC code loaded into the input register for IDAC1.	0x0	R/W

Address: 0x3C, Reset: 0x00, Name: CH2_INPUT_LSB

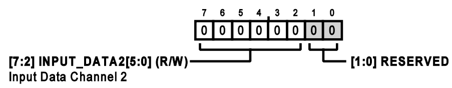


Table 67. Bit Descriptions for CH2_INPUT_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	INPUT_DATA2[5:0]	Input Data Channel 2. This is the DAC code loaded into the input register for IDAC2.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x3D, Reset: 0x00, Name: CH2_INPUT_MSB

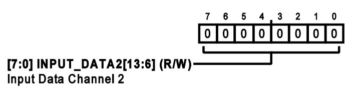


Table 68. Bit Descriptions for CH2_INPUT_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	INPUT_DATA2[13:6]	Input Data Channel 2. This is the DAC code loaded into the input register for IDAC2.	0x0	R/W

Address: 0x3E, Reset: 0x00, Name: CH3_INPUT_LSB

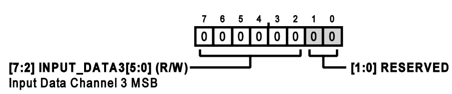
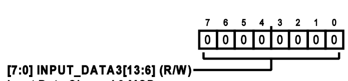


Table 69. Bit Descriptions for CH3_INPUT_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	INPUT_DATA3[5:0]	Input Data Channel 3 MSB. This is the DAC code loaded into the input register for IDAC3.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x3F, Reset: 0x00, Name: CH3_INPUT_MSB



REGISTER DETAILS

Table 70. Bit Descriptions for CH3_INPUT_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	INPUT_DATA3[13:6]	Input Data Channel 3 MSB. This is the DAC code loaded into the input register for IDAC3.	0x0	R/W

Address: 0x40, Reset: 0x00, Name: CH4_INPUT_LSB

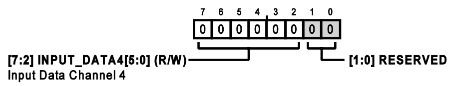


Table 71. Bit Descriptions for CH4_INPUT_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	INPUT_DATA4[5:0]	Input Data Channel 4. This is the DAC code loaded into the input register for IDAC4.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x41, Reset: 0x00, Name: CH4_INPUT_MSB

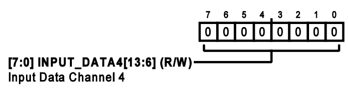


Table 72. Bit Descriptions for CH4_INPUT_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	INPUT_DATA4[13:6]	Input Data Channel 4. This is the DAC code loaded into the input register for IDAC4.	0x0	R/W

Address: 0x42, Reset: 0x00, Name: CH5_INPUT_LSB

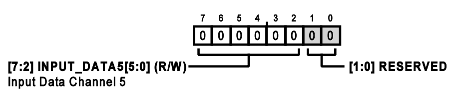


Table 73. Bit Descriptions for CH5_INPUT_LSB

Bits	Bit Name	Description	Reset	Access
[7:2]	INPUT_DATA5[5:0]	Input Data Channel 5. This is the DAC code loaded into the input register for IDAC5.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x43, Reset: 0x00, Name: CH5_INPUT_MSB

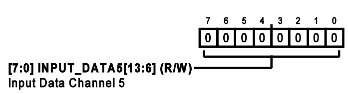


Table 74. Bit Descriptions for CH5_INPUT_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	INPUT_DATA5[13:6]	Input Data Channel 5. This is the DAC code loaded into the input register for IDAC5.	0x0	R/W

Address: 0x44, Reset: 0x3F, Name: RESERVED

REGISTER DETAILS

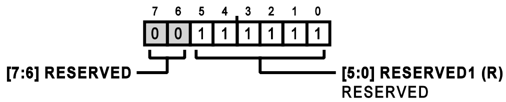


Table 75. Bit Descriptions for RESERVED

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	RESERVED1	RESERVED.	0x3F	R

OUTLINE DIMENSIONS

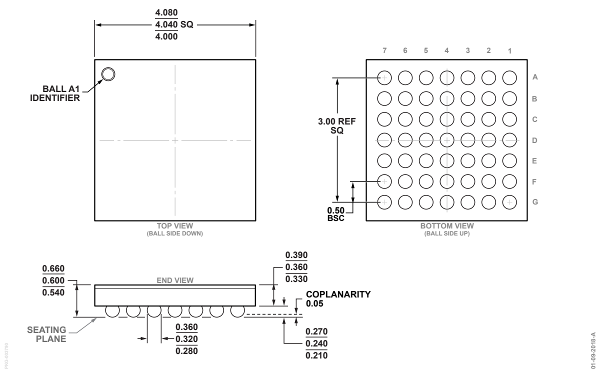


Figure 78. 49-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-49-5)
Dimensions shown in millimeters

Updated: February 06, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD5770RBCBZ-RL7	-40°C to +105°C	49-Ball WLCSP (4.04 mm x 4.04 mm x 0.60 mm)	Reel, 1500	CB-49-5

1 Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-AD5770RSDZ	Evaluation Board

1 Z = RoHS Compliant Part.