Octal, 16-Bit nanoDAC+ with SPI Interface

FEATURES

- High performance
  - High relative accuracy (INL): ±3 LSB maximum at 16 bits
  - Total unadjusted error (TUE): ±0.14% of FSR maximum
  - Offset error: ±1.5 mV maximum
  - Gain error: ±0.06% of FSR maximum
- Wide operating ranges
  - −40°C to +125°C temperature range
  - 2.7 V to 5.5 V power supply
- Easy implementation
  - User selectable gain of 1 or 2 (GAIN pin/gain bit)
  - Reset to zero scale or midscale (RSTSEL pin)
  - 1.8 V logic compatibility
- 50 MHz SPI with readback or daisy chain
- 20-lead, TSSOP and LFCSP RoHS-compliant packages

APPLICATIONS

- Optical transceivers
- Base station power amplifiers
- Process control (PLC input/output cards)
- Industrial automation
- Data acquisition systems

GENERAL DESCRIPTION

The AD5676 is a low power, octal, 16-bit buffered voltage output digital-to-analog converter (DAC). The device includes a gain select pin, giving a full-scale output of V_{REF} (gain = 1) or 2 × V_{REF} (gain = 2). The AD5676 DAC operates from a single 2.7 V to 5.5 V supply and is guaranteed monotonic by design. The AD5676 is available in 20-lead TSSOP and LFCSP packages.

The internal power-on reset circuit and the RSTSEL pin of the AD5676 ensure that the output DACs power up to zero scale or midscale and then remain there until a valid write takes place. The AD5676 contains a per channel power-down mode that typically reduces the current consumption of the device to 1 µA.

The AD5676 employs a versatile serial peripheral interface (SPI) that operates at clock rates up to 50 MHz, and contains a V_{LOGIC} pin intended for 1.62 V to 5.5 V logic.

Table 1. Octal nanoDAC+® Devices

Interface	Reference	16-Bit	12-Bit
SPI	Internal	AD5676R	AD5672R
	External	AD5676	Not applicable
I²C	Internal	AD5675R	AD5671R
	External	AD5675	Not applicable

PRODUCT HIGHLIGHTS

1. High relative accuracy (INL) 16-bit: ±3 LSB maximum.
2. −40°C to +125°C temperature range.
3. 20-lead, TSSOP and LFCSP RoHS-compliant packages.

FUNCTIONAL BLOCK DIAGRAM

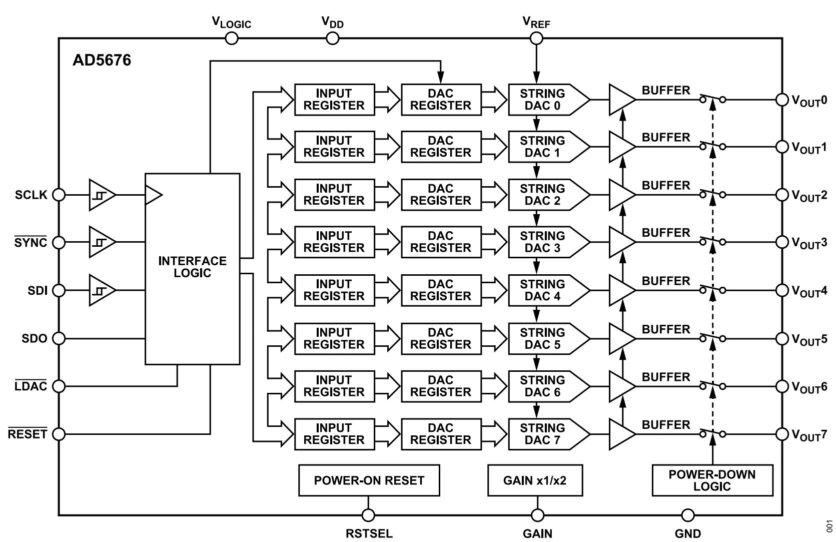

Figure 1.

DOCUMENT FEEDBACK
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REVISION HISTORY

7/2023—Rev. D to Rev. E

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, resistive load (R_L) = 2 kΩ, capacitive load (C_L) = 200 pF, all specifications −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[1]								
Resolution	16			16			Bits	
Relative Accuracy (INL)[2]		±1.8	±8		±1.8	±3	LSB	Gain = 1
		±1.7	±8		±1.7	±3	LSB	Gain = 2
Differential Nonlinearity (DNL)[2]		±0.7	±1		±0.7	±1	LSB	Gain = 1
		±0.5	±1		±0.5	±1	LSB	Gain = 2
Zero Code Error[2]		0.8	4		0.8	1.6	mV	Gain = 1 or gain = 2
Offset Error[2]		−0.75	±6		−0.75	±2	mV	Gain = 1
		−0.1	±4		−0.1	±1.5	mV	Gain = 2
Full-Scale Error[2]		−0.018	±0.28		−0.018	±0.14	% of full-scale range (FSR)	Gain = 1
		−0.013	±0.14		−0.013	±0.07	% of FSR	Gain = 2
Gain Error[2]		+0.04	±0.24		+0.04	±0.12	% of FSR	Gain = 1
		−0.02	±0.12		−0.02	±0.06	% of FSR	Gain = 2
Total Unadjusted Error (TUE)		+0.03	±0.3		+0.03	±0.18	% of FSR	Gain = 1
		+0.006	±0.25		+0.006	±0.14	% of FSR	Gain = 2
Offset Error Drift[2]		±1			±1		µV/°C	
DC Power Supply Rejection Ratio (PSRR)[2]		0.25			0.25		mV/V	DAC code = midscale, V_{DD} = 5 V ± 10%
DC Crosstalk[2]		±2			±2		µV	Due to single channel, full-scale output change
		±3			±3		µV/mA	Due to load current change
		±2			±2		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS								
Output Voltage Range	0		V_{REF}	0		V_{REF}	V	Gain = 1
	0		2 × V_{REF}	0		2 × V_{REF}	V	Gain = 2
Output Current Drive (I_{OUT})			15			15	mA	
Capacitive Load Stability		2			2		nF	R_L = ∞
		10			10		nF	R_L = 1 kΩ
Resistive Load[3]	1			1			kΩ	
Load Regulation		183			183		µV/mA	5 V ± 10%, DAC code = midscale, −30 mA ≤ I_{OUT} ≤ +30 mA
		177			177		µV/mA	3 V ± 10%, DAC code = midscale, −20 mA ≤ I_{OUT} ≤ +20 mA
Short-Circuit Current[4]		40			40		mA	
Load Impedance at Rails[5]		25			25		Ω	
Power-Up Time		2.5			2.5		µs	Exiting power-down mode, V_{DD} = 5 V
REFERENCE INPUT								
Reference Input Current		398			398		µA	V_{REF} = V_{DD} = V_{LOGIC} = 5.5 V, gain = 1
		789			789		µA	V_{REF} = V_{DD} = V_{LOGIC} = 5.5 V, gain = 2
Reference Input Range	1		V_{DD}	1		V_{DD}	V	Gain = 1
	1		V_{DD}/2	1		V_{DD}/2	V	Gain = 2
Reference Input Impedance		14			14		kΩ	Gain = 1
		7			7		kΩ	Gain = 2

SPECIFICATIONS

Table 2. (Continued)

Parameter	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit	Test Conditions/Comments
LOGIC INPUTS								
Input Current			±1			±1	μA	Per pin
Input Voltage								
Low, V_{IL}			0.3 × V_{LOGIC}			0.3 × V_{LOGIC}	V	
High, V_{IH}	0.7 × V_{LOGIC}			0.7 × V_{LOGIC}			V	
Pin Capacitance		3			3		pF	
LOGIC OUTPUTS (SDO)								
Output Voltage								
Low, V_{OL}			0.4			0.4	V	I_{SINK} = 200 μA
High, V_{OH}	V_{LOGIC} − 0.4			V_{LOGIC} − 0.4			V	I_{SOURCE} = 200 μA
Floating State Output Capacitance		4			4		pF	
POWER REQUIREMENTS								
V_{LOGIC}	1.62		5.5	1.62		5.5	V	
V_{LOGIC} Supply Current (I_{LOGIC})			3			3	μA	Power-on, −40°C to +105°C
			3			3	μA	Power-on, −40°C to +125°C
			3			3	μA	Power-down, −40°C to +105°C
			3			3	μA	Power-down, −40°C to +125°C
V_{DD}	2.7		5.5	2.7		5.5	V	Gain = 1
	V_{REF} + 1.5		5.5	V_{REF} + 1.5		5.5	V	Gain = 2
V_{DD} Supply Current (I_{DD})								
Normal Mode[6]		1.1	1.26		1.1	1.26	mA	−40°C to +85°C
		1.1	1.3		1.1	1.3	mA	−40°C to +105°C
All Power-Down Modes[7]		1	1.7		1	1.7	μA	Three-state, −40°C to +85°C
		1	1.7		1	1.7	μA	Power-down to 1 kΩ, −40°C to +85°C
		1	2.5		1	2.5	μA	Three-state, −40°C to +105°C
		1	2.5		1	2.5	μA	Power-down to 1 kΩ, −40°C to +105°C
		1	5.5		1	5.5	μA	Three-state, −40°C to +125°C
		1	5.5		1	5.5	μA	Power-down to 1 kΩ, −40°C to +125°C

1 DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when V_{REF} = V_{DD} with gain = 1 or when $V_{REF}/2$ = V_{DD} with gain = 2. Linearity calculated using a reduced code range of 256 to 65,280.

2 See the Terminology section.

3 Channel 0, Channel 1, Channel 2, and Channel 3 can together source/sink 40 mA. Similarly, Channel 4, Channel 5, Channel 6, and Channel 7 can together source/sink 40 mA up to a junction temperature of 125°C.

4 V_{DD} = 5 V. The AD5676 includes current limiting that is intended to protect the device during temporary overload conditions. Junction temperature can be exceeded during current limit. Operation above the specified maximum operation junction temperature can impair device reliability.

5 When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV.

6 Interface inactive. All DACs active. DAC outputs unloaded.

7 All DACs powered down.

SPECIFICATIONS

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, all specifications −40°C to +125°C, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage Settling Time[1]		5	8	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		0.8		V/µs	
Digital-to-Analog Glitch Impulse[1]		1.4		nV-sec	1 LSB change around major carry, gain = 1
Digital Feedthrough[1]		0.13		nV-sec	
Digital Crosstalk[1]		0.1		nV-sec	
Analog Crosstalk[1]		−0.25		nV-sec	Gain = 1
		−1.3		nV-sec	Gain = 2
DAC-to-DAC Crosstalk[1]		−2.0		nV-sec	
Total Harmonic Distortion (THD)[1, 2]		−80		dB	T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Output Noise Spectral Density (NSD)[1]		80		nV/√Hz	DAC code = midscale, bandwidth = 10 kHz, gain = 2
Output Noise		6		µV p-p	0.1 Hz to 10 Hz, gain = 1
Signal-to-Noise Ratio (SNR)		90		dB	T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Spurious-Free Dynamic Range (SFDR)		83		dB	T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Signal-to-Noise-and-Distortion Ratio (SINAD)		80		dB	T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz

[1] See the Terminology section.

[2] Digitally generated sine wave (f_{OUT}) at 1 kHz.

SPECIFICATIONS

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2. $V_{DD} = 2.7$ V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; $V_{REF} = 2.5$ V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

		1.62 V ≤ V_{LOGIC} < 2.7 V		2.7 V ≤ V_{LOGIC} ≤ 5.5 V		
Parameter	Symbol	Min	Max	Min	Max	Unit
SCLK Cycle Time	t_1	20		20		ns
SCLK High Time	t_2	8		8		ns
SCLK Low Time	t_3	10		12		ns
$\overline{\text{SYNC}}$ to SCLK Falling Edge Setup Time	t_4	15		11		ns
Data Setup Time	t_5	2		3		ns
Data Hold Time	t_6	2		2		ns
SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge	t_7	4		4		ns
Minimum $\overline{\text{SYNC}}$ High Time	t_8	15		12		ns
$\overline{\text{SYNC}}$ Rising Edge to $\overline{\text{SYNC}}$ Rising Edge (DAC Register Updates)	t_9	870		830		ns
$\overline{\text{SYNC}}$ Falling Edge to SCLK Fall Ignore	t_{10}	4		4		ns
$\overline{\text{LDAC}}$ Pulse Width Low	t_{11}	8		8		ns
$\overline{\text{SYNC}}$ Rising Edge to $\overline{\text{LDAC}}$ Rising Edge	t_{12}	25		25		ns
$\overline{\text{SYNC}}$ Rising Edge to $\overline{\text{LDAC}}$ Falling Edge	t_{13}	25		25		ns
$\overline{\text{LDAC}}$ Falling Edge to $\overline{\text{SYNC}}$ Rising Edge	t_{14}	840		800		ns
Minimum Pulse Width Low	t_{15}	8		10		ns
$\overline{\text{RESET}}$ Activation Time	t_{16}	90		90		ns
Power-Up Time[1]		5.5		5.5		µs

[1] Time to exit power-down to normal mode of AD5676 operation, $\overline{\text{SYNC}}$ rising edge to 90% of DAC midscale value, with output unloaded.

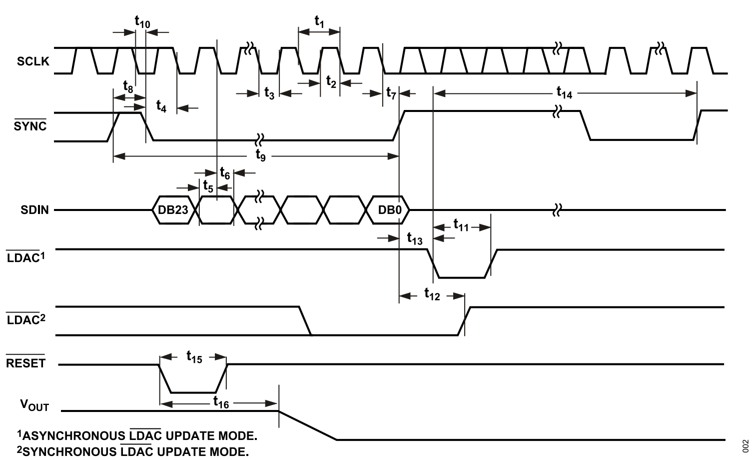


Figure 2. Serial Write Operation

DAISY-CHAIN AND READBACK TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 4 and Figure 5. $V_{DD} = 2.7$ V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; $V_{REF} = 2.5$ V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. $V_{DD} = 2.7$ V to 5.5 V.

SPECIFICATIONS

Table 5.

		$1.62\ V \le V_{LOGIC} < 2.7\ V$		$2.7\ V \le V_{LOGIC} \le 5.5\ V$		
Parameter	Symbol	Min	Max	Min	Max	Unit
SCLK Cycle Time	t_1	130		110		ns
SCLK High Time	t_2	33		23		ns
SCLK Low Time	t_3	12		7		ns
$\overline{SYNC}$ to SCLK Falling Edge	t_4	80		80		ns
Data Setup Time	t_5	2		2		ns
Data Hold Time	t_6	2		2		ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_7	35		10		ns
Minimum $\overline{SYNC}$ High Time	t_8	55		30		ns
SDO Data Valid from SCLK Rising Edge	t_9	60		50		ns
$\overline{SYNC}$ Rising Edge to SCLK Falling Edge	t_{10}	2		6		ns
$\overline{SYNC}$ Rising Edge to SDO Disable	t_{11}	40		35		ns

CIRCUIT AND TIMING DIAGRAMS

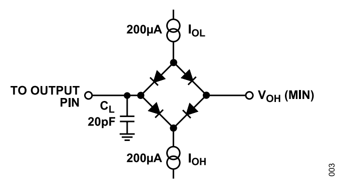


Figure 3. Load Circuit for Digital Output (SDO) Timing Specifications

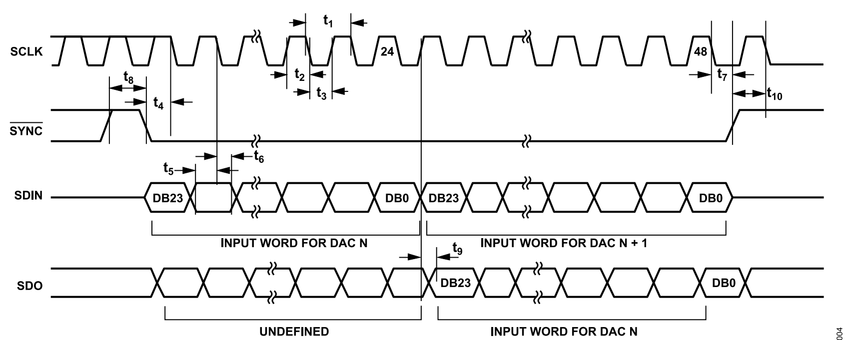


Figure 4. Daisy Chain Timing Diagram

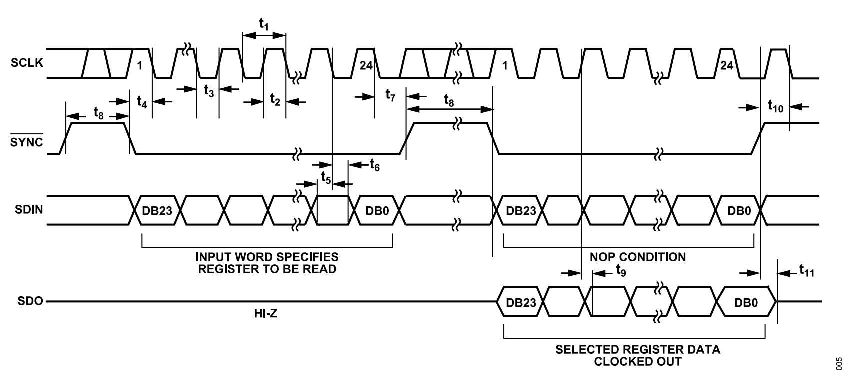


Figure 5. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{LOGIC} to GND	−0.3 V to +7 V
$V_{OUT}x$ to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	125°C
Reflow Soldering Peak Temperature, Pb-Free (J-STD-020)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

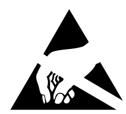
Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
20-Lead TSSOP (RU-20)[1]	98.65	44.39	17.58	1.77	43.9	°C/W
20-Lead LFCSP (CP-20-8)[2]	82	16.67	32.5	0.43	22	°C/W

1 Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51.

2 Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

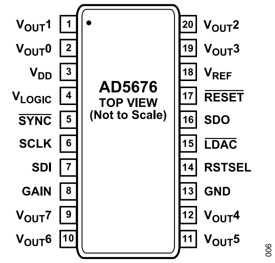
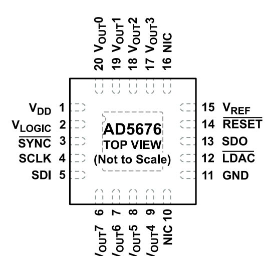


Figure 6. 20-Lead TSSOP Pin Configuration

Table 8. 20-Lead TSSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{OUT}1$	Analog Output Voltage from DAC 1. The output amplifier has rail-to-rail operation.
2	$V_{OUT}0$	Analog Output Voltage from DAC 0. The output amplifier has rail-to-rail operation.
3	V_{DD}	Power Supply Input. The AD5676 operates from 2.7 V to 5.5 V. Decouple V_{DD} with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	V_{LOGIC}	Digital Power Supply. Voltage ranges from 1.62 V to 5.5 V.
5	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, data transfers in on the falling edges of the next 24 clocks.
6	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data transfers at rates of up to 50 MHz.
7	SDI	Serial Data Input. The AD5676 has a 24-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input.
8	GAIN	Span Set. When this pin is tied to GND, all eight DAC outputs have a span from 0 V to V_{REF}. If this pin is tied to V_{LOGIC}, all eight DACs output a span of 0 V to 2 × V_{REF}.
9	$V_{OUT}7$	Analog Output Voltage from DAC 7. The output amplifier has rail-to-rail operation.
10	$V_{OUT}6$	Analog Output Voltage from DAC 6. The output amplifier has rail-to-rail operation.
11	$V_{OUT}5$	Analog Output Voltage from DAC 5. The output amplifier has rail-to-rail operation.
12	$V_{OUT}4$	Analog Output Voltage from DAC 4. The output amplifier has rail-to-rail operation.
13	GND	Ground Reference Point for All Circuitry on the Device.
14	RSTSEL	Power-On Reset. Tie this pin to GND to power up all eight DACs to zero scale. Tie this pin to V_{LOGIC} to power up all eight DACs to midscale.
15	$\overline{LDAC}$	Load DAC. $\overline{LDAC}$ operates in two modes, asynchronously and synchronously. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to update simultaneously. This pin can also be tied permanently low.
16	SDO	Serial Data Output. Use this pin to daisy-chain a number of devices together, or use it for readback. The serial data transfers on the rising edge of SCLK and is valid on the falling edge.
17	$\overline{RESET}$	Asynchronous Reset Input. The $\overline{RESET}$ input is falling edge sensitive. When $\overline{RESET}$ is low, all $\overline{RESET}$ pulses are ignored. When $\overline{RESET}$ is activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin.
18	V_{REF}	Reference Input Voltage.
19	$V_{OUT}3$	Analog Output Voltage from DAC 3. The output amplifier has rail-to-rail operation.
20	$V_{OUT}2$	Analog Output Voltage from DAC 2. The output amplifier has rail-to-rail operation.



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE TIED TO GND.

Figure 7. 20-Lead LFCSP Pin Configuration

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 9. 20-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The AD5676 operate from 2.7 V to 5.5 V. Decouple V_{DD} with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
2	V_{LOGIC}	Digital Power Supply. The voltage on this pin ranges from 1.62 V to 5.5 V.
3	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, data transfers in on the falling edges of the next 24 clocks.
4	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data transfers at rates of up to 50 MHz.
5	SDI	Serial Data Input. This device has a 24-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input.
6	$V_{OUT}7$	Analog Output Voltage from DAC 7. The output amplifier has rail-to-rail operation.
7	$V_{OUT}6$	Analog Output Voltage from DAC 6. The output amplifier has rail-to-rail operation.
8	$V_{OUT}5$	Analog Output Voltage from DAC 5. The output amplifier has rail-to-rail operation.
9	$V_{OUT}4$	Analog Output Voltage from DAC 4. The output amplifier has rail-to-rail operation.
10, 16	NIC	Not Internally Connected.
11	GND	Ground Reference Point for All Circuitry on the Device.
12	$\overline{\text{LDAC}}$	Load DAC. $\overline{\text{LDAC}}$ operates in two modes, asynchronously and synchronously. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. That allows all DAC outputs to update simultaneously. This pin can also be tied permanently low.
13	SDO	Serial Data Output. This pin can be used to daisy-chain a number of devices together, or it can be used for readback. The serial data transfers on the rising edge of SCLK and is valid on the falling edge.
14	$\overline{\text{RESET}}$	Asynchronous Reset Input. The $\overline{\text{RESET}}$ input is falling edge sensitive. When $\overline{\text{RESET}}$ is low, all $\overline{\text{RESET}}$ pulses are ignored. When $\overline{\text{RESET}}$ is activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin.
15	V_{REF}	Reference Input Voltage.
17	$V_{OUT}3$	Analog Output Voltage from DAC 3. The output amplifier has rail-to-rail operation.
18	$V_{OUT}2$	Analog Output Voltage from DAC 2. The output amplifier has rail-to-rail operation.
19	$V_{OUT}1$	Analog Output Voltage from DAC 1. The output amplifier has rail-to-rail operation.
20	$V_{OUT}0$	Analog Output Voltage from DAC 0. The output amplifier has rail-to-rail operation.
	EPAD	Exposed Pad. The exposed pad must be tied to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

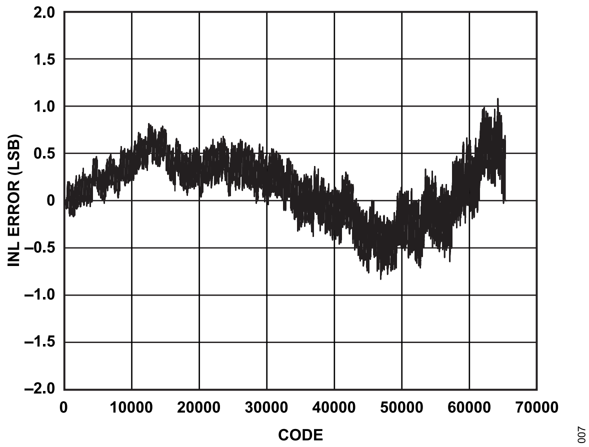


Figure 8. INL Error vs. Code

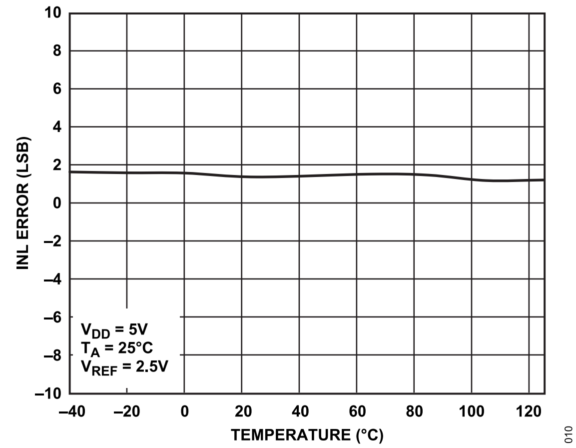


Figure 11. INL Error vs. Temperature

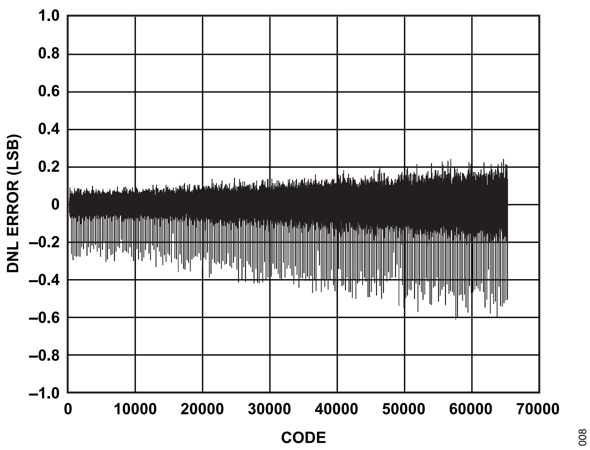


Figure 9. DNL Error vs. Code

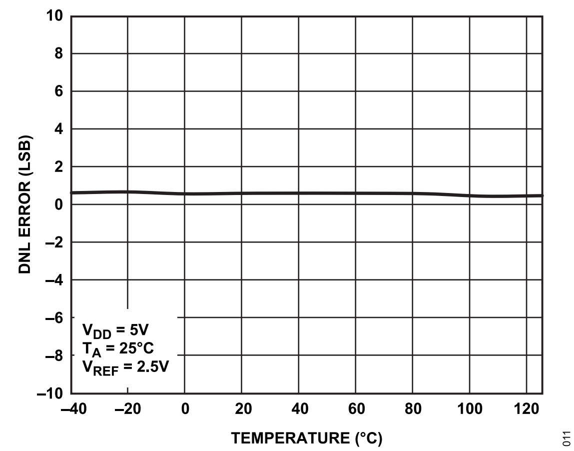


Figure 12. DNL Error vs. Temperature

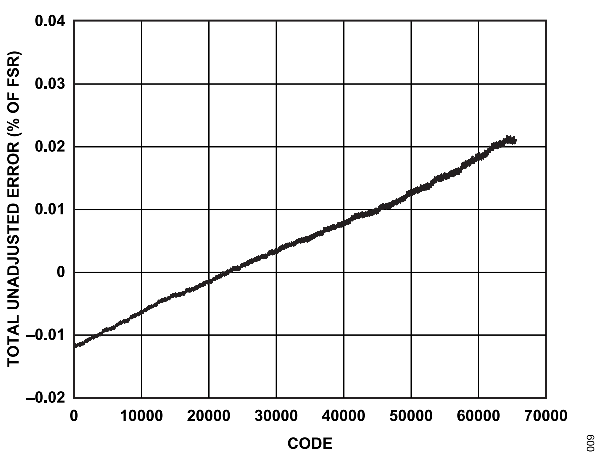


Figure 10. TUE vs. Code

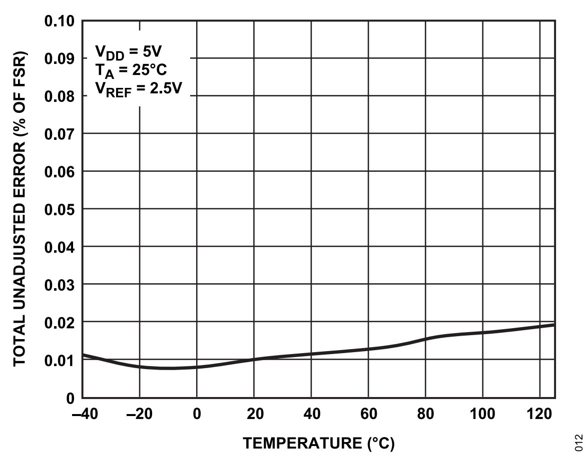


Figure 13. TUE vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

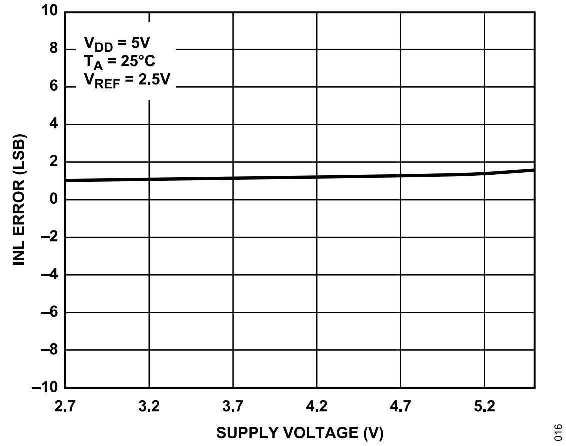


Figure 14. INL Error vs. Supply Voltage

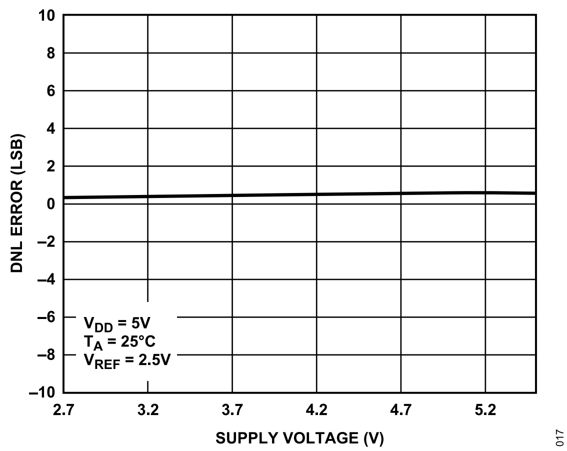


Figure 15. DNL Error vs. Supply Voltage

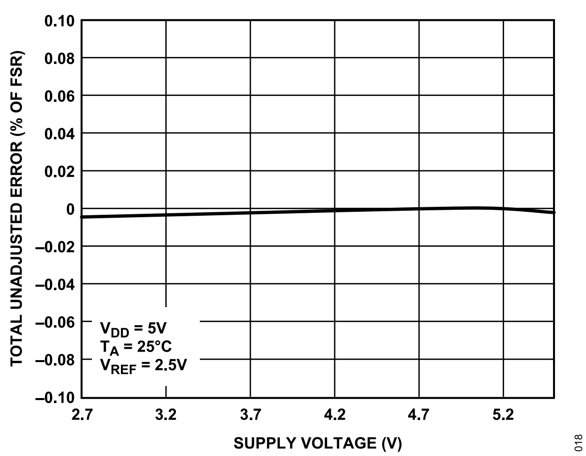


Figure 16. TUE vs. Supply Voltage

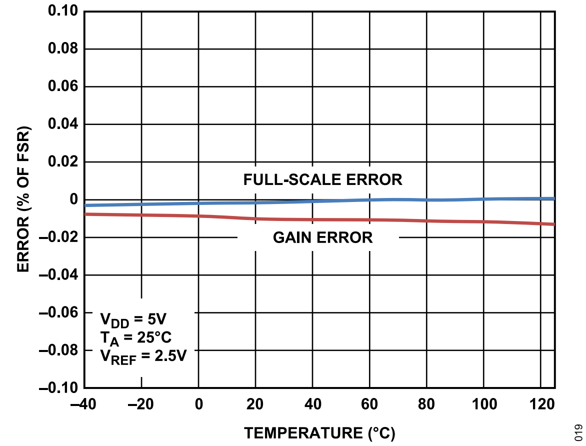


Figure 17. Gain Error and Full-Scale Error vs. Temperature

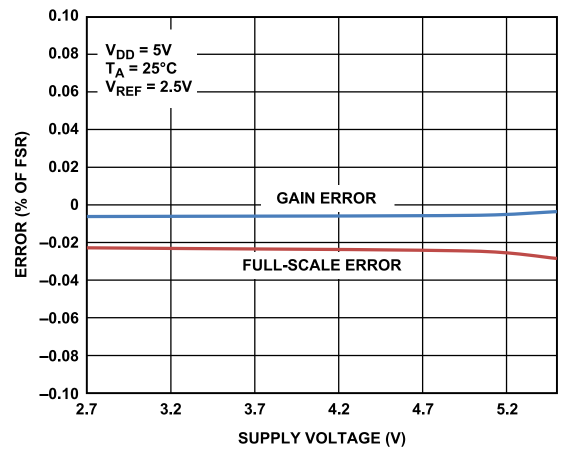


Figure 18. Gain Error and Full-Scale Error vs. Supply Voltage

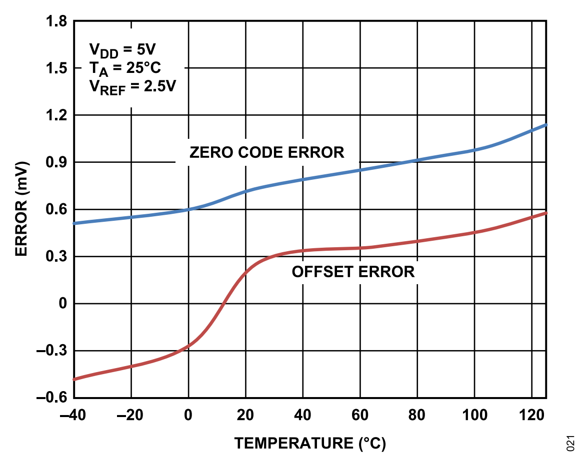


Figure 19. Zero Code Error and Offset Error vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

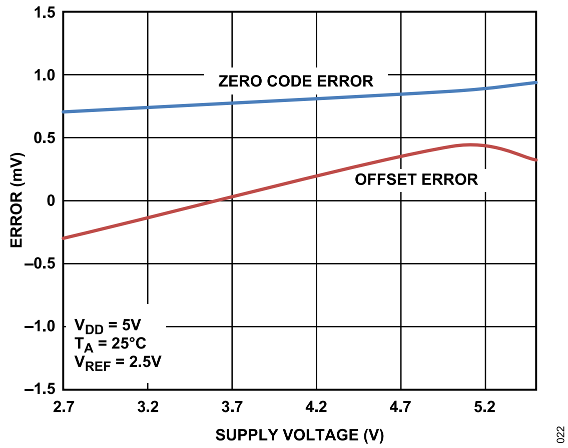


Figure 20. Zero Code Error and Offset Error vs. Supply Voltage

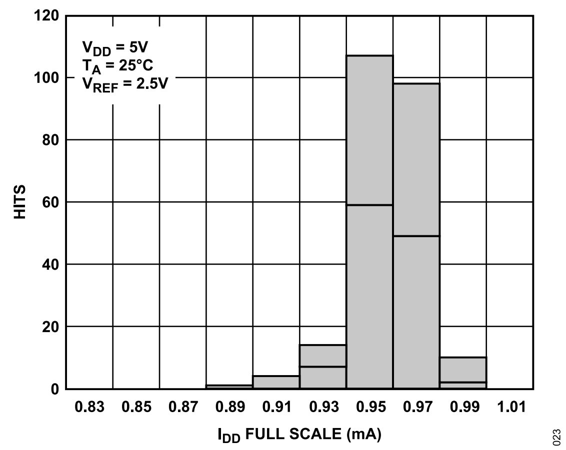


Figure 21. I_{DD} Histogram with External Reference

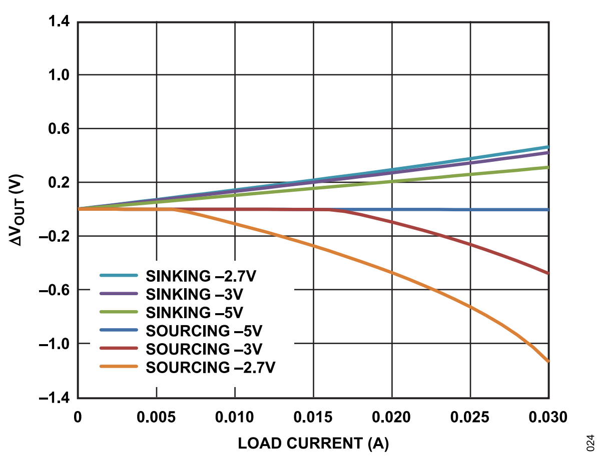


Figure 22. Headroom/Footroom (ΔV_{OUT}) vs. Load Current

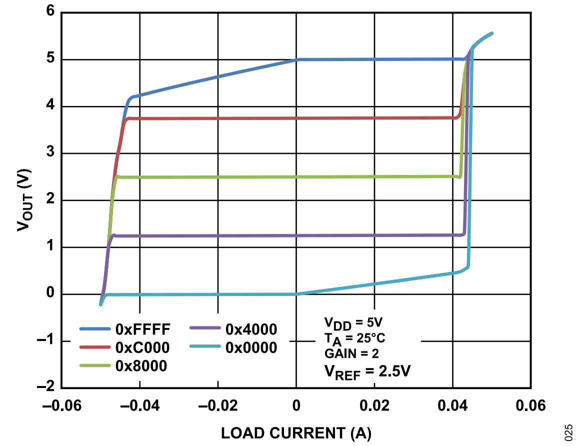


Figure 23. Source and Sink Capability at 5 V

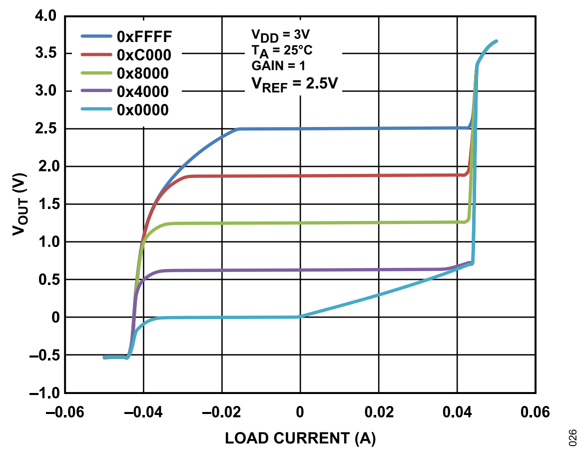


Figure 24. Source and Sink Capability at 3 V

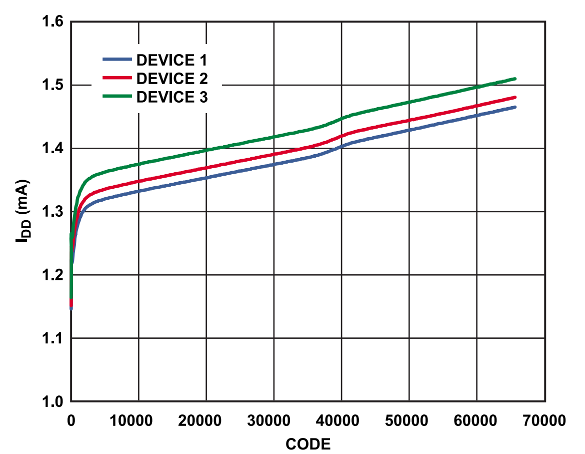


Figure 25. I_{DD} vs. Code

TYPICAL PERFORMANCE CHARACTERISTICS

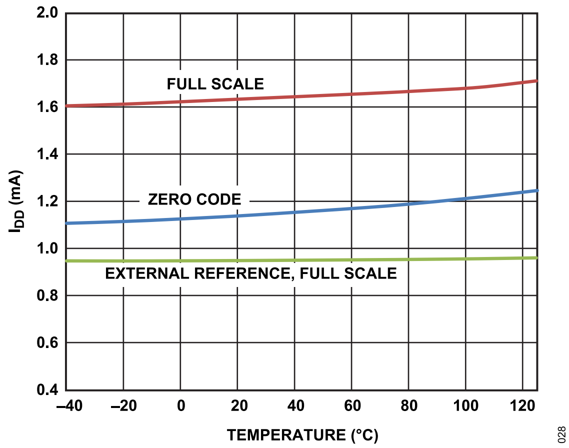


Figure 26. I_{DD} vs. Temperature

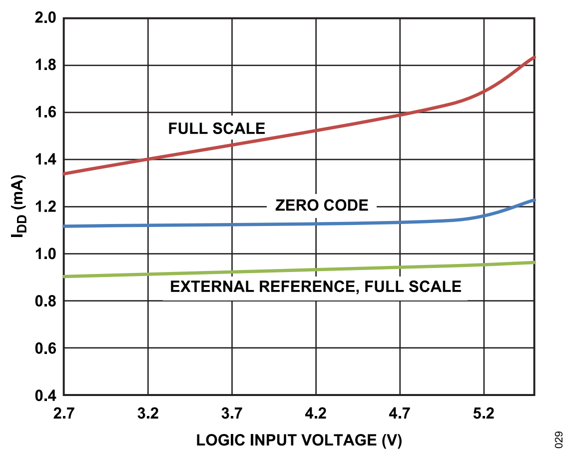


Figure 27. I_{DD} vs. Supply Voltage

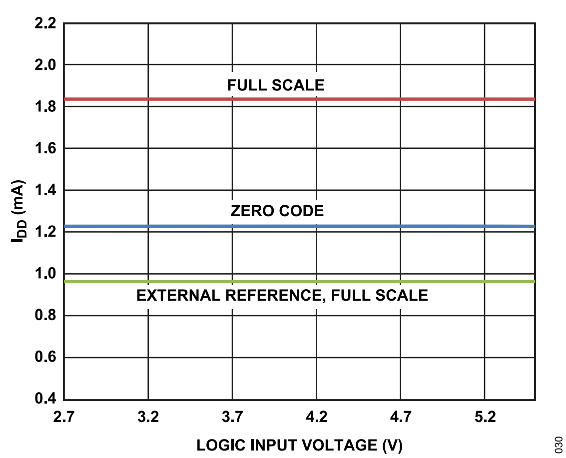


Figure 28. I_{DD} vs. Logic Input Voltage

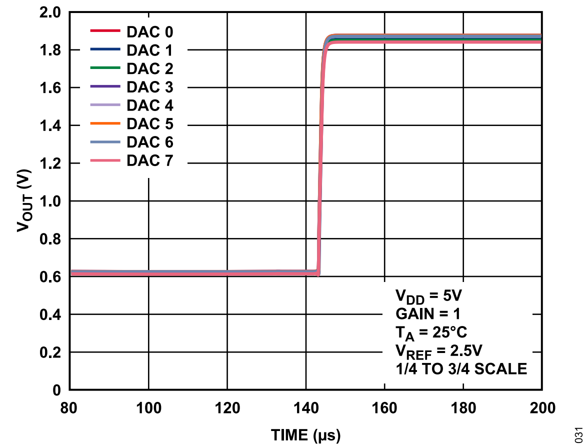


Figure 29. Full-Scale Settling Time

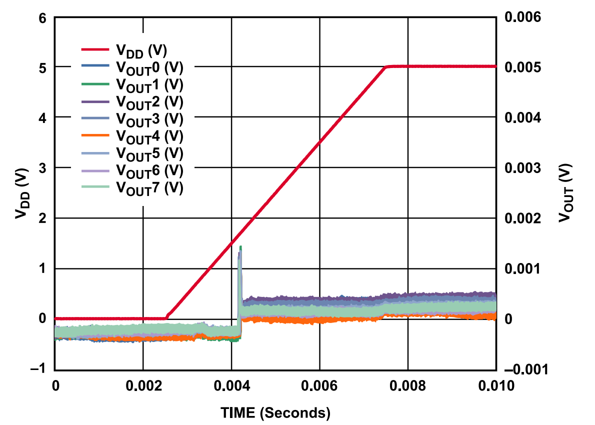


Figure 30. Power-On Reset to 0 V and Midscale

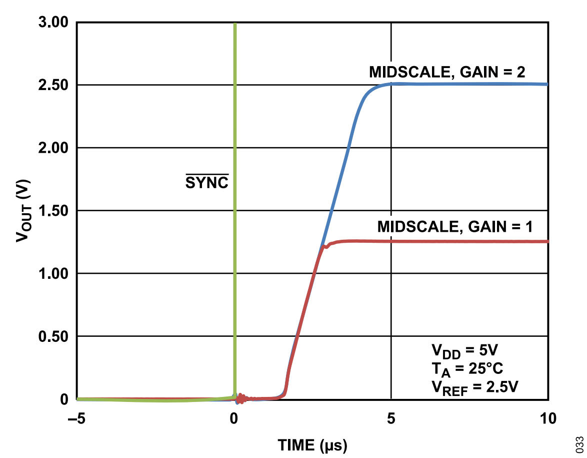


Figure 31. Exiting Power-Down to Midscale

TYPICAL PERFORMANCE CHARACTERISTICS

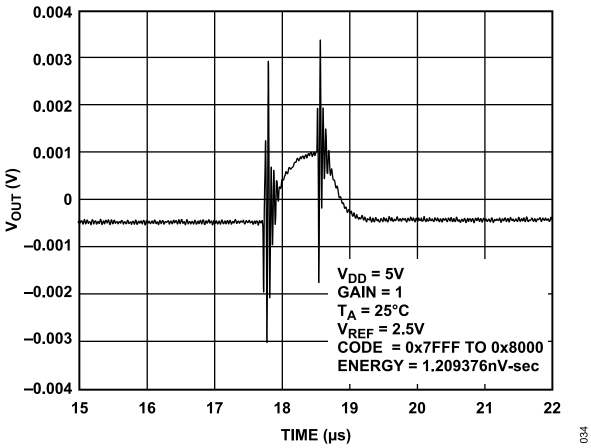


Figure 32. Digital-to-Analog Glitch Impulse

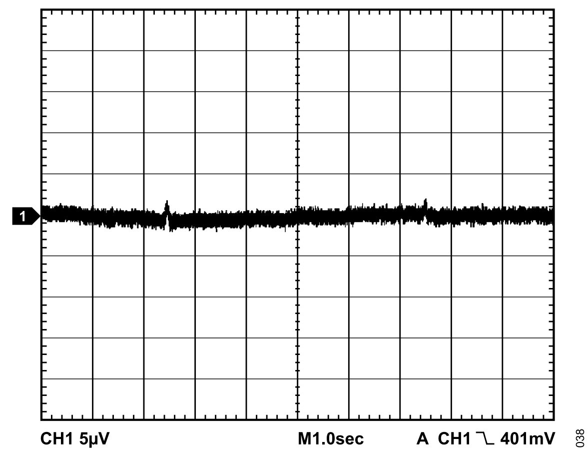


Figure 35. 0.1 Hz to 10 Hz Output Noise

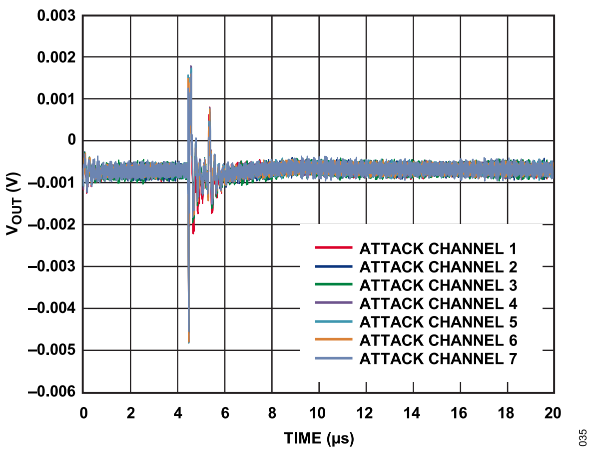


Figure 33. Analog Crosstalk

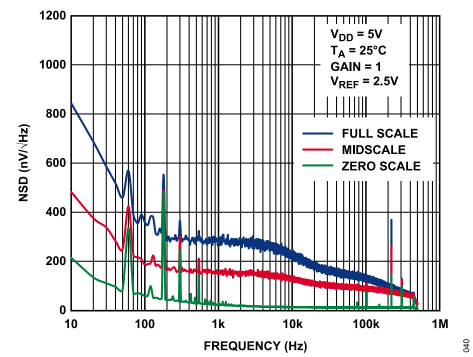


Figure 36. Noise Spectral Density (NSD)

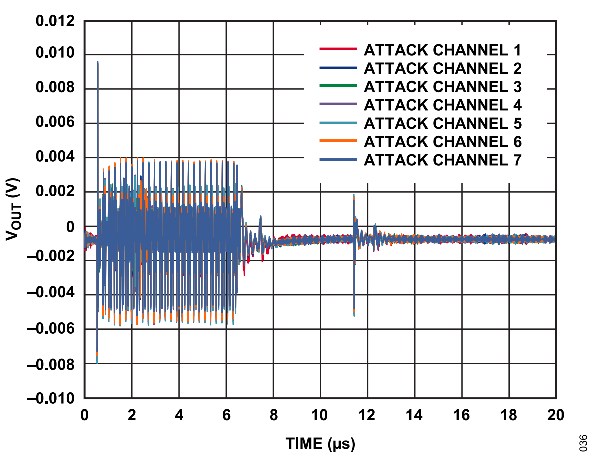


Figure 34. DAC-to-DAC Crosstalk

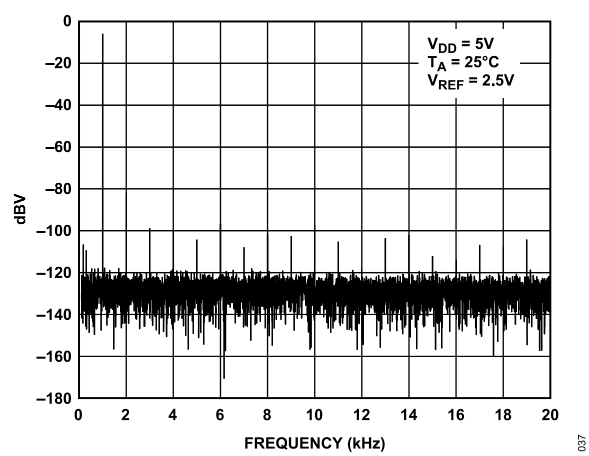


Figure 37. THD at 1 kHz

TYPICAL PERFORMANCE CHARACTERISTICS

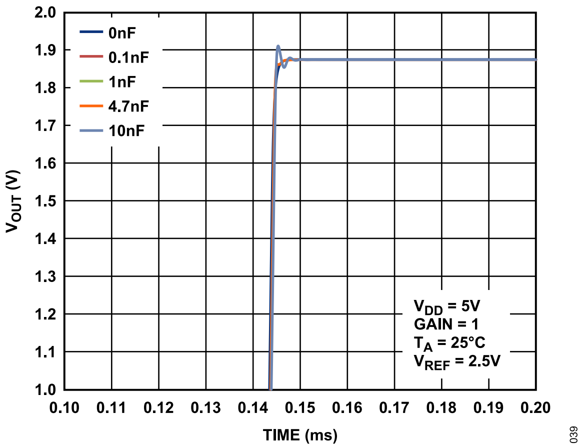


Figure 38. Settling Time for Various Capacitive Loads

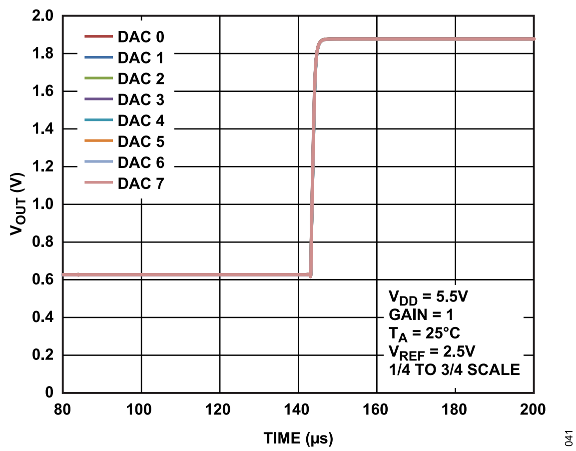


Figure 39. Settling Time, 5.5 V

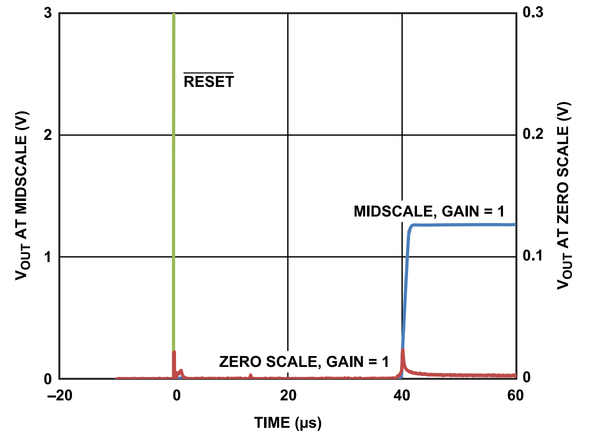


Figure 40. Hardware Reset

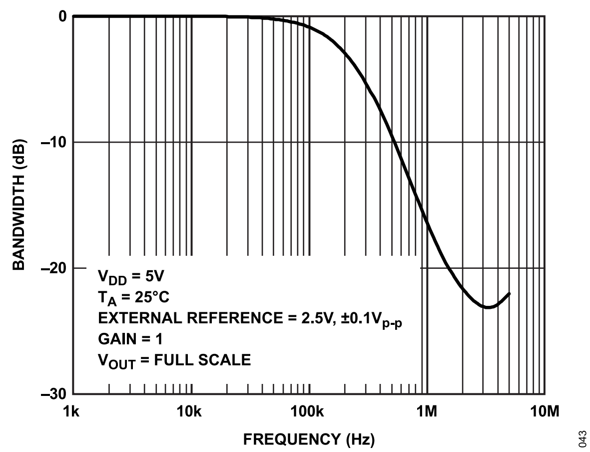


Figure 41. Multiplying Bandwidth, External Reference

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)

DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity. The AD5676 is guaranteed monotonic by design.

Zero Code Error

Zero code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output is 0 V. The zero code error is always positive because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero code error is expressed in mV.

Full-Scale Error

Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in percent of full-scale range (% of FSR).

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % of FSR.

Offset Error Drift

Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in µV/°C.

Offset Error

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured with Code 256 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to the change in V_{DD} for full-scale output of the DAC. It is measured in mV/V. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the rising edge of $\overline{\text{SYNC}}$.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000).

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Noise Spectral Density (NSD)

NSD is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz.

DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in µV/mA.

Digital Crosstalk

Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

Analog Crosstalk

Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. To measure analog crosstalk, load one of the input registers with a full-scale code change (all 0s to all 1s and vice versa). Then, execute a software $\overline{\text{LDAC}}$ and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands while monitoring

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the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference with full-scale code loaded to the DAC appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)

THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. THD is measured in decibels.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5676 is an octal 16-bit, serial input, voltage output DAC. The device operates from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5676 in a 24-bit word format via a 3-wire serial interface. The AD5676 incorporates a power-on reset circuit to ensure that the DAC output powers up to a known output state. The device also has a software power-down mode that reduces the typical current consumption to typically 1 µA.

TRANSFER FUNCTION

The gain of the output amplifier can be set to ×1 or ×2 using the gain select pin (GAIN) on the TSSOP package or the gain bit on the LFCSP package. When the GAIN pin is tied to GND, all eight DAC outputs have a span from 0 V to V_{REF}. When the GAIN pin is tied to V_{LOGIC}, all eight DACs output a span of 0 V to 2 × V_{REF}. When using the LFCSP package, the gain bit in the gain setup register is used to set the gain of the output amplifier. The gain bit is 0 by default. When the gain bit is 0 the output span of all eight DACs is 0 V to V_{REF}. When the gain bit is 1 the output span of all eight DACs is 0 V to 2 × V_{REF}. The gain bit is ignored on the TSSOP package.

DAC ARCHITECTURE

The DAC architecture implements a segmented string DAC with an internal output buffer. Figure 42 shows the internal block diagram.

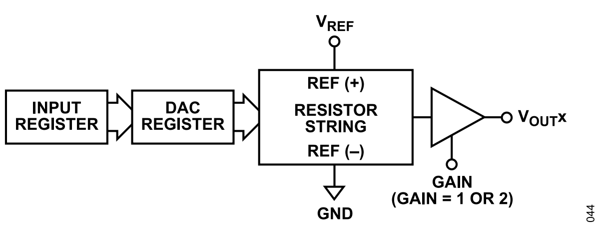


Figure 42. Single DAC Channel Architecture Block Diagram

Figure 43 shows the simplified segmented resistor string DAC structure. The code loaded to the DAC register determines the switch on the string that is connected to the output buffer.

Because each resistance in the string has the same value, R, the string DAC is guaranteed monotonic.

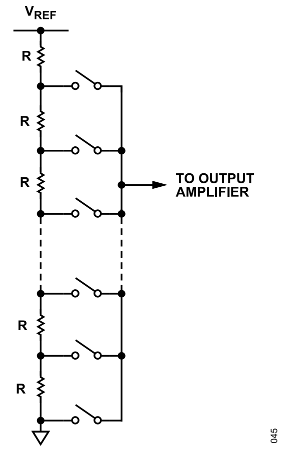


Figure 43. Simplified Resistor String Structure

OUTPUT AMPLIFIERS

The output buffer amplifier generates rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. The actual range depends on the value of V_{REF}, the gain setting, the offset error, and the gain error.

The output amplifiers can drive a load of 1 kΩ in parallel with 10 nF to GND. The slew rate is 0.8 V/µs with a typical ¼ to ¾ scale settling time of 5 µs.

SERIAL INTERFACE

The AD5676 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and SDI) that is compatible with SPI, QSPI™, and MICROWIRE interface standards as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence. The AD5676 contains an SDO pin that allows the user to daisy-chain multiple devices together (see the Daisy-Chain Operation section) or for readback.

Input Shift Register

The input shift register of the AD5676 is 24 bits wide. Data is loaded MSB first (DB23), and the first four bits are the command bits, C3 to C0 (see Table 10), followed by the 4-bit DAC address bits, A3 to A0 (see Table 11), and finally, the 16-bit data-word.

The data-word comprises 16-bit input code, followed by zero, two, or four don't care bits. These data bits are transferred to the input register on the 24 falling edges of SCLK and are updated on the rising edge of $\overline{SYNC}$.

Commands execute on individual DAC channels, combined DAC channels, or on all DACs, depending on the address bits selected.

THEORY OF OPERATION

Table 10. Command Bit Definitions

Command				
C3	C2	C1	C0	Description
0	0	0	0	No operation
0	0	0	1	Write to Input Register n (where n = 1 to 8, depending on the DAC selected from the address bits in Table 11), dependent on $\overline{\text{LDAC}}$
0	0	1	0	Update the DAC register with contents of Input Register n
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up the DAC
0	1	0	1	Hardware $\overline{\text{LDAC}}$ mask register
0	1	1	0	Software reset (power-on reset)
0	1	1	1	Gain setup register (LFCSP package only)
1	0	0	0	Set up the DCEN register (daisy-chain enable)
1	0	0	1	Set up the readback register (readback enable)
1	0	1	0	Update all channels of the input register simultaneously with the input data
1	0	1	1	Update all channels of the DAC register and input register simultaneously with the input data
1	1	0	0	Reserved
…	…	…	…	
1	1	1	1	No operation, daisy-chain mode

Table 11. Address Bits and Selected DACs

Address Bits				Selected Output DAC Channel
A3	A2	A1	A0	
0	0	0	0	DAC 0
0	0	0	1	DAC 1
0	0	1	0	DAC 2
0	0	1	1	DAC 3
0	1	0	0	DAC 4
0	1	0	1	DAC 5
0	1	1	0	DAC 6
0	1	1	1	DAC 7

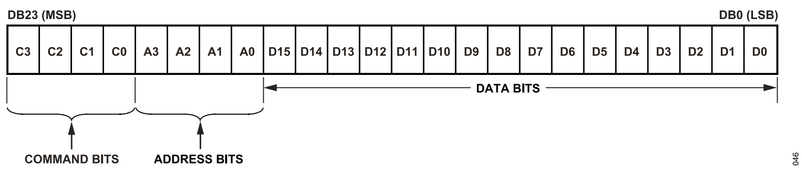


Figure 44. Input Shift Register Content

THEORY OF OPERATION

STANDALONE OPERATION

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the SDI line is clocked into the 24-bit input shift register on the falling edge of SCLK. After the last of the 24 data bits is clocked in, bring $\overline{\text{SYNC}}$ high. The programmed function is then executed, that is, an $\overline{\text{LDAC}}$ dependent change in the DAC register contents and/or a change in the mode of operation occurs.

If $\overline{\text{SYNC}}$ is taken high at a clock before the 24^{th} clock, it is considered a valid frame, and invalid data may be loaded to the DAC. Bring $\overline{\text{SYNC}}$ high for a minimum of 9.65 ns (single channel, see t_8 in Table 4) before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. Idle $\overline{\text{SYNC}}$ at the rails between write sequences for even lower power operation. The $\overline{\text{SYNC}}$ line is kept low for 24 falling edges of SCLK, and the DAC is updated on the rising edge of $\overline{\text{SYNC}}$.

When data is transferred into the input register of the addressed DAC, all DAC registers and outputs update by taking $\overline{\text{LDAC}}$ low while the $\overline{\text{SYNC}}$ line is high.

WRITE AND UPDATE COMMANDS

Write to Input Register N (Dependent on $\overline{\text{LDAC}}$)

Command 0001 allows the user to write to the dedicated input register for each DAC individually. When $\overline{\text{LDAC}}$ is low, the input register is transparent (if not controlled by the $\overline{\text{LDAC}}$ mask register).

Update DAC Register With Contents of Input Register N

Command 0010 loads the DAC registers and outputs with the contents of the selected input registers and updates the DAC outputs directly. Data Bit D7 to Bit D0 determine which DACs have data from the input register transferred to the DAC register. Setting a bit to 1 transfers data from the input register to the appropriate DAC register.

Write to and Update DAC Channel N (Independent of $\overline{\text{LDAC}}$)

Command 0011 allows the user to write to the DAC registers and updates the DAC outputs directly. The address bits are used to select the DAC channel.

DAISY-CHAIN OPERATION

For systems that contain several DACs, the SDO pin can daisy-chain several devices together and is enabled through a software executable daisy-chain enable (DCEN) command. Command 1000 is reserved for this DCEN function (see Table 10). The daisy-chain mode is enabled by setting Bit DB0 in the DCEN register. The default setting is standalone mode, where DB0 = 0. Table 12 shows how the state of the bit corresponds to the mode of operation of the device.

Table 12. Daisy-Chain Enable (DCEN) Register

DB0	Description
0	Standalone mode (default)
1	DCEN mode

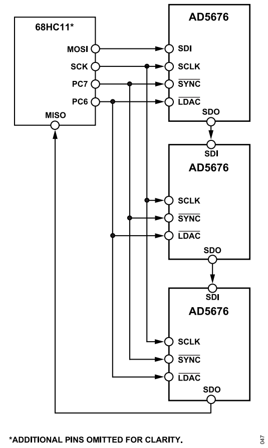


Figure 45. Daisy-Chaining the AD5676

The SCLK pin is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the input shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the SDI input on the next DAC in the chain, a daisy-chain interface is constructed. Each DAC in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × N, where N is the total number of devices updated. If $\overline{\text{SYNC}}$ is taken high at a clock that is not a multiple of 24, it is considered a valid frame, and invalid data may be loaded to the DAC. When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ goes high, which latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register. The serial clock can be continuous or a gated clock. If $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles, a continuous SCLK source is used. In gated clock mode, use a burst clock containing the exact number of clock cycles, and take $\overline{\text{SYNC}}$ high after the final clock to latch the data.

READBACK OPERATION

Readback mode is invoked through a software executable readback command. If the SDO output is disabled via the daisy-chain mode disable bit in the control register, it is enabled automatically for the duration of the read operation, after which it is disabled again. Command 1001 is reserved for the readback function. This command, in association with the address bits, A3 to A0, selects the DAC input register to read. Note that, during readback, only one DAC register can be selected. The remaining data bits in the write sequence are don't care bits. During the next SPI write, the data appearing on the SDO output contains the data from the previously addressed register.

THEORY OF OPERATION

For example, to read back the DAC register for Channel 0, implement the following sequence:

1. Write 0x900000 to the AD5676 input register. This configures the device for read mode with the DAC register of Channel 0 selected. Note that all data bits, DB15 to DB0, are don't care bits.
2. Follow this with a second write, a no operation (NOP) condition, 0x000000 or 0xF00000 when in daisy-chain mode. During this write, the data from the register is clocked out on the SDO line. DB23 to DB20 contain undefined data, and the last 16 bits contain the DB19 to DB4 DAC register contents.

When $\overline{SYNC}$ is high the SDO pin is driven by a weak latch which holds the last data bit. The SDO pin can be overdriven by the SDO pin of another device, thus allowing multiple devices to be read using the same SPI interface.

POWER-DOWN OPERATION

The AD5676 provides two separate power-down modes. Command 0100 is designated for the power-down function (see Table 10). These power-down modes are software programmable by setting 16 bits, Bit DB15 to Bit DB0, in the input shift register. There are two bits associated with each DAC channel. Table 13 shows how the state of the two bits corresponds to the mode of operation of the device.

Table 13. Modes of Operation

Operating Mode	PD1	PD0
Normal Operation	0	0
Power-Down Modes		
1 kΩ to GND	0	1
Three-State	1	1

Any or all DACs (DAC 0 to DAC 7) power down to the selected mode by setting the corresponding bits. See Table 14 for the contents of the input shift register during the power-down/ power-up operation.

When both Bit PD1 and Bit PD0 in the input shift register are set to 0, the device works normally with its normal power consumption of 1.1 mA typically. However, for the two power-down modes, the supply current falls to 1 µA typically. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. Therefore the DAC channel output impedance is defined when the channel is powered down. There are two different power-down options. The output is connected internally to GND through either a 1 kΩ resistor, or it is left open-circuited (three-state). The output stage is shown in Figure 46.

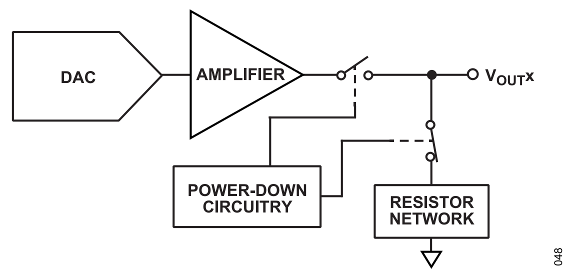


Figure 46. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The DAC register updates while the device is in power-down mode. The time required to exit power-down is typically 5 µs for V_{DD} = 5 V.

Table 14. 24-Bit Input Shift Register Contents of Power-Down/Power-Up Operation[1]

			DAC 7	DAC 6	DAC 5	DAC 4	DAC 3	DAC 2	DAC 1	DAC 0
[DB23:DB20]	DB19	[DB18:DB16]	[DB15: B14]	[DB13: B12]	[DB11: B10]	[DB9:DB8]	[DB7:DB6]	[DB5:DB4]	[DB3:DB2]	[DB1:DB0]
0100	0	XXX	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]

[1] X means don't care.

THEORY OF OPERATION

LOAD DAC (HARDWARE LDAC PIN)

The AD5676 DAC has a double buffered interface consisting of two banks of registers: input registers and DAC registers. The user can write to any combination of the input registers. Updates to the DAC register are controlled by the LDAC pin.

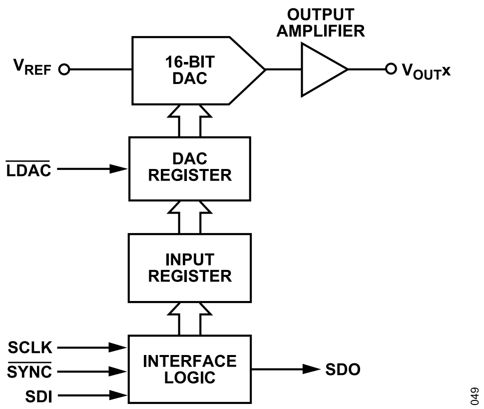


Figure 47. Simplified Diagram of Input Loading Circuitry for a Single DAC

Instantaneous DAC Updating (LDAC Held Low)

LDAC is held low while data is clocked into the input register using Command 0001. Both the addressed input register and the DAC register are updated on the rising edge of SYNC and the output begins to change (see Table 16).

Deferred DAC Updating (LDAC Is Pulsed Low)

LDAC is held high while data is clocked into the input register using Command 0001. All DAC outputs are asynchronously updated by taking LDAC low after SYNC is taken high. The update occurs on the falling edge of LDAC.

LDAC MASK REGISTER

Command 0101 is reserved for this hardware LDAC function. Address bits are ignored. Writing to the DAC using Command 0101 loads the 8-bit LDAC register (DB7 to DB0). The default for each channel is 0; that is, the LDAC pin works normally. Setting the bits to 1 forces this DAC channel to ignore transitions on the LDAC pin, regardless of the state of the hardware LDAC pin. This flexibility is useful in applications where the user wants to select which channels respond to the LDAC pin.

Table 15. LDAC Overwrite Definition

Load LDAC Register		
LDAC Bits (DB7 to DB0)	LDAC Pin	LDAC Operation
00000000	1 or 0	Determined by the LDAC pin.
11111111	X[1]	DAC channels update and override the LDAC pin. DAC channels see LDAC as 1.

[1] X means don't care.

The LDAC register gives the user extra flexibility and control over the hardware LDAC pin (see Table 15). Setting the LDAC bits (DB0 to DB7) to 0 for a DAC channel means that the update for this channel is controlled by the hardware LDAC pin.

Table 16. Write Commands and LDAC Pin Truth Table[1]

Command	Description	Hardware LDAC Pin State	Input Register Contents	DAC Register Contents
0001	Write to Input Register n (dependent on LDAC)	V_{LOGIC}	Data update	No change (no update)
		GND[2]	Data update	Data update
0010	Update the DAC register with contents of Input Register n	V_{LOGIC}	No change	Updated with input register contents
		GND	No change	Updated with input register contents
0011	Write to and update DAC Channel n	V_{LOGIC}	Data update	Data update
		GND	Data update	Data update

[1] A high to low hardware LDAC pin transition always updates the contents of the DAC register with the contents of the input register on channels that are not masked (blocked) by the LDAC mask register.

[2] When LDAC is permanently tied low, the LDAC mask bits are ignored.

THEORY OF OPERATION

HARDWARE RESET ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ pin is an active low reset that allows the outputs to be cleared to either zero scale or midscale. The clear code value is user selectable via the $\overline{\text{RESET}}$ select pin. It is necessary to keep the $\overline{\text{RESET}}$ pin low for a minimum time (see Table 4) to complete the operation (see Figure 2). When the $\overline{\text{RESET}}$ signal is returned high, the output remains at the cleared value until a new value is programmed. While the $\overline{\text{RESET}}$ pin is low, the outputs cannot be updated with a new value. Any events on the $\overline{\text{LDAC}}$ or $\overline{\text{RESET}}$ pins during power-on reset are ignored. If the $\overline{\text{RESET}}$ pin is pulled low at power-up, the device does not initialize correctly until the pin is released.

RESET SELECT PIN (RSTSEL)

The AD5676 contains a power-on reset circuit that controls the output voltage during power-up. By connecting the RSTSEL pin low, the output powers up to zero scale. Note that this is outside the linear region of the DAC; by connecting the RSTSEL pin high, V_{OUT}x power up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC.

The RSTSEL pin is only available on the TSSOP package. When the AD5676 LFCSP package is used the outputs power up to 0 V.

SOFTWARE RESET

A software executable reset function is also available, which resets the DAC to the power-on reset code. Command 0110 is designated for this software reset function. The address bits must be set to 0x0 and the data bits set to 0x1234 for the software reset command to execute.

AMPLIFIER GAIN SELECTION ON LFCSP PACKAGE

The output amplifier gain setting for the LFCSP package is determined by the state of Bit DB2 in the gain setup register (see Table 17 and Table 18).

Table 17. Gain Setup Register

Bit	Description
DB2	Amplifier gain setting DB2 = 0; amplifier gain = 1 (default) DB2 = 1; amplifier gain = 2

Table 18. 24-Bit Input Shift Register Contents for Gain Setup Command

DB23 (MSB)	DB22	DB21	DB20	DB19 to DB3	DB2	DB1	DB0 (LSB)
0	1	1	1	Don't care	Gain	Reserved; set to 0	Reserved; set to 0

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The AD5676 is typically powered by the following supplies: V_{DD} = 3.3 V and V_{LOGIC} = 1.8 V.

The ADP7118 can be used to power the V_{DD} pin. The ADP160 can be used to power the V_{LOGIC} pin. This setup is shown in Figure 48. The ADP7118 can operate from input voltages up to 20 V. The ADP160 can operate from input voltages up to 5.5 V.

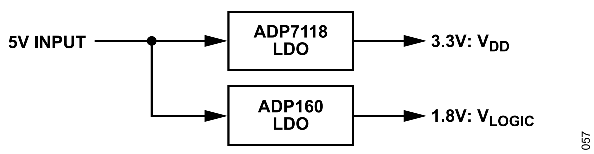


Figure 48. Low Noise Power Solution for the AD5676

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5676 is via a serial bus that uses a standard protocol that is compatible with DSP processors and microcontrollers. The communications channel requires a 3-wire or 4-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The AD5676 requires a 24-bit data-word with data valid on the rising edge of $\overline{SYNC}$.

AD5676 TO ADSP-BF531 INTERFACE

The SPI interface of the AD5676 can easily connect to industry-standard DSPs and microcontrollers. Figure 49 shows the AD5676 connected to the Analog Devices, Inc. Blackfin® DSP. The Blackfin has an integrated SPI port that can connect directly to the SPI pins of the AD5676.

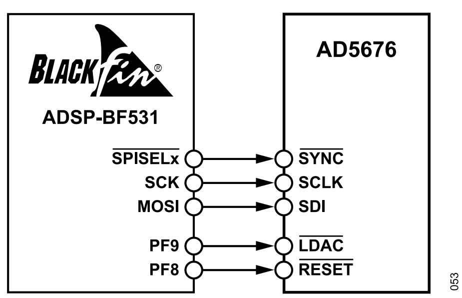


Figure 49. ADSP-BF531 Interface

AD5676 TO SPORT INTERFACE

The Analog Devices ADSP-BF527 has one SPORT serial port. Figure 50 shows how a SPORT interface controls the AD5676.

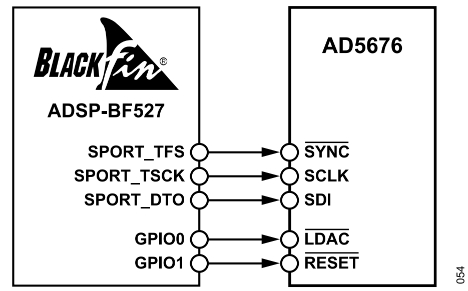


Figure 50. SPORT Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the PCB on which the AD5676 is mounted so that the AD5676 lies on the analog plane.

The AD5676 must have ample supply bypassing of 10 μF in parallel with 0.1 μF on each supply, located as close to the package as possible, ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where many devices are on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

The GND plane on the device can be increased (as shown in Figure 51) to provide a natural heat sinking effect.

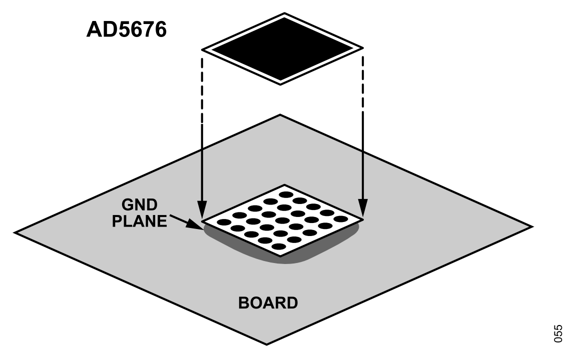


Figure 51. Pad Connection to Board

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. *i*Coupler® products from Analog Devices provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5676 makes the device ideal for isolated interfaces because the number of interface lines is kept

APPLICATIONS INFORMATION

to a minimum. Figure 52 shows a 4-channel isolated interface to the AD5676 using an ADuM1400. For further information, visit www.analog.com/icoupler.

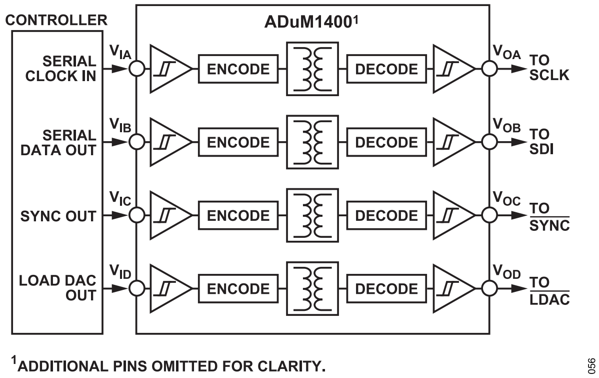
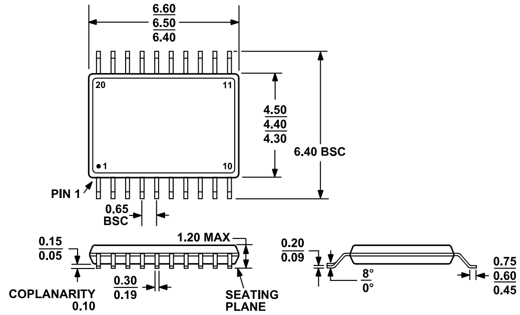


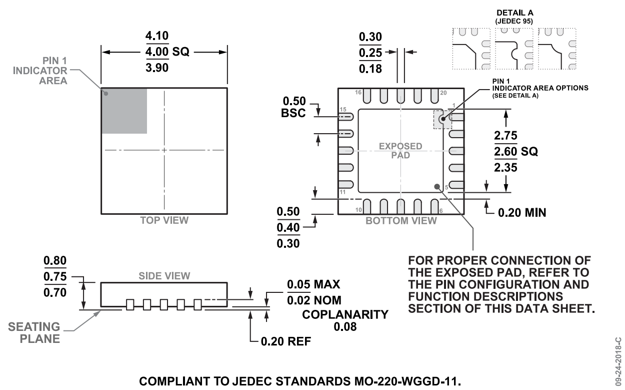
Figure 52. Isolated Interface

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 53. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-11.

Figure 54. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-8)
Dimensions shown in millimeters

Updated: July 13, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD5676ACPZ-REEL7	-40°C to +125°C	20-Lead LFCSP (4mm x 4mm w/ EP)	Reel, 1500	CP-20-8
AD5676ACPZ-RL	-40°C to +125°C	20-Lead LFCSP (4mm x 4mm w/ EP)	Reel, 5000	CP-20-8
AD5676ARUZ	-40°C to +125°C	20-Lead TSSOP		RU-20
AD5676ARUZ-REEL7	-40°C to +125°C	20-Lead TSSOP	Reel, 1000	RU-20
AD5676BCPZ-REEL7	-40°C to +125°C	20-Lead LFCSP (4mm x 4mm w/ EP)	Reel, 1500	CP-20-8
AD5676BCPZ-RL	-40°C to +125°C	20-Lead LFCSP (4mm x 4mm w/ EP)	Reel, 5000	CP-20-8
AD5676BRUZ	-40°C to +125°C	20-Lead TSSOP		RU-20
AD5676BRUZ-REEL7	-40°C to +125°C	20-Lead TSSOP	Reel, 1000	RU-20

[1] Z = RoHS Compliant Part.

RESOLUTION AND ACCURACY OPTIONS

Model[1]	Resolution	Accuracy
AD5676ARUZ	16 Bits	±8 LSB INL
AD5676ARUZ-REEL7	16 Bits	±8 LSB INL

OUTLINE DIMENSIONS

Model[1]	Resolution	Accuracy
AD5676BRUZ	16 Bits	±3 LSB INL
AD5676BRUZ-REEL7	16 Bits	±3 LSB INL
AD5676ACPZ-REEL7	16 Bits	±8 LSB INL
AD5676ACPZ-RL	16 Bits	±8 LSB INL
AD5676BCPZ-REEL7	16 Bits	±3 LSB INL
AD5676BCPZ-RL	16 Bits	±3 LSB INL

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-AD5676SDZ	Evaluation Board

[1] Z = RoHS Compliant Part.

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).